Metal-induced dislocation nucleation for metastable SiGe/Si

V. Higgs
Kings College London, London WC2R 2LS, United Kingdom

P. Kightley and P. J. Goodhew
University of Liverpool, Liverpool L69 3BX, United Kingdom

P. D. Augustus
Plessey Research Caswell, Towcester NN12 8EQ, United Kingdom

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A new mechanism of misfit dislocation nucleation is demonstrated. Deliberate contamination with approximately 0.003 monolayers of Cu and subsequent annealing at 600 °C is shown by transmission electron microscopy, photoluminescence, and defect etching to produce dislocation half loops in a 1.1 μm layer of $Si_{0.93}Ge_{0.07}$ on a silicon substrate.

The introduction of dislocations into a misfitting crystal boundary was first treated theoretically by van der Merwe.[1] This model, and more recently other models,[2–7] use a thermodynamic argument to derive an equilibrium expression that describes the point of introduction of the dislocations. These arguments are often only applicable to specific growth systems. Until the nucleation mechanisms of misfit dislocations are identified and incorporated into dynamic models, no theory will be able to describe misfit dislocation generation for every system. Various experimental derivations of the so called "critical" point or "critical thickness" of dislocation introduction were rationalized by Gourley *et al.*[8] who showed that the detected critical points were often determined by the detection limit of the analytical technique used. The critical stress at which dislocations are introduced has also been shown to be continuous rather than a sharp point delineating the onset of dislocation introduction.[9] The probable mechanisms of dislocation introduction have been reviewed,[10] and since this work three mechanisms have been reported for the SiGe system. Centers of misfit dislocation generation can be traced to defective growth on contaminated areas of the substrate.[11] Also a stacking fault that can act as a regenerative source of loops[12] and gross Cu-rich precipitates[13] (of rectangular dimension 45 nm within a $Si_{0.84}Ge_{0.16}$ layer) can also lead to the formation of misfit dislocations through loop nucleation. These mechanisms appear to be specific only to the samples used for their study. When wafers are prepared without contamination so that gross defects and stacking faults are not present, then no general mechanism exists to describe the dislocation introduction. The nucleation of misfit dislocations for SiGe has been observed *in situ*;[14,15] however, the authors concentrate upon the motion of the defects rather than the mechanisms of nucleation.

This letter sets out to show that very low levels of metallic contamination and post-growth processing can enable misfit dislocation formation. In our experiment a 1.1-μm-thick $Si_{0.93}Ge_{0.07}$ epilayer was grown at 500 °C onto a carefully prepared silicon substrate. The as-received epilayer contained no misfit dislocations as detected by either transmission electron microscopy (TEM) or chemical etching. Furthermore, the dislocation-related luminescence bands (ascribed $D1$ to $D4$) associated with dislocations in silicon were not present. A deliberate low level contamination with Cu of silicon samples that contain many dislocations dramatically enhances their luminescence.[16] The deliberate Cu contamination procedure involves the controlled back-plating of approximately 0.003 monolayers of Cu, from Cu-dosed ultrapure HF acid, followed by a thermal diffusion stage at 600 °C. For bulk silicon the dislocation structure, determined by TEM, does not noticeably alter after the Cu contamination procedure,[17] i.e., there is no change in the distribution of types of dislocation and no observed precipitation. When the same procedure is used on a "metastable" $Si_{0.93}Ge_{0.07}$ layer the barrier to plastic relaxation is reduced and misfit dislocations are introduced. In this experiment our SiGe wafer was cleaved into four samples. Three control samples were prepared. The first was the as-received layer, the second had a 600 °C anneal, and the third was dipped in ultra-pure HF (that had not been Cu contaminated) and was then annealed at 600 °C. The fourth sample was contaminated with Cu and annealed at 600 °C as described above. Figure 1(a) shows an optical micrograph of a defect etched[18] SiGe(control) sample that received the 600 °C anneal only. Figure 1(b) is a micrograph of the sample that was Cu contaminated and then given the 600 °C anneal. An etch pit density of $\langle 10^2$ cm^{-2} is shown in Fig. 1(a) and was approximately the same for all three control samples. The pit density has risen in Fig. 1(b) and a cross-hatch of line density 2×10^5 cm^{-1} has appeared. The photoluminescence spectra corresponding to the samples used for Figs. 1(a) and 1(b) are shown in Figs. 2(a) and 2(b). The three control samples had spectra similar to Fig. 2(a). The spectra are characterized by a broad weak continuum onto which is superimposed a band with its zero phonon line at 767 meV which is labeled P on the figure. Examination of the luminescence at this energy, in particular the vibronic sideband and local mode frequencies, show it to be characteristic of a C-O complex in the silicon. For the sample that was Cu contaminated there are also present the dislocation-related luminescence bands ($D1$ to $D4$). This shows that if the surface is contaminated with Cu and then annealed at 600 °C misfit dislocations are generated. A similar experiment was performed at 300 °C but no dislocations were generated. These

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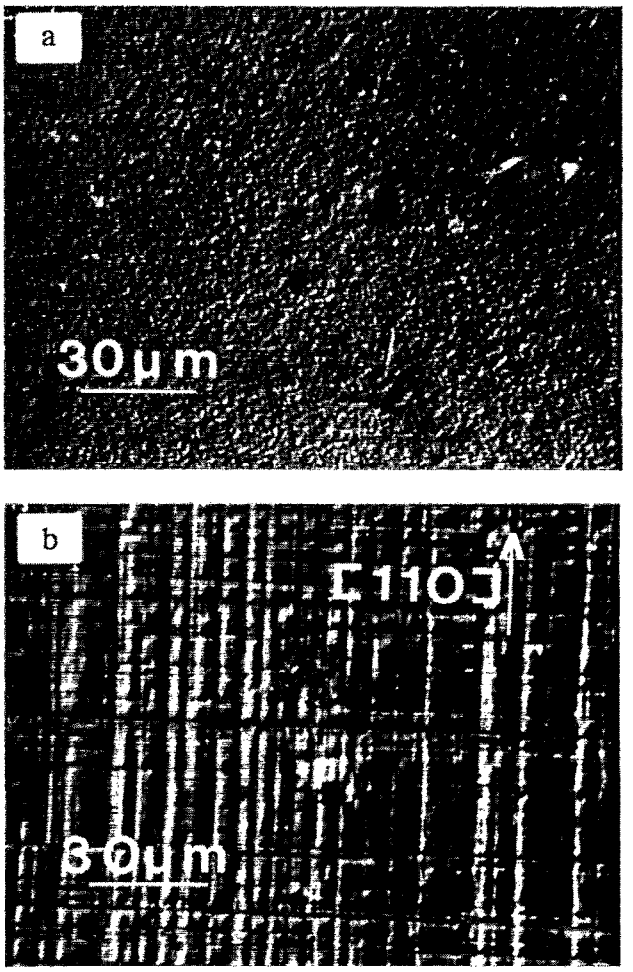

FIG. 1. (a) Optical micrograph of a Schimmel etched portion of the as-received and then annealed (at 600 °C) sample. The etch pit density for this and all the control samples was approximately 10^2 cm $^{-2}$. (b) Optical micrograph of a Schimmel etched portion of the layer after Cu contamination and the 600 °C anneal. The etch pit density has increased and a cross-hatch pattern of line density 2×10^5 cm $^{-1}$ is measured.

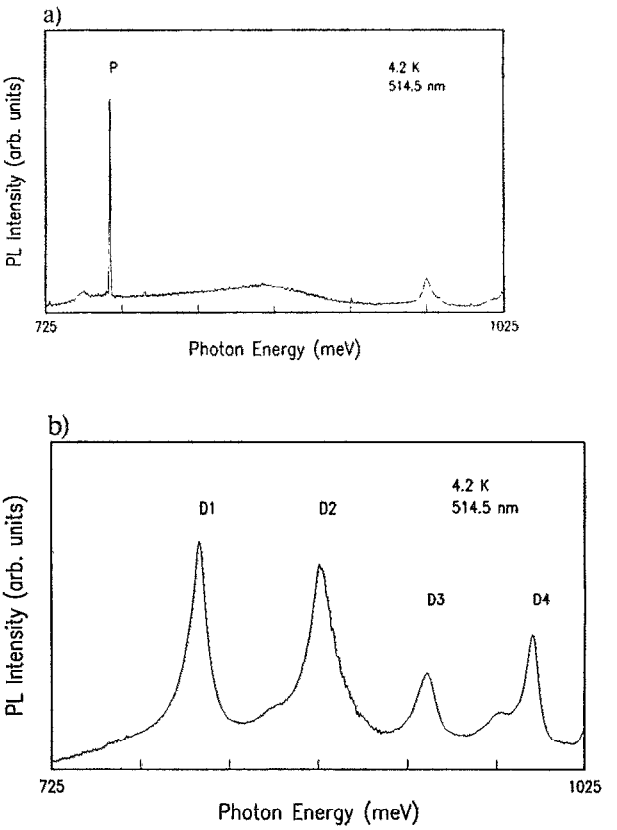

FIG. 2. (a) Photoluminescence spectrum of the sample used for Fig. 1(a). All the control samples had similar spectra. No dislocation bands (*D* bands) are present. (b) Photoluminescence spectrum of the sample after Cu contamination and 600 °C anneal. Strong dislocation related luminescence bands *D*1 to *D*4 are present.

results were confirmed by TEM diffraction contrast experiments which showed that the dislocation array generated for the contaminated sample annealed at 600 °C consisted primarily of $(a/2)\langle110\rangle60°$ dislocation and $(a/2)\langle110\rangle$ dislocations in approximately edge orientation.

Figure 3 shows a plan-view transmission electron micrograph of the entire thickness of the 1.1 μm $Si_{0.93}Ge_{0.07}$ layer and some of the substrate. A dense array of misfit dislocations has been formed at the interface between the $Si_{0.93}Ge_{0.07}$ and the Si substrate. These dislocations are introduced via a surface loop nucleation mechanism. Confirmation of the operation of surface loop nucleation was obtained using stereomicroscopy. The plan-view TEM samples were prepared by chemical jet etching from the substrate side leaving the epilayer intact. The thinnest area of the specimen is thus well away from the heterointerface and the misfit dislocation array. Figure 4 shows a stereo pair of a dislocation half loop, marked *A*, from this thinner area of the TEM specimen. The half loop is situated in the *Si*Ge epilayer and has not yet propagated to the SiGe/Si

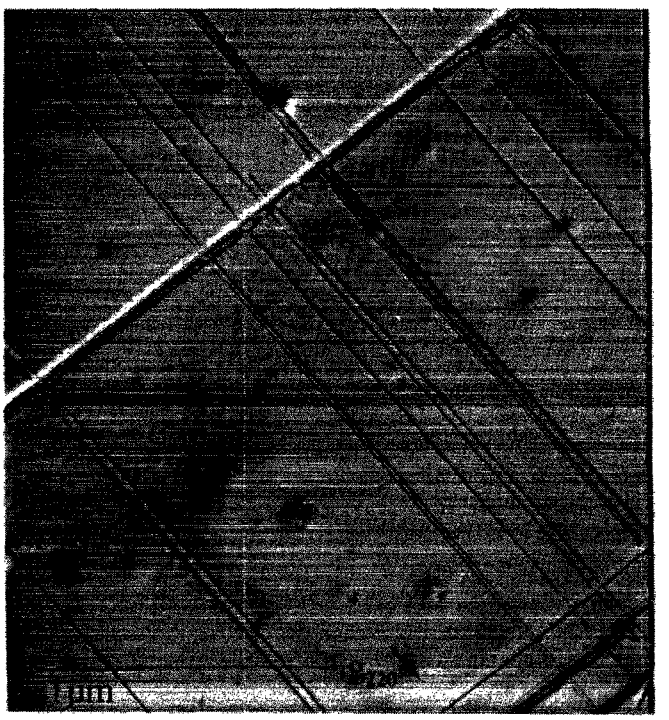

FIG. 3. Transmission electron micrograph, g_{220}, of the misfit dislocation array that was formed during the contamination and anneal cycle.

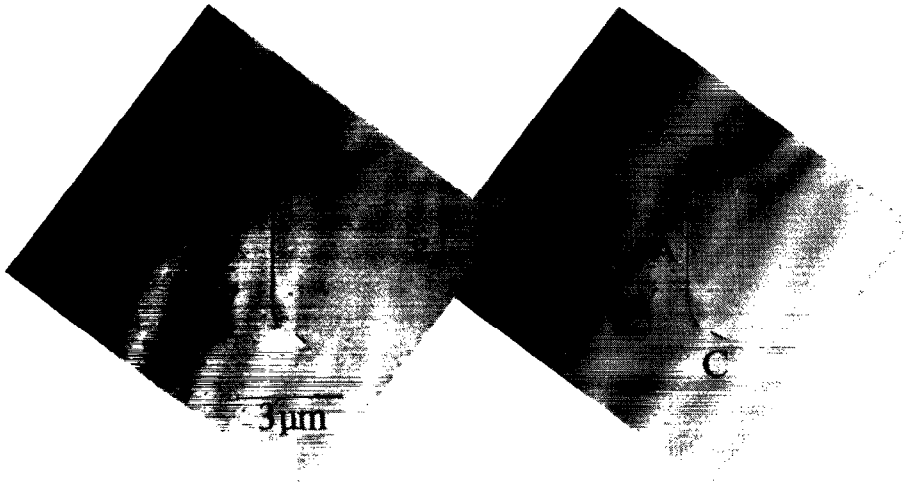

FIG. 4. Stereo transmission electron micrographs of a surface half loop. This loop, labeled *A*, penetrates the epilayer by approximately 2000 Å from the top surface. The threading portions at each end terminate at the top surface. The dislocations *B* and *C* are the threading ends of larger half loops.

interface. The analysis showed that the half loop extended approximately 2000 Å into the bulk from the surface, the ends of the loop that display oscillatory contrast terminating at the free surface. The other dislocations, *B* and *C*, pass through the thickness of the TEM sample and presumably are the threading ends of separate loops. Unlike the dislocation sources outlined previously[11–13] there is no obvious source of these defects; whatever is causing the loops to nucleate is not apparent from TEM diffraction contrast analysis.

From this evidence of small half loops close to the surface after Cu contamination it is concluded that the source of misfit dislocations is activated by a surface defect. Surface stress, particularly for high misfits, has been shown to be able to alter the predictions of equilibrium critical thickness theories significantly.[19] If Cu forms a complex surface defect that alters the local surface stress then it is possible that this will act as a nucleation center for the dislocation half loops. However, either the defect is so small that it cannot be imaged in the electron microscope or the Cu diffuses away during the annealing after the loop has been formed. This study has established that metallic contamination can initiate the nucleation of surface half loops which become the components of misfit relaxation in strained Si/Ge epitaxial layers. This occurs at a level of contamination where no obvious precipitates can be detected by transmission electron microscopy. This observation has important implications for the growth and processing of metastable strained Si/Ge layers. If the moderately high temperatures, normally associated with device processing, are applied to Si/Ge epitaxial layers when the material has been inadvertently contaminated with metallic impurities, then misfit dislocations may be introduced. The impurities could be introduced during epitaxial growth or during subsequent processing. In either case the misfit dislocations generated are likely to be detrimental to device performance.

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