Application of photoluminescence characterization to the development and manufacturing of high-efficiency silicon solar cells

M. D. Abbott,[a] J. E. Cotter, F. W. Chen, T. Trupke, R. A. Bardos, and K. C. Fisher
Centre of Excellence for Advanced Silicon Photovoltaics and Photonics, University of New South Wales, Sydney 2052, Australia

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Characterization techniques based on quasi-steady-state photoluminescence have recently emerged as accurate, fast, and powerful tools for developing high-efficiency silicon solar cells. These techniques are contactless and provide complementary spatial and injection level dependent information about recombination. In this paper, we demonstrate the application of different photoluminescence techniques to several important aspects of high-efficiency solar cell fabrication: wafer handling, furnace contamination, process-induced defects, cell design, and cell process monitoring. The experimental results demonstrate that photoluminescence characterization techniques are excellent tools for laboratory experiments and also potentially for industrial process monitoring. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2398724]

INTRODUCTION

Characterization techniques based on quasi-steady-state photoluminescence (PL) have recently emerged as powerful tools for developing and monitoring the fabrication of high-efficiency silicon solar cells. Much of the work presented to date has focused on the development and fundamental physics of these techniques.[1–4] In this paper we apply these techniques to characterize several important aspects of high-efficiency solar cell fabrication—wafer handling, furnace contamination, process-induced defects, cell design, and cell process monitoring. In doing so we show that PL techniques are broadly applicable to solar cell development, give insight into the operation of high-efficiency solar cell devices, and identify how device performance can be improved. PL characterization techniques are shown to be an excellent tool both for laboratory experiments and as a potential factory process monitoring tool.

Light emission from silicon, either in the form of PL or electroluminescence (EL), has long been used to characterize defect, dopant, and device properties. EL spectra and photographic images of EL emission from a silicon *p-n* junction were reported by Chynoweth and McKay in 1956.[5] EL imaging as a tool for finding faults in silicon integrated circuits was reported by Khurana and Chiang in 1986.[6] In that work, an image intensified solid state camera was used combined with an optical microscope. Cooled charge-coupled device (CCD) camera systems were introduced[7] and since then a wide variety of commercial tools, with and without intensification, have become available including longer wavelength imaging systems.[8]

Spectrally resolved PL has been widely used, typically at cryogenic temperatures, to investigate dopant and defect properties in silicon and to determine the absorption coefficient for band to band transitions.[9,10] PL mapping has been used to measure the spatially resolved distribution of defects in silicon wafers[11] and silicon-on-insulator (SOI) wafers.[12] Photoluminescence analysis at liquid helium temperatures has been used to determine boron and phosphorus concentrations in silicon.[13]

Application to solar cell characterization has focused on using scanning room-temperature photoluminescence (RTPL) spectroscopy to assess spatial variations of the material quality, to correlate such variations with dislocation densities, and to determine diffusion length maps.[14,15] Studies have also used RTPL to characterize fabrication processes, in particular, to relate initial material quality to finished solar cells and to examine the impact of various processing steps including gettering and hydrogenation.[16–18] More quantitative work has been presented in which PL of silicon wafers was used to determine the upper limit of a solar cell's open-circuit voltage.[19] Similar investigations were carried out for hydrogenated amorphous silicon (*a*-Si:H)/crystalline silicon (*C*-Si) heterojunctions[20] and $Cu(InGa)Se_2$.[21] Spectrally resolved electroluminescence measurements on silicon solar cells with different surface textures have been used to determine the absorptivity and thus the light trapping properties of those cells.[22] More recently, electroluminescence imaging of finished silicon solar cells has been used as a technique for measuring the spatially resolved diffusion length and for fault finding in silicon solar cells and solar modules.[23]

In this paper, we demonstrate the versatility and utility of three PL techniques specifically for the development and monitoring of silicon solar cell fabrication processes. Because PL is a contactless, open-circuit measurement technique, it can be applied to analyze partially completed solar cells, yielding information about every process in the fabrication sequence. Injection level dependent quasi-steady-state photoluminescence (QSS-PL) lifetime measurements have been shown experimentally to be unaffected by artifacts such as trapping[3] or depletion region modulation[1] (DRM) that cause an overestimation of the lifetime at low carrier concentrations in photoconductance (PC) measurements. Thus, unlike photoconductance techniques, the QSS-PL technique is

[a]FAX: 61-2-9662-4240; electronic mail: mal.abbott@gmail.com

able to examine recombination processes at injection levels as low as 10^9 cm^{-3}. This is significant since many sources of increased recombination and shunting only dominate device characteristics at low injection. By varying the optical generation rate in QSS-PL measurements, it is possible to determine the *area-averaged* injection level dependent effective minority carrier lifetime over more than six orders of magnitude of carrier density, yielding detailed information about the nature of the dominant recombination processes. In the suns-PL technique[2] this information is related to the terminal characteristics of the finished solar cell—in the form of pseudo-current-voltage and pseudo-local ideality factor curves—providing additional insight into the operation of prototype and partially completed solar cells. Finally, because it is possible to image the PL signal—something that is not possible with photoconductance techniques—spatially resolved information about both recombination and junction shunting can be collected in a very short time with the sample under uniform illumination at intensities from a fraction of a sun to many suns. It should be noted that photoconductance can be used to resolve spatial information using mapping techniques; however, to do so requires very long data acquisition times. The injection level dependent and spatially resolved information obtained from the combination of QSS-PL lifetime measurements, PL imaging, and suns-PL can be used to quickly and effectively discover and analyze problems, to develop and optimize processes, and to monitor existing fabrication sequences for faults and problems, as will be shown below.

PL imaging has several advantages over other existing imaging techniques. It has been shown[24] to be orders of magnitude faster than infrared lifetime mapping[25] (ILM) and carrier density imaging (CDI).[26] Moreover, the latter measurements must be carried out at elevated sample temperature to improve the sensitivity[27] and suffer from artifacts resulting from trapping and from the DRM effect. By using PL imaging rather than EL imaging the measurement is fully contactless and can be performed on wafers at any stage of cell fabrication. This is a great advantage since it allows individual processing steps to be easily isolated and characterized without requiring a finished device. It also potentially allows in-line process monitoring to provide faster feedback in a production line and monitoring of initial wafer quality.

It should be noted that there are also some disadvantages to using characterization techniques that are based on photoluminescence compared to other techniques. Photoluminescence measurements are harder to calibrate since the signal strength for a given minority carrier lifetime is dependent on the particular sample and is affected by parameters such as the optical coupling (i.e., surface morphology) and bulk doping. Self-consistent techniques have been developed to aid in the absolute calibration of QSS-PL lifetime curves;[28] however, even with such calibration techniques the need still exists to calibrate each type of sample separately. Another challenge in PL techniques, that can be difficult in practice, is the unambiguous separation of luminescence signal from the optical excitation.

PHOTOLUMINESCENCE TECHNIQUES

In this paper we apply recently established photoluminescence techniques to issues related to the fabrication of solar cell devices. Three different techniques are used: (1) QSS-PL lifetime measurements to characterize minority carrier recombination as a function of injection level, (2) suns-PL to describe the solar cell terminal characteristics in terms of the recombination, and (3) PL imaging to spatially resolve recombination and junction shunting effects. These techniques do not analyze the spectral distribution of the PL signal, rather they use the relationship between band to band radiation and the separation of the quasi-Fermi energies[29] to extract the minority carrier concentration.

Quasi-steady-state photoluminescence

Photoluminescence measurements in quasi-steady-state are used to determine the spatially averaged injection level dependent effective minority carrier lifetime $\tau(\Delta n)$ in silicon wafers.[1] Carriers are generated by an incident light pulse with variable intensity. The measured relative photoluminescence signal I_{PL} is converted into a spatially averaged minority carrier concentration Δn using

$$I_{\mathrm{PL}} = A_i B(N_{D/A} + \Delta n)\Delta n, \tag{1}$$

where A_i is a scaling factor that is determined using a recently introduced self-consistent calibration procedure,[28] B is the radiative recombination coefficient, and $N_{D/A}$ is the bulk doping concentration. Equation (1) can be rewritten as

$$\Delta n = -\frac{N_{D/A}}{2} + \sqrt{\left(\frac{N_{D/A}}{2}\right)^2 + \frac{I_{\mathrm{PL}}}{A_i B(T)}}. \tag{2}$$

The effective minority carrier lifetime is then extracted using the derivative of Eq. (2) and with $d\Delta n/dt = G(t) - \Delta n/\tau_{\mathrm{eff}}$,[30] we find

$$\tau_{\mathrm{eff}} = \frac{\Delta n}{G(t) - (dI_{\mathrm{PL}}/dt)[1/(N_{D/A} + 2\Delta n)B(T)A_i]}. \tag{3}$$

The absolute value of the average generation rate is calculated using a measurement of the incident photon flux combined with the front surface reflection of the sample using

$$G(t) = \frac{1}{d} J_\gamma (1 - R_f), \tag{4}$$

where d is the sample thickness, J_γ is the incident photon flux measured with a calibrated detector, and R_f is the front surface reflection. The injection level dependent effective minority carrier lifetime is then measured by varying the illumination intensity and plotting the effective lifetime as a function of carrier concentration.

Suns-PL

A variation on the QSS-PL technique is suns-PL[2] in which the PL signal is used to generate a pseudo-current-voltage curve. The implied voltage of the wafer is calculated by first converting the measured PL signal into a value for the separation of the quasi-Fermi energies using the equation

$$I_{\mathrm{PL}} = A_i B n_i^2 \exp(\Delta\eta/kT), \tag{5}$$

where n_i is the intrinsic carrier concentration and $\Delta\eta$ is the separation of the quasi-Fermi energies within the sample. QSS-PL data can be converted into a pseudo-current-voltage curve by first converting the quasi-Fermi level separation into an implied voltage. In an ideal solar cell the terminal voltage U is given by $eU=\Delta\eta$ where e is the elementary charge.[2] Combining this with Eq. (5) yields an expression for implied voltage in terms of the measured PL intensity:

$$U = \frac{kT}{e} \ln\left(\frac{I_{\mathrm{PL}}}{A_i B n_i^2}\right). \tag{6}$$

By varying the generation rate, which is achieved by variation of the illumination intensity, suns-PL is able to produce pseudo-current-voltage curves across a range of implied cell voltages. The resulting data are similar to those provided by suns-V_{oc} (Ref. 31) analysis and can be used to predict the electrical terminal characteristics of finished devices. However, unlike the suns-V_{oc} technique, the suns-PL technique has the advantage that it can be carried out at any intermediate step in a processing sequence because it does not require a specific device structure such as a *p-n* junction. It should be noted that the suns-PL technique uses a monochromatic light source to generate carriers and as such the calculated voltage may differ slightly from the cell voltage under AM1.5 standard testing conditions.

The generation rate versus implied voltage curve measured with the suns-PL technique can be analyzed using the *m-V* analysis that is employed on dark *IV* curves. This technique has been shown to be useful for interpreting recombination mechanisms.[32] In the technique the value of m represents the local ideality factor, i.e., the slope of the $\ln(I)$-V at each voltage:

$$m = \frac{1}{V_T}\left(\frac{dV}{d(\ln I)}\right). \tag{7}$$

The value is extracted by calculating the normalized gradient at each point on the $\ln(I)$-V curve to yield a pseudo-local ideality factor (m) versus implied voltage (V_{imp}) curve.

PL imaging

PL imaging is used to resolve the recombination (i.e., the relative effective minority carrier lifetime) spatially.[4] In this technique, the entire sample is uniformly illuminated at a constant intensity. A cooled CCD camera is used to capture an image of the PL emission across the wafer. The number of photons captured by each pixel is related to the local separation of the quasi-Fermi energies, as per Eq. (5). Further, at low to moderate injection levels, the per-pixel photon count is approximately proportional to the local effective lifetime at the location imaged by that pixel. The resulting images resolve areas of low local effective lifetime or local junction shunting, which appear as dark regions in the image. Conversely, areas of high local effective lifetime appear as light regions in the image.

Photoluminescence experimental setup

QSS-PL measurements were made using a Sinton Consulting photoconductance (PC) bridge[33] modified to incorporate a 2×2 cm^2 silicon detector. Excitation was provided by an 810 nm light-emitting diode (LED) array and the relative output intensity was measured using a beam splitter and silicon reference sensor. The signals were sampled with a 16 bit data acquisition system. The data collection, signal filtering, and processing were performed with custom built software. PL images were captured using a cooled CCD camera. Carrier excitation was performed with a 25 W diode laser operating at 815 nm. The image exposure time for all images shown here was 1 s. A more detailed description of the QSS-PL and PL imaging setups has been presented elsewhere.[1,4]

It should be noted that, while all QSS-PL measurements are calibrated, the PL imaging measurements are not calibrated. As a result, the gray scale information apparent in a particular image is only representative of lifetime variation within that particular sample. Nonetheless, the images provide important spatial information about recombination within individual wafers. Quantitative comparison between wafers is performed using calibrated QSS-PL measurements of injection level dependent effective minority carrier lifetime. Future developments of the PL imaging system will incorporate a calibration process that will allow quantitative comparisons between measurements.

RESULTS AND DISCUSSION

The three PL techniques described were used to monitor and characterize the processing and cell fabrication efforts in the laboratories at UNSW. The following sections present a number of observations regarding our device operation and processing techniques. Each section covers an important aspect of high-efficiency solar cell fabrication, wafer handling, furnace contamination, process-induced defects, cell design, and process monitoring. The wealth of information and insight provided by PL over this wide range of applications demonstrate its power as a characterization technique.

MANUAL WAFER HANDLING

Wafer handling is a necessary part of solar cell processing. Poor handling can lead to breakages or finished cells with poor electrical performance. In the case of poor electrical performance, it is not always apparent that handling is an issue. In this work, we examine three aspects of manual wafer handling, wafer drying prior to high-temperature furnace processing, handling of silicon nitride coated silicon wafers, and formation of microcracks.

Drying technique

PL imaging was used to characterize three different techniques used to dry samples after RCA cleaning, prior to high-temperature furnace diffusions. In the first technique, traditionally used at UNSW on samples that are too small to spin dry, wafers were dried using pressurized N_2 while holding the wafer by its edges with clean plastic tweezers. In the

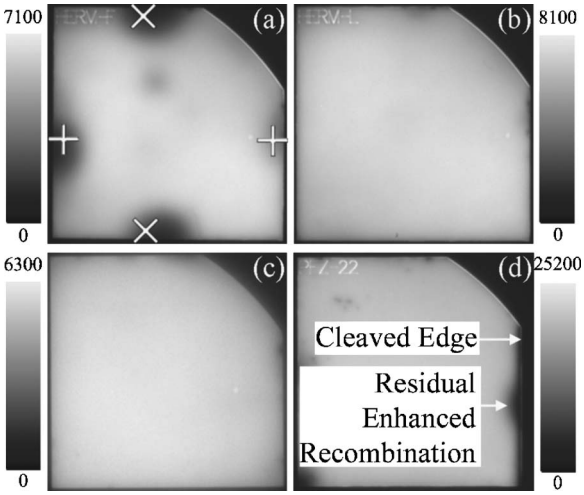

FIG. 1. ~1 sun PL image of a furnace diffused 1 Ω cm *n*-type Czochralski (CZ) wafer (a) dried using tweezers (Ref. 47), (b) dried in a furnace(Ref. 47), (c) and dried in a microwave, and (d) 1 Ω cm *p*-type FZ wafer with laser cleaved edge. The locations of tweezers during drying are marked as (×) before furnace step 1 and (+) before furnace step 2.

second technique, wafers were directly loaded into the mouth of a quartz furnace where they were exposed to a warm flow of nitrogen gas to evaporate water. In the third technique, wafers were placed in an ordinary kitchen microwave oven and dried for 1.75 min to evaporate water. After drying, the wafers were loaded into a diffusion furnace for a light boron deposition. The samples were then removed, stripped of boron dopant glass in HF acid, and loaded into an oxidation furnace for surface oxidation. The location of the tweezers on the wafer edge during wafer drying by the first technique was recorded before each furnace step.

The use of plastic tweezers was found to be a source of recombination in the wafers. PL images of tweezer dried wafers, shown in Fig. 1(a), display dark regions of high recombination at all locations of tweezer contact. The PL intensity in the dark regions is six times lower than in the light region at the center of the sample. Despite the contact area being located on the very edge of the wafer, the recombination is observed in a semicircle pattern several millimeters into the wafer. This enhanced recombination is still present after removing a 1 mm strip from the edge, shown in Fig. 1(d), suggesting that the recombination source is located far within the wafer bulk and not just at the contact surface. These results indicate that a source of contamination or crystallographic damage is deposited on the edge during drying, then driven into the bulk during the subsequent high-temperature furnace process. Both alternative methods of cleaning, furnace mouth drying [Figure 1(b)] and microwave drying [Fig. 1(c)], avoid the introduction of such enhanced recombination.

Increased recombination due to the tweezers results in a wide deviation in effective minority carrier lifetimes across a batch of samples. Injection level dependent effective minority carrier lifetime curves measured using QSS-PL, shown in Fig. 2, demonstrate the difference between a batch of samples fabricated with tweezer drying (red) and with microwave drying (black). The lifetime of four tweezer dried

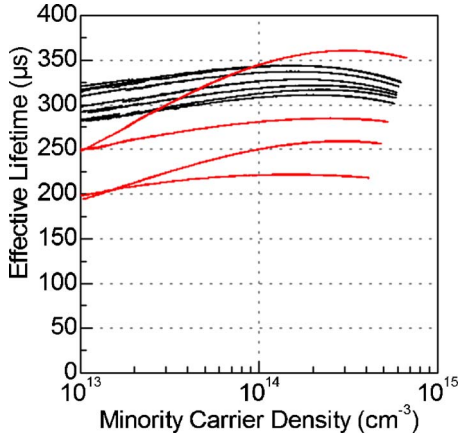

FIG. 2. (Color online) Injection level dependent effective minority carrier lifetime measured using QSS-PL of wafers (red) with tweezer drying and (black) with microwave drying.

samples varies by 140 μs while the deviation across eight microwave dried samples is only 30 μs. The process of contamination due to the tweezers occurs to a different extent on each individual wafer, creating a significant variation in effective lifetime. Samples dried without tweezers yield more consistent results, which clearly facilitates a systematic optimization of processing parameters. Figure 2 also highlights that the improved drying method on average results in an improvement in the effective minority carrier lifetime.

Handling of silicon nitride coated silicon wafers

PL imaging was used to characterize the surface passivation quality of silicon nitride thin-film coatings on silicon wafers. Manual handling was found to have a significant impact on the recombination at the surface. Silicon nitride films were deposited on *n*-type, float zoned silicon wafers by plasma enhanced chemical vapor deposition (PECVD) using a Roth&Rau AK400 machine. The resulting films had a refractive index of 2.00 and a thickness of about 75 nm.

Visually, the films appear uniform and devoid of features. However, PL images reveal several sources of locally enhanced minority carrier recombination. Measurement of the wafer thickness using a metallic micrometer, before and after silicon nitride deposition, results in enhanced recombination in an area the exact size of the micrometer head [see Fig. 3(a)]. Surface scratches, both on the predeposited silicon surface and on the silicon nitride layer itself, cause localized enhanced recombination of carriers. In Fig. 3(b) the labeled

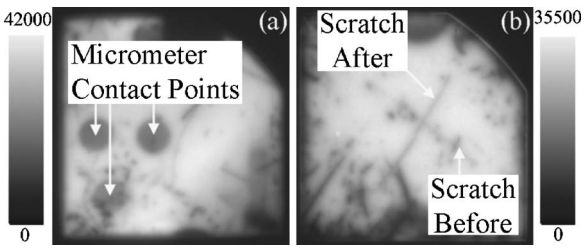

FIG. 3. ~1 sun PL image of a 1 Ω cm *n*-type wafer with PECVD silicon nitride surface layer with enhanced recombination due to (a) micrometer and (b) surface scratches (Ref. 48).

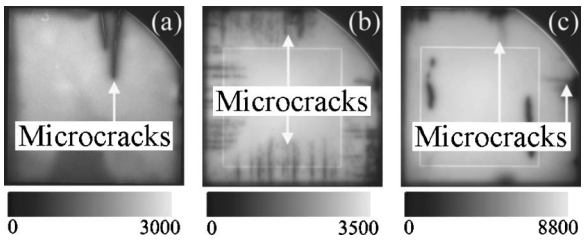

FIG. 4. ~1 sun PL image of partially processed 1 Ω cm *n*-type FZ wafers: (a) silicon nitride coated wafer with two large microcracks extending from the top edge (Ref. 48), (b) wafer cleaved with poor cleaving process resulting in microcracks extending from the four cleaved edges, and (c) furnace diffused wafer with microcracks extending from the contact points with a quartz boat.

scratches were created deliberately with a diamond pen. The other scratches observed in the PL image are due to poor wafer loading and unloading from the PECVD chamber and from characterization equipment. Silicon nitride coated surfaces are very susceptible to such handling-induced defects and PL imaging provided an excellent tool to monitor and determine their cause.

Microcracks

Incorrect handling of silicon wafers, particularly in a high-throughput production line, can result in microcracks within a wafer. These defects mechanically weaken the silicon wafer and may result in wafer breakages and reduced yield. In the worst case these breakages may occur within the machinery and result in production line downtime. Microcracks can also negatively impact the electrical performance of a wafer by increasing carrier recombination, by causing junction shunting, or by creating open circuits in the grid metallization.

Microcracks can be detected with PL imaging because of their distinctive shape; various examples are shown in Fig. 4. The presence of the microcrack results in increased recombination of minority carriers in the region of the crack, appearing as a dark region in the PL image. The wafer shown in Fig. 4(a) has two large cracks of unknown origin extending from the top to its center. The wafer in Fig. 4(b) exhibits microcracks along every edge extending into the center. This 2×2 in.^{2} sample has been cleaved from a single 4 in. wafer. All eight wafers cleaved from two 4 in. starting wafers exhibit the same PL image characteristics indicating that the cracks are a result of a poor cleaving process. The sample in Fig. 4(c) has microcracks extending from two points at either side of the round wafer edge. The location of these correlates to the contact points with the quartz wafer boat used during high-temperature furnace processing. In this case, the wafers were slightly thicker than usual, making them more difficult to fit into the slots of the quartz wafer boat.

FURNACE CONTAMINATION

Contamination during high-temperature furnace processes can reduce bulk lifetime and lead to poor electrical properties of finished cells. It has also been demonstrated that contamination will spread from one wafer to others in the same furnace tube[34] or in subsequent batches. There are

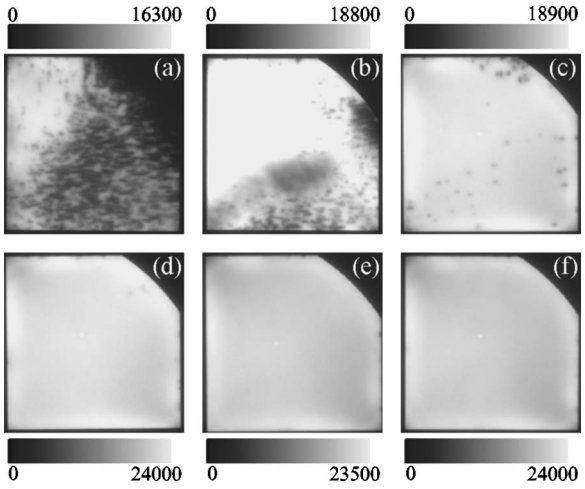

FIG. 5. ~1 sun PL images of samples contaminated during a phosphorus furnace diffusion: (a) sample with worst contamination, (b) sample in the slot next to the contaminated sample, (c) sample further down the furnace tube in the direction of the gas flow, and [(d)–(f)] samples closer to the gas injector (Ref. 47).

many possible sources of contamination on a factory floor and with a large number of wafers being processed in multiple furnaces, it is important to isolate and rectify any potential problems quickly.

Routine monitoring of high-efficiency solar cell fabrication with PL imaging detected one such furnace contamination problem. Eight samples were prepared on 230 μm thick, 1 Ω cm *n*-type wafers. The wafer surface was diffused with phosphorus (~100 Ω/□ front and ~200 Ω/□ rear) to create a high-low junction. A 400 nm thick thermal oxide was grown on both sides for surface passivation and to provide a diffusion and plating mask to be used in subsequent steps. The samples were characterized with PL techniques after furnace processing.

Images of six of the wafers described above are shown in Fig. 5. The top left wafer [labeled (a)] was unintentionally contaminated before or during the furnace loading step. This contamination spread to the adjacent wafers [labeled (b) and (c)] in the direction of the gas flow, whereas other wafers in the same furnace tube [(d)–(f)] but upstream of the gas flow were unaffected by the contamination.

The injection level dependent effective minority carrier lifetime curves measured on the samples, shown in Fig. 6, quantify the increased recombination due to the furnace contamination. The bulk lifetime of wafer (a) is 100 μs less than partially contaminated sample (c). The uncontaminated samples [(d)–(f)] display no difference in effective lifetime between the three wafers. In the QSS-PL technique light pulse profiles with a rising and a falling branch are used, i.e., the lifetime at each injection level is measured twice during one pulse. The deviation in the lifetimes obtained from the rising and falling branches of the light pulse, respectively, at injection levels below 10^{11} is due to a hysteresis effect caused by suboptimal amplifier and excitation pulse settings used in this measurement.

In a high-throughput manufacturing environment the ability to quickly detect a contaminated furnace would be of great benefit to improve the yield. Routine PL monitoring

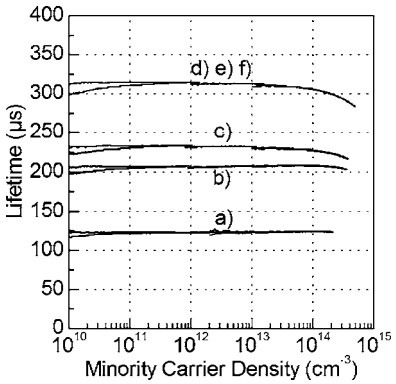

FIG. 6. Injection level dependent effective minority carrier lifetimes measured using QSS-PL after contamination during phosphorus furnace diffusion (Ref. 47). Labels match those in the PL images in Fig. 5.

can be used to identify an individual contaminated wafer and remove it from the line, or identify furnace stacks that require cleaning before the contamination ruins a large number of cells.

PROCESS-INDUCED DEFECTS

During device optimization it is important to understand the influence of individual processing steps. As a fully contactless measurement, PL techniques are capable of identifying the effect a particular process step has on recombination without requiring a finished device. This allows the influence of individual processing steps to be characterized effectively and rapidly.

Surface scratches

Surface damage due to mechanical scratching and abrasion can occur for many reasons and results in increased minority carrier recombination. Reducing recombination at a wafer surface is an important part of high-efficiency solar cell design, particularly for thin wafers with a high bulk lifetime. A reduction in surface recombination is often achieved using surface diffusions with surface coatings such as silicon nitride or silicon dioxide. Subsequent processing or mishandling can reduce the effectiveness of these surface passivation techniques. Here, we use PL to characterize the influence of mechanical scratching on a wafer with a p^+-n-n^+ structure and a thermally grown oxide on all surfaces.

Samples were prepared on 290 μm thick, polished 1 Ω cm, n-type float zoned wafers. The front surface was diffused with boron ($\sim$100 $\Omega/\square$) to create an emitter and the rear surface was diffused with phosphorus ($\sim$100 $\Omega/\square$) to create a high-low junction. A 120 nm thick thermal oxide was grown on both sides for surface passivation. A laser was used to scribe an isolation trench through the boron emitter to mitigate the influence of edge recombination. The trench was cut in a square pattern with dimensions of 2.8×2.8 cm^2 and was passivated with a phosphorus diffusion ($\sim$100 $\Omega/\square$) and thermal oxidation ($\sim$120 nm). The samples were scratched with a diamond pen to induce surface damage. One sample was scratched on the rear side around the edge of the active area, characterized with PL, then scratched again to cover the rear surface. The other sample was scratched on the front side in two locations at the edge of the active area. The samples were characterized with PL after the initial furnace processing and after scratching.

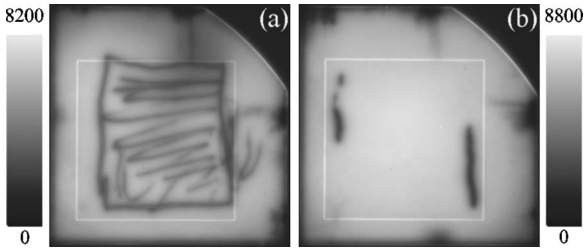

FIG. 7. $\sim$1 sun PL images of partially completed solar cells with a boron diffused junction on the front surface and phosphorus high-low diffusion on the rear. Images were taken after diamond pen scratching the (a) rear high-low side of sample 1 and (b) the front boron diffused junction of sample 2.

Photoluminescence images, shown in Fig. 7, demonstrate the location and severity of the scratches.

QSS-PL characterization of the first sample, shown in Fig. 8, reveals that scratching the rear high-low diffusion lowers the spatially averaged minority carrier lifetime by an amount that is approximately constant at all injection levels. In this case, the first single scratch (Fig. 8, red) causes a reduction in effective lifetime of between 150 and 200 μs at

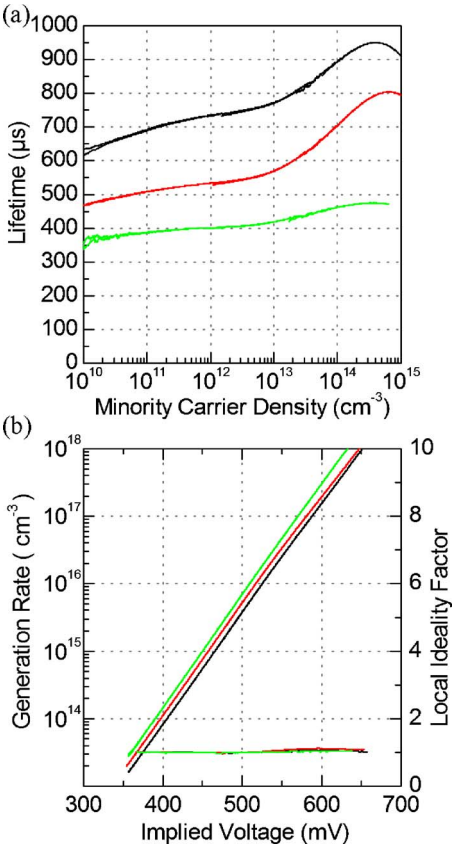

FIG. 8. (Color online) QSS-PL characterization of a 1 Ω cm n-type FZ wafer with a phosphorus diffused high-low junction on the rear surface and a boron diffused floating junction on the front and 120 nm thermal oxide on both sides: (black) initial characterization, (red) after a small scratch through the high-low junction with a diamond pen, and (green) after a large number of scratches through the high-low junction. Data are presented as (a) injection level dependent effective minority carrier lifetime and (b) pseudo-current-voltage curve and pseudo-m-V curve.

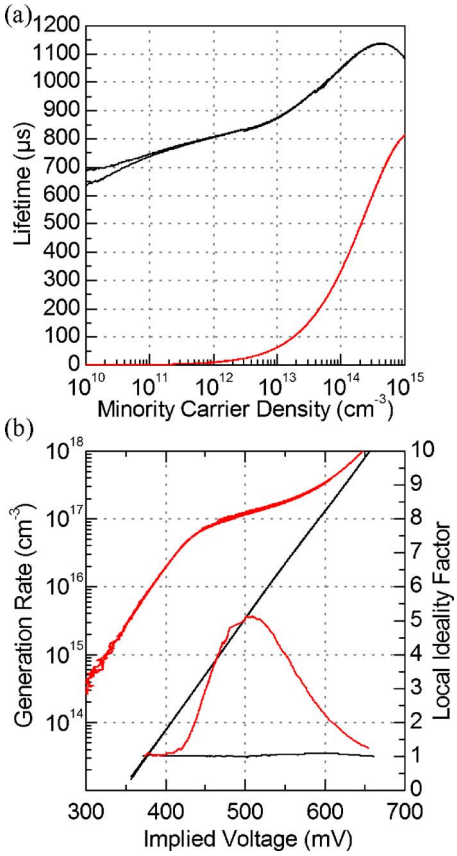

FIG. 9. (Color online) QSS-PL characterization of a 1 Ω cm *n*-type FZ wafer with a phosphorus diffused high-low junction on the rear surface and a boron diffused junction on the front and 120 nm thermal oxide on both sides: (black) initial characterization and (red) after a small scratch through the junction with a diamond pen. Data are presented as (a) injection level dependent effective minority carrier lifetime and (b) pseudo-current-voltage curve with corresponding pseudo-*m*-*V* curve.

all injection levels. Scratching the entire rear surface lowers the effective lifetime further, with a more pronounced effect at higher injection levels. In a finished device, the completely scratched rear surface lowers the open-circuit voltage by approximately 20 mV compared to the unscratched surface.

In comparison, scratching the front side *p*-*n* junction causes a significant reduction in effective lifetime, particularly in low injection conditions. The pseudo-current-voltage characteristics, shown in Fig. 9, indicate a difference in electrical performance changing from high voltages to low voltages that results in a "hump" in the pseudolocal ideality factor. In this case, the two scratches cause a small reduction in the open-circuit voltage and a large reduction in the maximum power point voltage that would significantly reduce the fill factor in a finished solar cell. Similar inflection points or "kinks" in *IV* curves of finished solar cells have been previously observed and studied in the literature. Experimental investigations and circuit simulations identified several detrimental mechanisms that cause kinks including shunted floating junction passivation[32] and resistance limited enhanced recombination in the form of damaged pyramid tips,[35] edge recombination,[32] and localized Schottky contacts between the metal fingers and base.[36] PL characterization provides a technique to investigate recombination mechanisms that dominate at lower implied voltages.

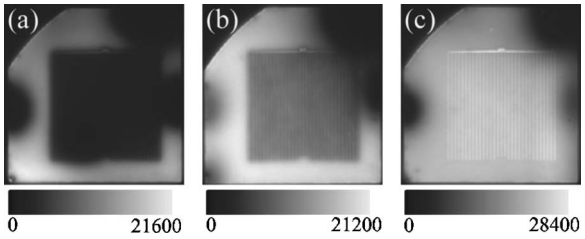

FIG. 10. ~1 sun PL images of samples after laser scribing, thermal cycling and surface passivation with prethermal cycle NaOH etch times of (a) 0 min, (b) 8 min and (c) 20 min (Ref. 47). Note the presence of tweezer marks on the edges of the wafers and encroaching on the cell area.

The QSS-PL characterization of the samples demonstrates the different effects that surface scratches have on the surface passivation provided by a high-low potential barrier and a *p*-*n* junction. In the case of the high-low barrier, the scratches have enhanced the overall recombination, particularly in regions close to the damaged area. In the case of the *p*-*n* junction, the emitter provides a path for minority carriers to reach the recombination sites, resulting in a much larger decrease in effective lifetime compared to the damage at the rear. At higher implied voltages the flow of carriers to the recombination site is resistively limited and as a result the recombination of minority carriers is reduced.

Laser-induced defects

Laser ablation combined with thermal cycles has been shown to introduce edge dislocations into the bulk of a silicon wafer.[37] With the correct use of post-ablation NaOH etching, the formation of these dislocations can be avoided.[38,39] Many solar cell structures incorporate laser ablation steps to form contacts or as an edge isolation technique or to sculpture the surface for specific cell designs.[40] A large number of dislocations are known to form recombination centers; it is therefore important to ensure that dislocations due to laser ablation are not introduced during solar cell fabrication.

Laser-formed grooves were created by ablation in three 1 Ω cm. *p*-type float zoned (FZ) wafers using a Nd:YAG (1064 nm) laser. The samples were etched using 12% NaOH for 0, 8, and 20 min and then loaded into an inert ambient and annealed for 2 h at 1000 °C. After furnace processing a second NaOH etch was performed to make the total etch time for each sample equal to 20 min. This was done to prevent any further introduction of dislocations into the sample during subsequent processing. The sample surfaces were then passivated with a phosphorus emitter diffusion and thermal oxidation. After processing the samples were characterized with PL imaging.

After thermal cycling, two of the samples [Figs. 10(a) and 10(b)] show increased recombination in the vicinity of the laser grooves due to laser-induced dislocations. The third sample (Fig. 10(c)), which was sufficiently etched to remove all laser damage, shows no enhanced recombination in the vicinity of the laser scribes. PL imaging provides an effective technique to monitor the groove etching process to ensure that laser-induced defects are not introduced.

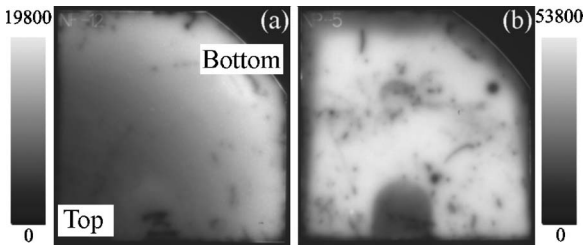

FIG. 11. ~1 sun PL image of silicon nitride passivated samples annealed at 500 °C for 5 min in (a) furnace 1 and (b) furnace 2 (Ref. 48).

All three samples display two other areas of increased recombination. The first is a region of high recombination on the left and right edges of the wafer, discussed in the wafer handling section and shown to be due to the plastic tweezers used in drying before furnace loading. The second is a region of high recombination in the top right corner, in the vicinity of the laser label used to identify samples. In this batch the laser label was scribed with a laser power that was too high and resulted in excessively deep labels that we were then unable to properly etch and diffuse.

Silicon nitride annealing

Postdeposition annealing has been shown to reduce the surface recombination velocity of some silicon nitride films.[41,42] Many of the experiments conducted to optimize this process focus on time and temperature of the annealing step. Monitoring of these experiments with PL imaging reveals that unexpected temperature gradients during annealing can have an influence on the effectiveness of the annealing. Temperature gradients within an annealing furnace occur for a variety of reasons and can result in a temperature difference of several hundred degrees across a wafer.[43]

Silicon nitride films were deposited on *n*-type, float zoned silicon wafers by plasma enhanced chemical vapor deposition using a Roth&Rau AK400 machine. After deposition half of the samples were loaded into furnace 1 for annealing and the other half were loaded into furnace 2. In both cases the samples were annealed at 400 °C for 5 min. PL images reveal that all samples annealed in furnace 1, Fig. 11(a), display a gradient in minority carrier lifetime from the top of the wafer to the bottom (top and bottom refer to the positions within the quartz boat during annealing). The samples annealed in furnace 2, Fig. 11(b), show no such gradient. Samples with this gradient have an implied open-circuit voltage that is on average 20 mV lower than the samples without such a gradient. This detrimental effect is attributed to a thermal gradient present in furnace 1 that is not present in furnace 2. The resulting different temperature profiles across the wafers affect the silicon nitride annealing process. The spatial information provided by PL imaging provides further insight into the effectiveness of an annealing process and can be used to ensure spatial effects, such as thermal gradients, do not affect the quality of an annealing process.

CELL DESIGN

During cell design, it is necessary to investigate the impact of the processing steps on device performance. PL techniques are useful for characterizing processes since they can be used directly after each fabrication step and they are capable of examining recombination at implied voltages as low as 300 mV. We have previously reported how PL was used to characterize a method of edge isolation for *n*-type silicon solar cells that involves a laser scribed isolation trench through the emitter.[44] Here we use PL to characterize a process of laser doping used to form a selective emitter.

Double-sided solar cells were prepared on 290 μm thick, polished, 1 Ω cm, *n*-type float zoned wafers. The front surface was diffused with boron (~100 $\Omega/\square$) to create an emitter and the rear surface was diffused with phosphorus (~100 $\Omega/\square$) to create a high-low junction. A 120 nm thick thermal oxide was grown on both sides for surface passivation, plating mask, and antireflection (AR) coating. Heavily doped contact regions were formed on the front and rear of the samples using a laser doping process in which a solid dopant layer is deposited on the silicon surface, then incorporated into the silicon through a laser-induced melting and recrystallization process.[45] Metal conductors were deposited on the heavily doped regions using a self-aligned electroless deposition of nickel and copper. The wafers were loaded into a furnace after nickel deposition to form a nickel silicide layer for improved adhesion and contact resistance.

The influence of the laser doping process was characterized using PL after every fabrication step. Typical PL curves, shown in Fig. 12, demonstrate the impact of the laser doping process on minority carrier recombination. On one sample (Fig. 12, gray curve), the heavy phosphorus laser doping process occurs first. After laser doping (Fig. 12, blue curve), a decrease in effective lifetime of 60 μs occurs at all injection levels. With the introduction of heavily diffused contacts it is usual to expect such an increase in recombination. This is equivalent to a drop in cell voltage of 5 mV and does not affect the fill factor of the device. On a second sample (Fig. 12, black curve), the boron laser doping is performed first. This doping process (Fig. 12, red curve) introduces an injection level dependent source of enhanced recombination, resulting in recombination statistics with an ideality factor greater than 1 and a reduction in effective lifetime at low injection levels of as much as 250 μs. The ideality factor greater than 1 indicates that some damage has occurred at the junction, which is plausible since a junction is present in the region of laser doping. When both phosphorus and boron laser doping steps are performed on a sample (Fig. 12, yellow curve), the recombination introduced by the boron diffusion dominates the device operation.

After metal plating (Fig. 12, green curve), the curve displays an inflection point or kink centered around 450 mV. Similar features have been reported in the dark *IV* curves of buried contact solar cells, that use the same metallization scheme, that are fabricated with inadequate doping in the contact regions. In these devices the kink is caused by localized points where sintered nickel makes contact to non-heavily doped parts of the cell, introducing a highly localized

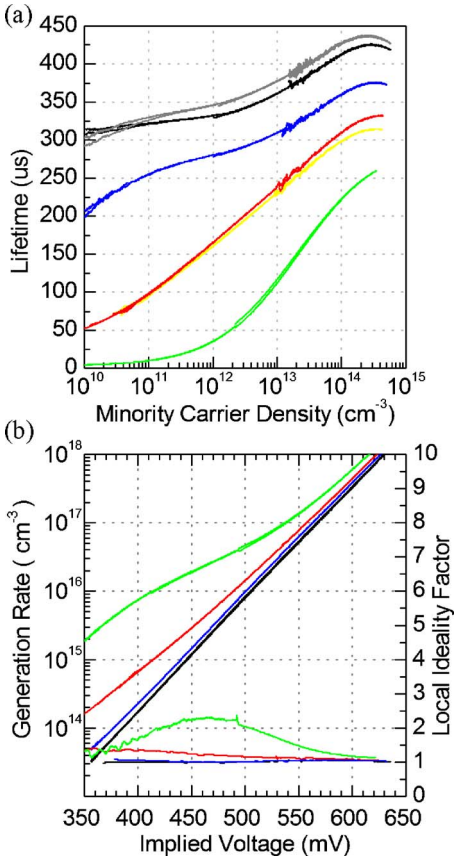

FIG. 12. (Color online) PL characterization of double-sided laser doped solar cells (black and gray) immediately after furnace diffusion, (blue) after laser doping process to form $n++$ contact, (red) after laser doping process to form $p++$ contact, (yellow) after laser doping to form both $n++$ and $p++$ contacts, and (green) finished cell with metal contacts on laser doped regions. Data are presented as (a) injection level dependent effective minority carrier lifetime and (b) pseudo-current-voltage curve with corresponding pseudo-m-V curve.

source of increased recombination.[36] Optical examination of the wafer surface after laser doping reveals the presence of some ablated holes where fluctuations in beam fluence have overheated the silicon during the doping process. These locations are poorly doped and provide sites for nickel to contact the bulk of the wafer. The PL characterization suggests that future optimization of the laser doping process should focus on the removal of these ablated regions, particularly during fabrication of the boron contact. Optimization of the nickel sintering process may also improve the performance of laser doped devices.

PROCESS MONITORING

Routine monitoring of the recombination characteristics of a batch of solar cells during fabrication is a useful technique to optimize device performance. The impact of each process step can be measured, assessed, and improved. PL techniques are extremely valuable as a tool to monitor solar cell fabrication efforts since they are fast and capable of detecting and interpreting a wide range of sources of increased recombination. Here we demonstrate the use of PL techniques to monitor the fabrication of batches of high-efficiency n-type solar cells. Solar cell fabrication followed

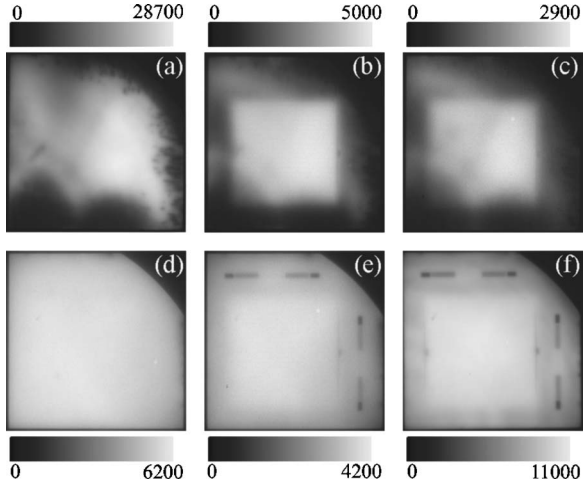

FIG. 13. ~1 sun PL image of (top) a poor quality batch of IBBC solar cells after various fabrication steps: (a) phosphorus front surface field and boron emitter, (b) heavy phosphorus base contact diffusion, (c) heavy boron emitter contact diffusion and (bottom) a good quality batch after the equivalent process steps (Ref. 47).

the process for interdigitated backside buried contact (IBBC) solar cells on n-type substrates.[46] The wafers were characterized with photoluminescence techniques after every fabrication step.

Cell characterization of poor batches of cells highlighted many issues in cell processing. One example is the spread of contamination and the effect of the heavy groove diffusion on lifetime. After the initial phosphorus surface diffusion a furnace contamination was detected in the PL images. The PL images, shown in Fig. 13 (top), demonstrate how further processing of the contaminated samples caused the contamination to be driven deeper into the wafer. After phosphorus groove diffusion the bulk lifetime of the contaminated sample improved in the region of the heavy phosphorus diffusion, which we attribute to phosphorus gettering. PL images of well processed cells, shown in Fig. 13 (bottom), show no detrimental features in the active cell area.

Monitoring our solar cell fabrication with photoluminescence for several months resulted in many changes to our fabrication sequence and process technology, including improved handling, detection of process-induced defects, and use of laser trench edge isolation. Suns-PL characterization of good quality cells incorporating these changes, shown in Fig. 14, black curves, indicates very little variation in implied voltage (>5 mV) across the batch. Similar characterization of a poor quality batch, shown in Fig. 14, red curves, indicates higher recombination and greater variation in cell performance within the batch. Continual process monitoring ensures that cell fabrication maintains the high level of performance seen in the good batch and that any anomalies are detected immediately and rectified before the next batch suffers the same fate.

CONCLUSION

Application and combination of three photoluminescence techniques, *spatially averaged QSS-PL lifetime, suns-PL*, and *PL imaging*, offer an unprecedented quality and

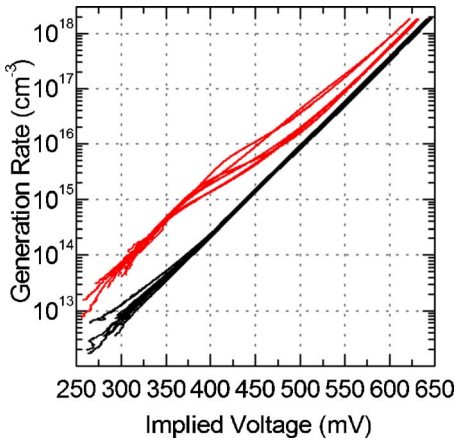

FIG. 14. (Color online) Suns-PL characterization of two batches of IBBC solar cells after the final diffusion stage: (red) poor quality batch and (black) a good quality batch incorporating process improvements discussed in this paper.

quantity of information that is beneficial for a wide spectrum of solar cell development and fabrication purposes. In a very short time, we have applied PL techniques to several key aspects of solar cell fabrication, including handling, contamination, process-induced defect generation, cell design, and process monitoring. PL techniques are fast (especially imaging), contactless, and provide complementary spatial and injection level dependent information about recombination. PL is thus a very powerful technique that is relevant to both well controlled laboratories and high-throughput solar cell factories. Routine monitoring for solar cell manufacturing requires exceptionally fast techniques, due to the high throughput of a typical line. All PL images presented here were made with a data acquisition time of 1 s per sample, which is fast enough for in-line integration in a typical production environment.

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