1.

i. (a)

ii. 因 if 之後沒有 else，且 Q 也沒有先給予一個值，所以為了讓 Q=Q，硬體部分會多合成一個 latch

2.

(a) minimum cover: B'D+CD

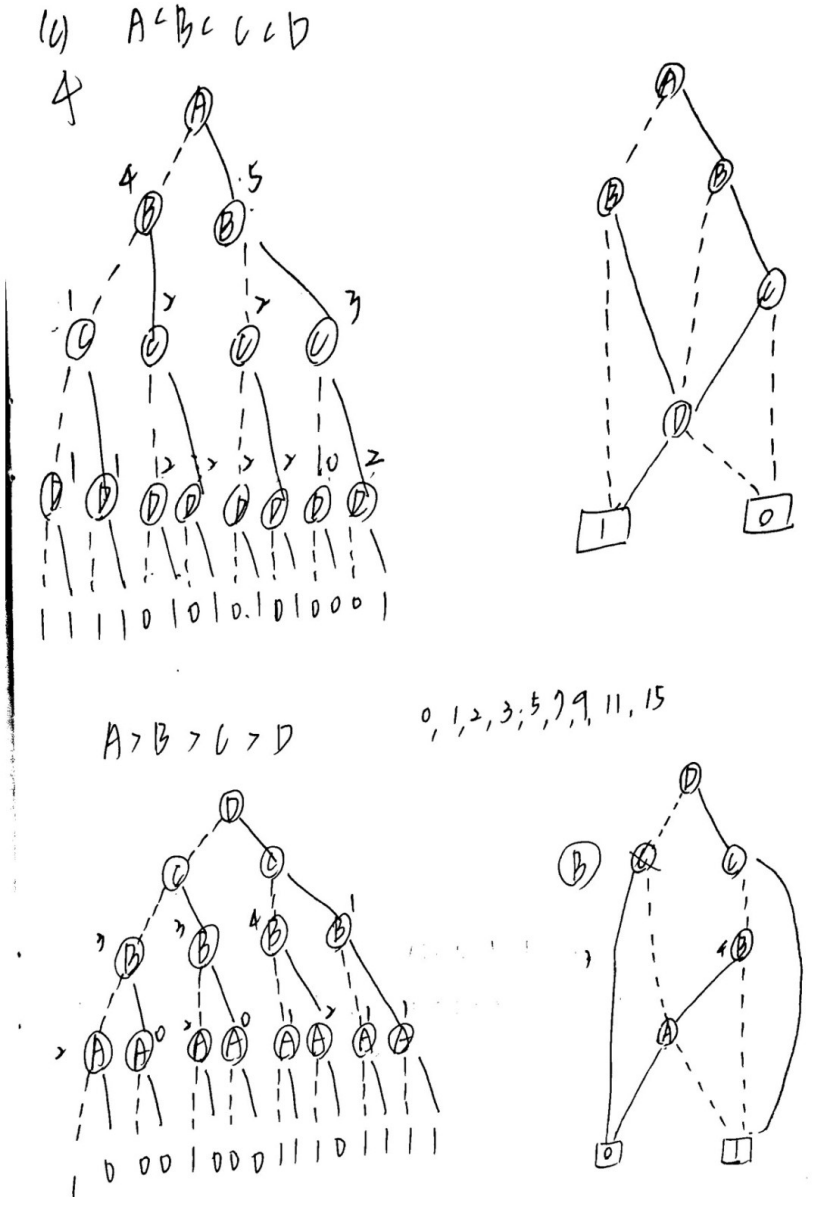
(b) P1: 10 10 11 11

P2: 10 11 11 01

P3: 11 10 11 01

P4: 11 11 01 01

(c)



(d) position cube

pro: 運算快, 資料結構簡單

con: minimum cover 難找

ROBDD

pro: tree 唯一

con: 需要較大的記憶體儲存

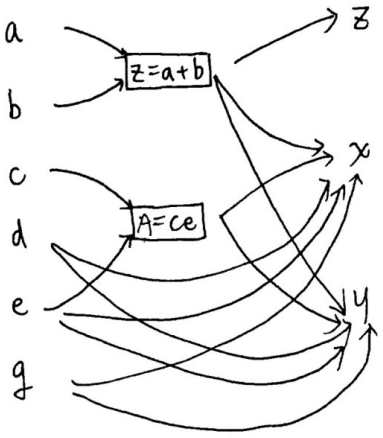
3.

(a)

	a	b	c	d	e	g
ace	1	0	1	0	1	0
bce	0	1	1	0	1	0
de	0	0	0	1	1	0
g	0	0	0	0	0	1
ad	1	0	0	1	0	0
bd	0	1	0	1	0	0
cde	0	0	1	1	1	0
ge	0	0	0	0	1	1
a	1	0	0	0	0	0
b	0	1	0	0	0	0

co-kernel : ce、de

(b)



X= Az+de+g before : 9+9+2=20 literals 、after : 5+5+2+2=14 literals

y= zd+dA+ge = d(A+z)+ge

z = a+b

A= ce

(c)

從 two-level circuit → multi-level circuit

Advantage : 可共用 gates , area ↓

Disadvantage : Multi-level circuit delay 變長

合併後的新 variable 也會佔 literal 數目

所以不一定能使 literal 數下降

4. Split: split the fanouts of a gate into several parts. Each part is driven with a copy of the original gate, loading decrease -> timing improve

Critical path collapsing: reduce the depth of logic networks, length of critical path decrease -> timing improve

Different: split 沒有改變深度，而 Critical path collapsing 則會

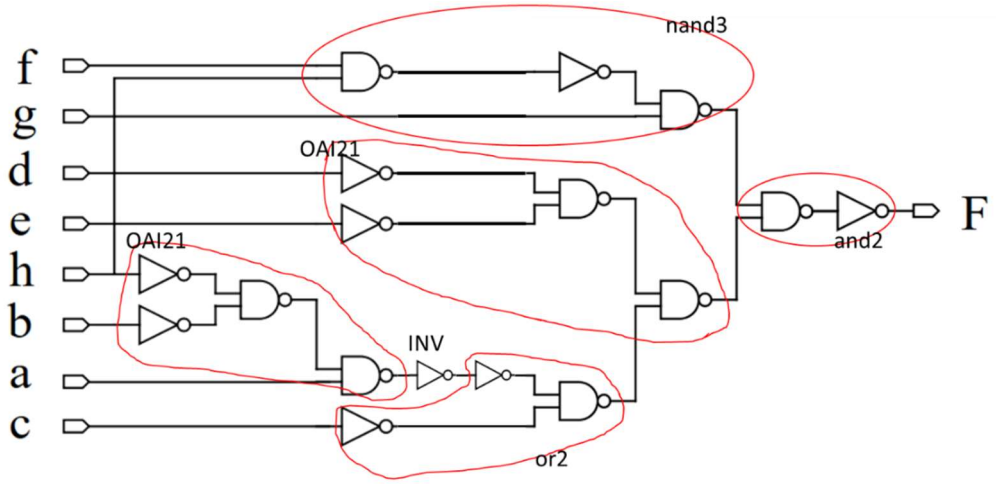
5.

i. supply voltage/ threshold voltages/ frequency

ii. Power Gating, Power gating design can reduce the leakage power when the block is powered off/ Power gating further reduces the standby power,

iii. Not always. Require longer wakeup time in the WAKE event, area increasing or IR drop…

6.



Minimum gate count = 6

7. (a)

gate	delay(ps)
1	4
2	2
3	12.5
4	6.65
5	5.65
6	9.44

(b)

longest sensitizable path:

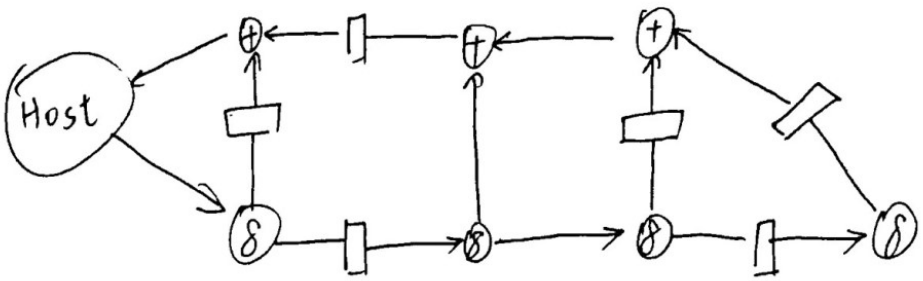
G1 → G3 → G4 → G6

path delay = 4 + 12.5 + 5.65 + 9.44

= 31.59 ps

8.

(a)



(b) critical path 上的 propagation delay 變小，

⇒ clock period 減小 (frequency 提高)