Institute of Electronics
Nat'l Yang Ming Chiao Tung Univ.

Final Exam
Jan. 4, 2023

Special Topics in Computer-Aided Design (IEE6661)

1. (15%) What are the keys to reduce power consumption at system level? In terms of power reduction, what are the difference between DVFS and clock gating techniques? What are the pros and cons of those two low-power techniques??

2. (15%) What are the difficulties for system verification of SoC designs? Why do we often use FPGA to help the verification of SOC designs? Do we have any other approach to verify the HW/SW integration at design stages? If any, please briefly explain how it works.

3. (10%) What is the purpose of using code coverage in simulation-based functional verification? Besides coverage analysis during, how can it help the other steps in the verification flow? Please briefly explain your reasons.

4. (10%) What are the pros and cons of using the simulation-based and formal-based approaches for functional verification? What are the keys to improve the capability of formal-based verification??

5. (15%) What are the difficulties for mixed-signal system verification? If analog behavioral models are available, how can it help the mixed-signal verification? What are the differences to build the models with Verilog and Verilog-A?

6. (10%) Given a 2-bit DAC circuit, please show the analog section of the behavioral model for this circuit based on Verilog-A. The maximum input voltage is 1.0V, and the signal frequency is 250MHz. The output signal has a 0.5ns rising time and a 0.4ns falling time, and its input-to-output delay time is 1ns.

7. (15%) Why does the difference between synthesis results and post-layout simulation often exist in analog circuits? If equation-based approach is used for analog design automation, how can I solve this issue? Please give at least two possible approaches with brief explanations about the reasons.

8. (10%) How to consider the layout-induced parasitic effects in analog behavior model and circuit sizing?