2018

1. (15%) What is power gating technique? What are the benefits of using this technique? Can we always gain power reduction by using power gating? Please briefly discuss the possible issues and limitations while using this technique.

A:
Power gating是在某些block不需要用到的時候關掉電源，以降低leakage power
由power switch fabric、Isolation and retention cell、Power controller組成
Benefits:可以降低leakage power
不一定always reduce power，比如用scan chain去restore data的話，會導致energy增加
Possible issues:Performance degradation:IR drop、in-rush current的noise

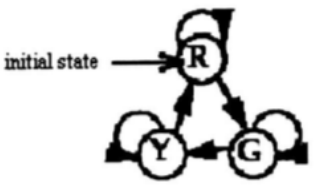
2. (15%) What are the advantages of using code coverage in simulation-based functional verification? If you got 100% statement coverage in the simulation, does it guarantee that the design is correct? Please explain the reasons of your answer.

Code coverage可以讓我們知道比如說哪幾statement、Path、toggle的被執行次數，相較於完全隨機的test pattern，可以有效減少需要的test pattern數
Quantitative sign-off criterion、Verify more but simulate less!
100% statement coverage不代表一定正確，只代表每個statement被執行過，無法確認functionality正確性，不知道電路實際行為是怎樣

3. (15%) What are the advantages and disadvantages of formal verification? What are the keys to improve the efficiency of formal verification??

優點: Ensures consistency with specification for all possible inputs (100% coverage)、Solve the completeness problem in simulation based methods
缺點:not general、memory intensive、Memory usage is strongly related with the size of systems to be verified、model checking有State explosion problem
如何improve:選擇適合的formal verification方法，比如CEC可以依照design的structure去決定要用BDD based還是learning based會比較有效率

4. (10%) Do the CTL formulas below satisfy the STG shown right ? Please answer "TRUE" or "FALSE".
   (a) **EG**(RED)
   (b) **AF**(GREEN)
   (c) **E**(RED **U** GREEN)
   (d) **A**(RED **U** GREEN)
   (e) **AG**(RED → **EX**(GREEN))

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5. (10%) Using the CTL formulas, how can we verify the design functionality? What are the issues of CTL-based verification?

Computation Tree shows all of the possible executions starting from the initial state of an FSM
再依據spec設計Computation Tree Logic formulas 去做state traversal，看有沒有違反CTL formulas
Issue: state explosion problem。可以用Symbolic Model Checking(SMC) BFS去做implicit state traversal解決

6. (10%) Why do we need analog behavioral models for mixed-signal system verification? Compared to the original Verilog language, what are the major extensions of Verilog-AMS?

Allow system simulation and architecture verification、
Allow mixed-level simulation with other digital circuits、Faster simulation time:
Allow whole chip simulation

Major Extensions:可以用mathematical equations 去model 類比電路的behavior
比如:

```
analog begin
        V(out) <+ (gain * V(in))+vdd-(id*rd);
end
```

7. (10%) Given a 4-phase sin-wave generator, please show the analog section of the behavioral model for this circuit based on Verilog-A. Its output voltage swing is 1.0V with 0.4V DC shift, and the phase difference between consecutive outputs is 90°. The signal frequency is 250MHz with maximum slew rate ±80MV/sec.

```
electrical n1,n2,n3,n4,out1,out2,out3,out4;
parameter real freq = 2.5e8;
analog begin
   V(n1) <+ 0.4+sin(2 * `M_PI * freq* $abstime);
   V(n2) <+ 0.4+sin(1/2 * `M_PI * freq* $abstime);
   V(n3) <+ 0.4+sin(1 * `M_PI * freq* $abstime);

   V(n4) <+ 0.4+sin(3/2 * `M_PI * freq* $abstime);

    V(out1) <+ slew(V(n1), 8.0e7 -8.0e7);
    V(out2) <+ slew(V(n2), 8.0e7 -8.0e7);
    V(out3) <+ slew(V(n3), 8.0e7 -8.0e7);
    V(out4) <+ slew(V(n4), 8.0e7 -8.0e7);
end
```

8. (15%) What are the benefits and limitations of simulation-based approach and equation-based approach for analog design automation? Why does the difference between synthesis results and post-layout simulation often exist?

Simulation-based:
Benefits: Accurate
Limitations: time-consuming、Hundreds of simulations may be required ->long simulation time

Equation-based:

Benefits:可用Geometric programming(GP ) solver find a feasible solution with minimum (or maximum) cost 、所花時間較Simulation-based短

Limitations : Simplified equations and parameter models often limit the accuracy of equation-based approaches

因為synthesis results並沒有實際routing、placement的足夠資訊，所以結果會和實際layout完的 post layout simulation有落差