Inst. of Electronics Engineering
National Chiao-Tung University

Midterm Exam
Nov. 6, 2019

Special Topics in Computer-Aided Design (IEE6661)

1. (5%) Given the following codes, which one will have the most gate counts after synthesis? Please briefly explain your reasons.

a)
```
input en,D;
reg Q;
always@(en or D)
  if (en) Q = D;
```

b)
```
input en,D;
reg Q;
always@(en or D)
  if (en) Q = D;
  else Q = 0;
```

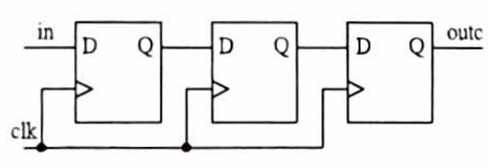
c)
```
input en,D;
reg Q;
always@(en or D)
  Q = 0;
  if (en) Q = D;
```

d)
```
input en,D;
output Q;
assign
  Q = en? D: 0;
```

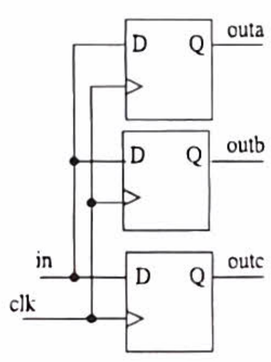
2. (5%) Given the Verilog code shown right, which one is most likely the corresponding circuit after synthesis? Please briefly explain your reasons.

```
input in;
output outa, outb, outc;
always @(posedge clk) begin
    outa = in;
    outb = outa;
    outc = outb;
end
```

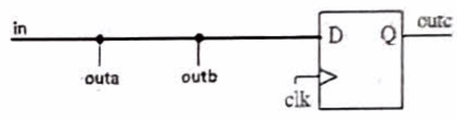
a)



b)



c)



d)
none of the above

3. (5%) If a two-level circuit is implemented to a multi-level circuit, what are the possible advantages and disadvantages of this change?

4. Consider the logic network defined by the following expressions:

x = abc + abd + ac'd' + b'c'd'

y = ace + ade + b'ce + b'de

z = c + d

x: (c+d)ab + (c+d)'(a+b')

y: (c+d)e(a+b')

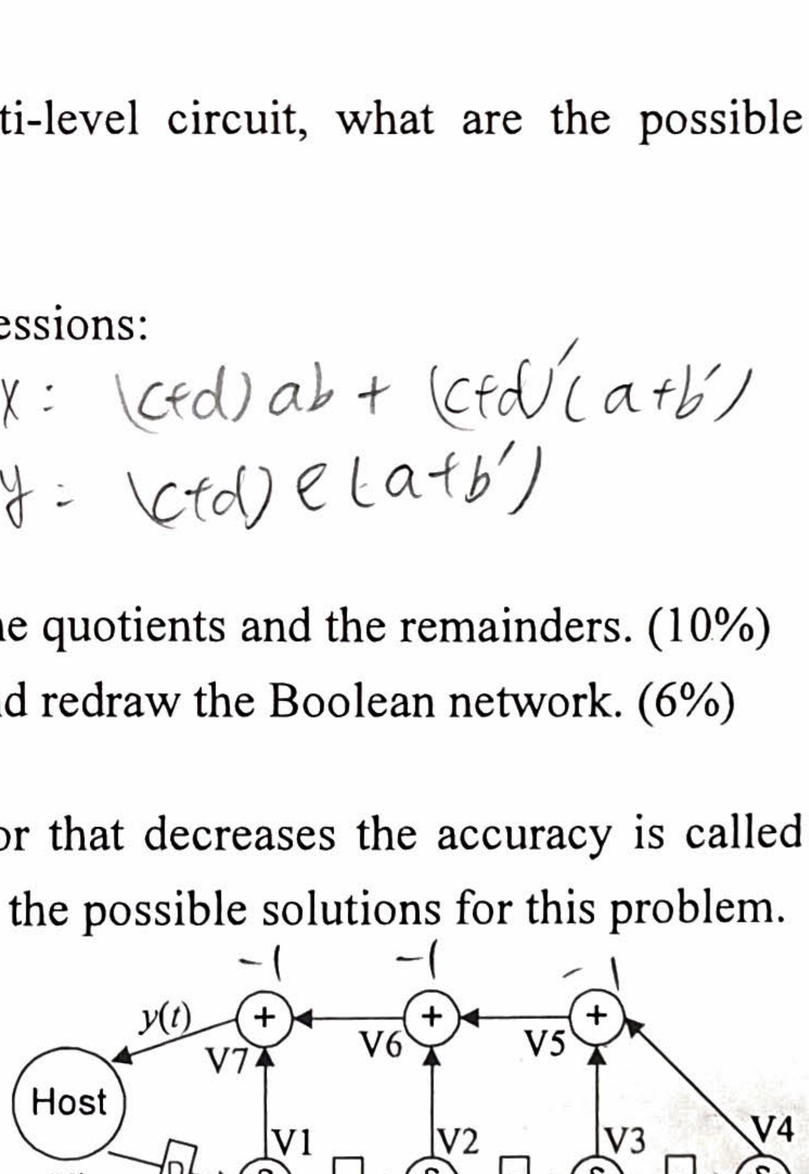
(a) Perform both x/z and y/z (weak division) and show the quotients and the remainders. (10%)

(b) Find the common sub-expression between x and y, and redraw the Boolean network. (6%)

5. (6%) In static timing analysis, one of the possible factor that decreases the accuracy is called false path. Please explain what a false path is and discuss the possible solutions for this problem.

6. (10%) For the circuit shown right:

Given a retiming (r1=-1, r2=-2, r3=-2, r4=-2, r5=-1, r6=-1, r7=-1), please redraw the new circuit after retiming.



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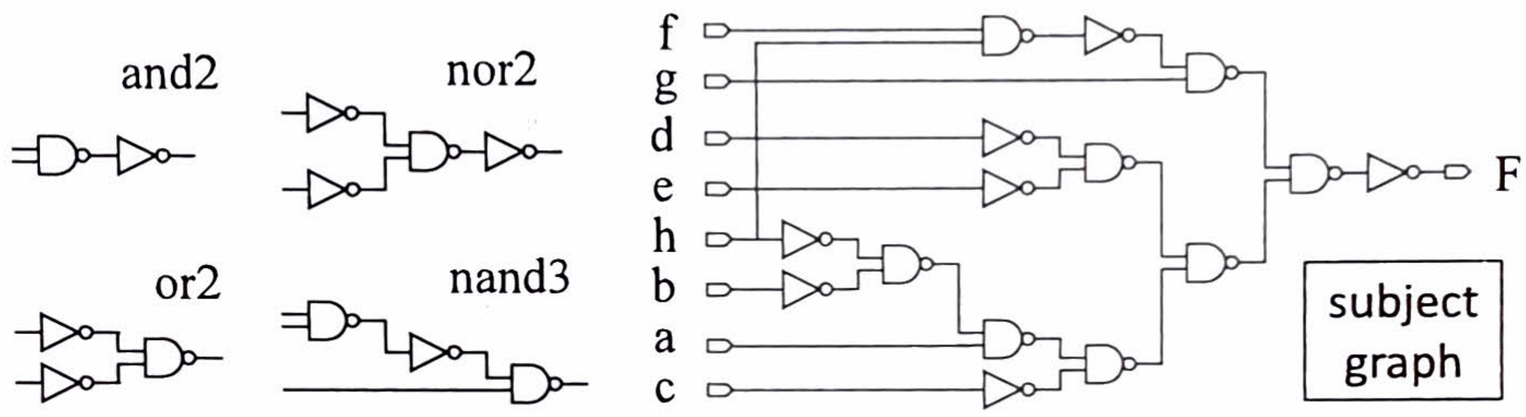
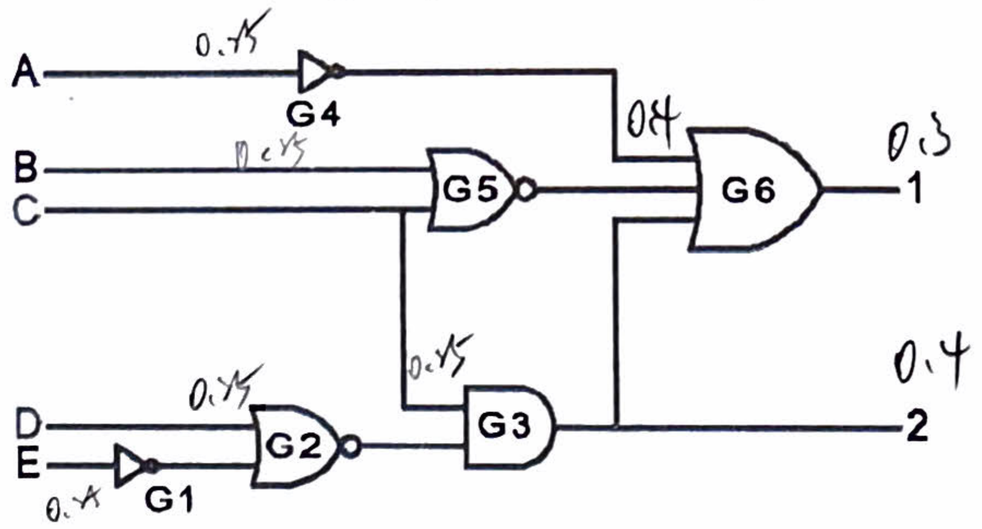
7. In the Boolean function F(A,B,C,D) = ∑(4,5,8,10,12,13,14) with don't care d(A,B,C,D) = ∑(0,2,9,15), there are 4 possible prime implicants, P1=AB, P2=AD', P3=BC', P4=C'D'.
   (a) Please find the minimum cover of this function by using column covering method. (8%)
   (b) Please show the positional cube representation of this function. (4%)
   (c) Please explain how to test whether P1 and P3 are able to apply REDUCE operation with the representation in (b). You don't have to show the REDUCE results. (4%)

8. (12%) Assume the available gates in the cell library are INV, AND2, OR2, NAND2, NOR2 and NAND3. The cost of INV is 1, the cost of NAND3 is 3, and the cost for other cells is 2. Inverter pairs are also allowed. Given the gate-level circuit shown below, what is the minimum cost after mapped to the given cell library? In addition, please also redraw the best covering on your answer sheet.



9. (5%) One popular technique to improve circuit timing is called "buffer insertion". Please discuss why and when this approach can improve the circuit timing. In your opinions, can we always get timing improvement by this technique??

10. Assume the delay time of each gate can be determined by the following lookup table. But the delay time of an inverter is only a half of the value obtained from the table. In order to simplify the calculation, the signal transition time is assumed as 50ps at each node in this problem. Assume the input capacitance of those gates is 0.25fF per input pin except G6, whose input capacitance is 0.4fF only. The output loading are 0.3fF and 0.4fF at node 1 and 2 respectively.
    (a) Please find the delay of each gate according to the lookup table. (12%)
    (b) Please find the longest path and its delay value for this circuit. (8%)



Total Output Load (fF)

Input Transition (ns)	0.2	0.3	0.4	0.5
0	3	5	7	10
0.1	4	7	11	15

Cell Delay (ps)