Inst. of Electronics Engineering
National Chiao-Tung University

Midterm Exam
Nov. 7, 2018

Special Topics in Computer-Aided Design (IEE6661)

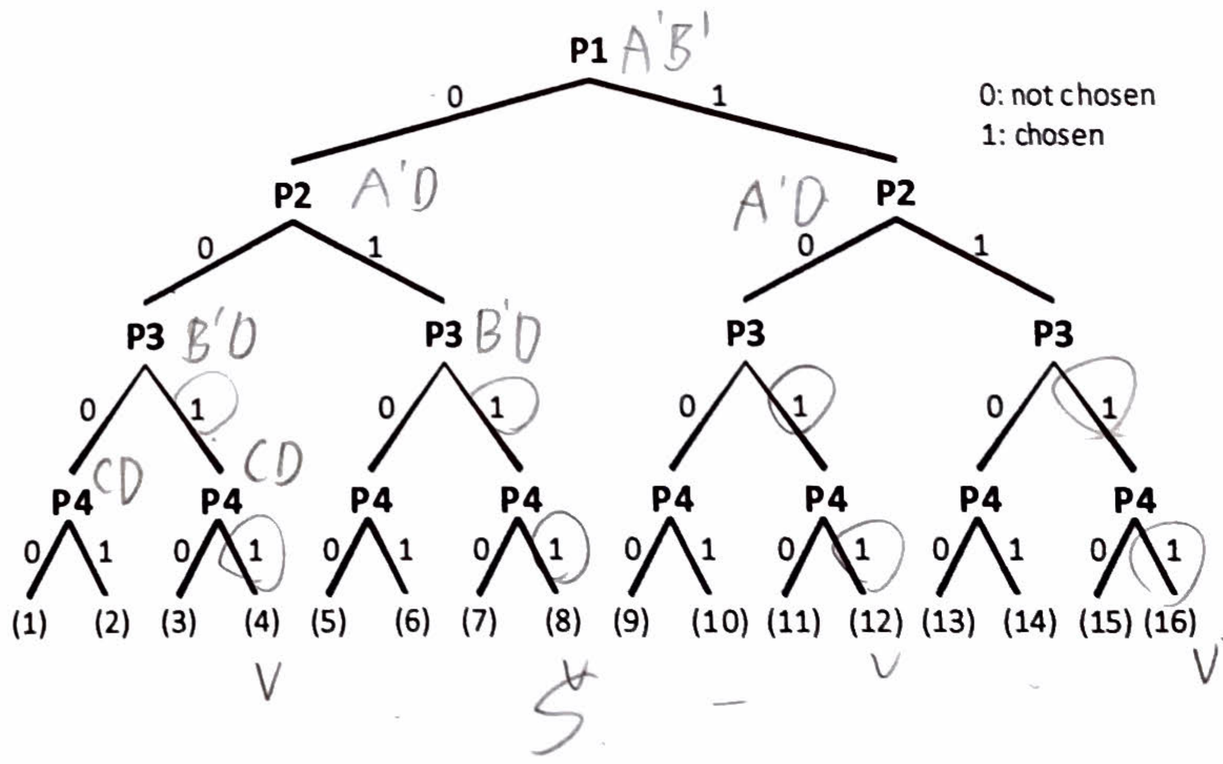
1. (6%) Please explain the conditions for generating a latch and a flip-flop and in the RTL synthesis step and give an example for each case using Verilog descriptions.

2. (6%) If a two-level circuit, f = ac + ad + bc + bd + e, is implemented to a multi-level circuit, f = (a + b)(c + d) + e, what are the possible advantages and disadvantages of this change?

3. (6%) One popular technique to improve circuit timing is called "splitting", which splits the fanouts of a gate into several parts. Each part is driven with a copy of the original gate. Please discuss why and when this approach can improve the circuit timing.

4. (a) Given a Boolean function F(A,B,C,D) = ∑(0,4,6,8,13,14) with don't care d(A,B,C,D) = ∑(2,9,12). Please use Quine-McCluskey algorithm to find all the prime implicants. (12%)
   (b) For the Boolean function in (a), please draw the corresponding ROBDD of it using the variable order A>B>C>D. (6%) don't care term are set to 1.
   (c) Can you generate the prime implicants from the BDD in (b)? Please briefly explain your reasons. (4%)

5. (8%) In the Boolean function F(A,B,C,D) = ∑(1,3,7,9,11,15) with don't care d(A,B,C,D) = ∑(0,2,5), there are 4 possible prime implicants, P1=A'B', P2=A'D, P3=B'D, P4=CD. Therefore, there are total 16 combinations of those 4 prime implicants as shown right. Assume we search the valid combinations with the least number of prime implicants from left to right by using the branch-and-bound algorithm. For each combination, please give a mark 'V' for valid case, a mark 'X' for invalid case, and a mark 'S' for the skipped case.



6. Consider the logic network defined by the following expressions:

   x = ace + bce + de +g

   y = ad + bd + cde + ge

   z = a + b

   (a) Perform both x/z and y/z (weak division) and show the quotients and the remainders. (10%)
   (b) Substitute z into x and y and redraw the Boolean network graph. (4%)

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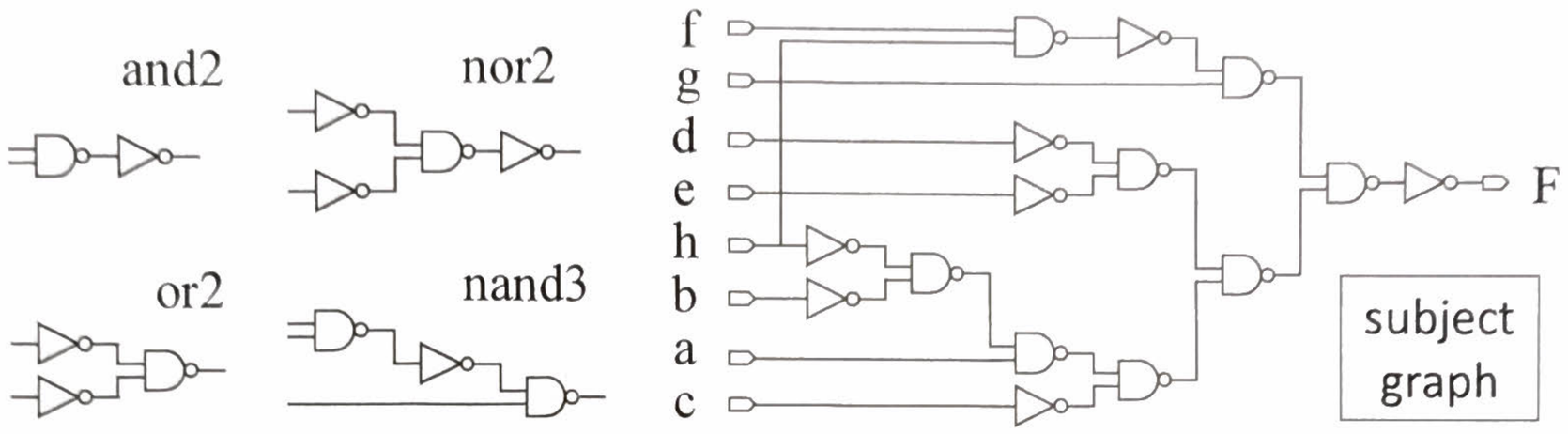
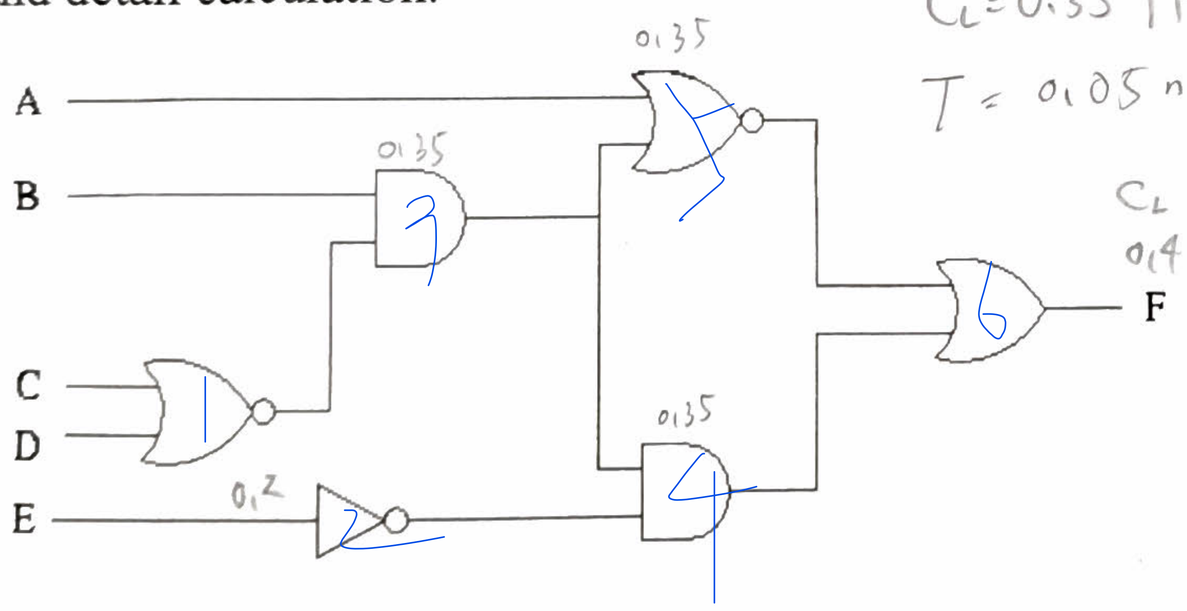
7. (12%) Assume the available gates in the cell library are INV, AND2, OR2, NAND2, NOR2 and NAND3. Given the gate-level circuit shown below, what is the minimum gate count after mapped to the given cell library? In addition, please also redraw the best covering on your answer sheet.



8. (12%) Assume the delay time of each gate can be determined by the following lookup table. But the delay time of an inverter is only a half of the value obtained from the table. In order to simplify the calculation, the signal transition time is assumed as 50ps at each node in this problem. Assume the input capacitance of those gates is 0.35fF per input pin except the inverter, whose input capacitance is 0.2fF only. The output loading at node F is 0.4fF. Please find the longest and shortest paths individually in the circuit shown below along with their delay values and detail calculation.

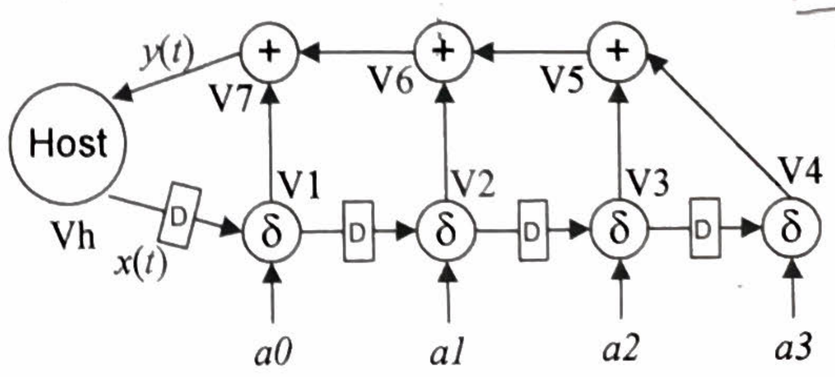


Total Output Load (fF)

Input Transition (ns)	0.2	0.3	0.4	0.5
0	3	5	7	10
0.1	4	7	11	15

Cell Delay (ps)

9. For the circuit shown right:



(a) Given a retiming (rh=0, r1=-1, r2=-1, r3=-2, r4=-2, r5=-1, r6=-1, r7=0), please redraw the new circuit after retiming. (8%)

(b) Assume the delay of each component is: Host=0, adder(+)=6ns, comparator(δ)=3ns, flip-flop(D)=0. What is its minimum clock period of the retimed circuit? (6%)