

Midterm**1. Design Style (10pts)**

Please answer the following statements (true or false).

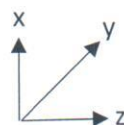
(2pts for each correct answer, extra penalty 2pts for each wrong answer)

- Gate Array design style can simplify the manufacturing process.
- Standard cell design style is not convenient for developing CAD tools.
- Full custom design style is very suitable for developing high-end CPUs.
- The design cycle time in standard cell design style is longer than that in gate array design style.
- Cell library does not need to be updated when technology advanced in standard cell design style.

2. Logic Basics (12pts)

Given $F = x'y'z' + x'yz + x'z' + y'z + xyz$, please answer the following questions:

- The minterm expansion of F' (3pts)
- The truth table of F (4pts)
- The *ON-set* and *OFF-set* of F (2pts)
- Blacken the corresponding corners in the given cube (3pts)



3. Two-Level Logic Minimization (20pts)

Assume $F = abc + a'bc + ab'c + abc'$, answer the following questions.

- Implement F using PLA (4pts)
- Use the Quine-McCluskey method to identify all prime implicants (6pts) and find the minimum cover of F (4pts)
- Given don't care $ab'c'$, perform "expand" operation in Espresso and show details. (6pts)

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1 1 1
0 1 1
1 0 1

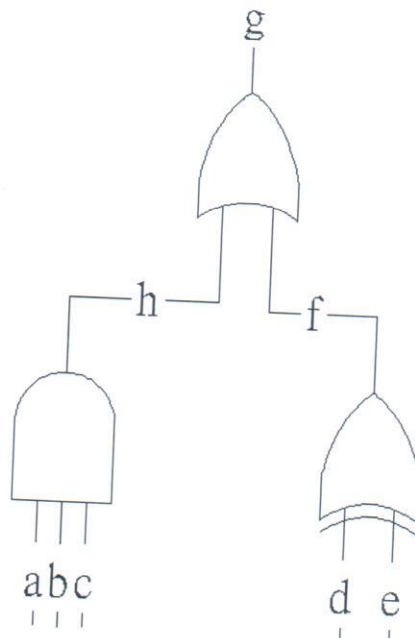
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4. Factor and Cofactor (10pts)

- Find the cofactor of $F = y'z + x'y + xz$ with respect to z (3pts)
- Is the result a tautology? Why? (7pts)

5. Optimization using Don't Care (10pts)

- In the following circuit, assume that $ODC_g = 0$, compute ODC_d (5pts) (Show your answer in terms of primary inputs.)



- b. Consider the logic network defined by the following expressions:

$$d = b'$$

$$f = (ad)'$$

$$e = (c + a)'$$

$$x = fe$$

$$y = d \oplus e$$

inputs are $\{a, b, c\}$, and outputs are $\{x, y\}$. If there is a cut $\{a, d, e\}$, compute $CDC_{cut}.$ (10)

6. Multiple-Level Logic Optimization (22pts)

- a. There are 6 expressions A-F, answer the following three questions:

A. $a + bc$

B. $(a + b)'c$

C. $(a + b)(c + d)$

D. $c(a' + b + c') + bd$

E. $(a + b + c)(a' + b + c)$

F. $(a + bc)d$

1. Which expressions are in the factored forms (2pts)?

2. Which expressions are in the algebraic factored forms (2pts)?

3. Which expressions are cube-free (2pts)?

- b. Apply the weak division procedure to the algebraic expression

$$F = abrs + abrt + abd + abe + abu + ghrs + ghrw + ghd + ghe + ghu + dp + eq + rstuw$$

with the divisor $D = ab + gh$. Show $Q = F/D$ and R . (8pts)

- c. For $F = uwxy + uvxy + tx + tz + rsw + rsv + vwxy$, find all kernels you can possibly find. (8pts)

7. Static Timing Analysis (16pts)

The delay graph is as follows. For all gates, the maximum delay and minimum delay are the same. The associated number above each gate is the delay of the gate.

- Why is it called STA? What is the difference between STA and dynamic timing analysis? (3pts)
- Please find the minimum and maximum delay from source to sink.
(4pts/4pts)
- Assume the required time at the sink is 12, do all the paths meet the constraint? If not, list the violation paths. (5pts)

