Inst. of Electronics Engineering
Nat'l Yang Ming Chiao Tung Univ.

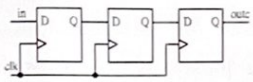
Midterm Exam
Nov. 9, 2022

Special Topics in Computer-Aided Design (IEE6661)

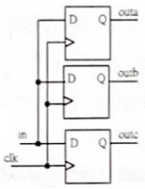
1. (5%) Given the Verilog code shown right, which one is most likely the corresponding circuit after synthesis? Please briefly explain your reasons.

```
input in;
output outa, outb, outc;
always @(posedge clk) begin
    outa = in;
    outb = outa;
    outc = outb;
end
```

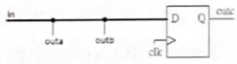
a)



b)



c)



d) none of the above

2. (5%) For an always statement with multiple edge-triggered signals, how to determine its clock pin and asynchronous control pins?

3. (a) Given a Boolean function F(A,B,C,D) = ∑(4,5,8,10,12,13,14) with don't care d(A,B,C,D) = ∑(0,2,9,15). If we would like to use Quine-McCluskey method to optimize this Boolean function, the first step is to sort all possible minterms. Please show the sorting results for this function F. (3%)

   (b) During the optimization, C1=A'BC', C2=A'C'D', C3=ABC' are three possible cubes. Please use the positional cube representation to represent the three cubes. (3%)

   (c) In (b), please use positional cube representation to test whether C1 and C2 can be merged to become a larger cube. Please also test the merging possibility for C1 vs C3. (4%)

   (d) Finally, there are 4 possible prime implicants, P1=AB, P2=AD', P3=BC', P4=C'D'. Please find the minimum cover of this function by using column covering method. (8%)

   (d) If ESPRESSO heuristic approach is adopted, why the complexity of logic optimization can be reduced? Does it always find the best result? (5%)

4. Consider the logic network defined by the following expressions:

   x = ab'c + ace + bcd + b'd + de, y = ac + d

   (a) How can we know if some part of function x can be substituted by function y? Please show your calculation process and explain your result. (8%)

   (b) In (a), do we really get improvement with the possible substitution in terms of the total number of literals? (3%)

   (c) After substitution, the two-level circuit is converted to a multi-level circuit. What are the possible advantages and disadvantages of this change? (5%)

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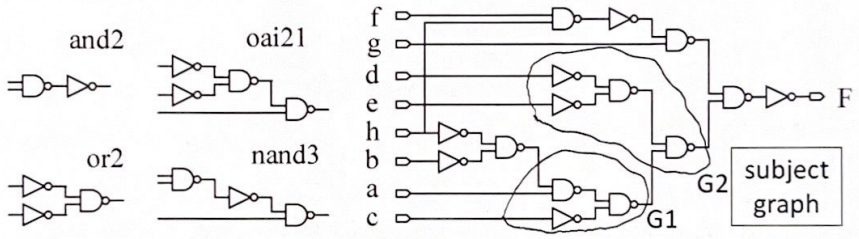
5. (a) In timing optimization, what are the key factors that need to be considered? Please briefly explain your reasons. (5%)
   (b) There is a timing optimization technique called "timing decomposition". Why can it improve the overall delay time? What is the possible cost of using this technique?? (5%)

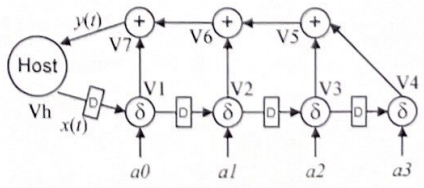
6. Assume the available gates in the cell library are INV, AND2, OR2, NAND2, OAI21 and NAND3. Inverter pairs are also allowed. Assume the input capacitance of OAI21 and NAND3 are 0.5fF for each input pin, and the input capacitance of other gates are 0.3fF for each input pin. Given the gate-level circuit shown below, please answer the following questions after mapped to the given cell library.



   (a) For group G1, how many choices do you have to implement this area? What is the related cost in terms of the number of gates? Please redraw every possible implementation results for group G1 on your answer sheet. (5%)
   (b) For group G2, you can implement the final node as NAND2 or OAI21. In terms of the total capacitance on each signal net (including the input pins to this area), which selection is better for low power purpose? Please explain your reasons. (5%)

7. (a) Why dual Vt design technique is able to reduce the overall power consumption? What is the possible overhead of this technique? (5%)
   (b) If dual Vt technique is applied in a single gate, it is called a mixed-Vt gate. Please explain the pros and cons of adopting mixed-Vt gates to implement digital circuits. (5%)

8. For the circuit shown right:
   (a) Given a retiming (rh=0, r1=-1, r2=-1, r3=-2, r4=-2, r5=-1, r6=-1, r7=0), please redraw the new circuit after retiming. (8%)
   (b) Since the adders and comparators are not changed, what is improved by the retiming technique? In which situation will you obtain more speedup through retiming? (5%)



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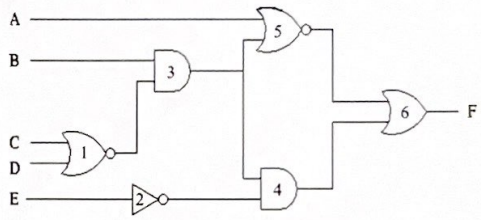
9. (8%) Assume the delay time and input capacitance of each gate can be determined by the following lookup table in liberty format. But the delay time of an inverter is only a half of the value obtained from the table. In order to simplify the calculation, the rising delay and falling delay are assumed to be the same. The delay values from different inputs are assumed equal, too. Rising time and falling time are also obtained from the same table. Assume the initial input transition time is 0.02 ns, and the output loading are 3fF at node F. What is the delay of gate 3 in this case?




```
lu_table_template(table10){
  variable_1 : total_output_net_capacitance;  // pF
  variable_2 : input_transition_time;  // ns
  index_1 ("0.002,0.003,0.006,0.013,0.025,0.050,0.100");
  index_2 ("0.020,0.035,0.060,0.120,0.210,0.420,0.830");
}
cell (NANDX1) {
  pin(A1) {
    direction: input;
    capacitance: 0.007;
  }
  pin(A2) {
    direction: input;
    capacitance: 0.007;
  }
  pin(ZN) {
    direction: output;
    capacitance: 0.0;
    internal_power() {…} // power omitted in this example
    timing() {
      cell_rise(table10) {  // cell delay at output rising
      value("0.013,0.016,0.020,0.023,0.030,0.040,0.050",\
      "0.015,0.019 0.023,0.026,0.037,0.047,0.060",\
      "0.019,0.022,0.028,0.033,0.046,0.060,0.077",\
      "0.026,0.030,0.033,0.043,0.055,0.080,0.104",\
      "0.040,0.041,0.046,0.059,0.076,0.099,0.147",\
      "0.066,0.069,0.073,0.084,0.108,0.144,0.189",\
      "0.122,0.124,0.129,0.139,0.160,0.209,0.279");
      }
      cell_fall(table10)   // cell delay at output is falling
      value(…);  // assume the same with rising
      rise_transition(table10)  // output rising time
      value(…);  // values are the same with cell_rise
      fall_transition(table10)  // output falling time
      value(…);  // values are the same with cell_fall
    }  // end timing
  }  // end pin
}  // end cell
```