CH6 Intro to SoC verification

P9.SoC pros
P10. Soc Challenges
P13. 為何 verification 重要 -> verification bottleneck
P15-P23 Integration(Hardware vs Software/Digital vs Analog/Testing issues)
P16. Hardware software integration -> system level design
P18. Mixed Signal(MS) Design 的 challenges 和 solutions
P19. Soc 的 Testing Challenges
//
P25. What is Verification
P26. Testing v.s. Verification
P28. When is verification complete? (why we need verification)
P30. Verification Approaches(Top-down/Bottom-up/Platform-based/System interface-based)
P31. Bottom-up verification Steps
//
P33. Design Sign-Off
//
P36. P37. Simulation-Based Verification (優缺點 & how to improve) / Simulator Improvements(Event-driven/Cycle-based/Transaction-based/Assistant hardware)
P38. Coverage-Driven Verification (coverage report/optimize regression suite/…)
P40. Testbench Automation (Generator/Predictor)
P41. Assertion-Based Verification (What is Assertions / How it can help design/ Avantage)
//
P42-P45 Static Verification Techniques
P43 HDL Linter
P44 Formal Verification (What is formal verification/ Advantage / Disadvantage)
P45 STA Static Timing Analysis
//
P46-P52 System Verification Solutions (Hardware vs Software / Digital vs Analog)
P47 Prototyping
P49 HW/SW Co-simulation
P52 System Verification : (key : unified verification platform / system -level language : System-C, System Verilog…)
//
P54 傳統 MS Design Approach
P55 Top-Down MS Design Flow
P56 Analog Behavioral Modeling (what is analog Behavioral Modeling / advantage)

P57 Keys to a good behavioral model
P58 Analog non-ideal effects -> Top-Down Modeling
P59 Bottom-Up Modeling Approach
P60 Bottom-Up Behavior Extraction 流程圖
//
P64 Reusing existing IP and platforms is the key / Verification bottleneck

CH7 Coverage-Driven Functional Verification

P8 Simulation-Based verification 評價
P9 Coverage-Driven Verification (coverage report/goal/優點) verify more but simulate less
P10 Coverage Report “Untested Code” line will be highlighted
P11 Typical Coverage-Driven Verification 流程圖
//
P15 Functional Coverage Metrices (Code coverage/FSM coverage/Other coverage)
// code coverage
P16 Statement Coverage
P17 Decision Coverage
P18 Path Coverage
P19 Expression Coverage(most popular3 analysis method)
P20,P21 Multiple sub-condition coverage (2 的 N 次),Basic Sub-Conditon
P22 Focused Expression Coverage (only N+1 patterns) x = (a&&b) || c -> check points -> for 100% coverage, only 4 patterns is required
P23 Toggle Coverage(bit 切換)
P24 Observability-Based Code Coverage **tag△**
P25 Probabilistic Observability Measure observable (機率)
P26 Assertion Coverage (可讀取的 comments/what is assertion/優點)
//
P27 Functional Coverage 優點/缺點/如何改善/difficulty -> FSM coverage is another option
P28 Conventional FSM coverage
P29 Semantic FSM coverage (從超多 state 與 state 的轉換化簡來 reduce complexity)
P30 不同階段要用的不同 code coverage 的方法 (Behavior 階段/RTL 階段/Gate 階段)
P31 module design/sub-system/system integration 要用的不同 code coverage 方法
//Testbench Generation
P35 Testbench Design 缺點/Automatic response checking
P36 Existing Approaches
P37 ATPG-Based(auto testing pattern generation) Approaches 優缺點
P39 Pattern Generation with EFSM

P41 Generate pattern by HSAT Solver(Hybrid-Satisfiablity)
P42 ILP(Integer Linear Programming)(整數線性規劃)
P43 FSM-Based Approaches (BDD-based technique)
P44 Test Sequence for a single STF
P45 Interacting FSM Model(IFSM) (BDD, image computation), used to solve the memory issues in formal techniques(分區、切小塊)
P46 Scheme of IFSM-Based Approach(流程圖)
P47 Semi-Auto Approaches (Key idea/Generator/Predictor/HVL(Hardware Verification Language))
P48 Challenge of Semi-Auto Approach (挑戰/改善方法)
*P49,P50 Coverage-Directed Test Generation (Random patterns are hard to cover all functionality -> 改善方法/Key idea)
P51 Hardware Implementation
// P54 Coverage-Assisted Debugging
P55 Debugging in Simulation
P56 Debugging Priority
P57 P58 P59 Coverage-Assisted Debugging

CH8 Intro to Formal verification

P3 Specification v.s. Verification
P4 Current Design Practice (reactive testbench/手動、random、mixed 測資->cannot get enough coverage and find all bugs)
P6 Formal Verification (What is Formal Verification/Methods/缺點)
P7 Simulation vs Formal Verification (Simulation 缺點/ Formal Verification 優點)
P8 Simulation 和 Formal Verification 的 Limitation
//
P10 Equivalence Checking (What is Equivalence Checking/優點/Limitation)
P11 Equivalence Checking 的 Example
P12 Combinational Equivalence Checking vs Sequential Equivalence Checking
// Combinational Equivalence Checking
*P13 Combinational Equivalence Checking (Goal/例子/False Alert?)
P14 Approaches for Combinational circuits (Functional methods/Structural methods)
P15 Functional Checking (Key idea)
P16 Functional Methods (ROBDD/ Equivalent 條件/verification 的複雜度)
P17 Structural Methods (Basic idea)
P18 Implications (Direct Implication/Indirect Implications(Learning))
P19 Learning : Identifying implications (Functional Learning/Recursive Learning)
P20 Learning for verification

P21 Implications for verification (key idea: using internal Equivalent points)
P22 Compare (Key) Points (logic cone/FEC tool)
P23 Logic Cones (What is Logic Cones)
P25 Summary (Two basic approaches : BDD-based 和 Learning-based 的優缺點/現今的 approach)
// Sequential Equivalence Checking
P27 Sequential Equivalence Checking (兩個 ckt equivalent 的條件)
P28 FSM Model
P29 p30 Represent FSM using BDD
P31 Characteristic Function **z=X(yk,x,i)**
P32 p33 State Transition Relation : **T(x,i,y) = sum (z)**
P34 Existential quantification
P35 p36 p37 Image computation/Forward & Reverse Image
P38 p39 Basic Approach of SEC (Reachability Analysis) (check outputs is reachable or not)
P40 Algorithm of Reachability Analysis
P41 debugging (When any mismatch is found, a "counter example" that illustrates the difference will be generated/ The counter example typically consists of.. (1) (2) (3))
//Model Checking
P43 What is Model Checking
P44 Specification & Temporal Logic
P45 **Computation Tree** (表達 FSM)
P46 **Computation Tree Logic(CTL)** [Formulas 由 (1) (2) (3) 建構而成->formal representations for the properties of the design] / (Logic operator 的定義 (五種符號)) / Temporal operator 的定義 Xp, Fp, Gp, pUq / Path quantifier 的定義 A, E
P47 Temporal Operator (X,F)
P48 Temporal Operator(G,U)
P49 CTL Formula (表達方式)
P50 Branching View of Time -> 要會看 CTL Formula
P51 CTL (圖示 AG p / AF p)
P52 CTL (圖示 EG p / EF p)
P55 Example Properties for TCL (以 CLT formula 表示兩條路不能同時綠燈)
P56 Example Properties for TCL(以 CLT formula 表示如果 road 上有一台車在等，未來某個時間燈一定會滿足綠色)
//
P57 **Symbolic Model Checking(SMC)** (原因:state explosion problem / Approach)
P58 Explicit State Traversal (**State Traversal graph , STG**)
P59 p60 Implicit State Traversal (概念 / 4 個 steps)
P61 Implicit State Traversal Algorithm
P62 Implicit State Traversal Example

P65 **Limitation** of SMC(Symbolic Model Checking)
P66 未來可改進的方向

CH9 Intro to AMS Behavioral Modeling in SoC

//
P3 AMS Blocks in SoC (Analog 定義/Mixed Signal 定義/Analog Design 為何難系統化)
P5 Noise Coupling in AMS Designs
P6 傳統 MS Design Approach (Solutions)
P7 傳統 Analog Simulation
P8 Top-Down AMS Design Flow
P9 Advantage of Top-Down Methodology (優點)
//
P11 Analog Behavioral Modeling (What is .. / 優點)
P12 Keys to a good Analog behavior model (2 個 key)
P13 Top-down modeling Approach (優點/2 個 issues : (1)缺乏 layout 的資訊(loading,parasitic)
(2)Inaccurate on non-ideal circuit properties)
➔ 改用 Bottom-Up
P14 P16 Bottom-Up Modeling Approach (許多優點)
P15 Bottom-UP Behavior Extraction 流程圖
P16 Accurate Behavior Extraction
P17 Characterization Mode (例子 Charge Pump Phase-Locked Loop(CPPLL))
P18 Extract Circuit Properties
P19 Case Study : 用 verilog-AMS 來描述 PLL behaviors (SPEC…)
//Application s of analog models
P25 Possible Applications : (許多 / Model Accuracy is the key issue to be solved->p51 有解決方法)
//Noise interaction in AMS systems
P29 Analog Performance Variations (PVT 三個效應對 performance 的影響/從 digital 會來 noise 對 analog 的影響->需要 Efficient Analyzer)
P30 Noise-Aware Behavioral Model (說明/Typical 解決方法&其缺點/較好的解決方法)
P31 Supply Noise 的來源(Issues)與對 analog 的 Impact
P32 Stochastic Analysis Approaches (2 個 issues)
P33 Regular Noise Analysis (2 個 issues)
➔ 解法 P34 Handle Irregular Supply Noise (2 種解決方法 與 其好處)
P35 Linear Model for Intermediate Parameters (Sensitivity analysis under different Vdd)
P37 Noise Issues in AMS Integration (用 noise-aware behavioral model 可能無法正確的分析 supply noise effects/原因)
- 解法 P38 SCORE Macro-model for Noise Interaction (**SCORE: State-Controlled Resistors**/能解決

的原因)

P39 Ideas of SCORE Macro-model

P40 Recursive Simulation Platform for PLL

//Yield Enhancement

P46 Process Variation [Device Variations]

P47 Yield Loss Issues

P48 Corner Simulation (issues/缺點/需要考慮…)

➔ 解決方法 P49 Monte Carlo(MC)Analysis (定義/如何分析/缺點)

➔ P50 Hierarchical Statistical Analysis (能較快)

*P51 Behavioral Monte Carlo Analysis(BMCS) (Behavioral mode accuracy 的解決方法(中間那段) / **SA : Sensitive Analysis**)

P52 Quasi-SA for CP(charge pump) (Vt variation..)

P53 Quasi-SA for VCO

P57 Design Centering (為避免 process variation 對良率造成的影響，用此方法改善)

P58 Acceptable Design Region

P60 Force-Directed **Nominal Point Moving (NPM)**

P61 Proposed Yield Enhancement Flow (3 個主要的 steps)

P62 P63 Behavioral Level Yield Enhancement / Behavioral Level Sizing

P64 **Principle component Analysis (PCA)**

P65 **FBMCS(Fast Behavioral Level Monte Carlo Simulation)**

//

*P70 Conclusions (Analog : Top-down Behavioral Modeling 是 for new design / Bottom-up 適合給 IP-based Soc designs) / (Accurate Behavioral Models 也有其他有用的應用: (1)分析 supply noise effects (2) 分析 design yield and make improvement)

CH10 Verilog-A Overview

P12 disciplines.h

P13 nature (user-defined attributes)

P15 P16 Structural Description Example(Modem)

P17 Structural Description (type, name, parameter)

P18 Behavioral Description (Contribution operator “<+” / 描述 電阻、電壓、電流)

P19 P20 P21 Verilog-A Mixed-level Description (16_QAM modulator)

P22 Analog System Simulation

//語法

P24 Module Declaration

P25 Interface Declaration

P26 Module Instantiation

P27 P28 Parameter Assigned by Order/Name
P29 P30 P31 P32 P33 (Data type/宣告 Integer/宣告 Real/宣告 Parameters/Parameters with Range)
//
P34 Declare Signals in different Systems (Conservative Systems/Signal Flow Systems)
P35 P36 Conservative System / 宣告:electrical (例子:電阻兩端電壓、電流)
P37 P38 Signal Flow System / 宣告:voltage, current(例子:voltage amplifier/current amplifier)
//
P39 Node and Branch (node, branch, port 的定義)
P40 Node Declaration
P41 Node Access (點電壓 or 電壓差表示法 : V(node1) / V(node1,node2))
P42 Branch Declaration and Access (for specifying distinct parallel paths/Branch 用法)
//
P44 Analog Model Properties (Ex: Non-linear diode model)
P49 Conditional Statements and Expressions (使用 ternary operator ?: / Ex: 選最大值 maximum model)
P50 Ex: Dead-band amplifier model
P51 使用 case / strobe
P52 使用 repeat (Ex : 重覆 loop 10 次累加 first 10 digits)
P53 使用 while (Ex: cnt，產生亂數直到 rand become zero)
P54 使用 for (Ex: 累加前 10 個偶數)
//
P55 Analog Operator (Time Derivative/Time Integral/Linear Time Delay/Discrete waveform filters/Laplace Transform filters/Z-transform filters)
P57 ddt_op (微分 example: 將 V(in)微分再乘上一個 scale 放大)
P59 idt_op (積分 example)
P60 LC(電感電容) example ((1)將 CxV 微分 得 電流 (2)將 V/L 積分 得 電流)
P61 Absolute Delay Operator (讓訊號延遲的語法)
P62 P63 Transition operator / example (將數位方形訊號轉成類比波型的語法)
P64 P65 P66 Slew Operator / example (將原本的訊號波型 bound 在一個更小的範圍中，可達到限制 gain 的效果)
//
P67 Laplace Transform Operators (continuous time filter)
P68 laplace_zp
P69 laplace_zd
P70 laplace_np
P71 laplace_nd
P72 Example: Butterworth Low-Pass Filter
//

P73 Z-Transform Operators (discrete time filter)
P75 Z-Transform Example
//
P76 Global Events (init_step(analysis_function) / final_step(analysis_function)) (在 simulation 所有動作前做 or 在 simulation 所有動作後做)
P77 Cross Event (找 expression = 0 時的 time 為何)
P78 Cross Event Example (Ex: Sample and hold)
P79 Timer Event (Ex: squarewave / 產生 clk 訊號語法)
//
P81 Verilog-A Basic Operator table
P82 Built-in Mathematical Functions table
P83 Transcendental Functions table
P84 Environment Parameters table

CH11 Real-Valued Verilog Models for Analog Circuits

//
P3 Difficulty in Mixed-Signal Verification (原因 & 解法)
P4 Behavioral Model (原理 / Tradeoff : between accuracy & speed)
P6 Why using Verilog-A model
P7 P8 P9 Advantage of Real-Valued Verilog Model(6 項優點)
P10 Difficulty to model analog behaviors(許多原因)
//Real-Valued Behavioral Models in Verilog
P12 Represent Continuous-Time Signals (Approach to represent analog signals in a digital simulator)(兩種方法 : (1) Piecewise-constant(PWC) (2)Piecewise-linear(PWL)))
P13 Model Comparison (比較: Real-Valued models vs Verilog-A models)
P14 Discrete Transfer Function
P15 Proper Circuit Partition (為了較容易得到 equation)
P16 Avoid Time Integration (combine analog block) (Ex: Single-slope ADC)
P17 Reshape Model Output (gate keeper : smooth sharp output signals)
P18 Timing Models (analog simulation 模擬真實的 timing 狀況)
P19 Interface Modeling (三種狀況與方法: (1) Digital in & out (2) Analog in & out (3) Digital <-> Analog)
P20 PWL Waveforms as Input/Output
P21 P22 Real Value Connection
P25 Multi-driven Problem of RVM(Real-Valued Model)
//Portable models for Verilog/Verilog-A
P28 Portable Methodology

P29 Verilog vs Verilog-A (Verilog 和 Verilog-A 都支援:3 項)
P29-P33 ADC w/ RC filter

CH12 Case Study of Behavioral Modeling for Mixed-Signal Systems

// Charge-Pump phase lock loop (CPPLL)
P3 Bottom-up Modeling Approach (Behavioral Extraction) (可以考慮到非理想效應 ； 對 existing blk 較適用)
P4 許多優點 Accurate Behavioral Extraction
P5 Characterization Mode (Ex: CPPLL)
P6 Extract Circuit Properties (observe output response)
P7 P8 Phase Freq Detector (Verilog-A code for PFD)
P9 Ideal Loop Filter Modeling
P10 Model CP+LF Together (key : Translating the current from to the voltage form.)
P11 – 14 CP+LF Response / Modeling
P15 Charge Pump Modeling (verilog-A code)
P16 VCO Modeling
//Delta-sigma A/D converter
P24 P25 SC Integrator in Verilog-A
P26 Quantizer and 1-bit ADC (verilog-A code)
P27 Non-ideal Effects (Finite OP Gain+Slew Rate+Settling Response+OP Noise / Noise: Swith Thermal Noise & Supply Noise)
P28 Characterization Mode (透過控制各種 switch 來形成自己想要的電路)
P29 Extraction from Simulation (Operate the modulator as the SC integrator (3 Patterns))
P30 OP DC Gain
P31 Settling Response
P32 Output Slew Rate
P33 Output Ripple Mode
P34 Extract Damping Response
P35 Thermal Noise
P36 OP Noise
P37 Random Noise Modeling (verilog-A code)
//Delta-sigma D/A converter
P43 1-bit D/A Convertor Model
P44 P45 P45 Biquad Circuit Model (verilog-A code)
P48 Direct Charge Transfer
P49 Characterization Mode (Extraction Patterns)

P50-P52 DC Gain Extraction – Biquad (add alpha, beta into verilog-A code)
P53-P55 DC Gain Extraction – DCT (add C into Verilog-A code)
P56 Slew Rate Extraction – Overall Filter (add into Verilog-A code)
//Transmission Link System
P62 Analog Part in Transmission Link (Transmitter, Receiver, Transmission line)
P63 PLL Design
P65 Serializer
P66 Mux8-1 Model (Mux2-1 verilog-A code)
P68 DeSerializer
P69 DeMultiplexer Model(Verilog-A code)
P70 Transmission Line Model
P73 DeSkew CDR
P74 Confidence Counter(CC) in CDR (TFF Up/Down Counter)
P75 CC Behavioral Model and Verilog-A code
P80 Modeling Design Hierarchy

CH13 Introduction to Automatic Design Optimization for Analog Circuit

//
P4 Mixed Signal Design Problem (Design Effort)
P6 Typical AMS Design Flow (三個 difficulties)
P10 Synthesis = Automation + Optimization (Optimize for performance / for yield)
P11 Automatic Circuit Sizing (四種分類 : Knowledge-based optimization/Simulation-based optimization/Pareto-Front-based optimization/Analytical equations-based optimization)
P12 Comparison of different approaches
//Knowledge-based Design Automation
P14 What is knowledge-based optimization (優缺點)
P17-P19 Design Procedure (Ex: 2-Stage OPA)
//Simulation-based optimization
P22 What is Simulation-based optimization (優缺點)
P23 Improve Simulation-Based Approach
P24 Parallel Recombinative SA(PRSA)
P26 Search Space Reduction
P27 Operation Region Constraint
P28 SA-Based Optimization Flow (流程圖)
//Pareto-Front-Based Optimization
P31 P32 What is Pareto Front (優缺點)
P33 Pareto Front Generation (multi-objective cost func.)

P34 Pareto Front with Diff. Constraints

//Equation-Based Optimization

P37 What is Equation-Based Optimization (優缺點)

P38 P39 GP-Based (Geometric Programming) Optimization

P40 P41 Iterative GP Approach (P41 缺點)

P42 Nonlinear Parameters (某些參數的曲線在不同 operation 非常不同)

➔ P43 用 Sub-Space Modeling 來 fit 曲線(piece-wise model)

//Simulation-Equation Based Method

P46 What is Simulation-Equation Based Method (Iterative vs Two Phase)

P47 Iterative Method (如何用 / 優點 & 缺點)

P48 Flow Chart of Iterative Method

P50 Two-Phase Method (如何用 / 優點 & 缺點)

//Bias-Driven Optimization

P55 Operating Range Reduction (可減少 operating range, Improve searching efficiency)

P56 Bias-Driven optimization flow

P57 gm vs gm/Id (gm/Id 因為 independent to transistor size -> 較容易 model)

P58 gm/Id Table Construction (方法、優點)

P59 performance constraints (Gain, Phase Margin, Gain-Bandwidth)

P60 Objective function (cost of area/power, optimization)

P61 Solve non-linear problem

P62 P63 Device Sizing Table (用 equation 推有很大的誤差，改善:改用 simulation data 來建 lookup table / 優點)

P65 Parasitic Capacitance Consideration (->預測 bandwidth, phase margin)

P66 Capacitance Prediction (建 table)

P67 Body Effect Transconductance(gmb)

P68 Extend Parameter Tables (to include non-ideal effects)

CH14 Automated Robust Design Optimization for Analog Circuit

//Motivation

P3 Mixed-Signal Design Problem (Design Effort)

P4 Analog Circuit Design Issues (6 種)

P5 Typical AMS Design Approach (4 項缺點)

P6 Prediction != Real Design (因為 非理想效應 : parasitic effects/process variations/aging effects)

P7 Layout-induced Parasitic Effects (Redesign loop 的原因 : 要畫完 layout 後才能知道寄生效應 / small change 就會對整個電路有很大影響)

P8 Process Variation Effects

P9 Aging Effects (1.negative-bias temperature instability 2.hot-carrier injection / Aging Effects 造成

的影響)

P10 Lifetime Yield (Lifetime Yield = Process Variations + Aging Effects)

P12 Robust Design Optimization Flow (How to consider the non-ideal effects in optimization flow ? => 分三方面有解法(1.For parasitic effects… 2.For process variations… 3.For lifetime yield…))

//Parasitic-Aware Synthesis Approach

P14 Parasitic Models (分兩種: Intra-module(device) & Inter-module(interconnect))

P15 Device Parasitic Model

P16 Interconnect Parasitic Model

P17 RC Delay (影響電路的 performance : Freq Response, Speed)

P18 IR-Drop (pre-sim post-sim 的 node voltage 不同，電流和 transconductance 也會改變)

P19 Sizing with Performance Model (方式、缺點)

P20 Worst Case Parasitic Corner (方式、缺點)

P21 Template-Based Retargeting Flow (像 ECO 的概念)

P22 Performance-Constrained Retargeting (針對 performance 的 sensitivity value)

P23 Parasitic-Aware Circuit Sizing (傳統 flow 的缺點(redesign loop) / 這個方法的優點(預先考慮 parasitic))

P24 Parasitic-Aware 流程圖

P25 Wire Length Estimation (Predict Routing Path)

P26 Rwire and Cwire Calculation (透過 wirelength 來計算這兩個的值)

P27 Parasitic Capacitance

P28 Parasitic Capacitance Consideration (用 lookup table)

P29 Parasitic-Aware Lookup Table

P30 Parasitic-Aware Performance

//Yield-Aware Synthesis Approach

P35 Yield Loss Issue (先進製程，parametric variability 會造成嚴重的 yield loss/Process Variation)

P36 Yield Analysis Method – Monte Carlo(方法) (Device variation 包含:W,L,tox)

P37 Yield Improvement Approaches (兩個方式:1.Leaving “enough” design margin 2. Design Centering / 缺點)

(“Center” cannot guarantee the yield-optimized design 原因: 因為 process sensitivity of each performance 可能會不同)

P38 Design Centering

P39 Worst Case Distance (WCD) Analysis (Corner Analysis 的缺點、Simulation-based evaluation(Monte Carlo)的缺點 -> 所以 Equation-based worst case distance(WCD))

P40 Yield-Aware Synthesis (比較 Simulation-based 和 Equation-based 的 優缺點，與各自如何進行改善)

P41 Simulation-Based Synthesis Using WCD (方法、缺點)

P42 Eq.-Based Synthesis via Centering (方法、缺點)

P43 Variation-Aware Synthesis Approach (結合兩種方法)

P44 Yield-Optimized circuit sizing flow (用 Eq.-Based approach、原因(優點))
P45 Hierarchical Variance Analysis (方法、優點)
P46 Cumulative Success Probability (CSP)
P49-P56 Ex: Low Dropout Regulator (LDO) (案例探討，如何優化)
//Aging-Aware Synthesis Approach
P58 Flexible Electronics (Thin-Film transistor(TFT), 優點與應用)
P59 Comparison of CMOS & Flexible TFT
P60 Flexible TDT 的 design Issues(缺點)
P61 Bending Effects
P62 Aging Effects
P63 Simulation-Based Aging Analysis (方式、缺點)
P64 2-Stage Design-for-Reliability Flow
P65 P66 Linear Performance Model for CMOS, Errors of Linear Model (無法應用在 TFT, 原因)
P67 DFR Flow for Flexible Electronics (automatic synthesis considering yield and reliability for TFT)
P68 Aging-Aware Circuit Sizing Flow
P69 Exponential Aging Model (方式)
P70 Predict Aging gm/Id & gds/Id (優點)
P71 Modify current and constraints