



Advanced Node Design Challenges

Custom Compiler Team
2023. Sep 25

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Agenda

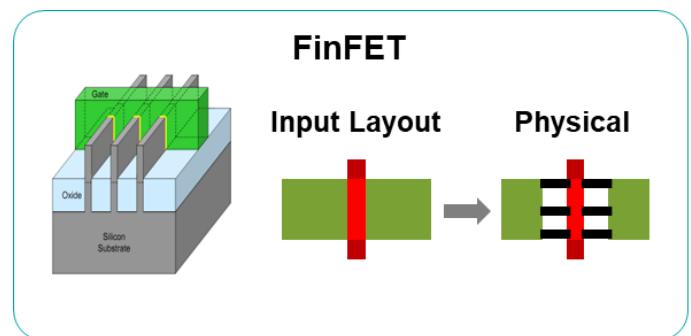
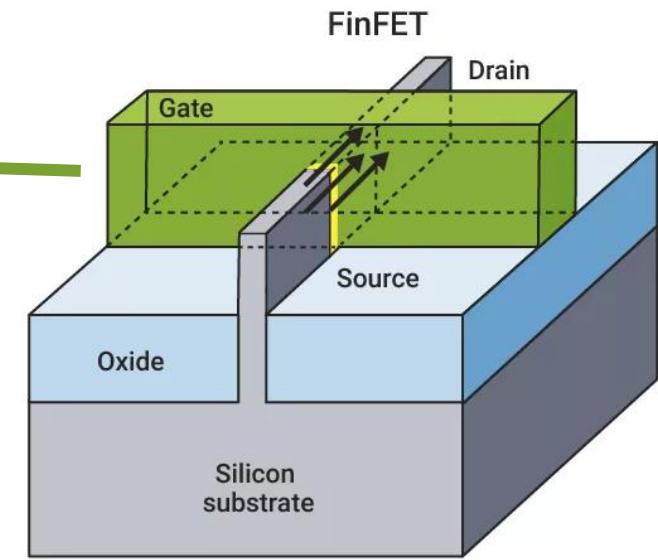
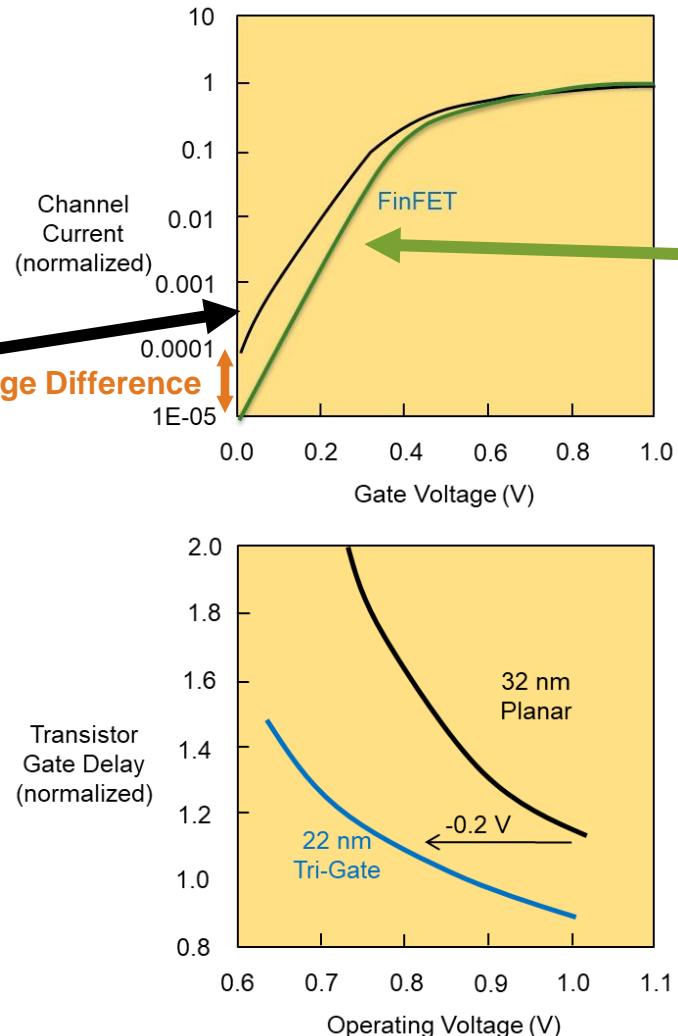
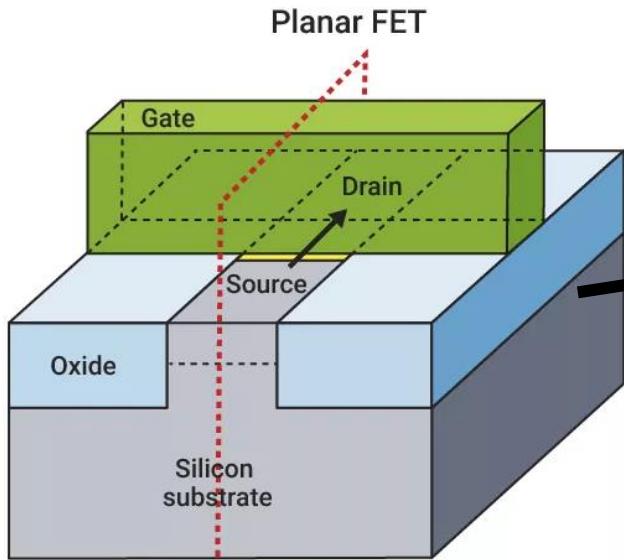
- Introduction
- Challenge of Advanced Node
- Challenge of Scaling and Strategies
- Challenge of Physical Implementation
- Challenge of Analog & Mixed-Signal Design
- Summary
- Q&A

Introduction

Technology Revolution



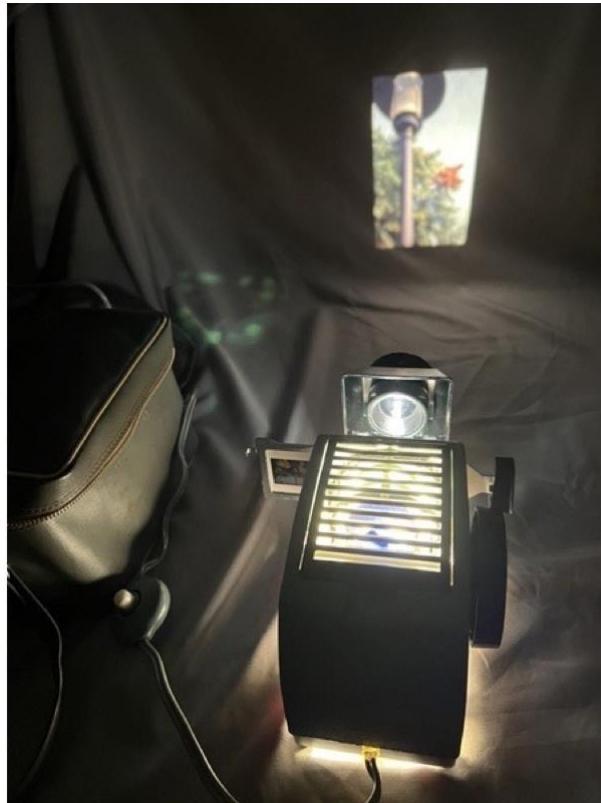
The Motivation: Planar to FinFET



Challenge of Advanced Node

Challenge of Advanced Node

- Manufacturing
 - Patterning
 - **Lithography, Etching**
- Physical limits
 - Light and Diffraction
 - Exposure and Imaging
 - Multiple Patterning
 - DUV, EUV



$$CD = k_1 \left(\frac{\lambda}{NA} \right)$$

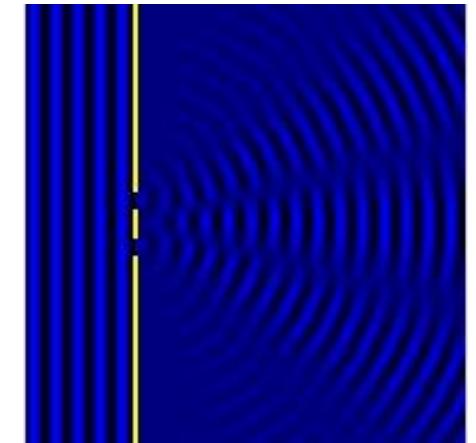
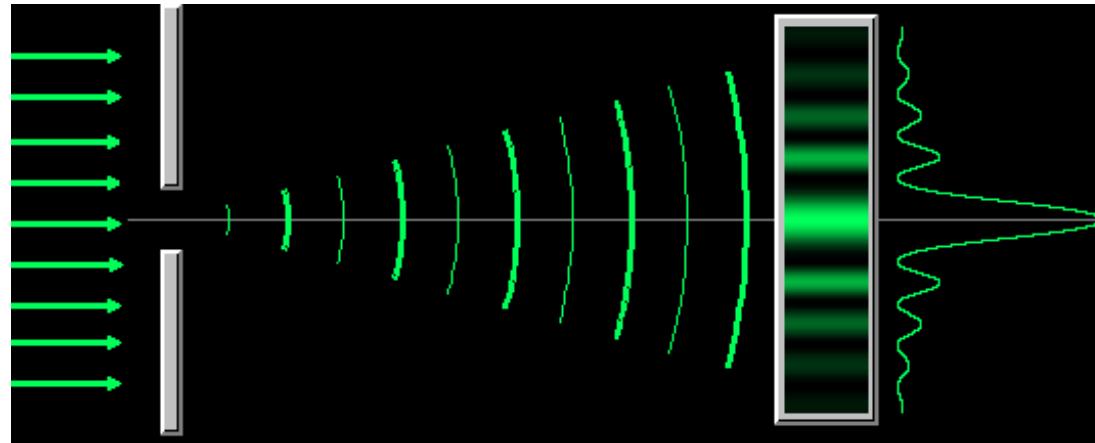
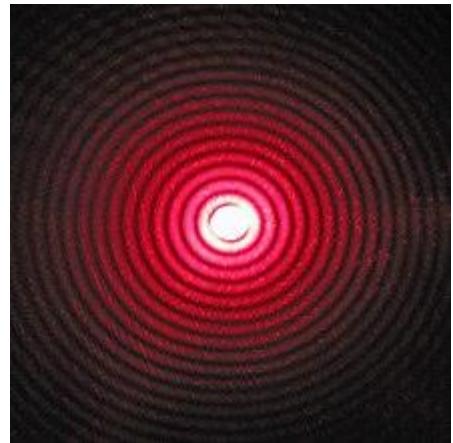
Half-Pitch

R (K1=0.4) nm	n	medium	$\lambda / n \text{ nm}$	NA	Power	
KrF dry	124	1	Air	248	0.8	40
ArF dry	103	1	Air	193	0.75	45
F ₂ dry	84	1	N ₂	157	0.75	–
ArF immersion	40	1.44	H ₂ O	134	1.35	90
EUV ($\lambda = 13.6 \text{ nm}$)	18	1	Vacuum	13.6	0.3	>250
EUV ($\lambda = 13.6 \text{ nm}$)	9	1	Vacuum	13.6	0.6	>500
EUV ($\lambda = 6.7 \text{ nm}$)	4.5	1	Vacuum	6.7	0.6	>1000

R= Resolution
CD = Critical Dimension

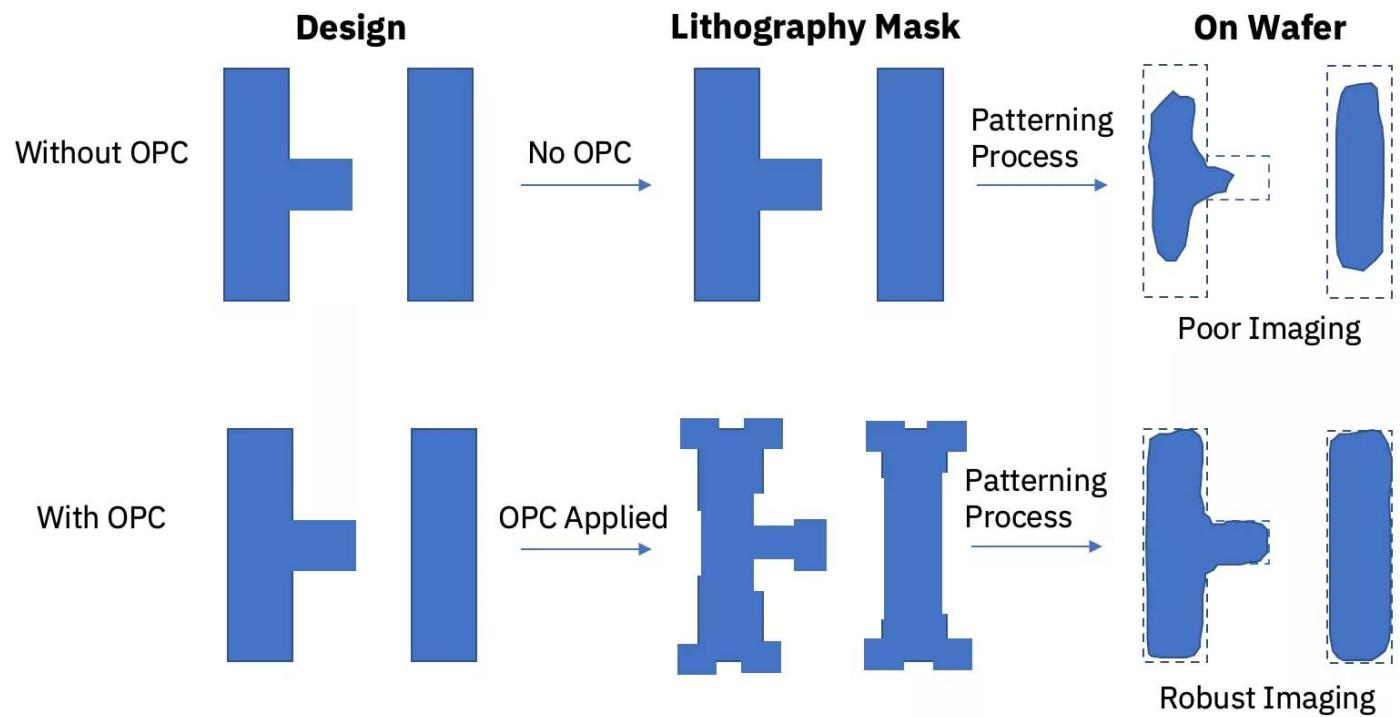
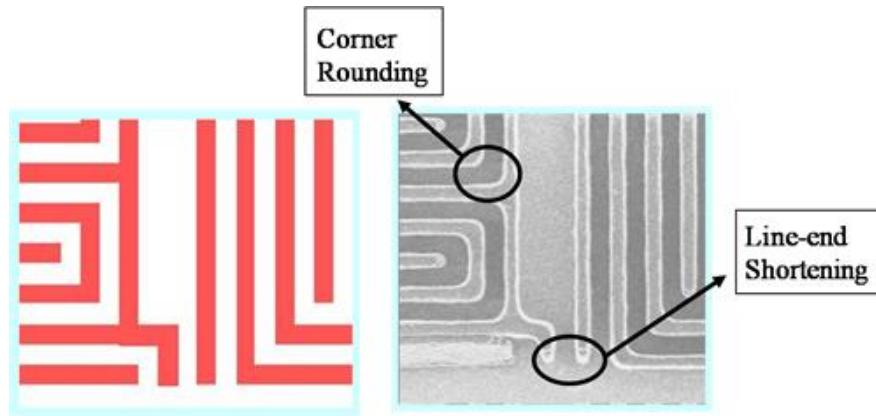
Lithography

Light and Diffraction



Lithography

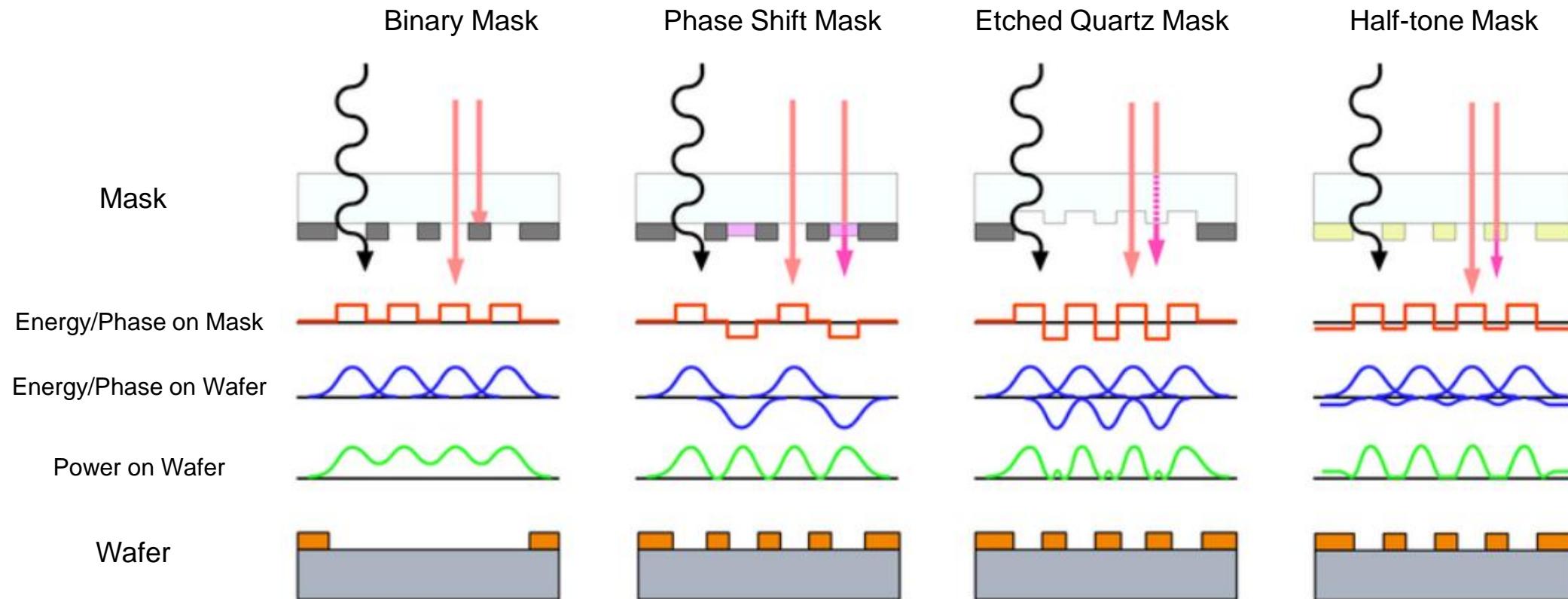
Exposure and Imaging



Optical Proximity Correction

Lithography

Exposure and Imaging

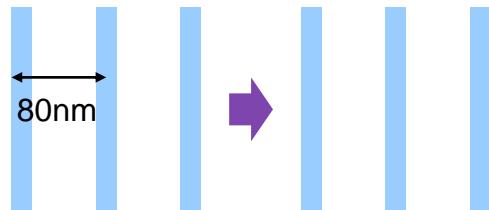


Phase Shift Mask

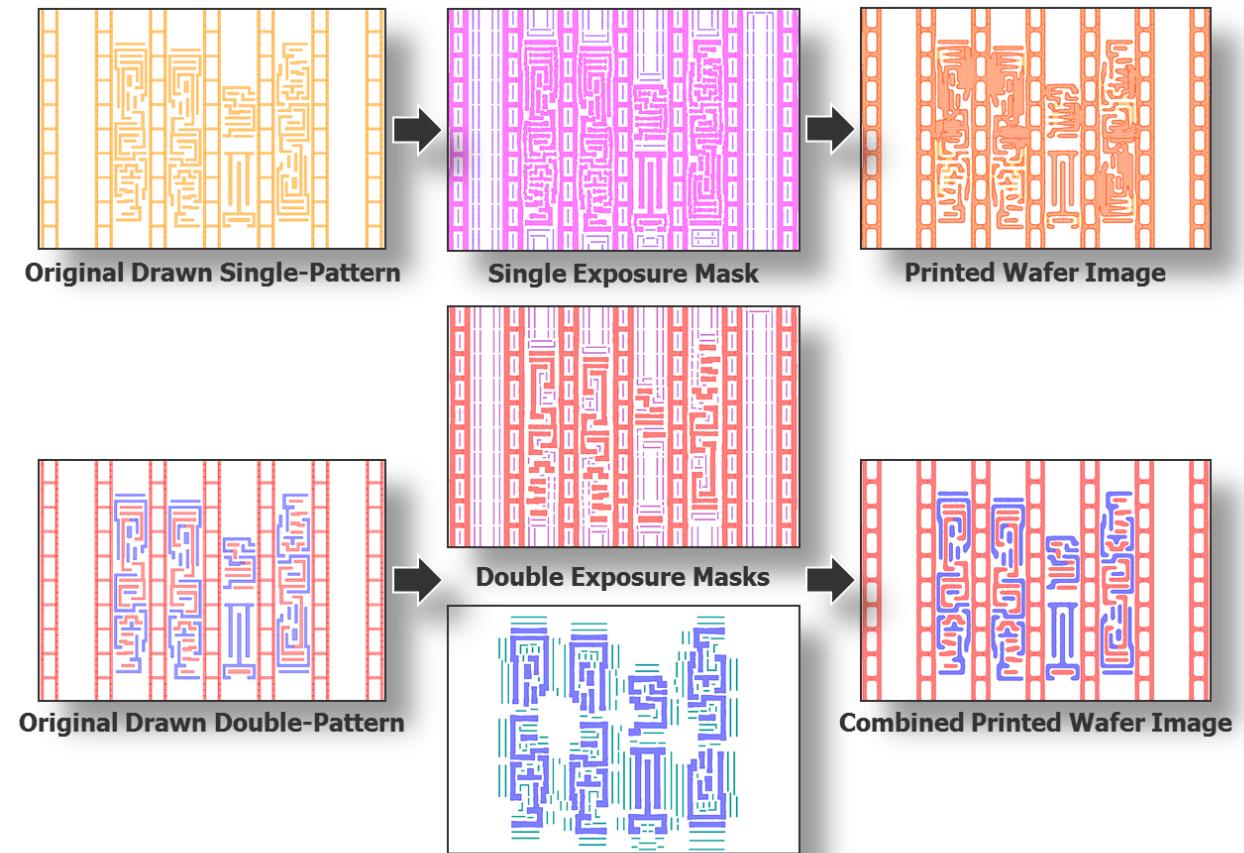
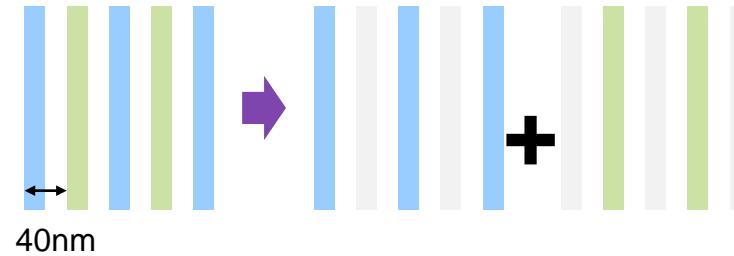
Lithography

Single Patterning vs Multiple Patterning

Single
Patterning

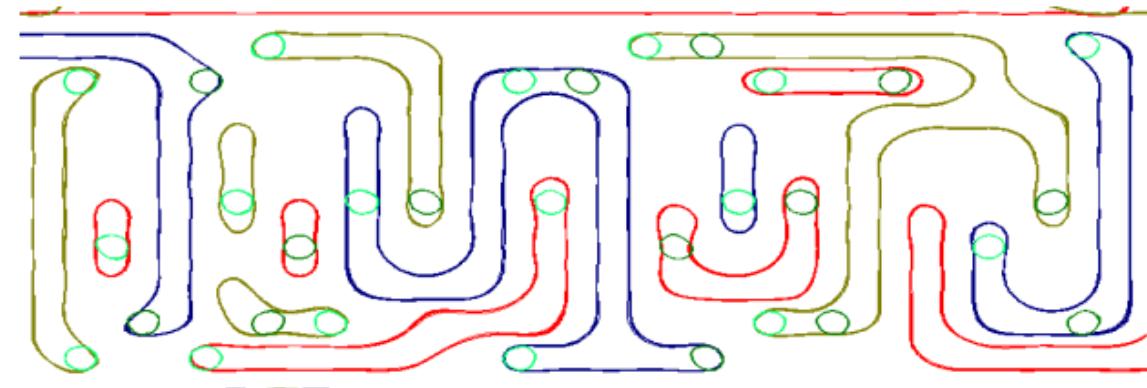
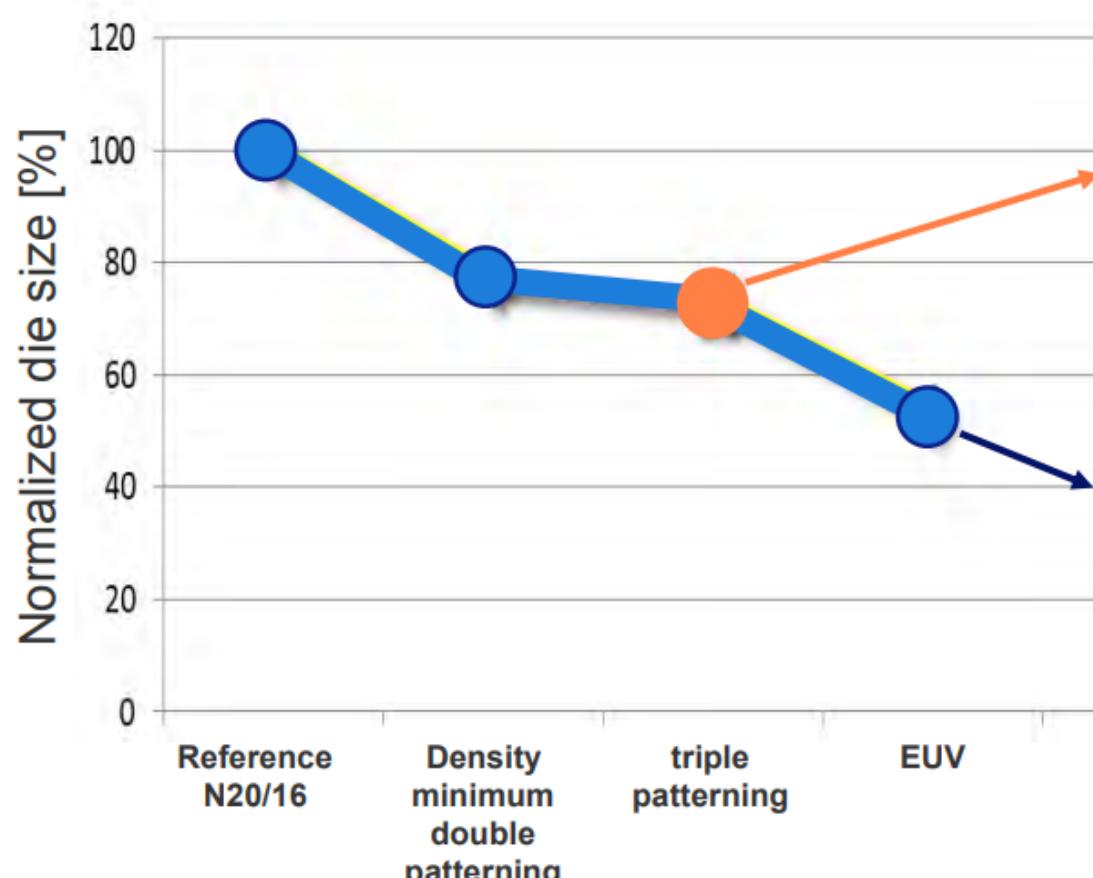


Multiple
Patterning

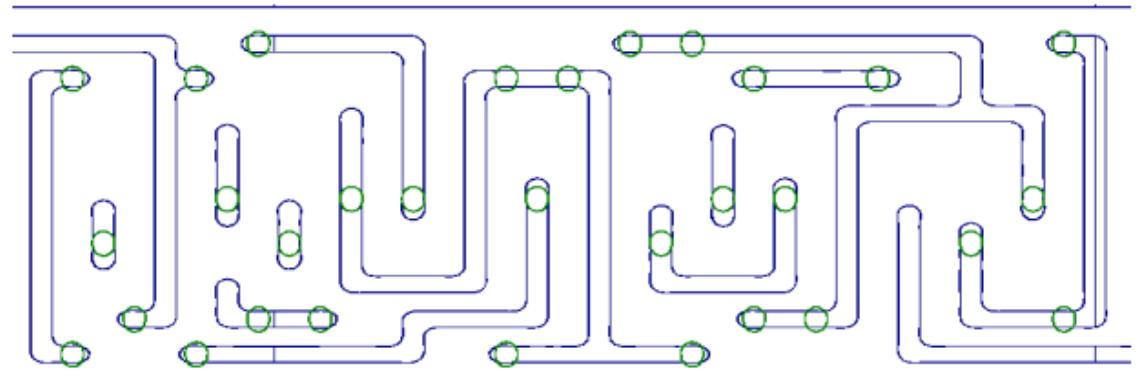


Only EUV can enable 50% scaling for the 10 nm node

Layout restrictions and litho performance limit shrink to ~25% using immersion



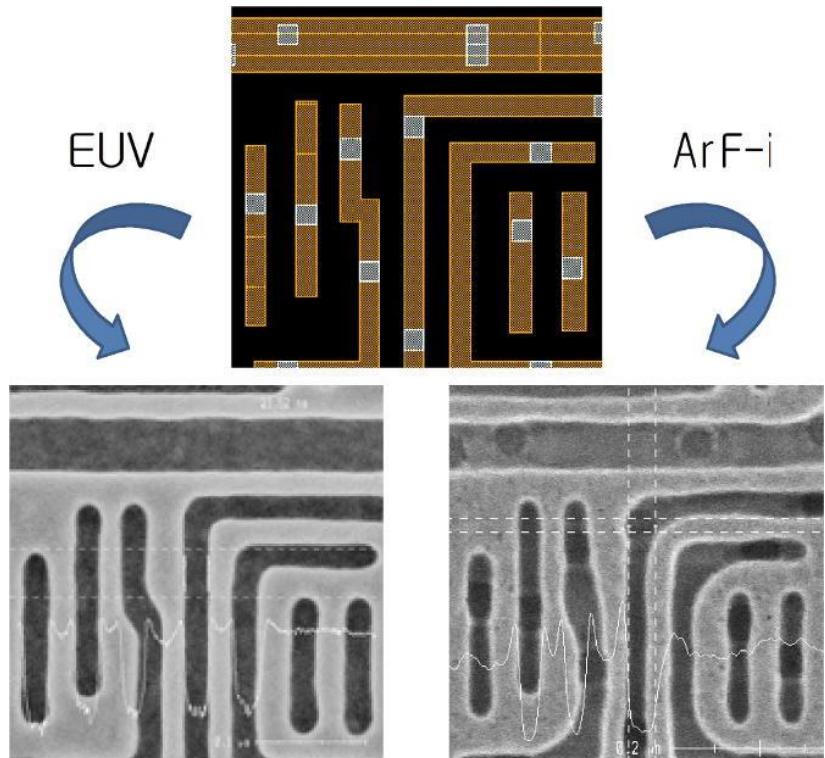
Triple patterning does not show an process window



EUV meets all litho requirements

Challenge of Advanced Node Manufacturing

Multiple Pattern & OPC



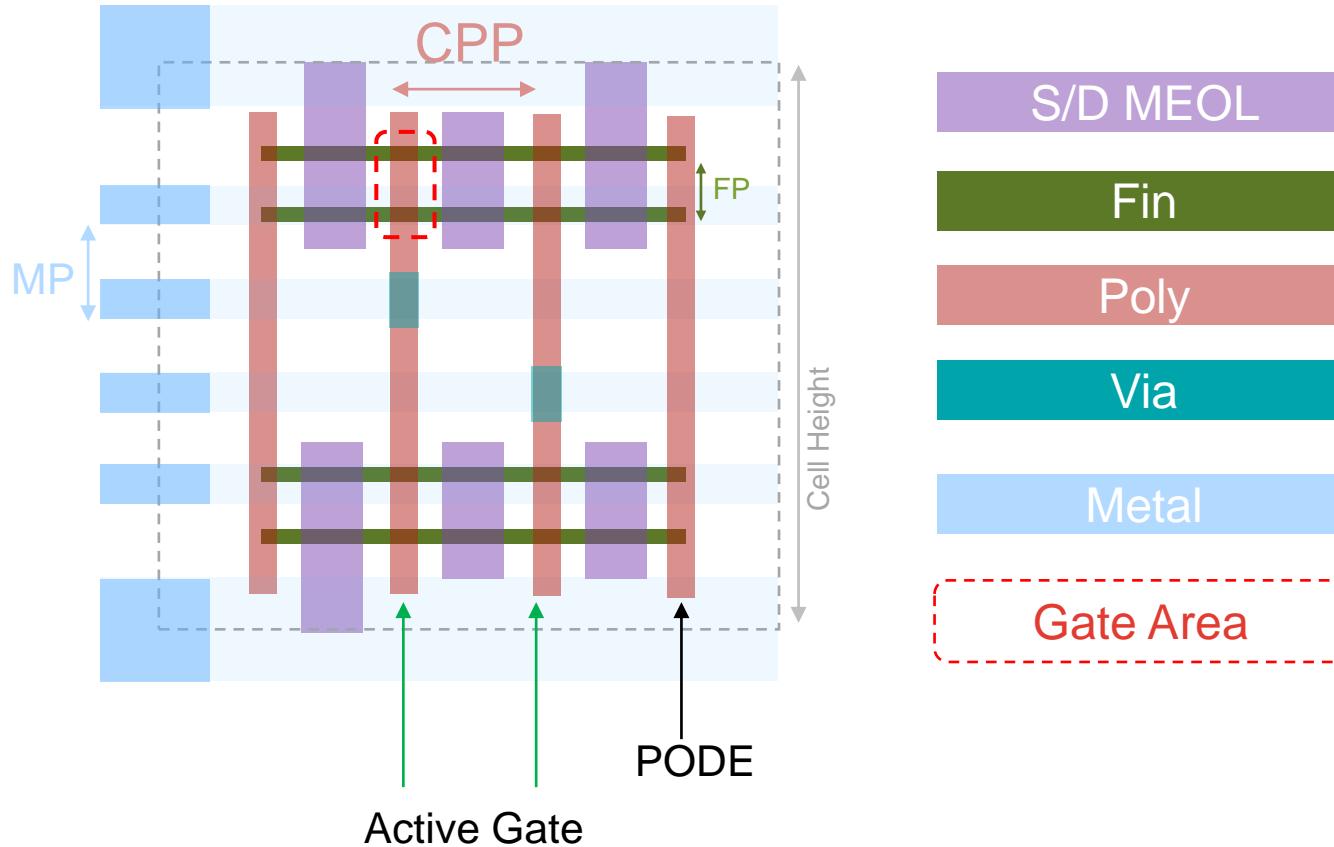
An example of the increased fidelity we're talking about. The pattern on the left was created using EUV, while the right side used conventional lithography. Image credit: Samsung

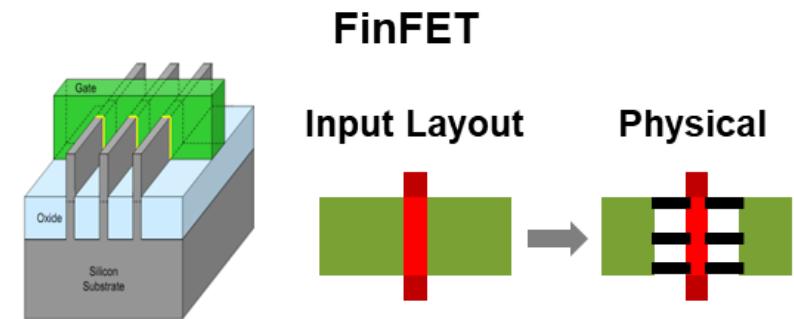
Challenge of Scaling and Strategies

Challenge of Scaling and Strategies

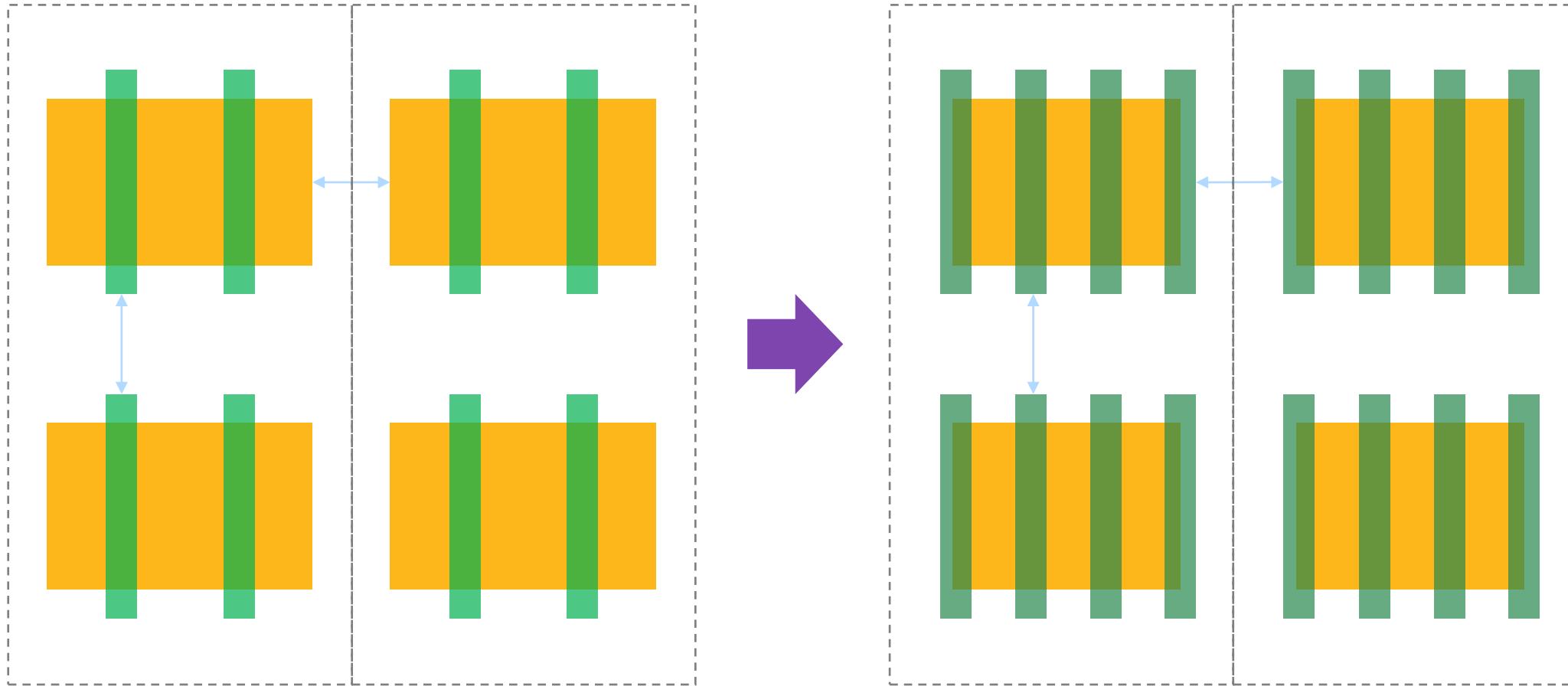
- Area Reduction
 - X-direction
 - Continuous Diffusion (CNOD)
 - Common Poly on Diffusion Edge (CPODE)
 - Y-direction
 - Cut Poly
 - Self-aligned Gate Contact (SAGC)

FinFET Layout Example





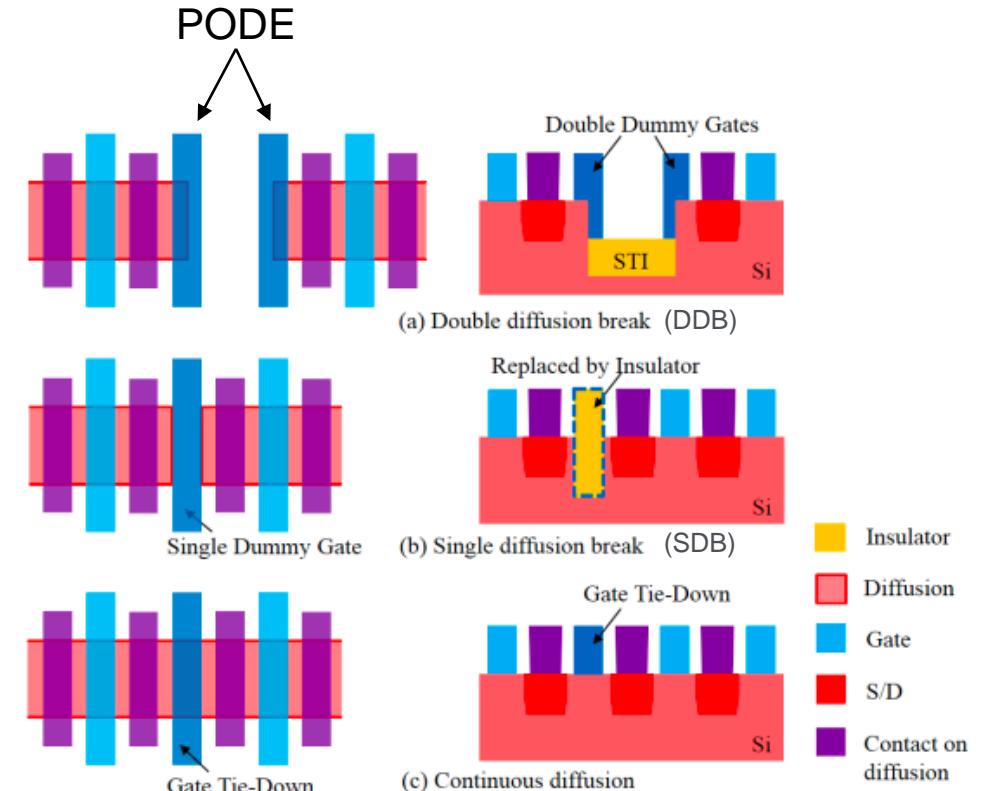
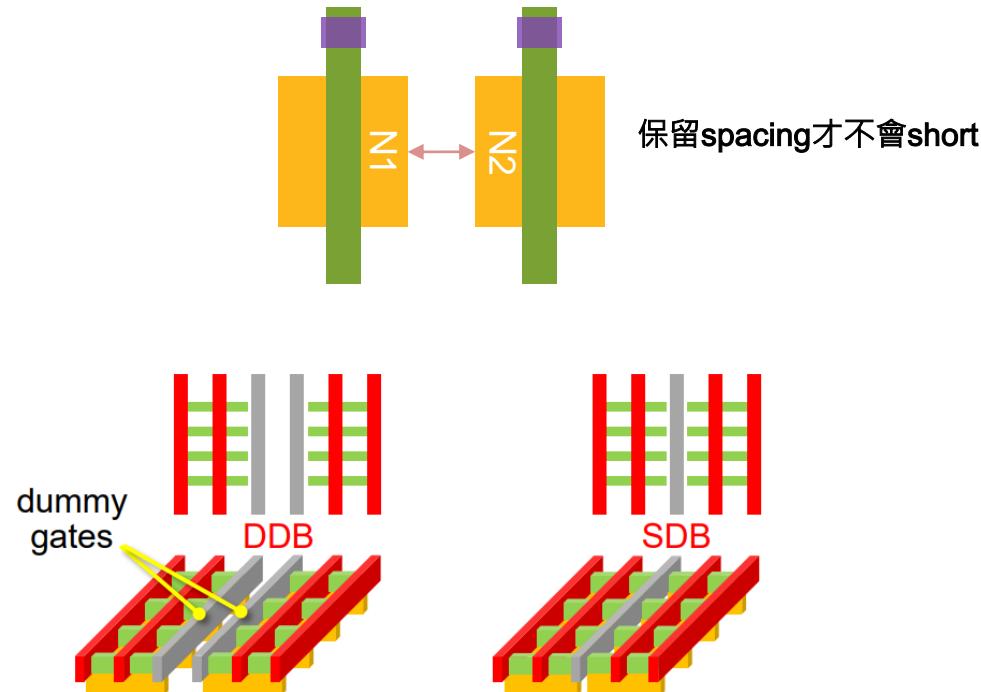
FinFET Layout Example



Overcome the challenges and keep scaling

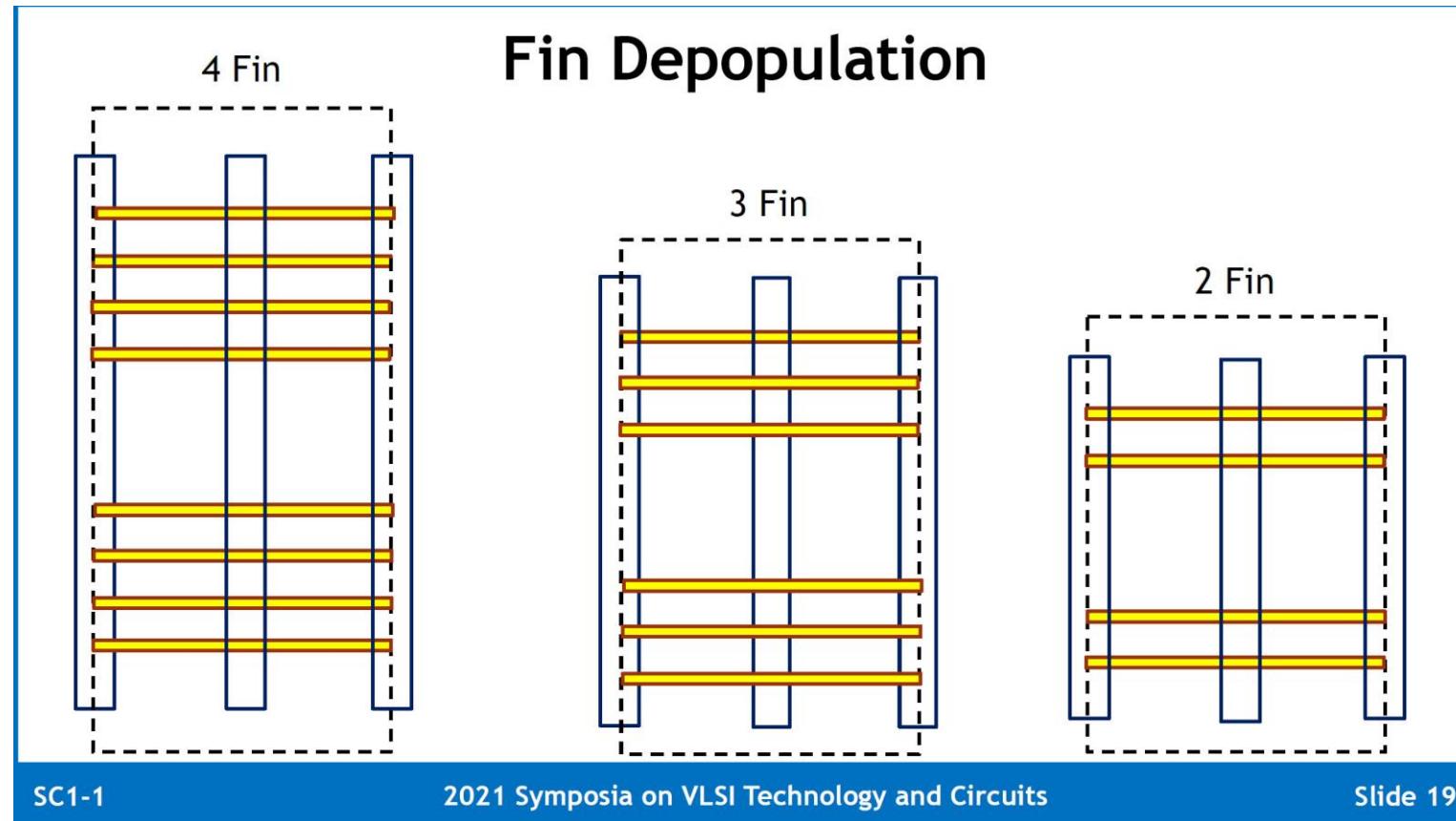
Reduce in X-axis

- Continuous Diffusion (CNOD)
- Common poly on diffusion edge (CPODE)



Overcome the challenges and keep scaling

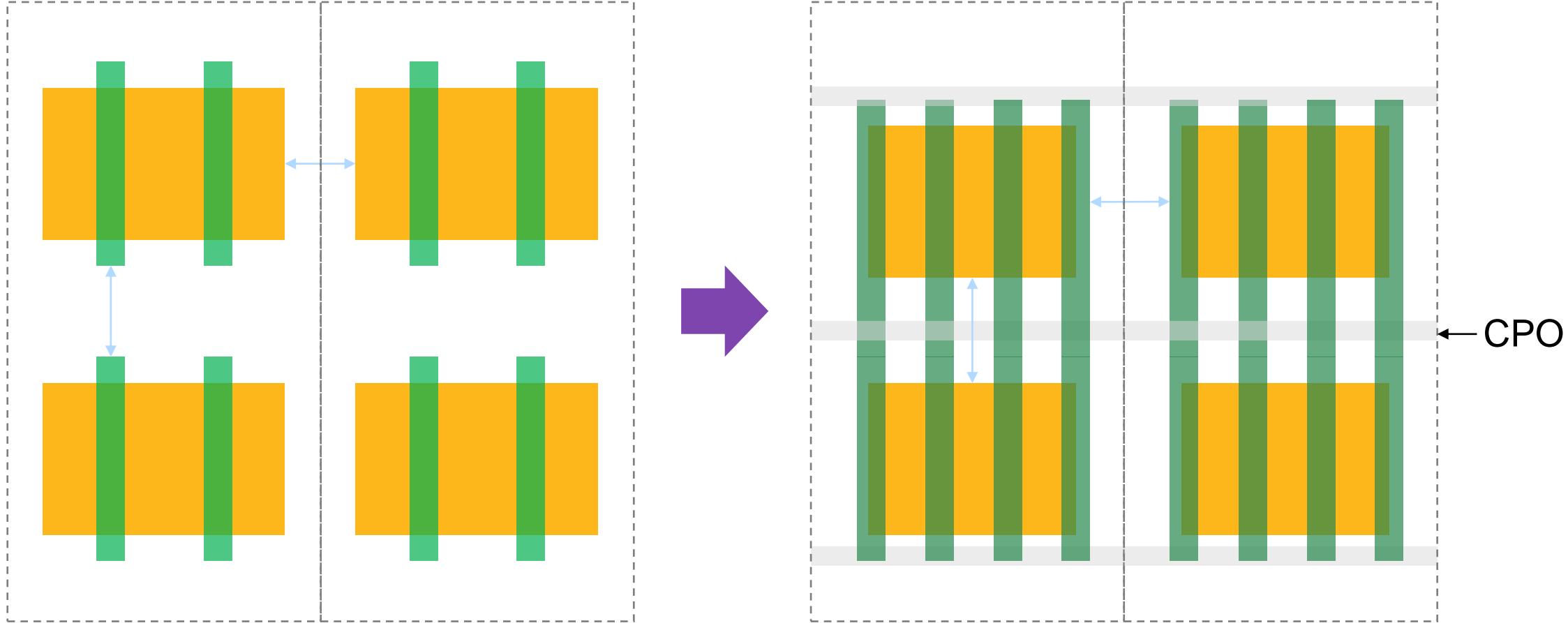
Reduce in Y-axis



Overcome the challenges and keep scaling

Reduce in Y-axis, Cut Poly

先做好一整根poly然後再將其切開(分段)
如此可以使生成出來的間距更緊緻

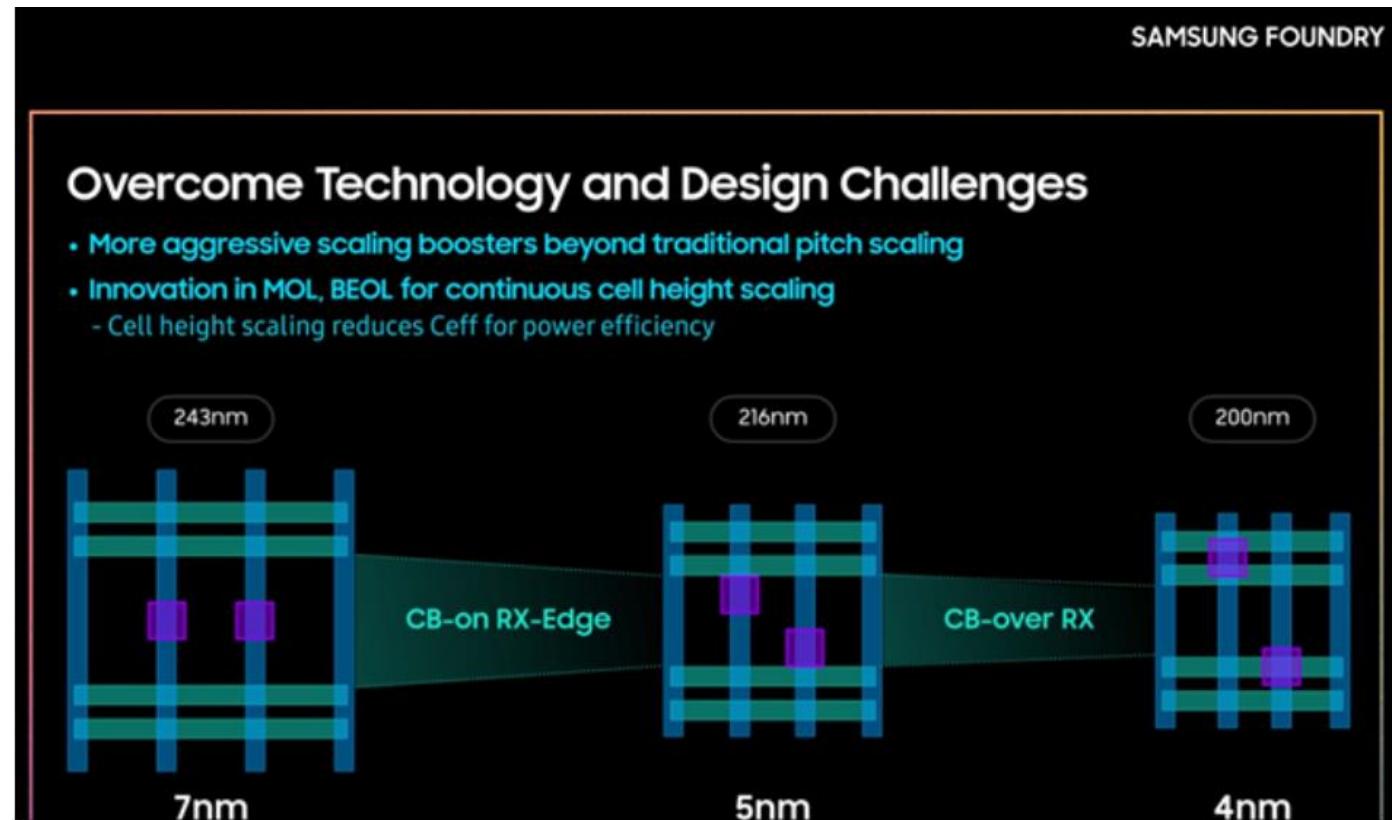
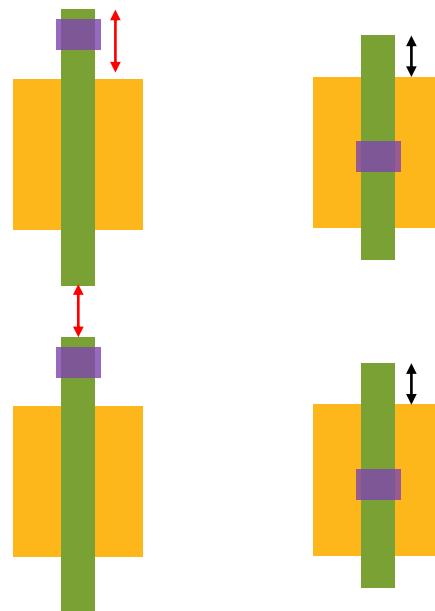


Overcome the challenges and keep scaling

Reduce in Y-axis

- Self-aligned gate contacts (SAGC)

- Gate contacts on active gate
- Less Space between OD rows
- Reduce R_{gate}

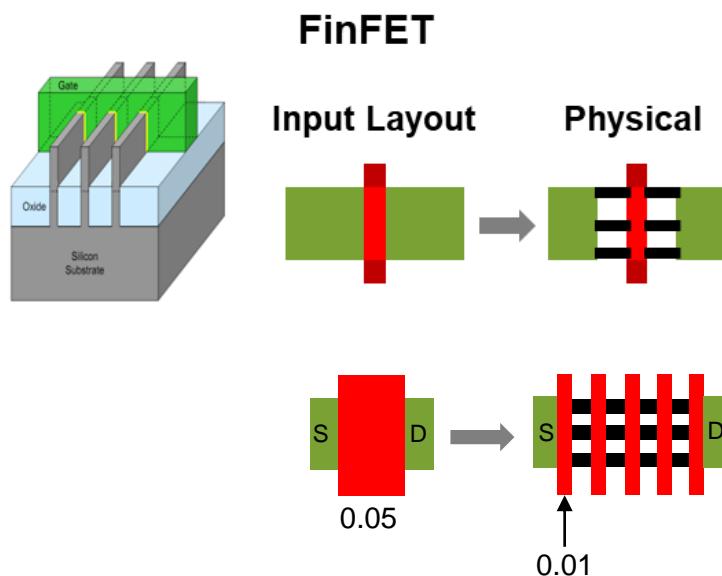


Challenge of Physical Implementation

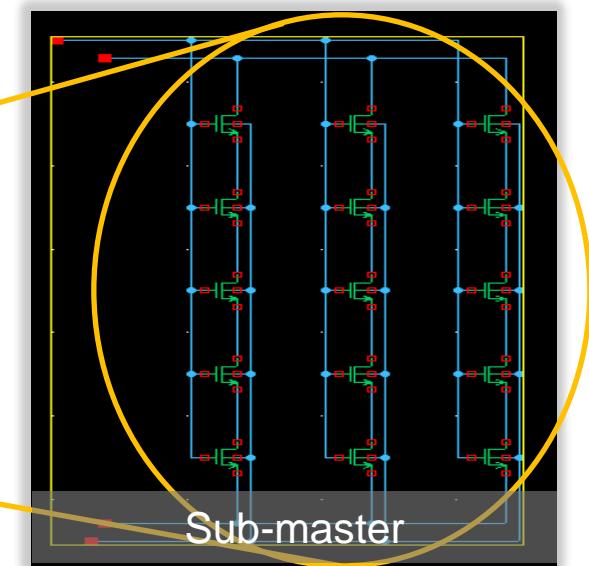
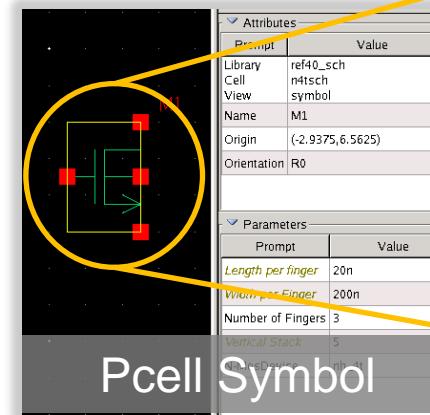
FinFET Design Challenges

Limits quantized device widths

- Only discrete widths and poly pitch possible 只會提供特定的寬度(以確保效能) · 較沒有彈性
- One schematic device map to many of layout units
- Groups of fins can be arranged in complex series and parallel combinations



**L = 86n
W = 200n
NF = 3
stack = 5**



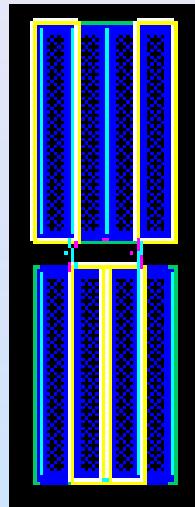
A New Paradigm

原本單顆的device可能會要使用更多finfet來完成

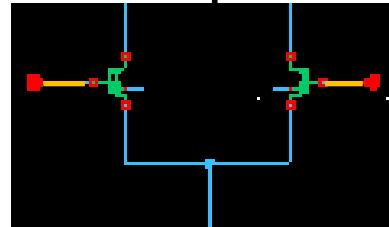
Planar



$M = \dots$
 $nf = \dots$



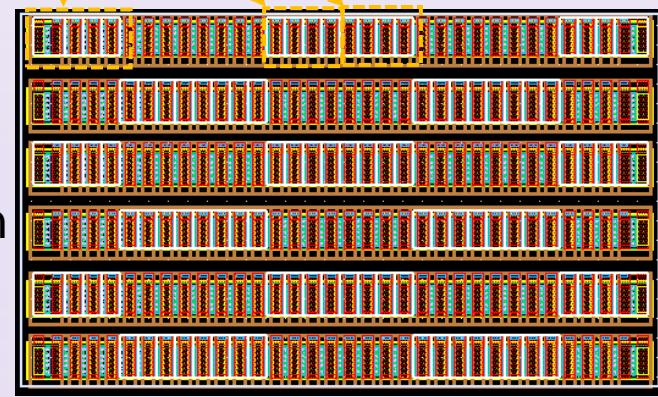
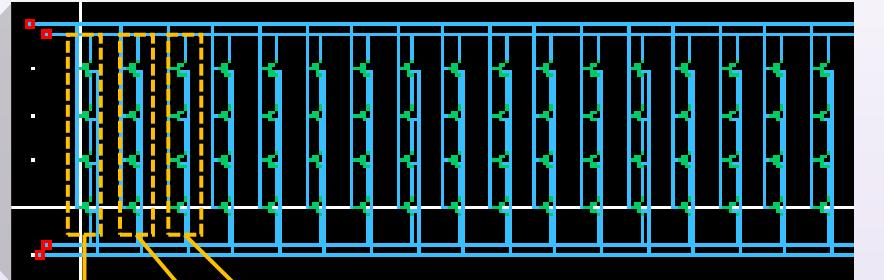
Diff pair



FinFET



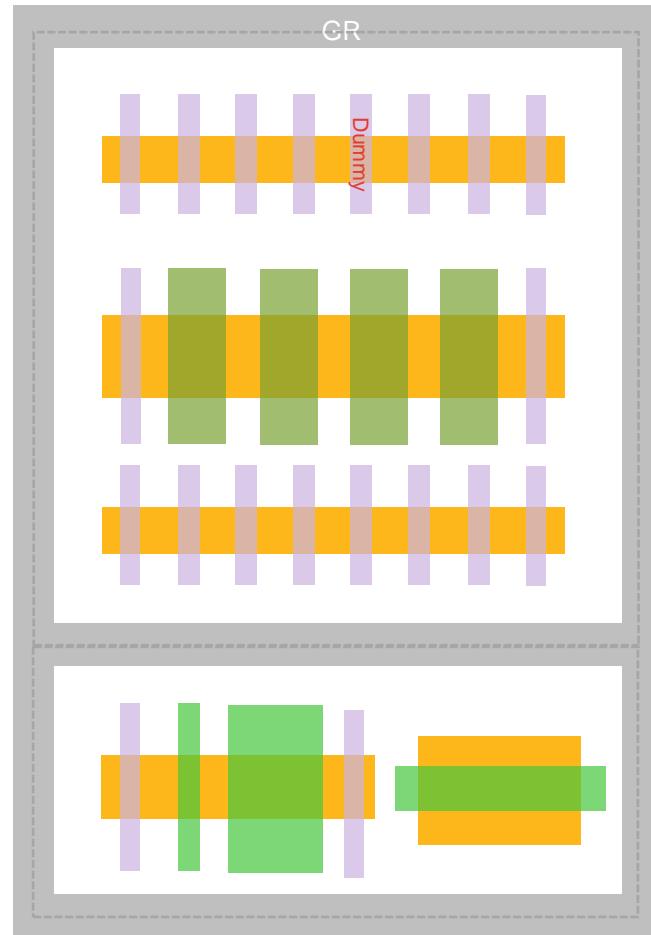
$M = \dots$
 $nfin = 1$
 $stack = n$



2 differential inputs

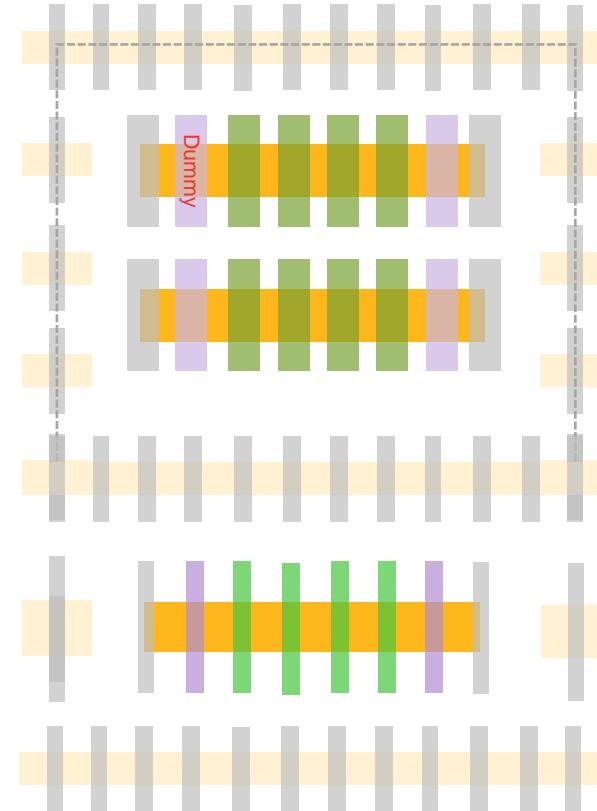
192 gates
connection

Layout Style Transformation

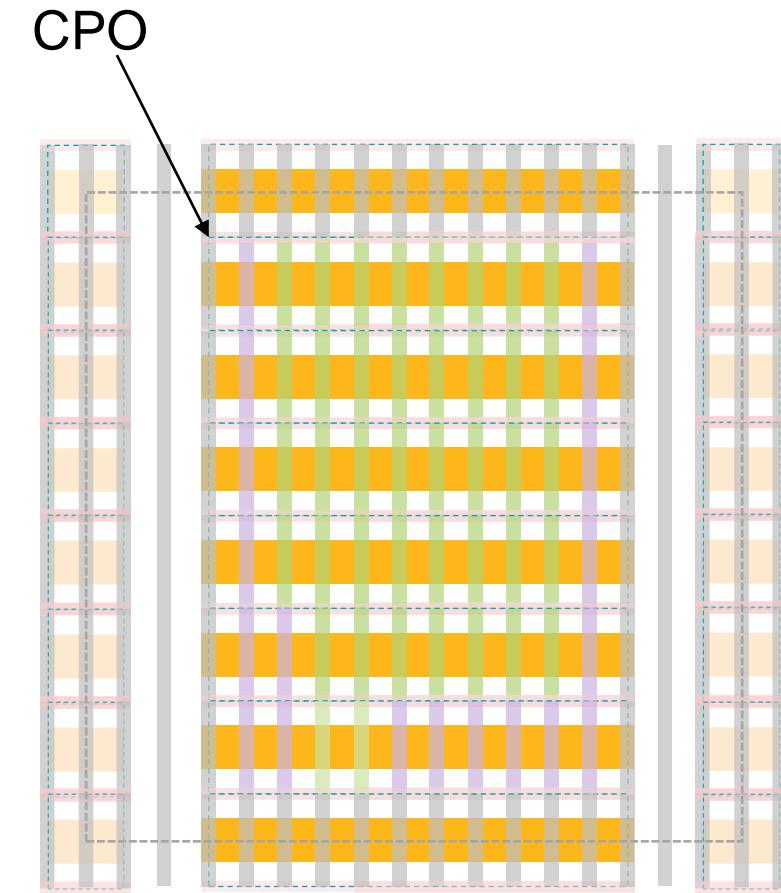


Planar

盡量將相同width, length...的fet擺在一起，
電路較不會影響彼此

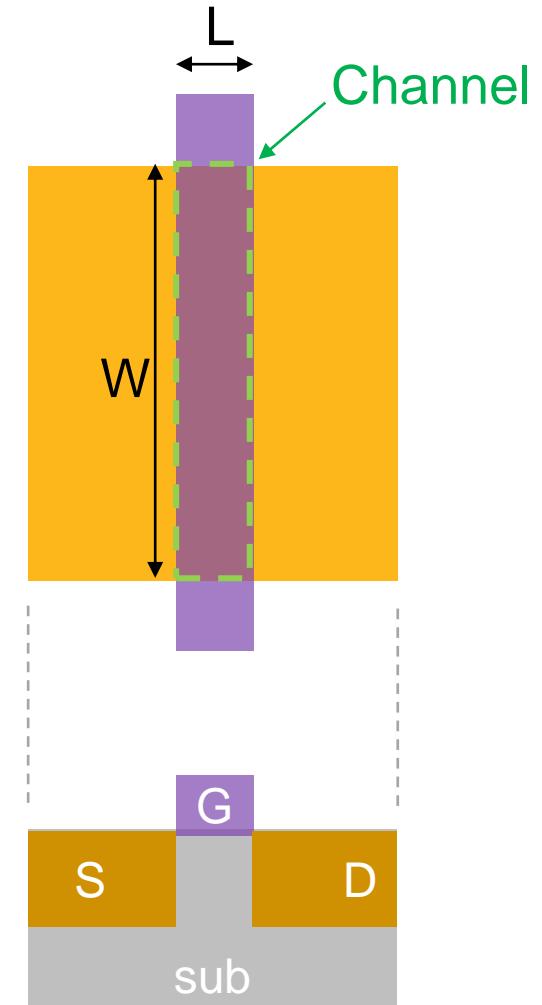
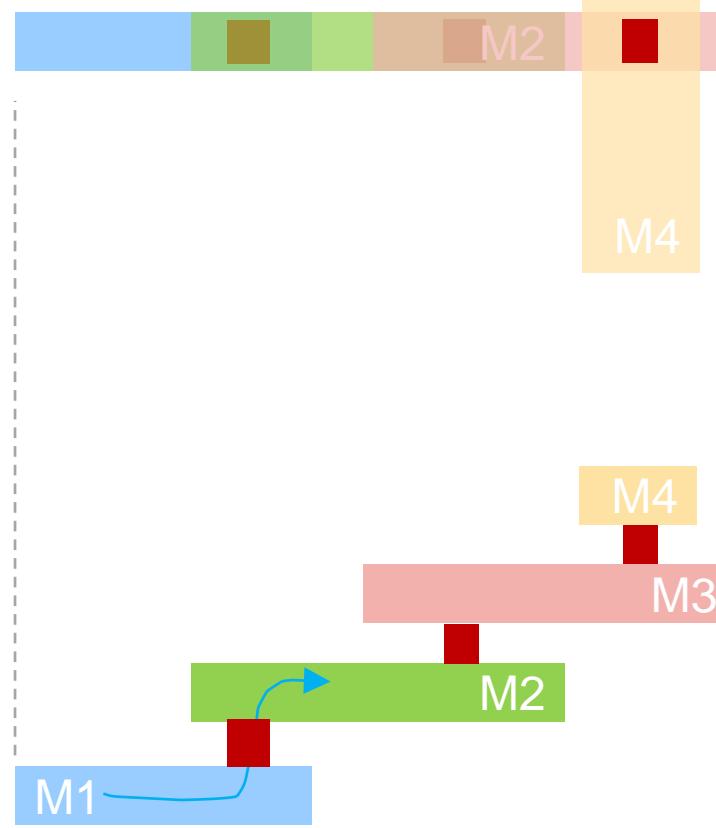
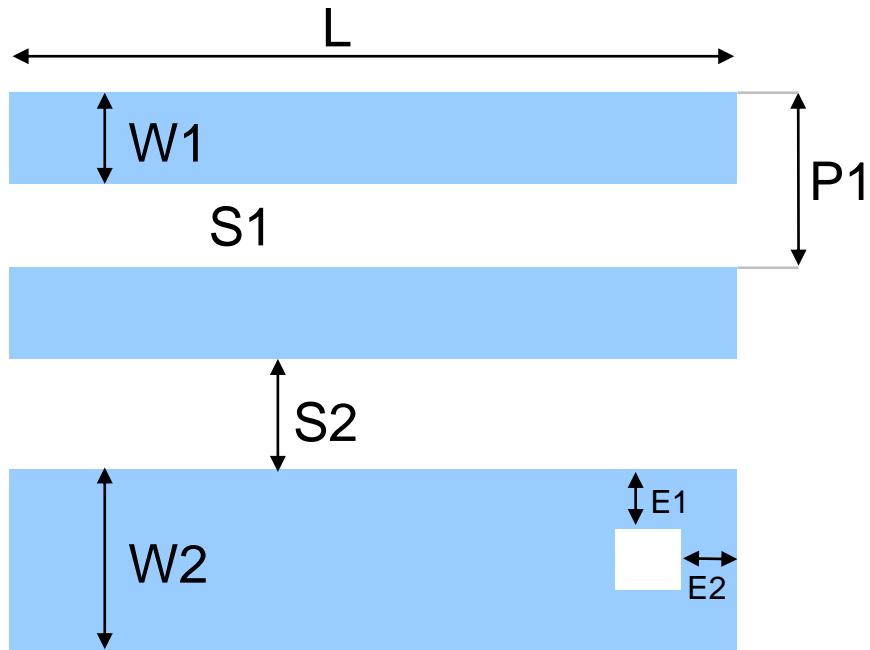


FinFET 16n ~7n

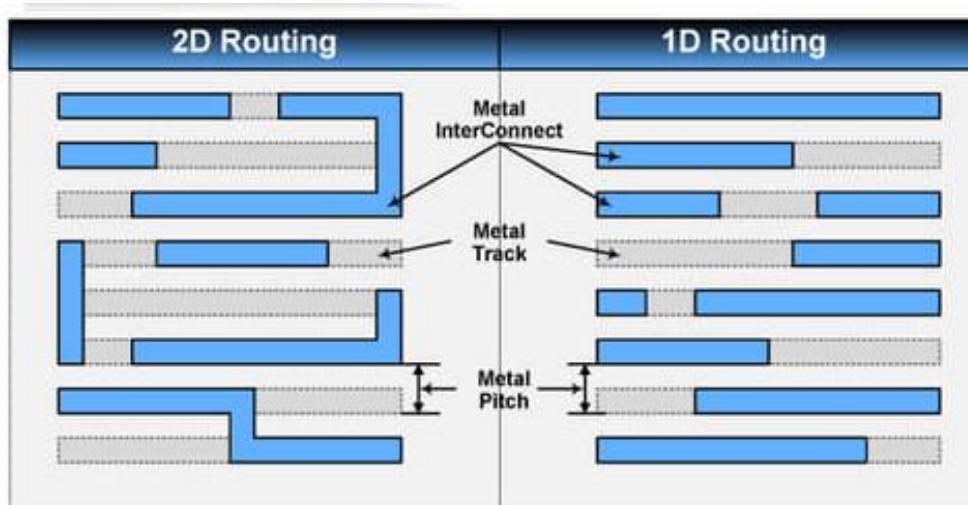
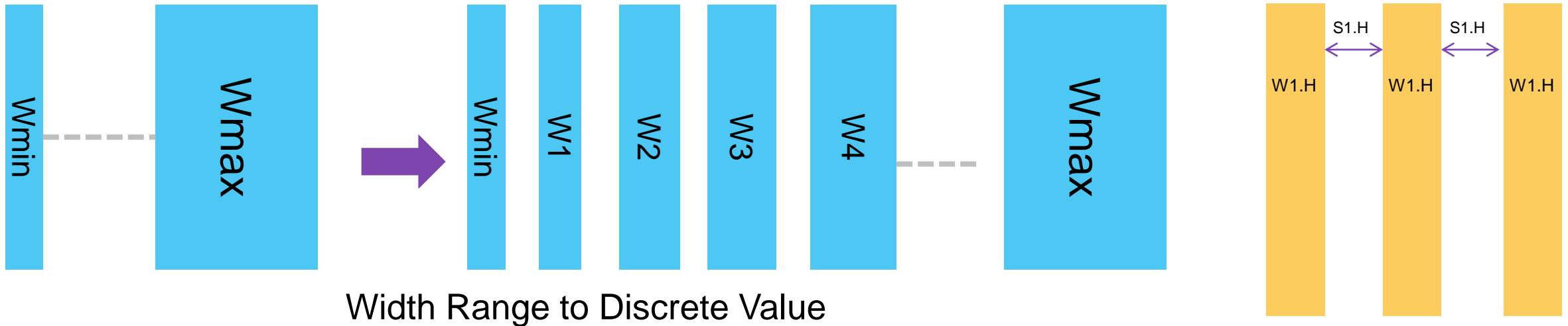


FinFET 5n~2n

Planar Layout Example & General Rule



Rule Change

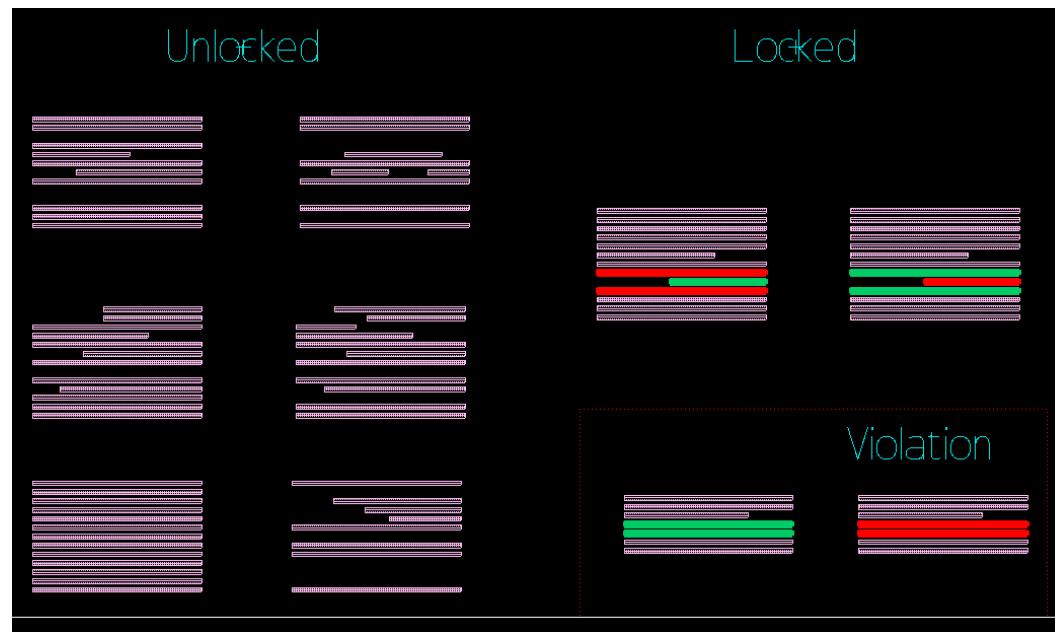


會有一些特殊規則以滿足製程的考量:
像是layout只能走單向不能走雙向...

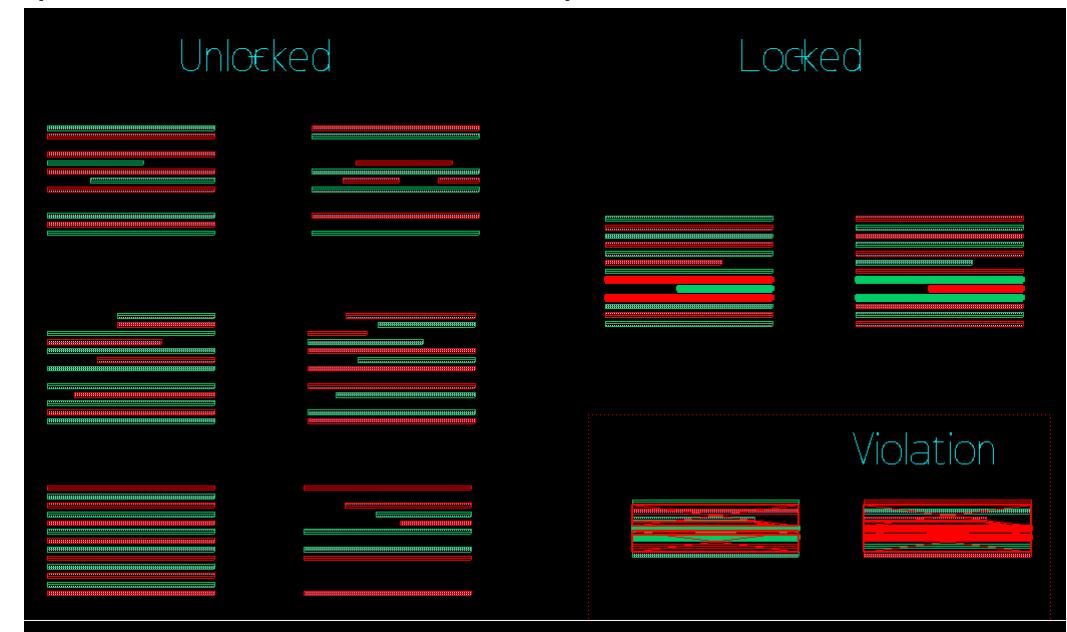


Prefer/Non-Prefer width

Metal Coloring



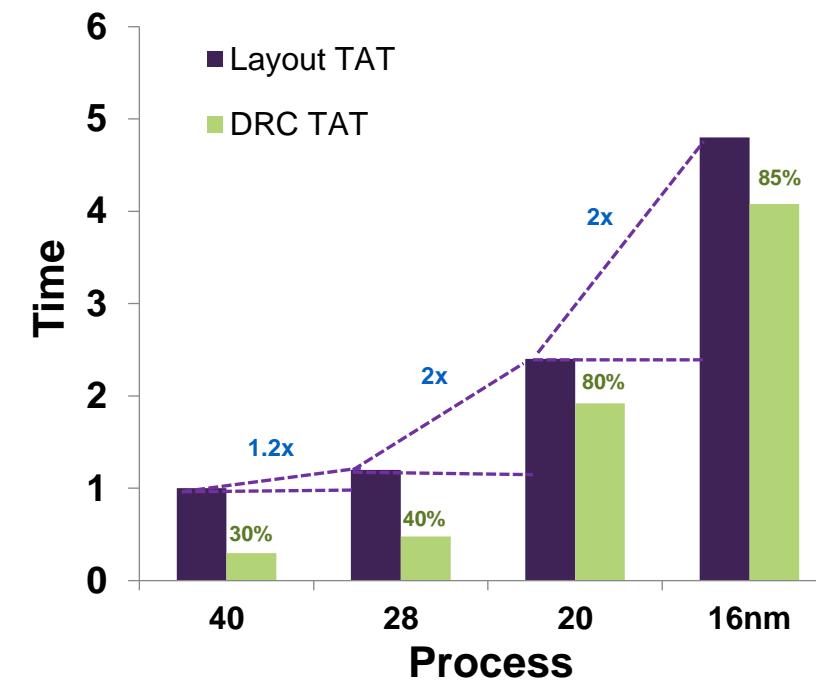
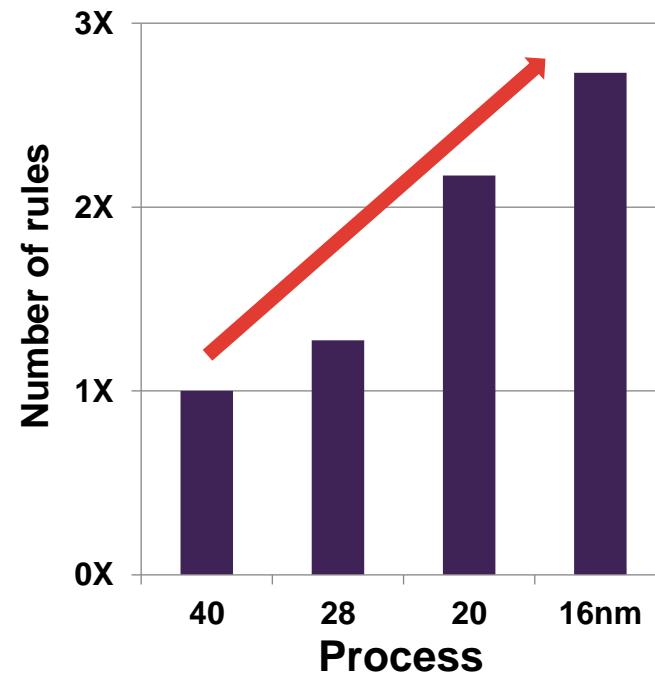
上色後，紅綠就分別代表一張不同的光罩
(因此下圖就是兩張不同的光罩)



Advanced Design Challenges

Complex DRC Rules

- Rule complexity has more than doubled since 40nm
 - DPT, MEOL layers, VDRC and FinFET devices

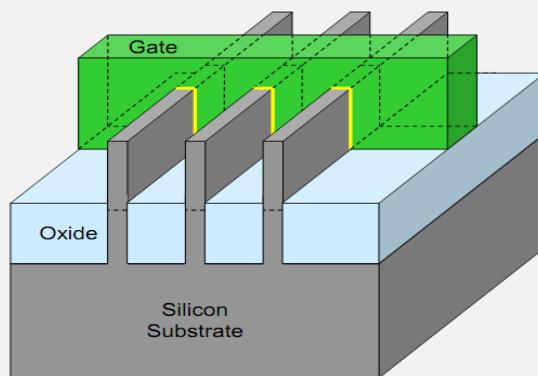
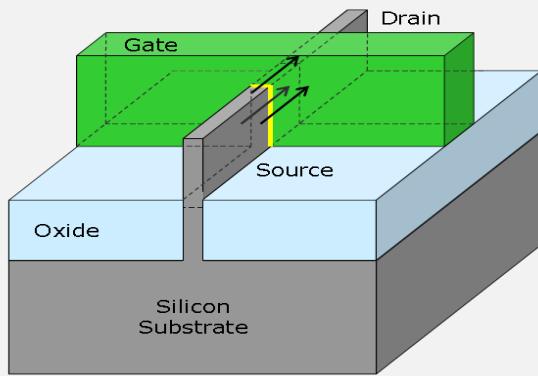


Tools Solution

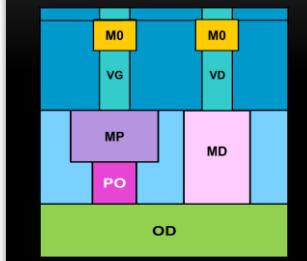
Tool Support

- **MPT** 不必等到設計完才上色 · 在設計的當下就已經上色完畢
 - Color: Color rendering, Assignment, DRD Decomposition, Track Pcell
 - Data I/O support Color mapping and Color attribute cell Swap
- **Fin**
 - wdieAlingment snapping
- **Poly**
 - Poly pitch and track snapping
- **MEOL**
 - Local interconnect
- **1D Route**
 - Constraint Aware Editing , Discrete value, Prefer Direction
- **Cut Poly, Cut Metal**
 - Erase layer, Highlight Connected
- **Unified Wiring**
 - Metal track region/ Track Pcell,
- **DRC**
 - ICV Live, Error View
- **EM,IR**
 - In-design EM, IR
- **Density Viewer**
- **VDRC**

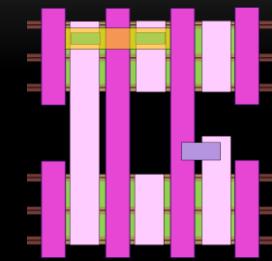
Rules



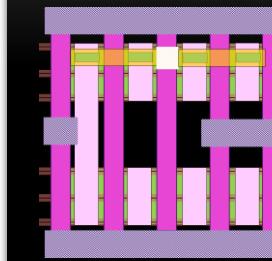
Device
Layers



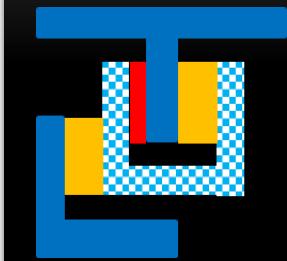
Local
Interconnect



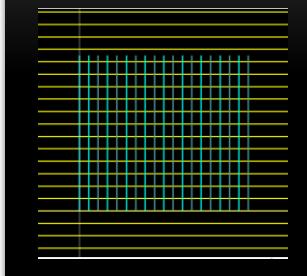
Cut
Layers



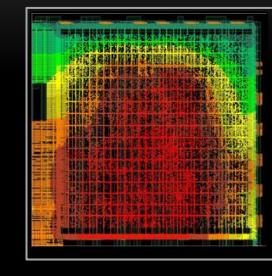
Coloring



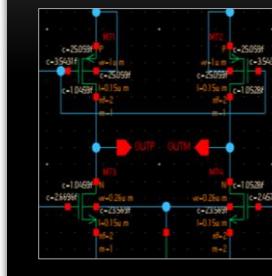
Routing
Tracks



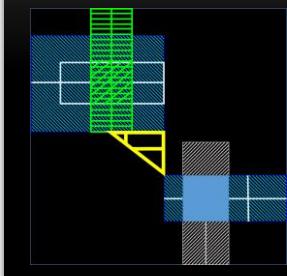
Electro-
migration



Parasitic
Extraction

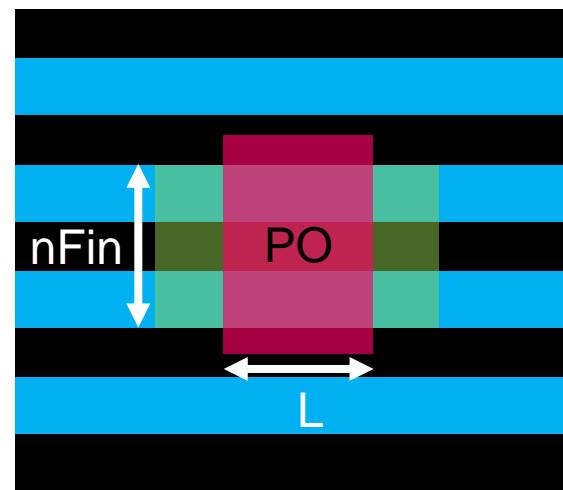


Physical
Verification

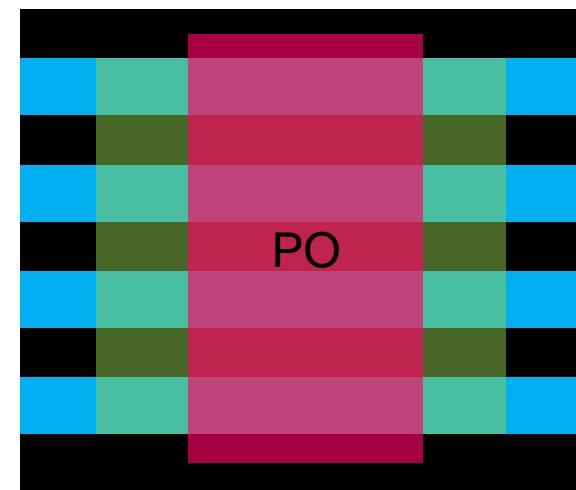


Discrete Device Sizes

- **Gate width**
 - Integer number of fins
- **Gate length**
 - Fixed and limited set of lengths
 - Must follow poly pitch rules for gates with different lengths
- **Custom Compiler solution**
 - New device parameters
 - Symbolic editor for creating device arrays
 - One to many mapping in schematic-driven layout
 - Design-rule driven layout



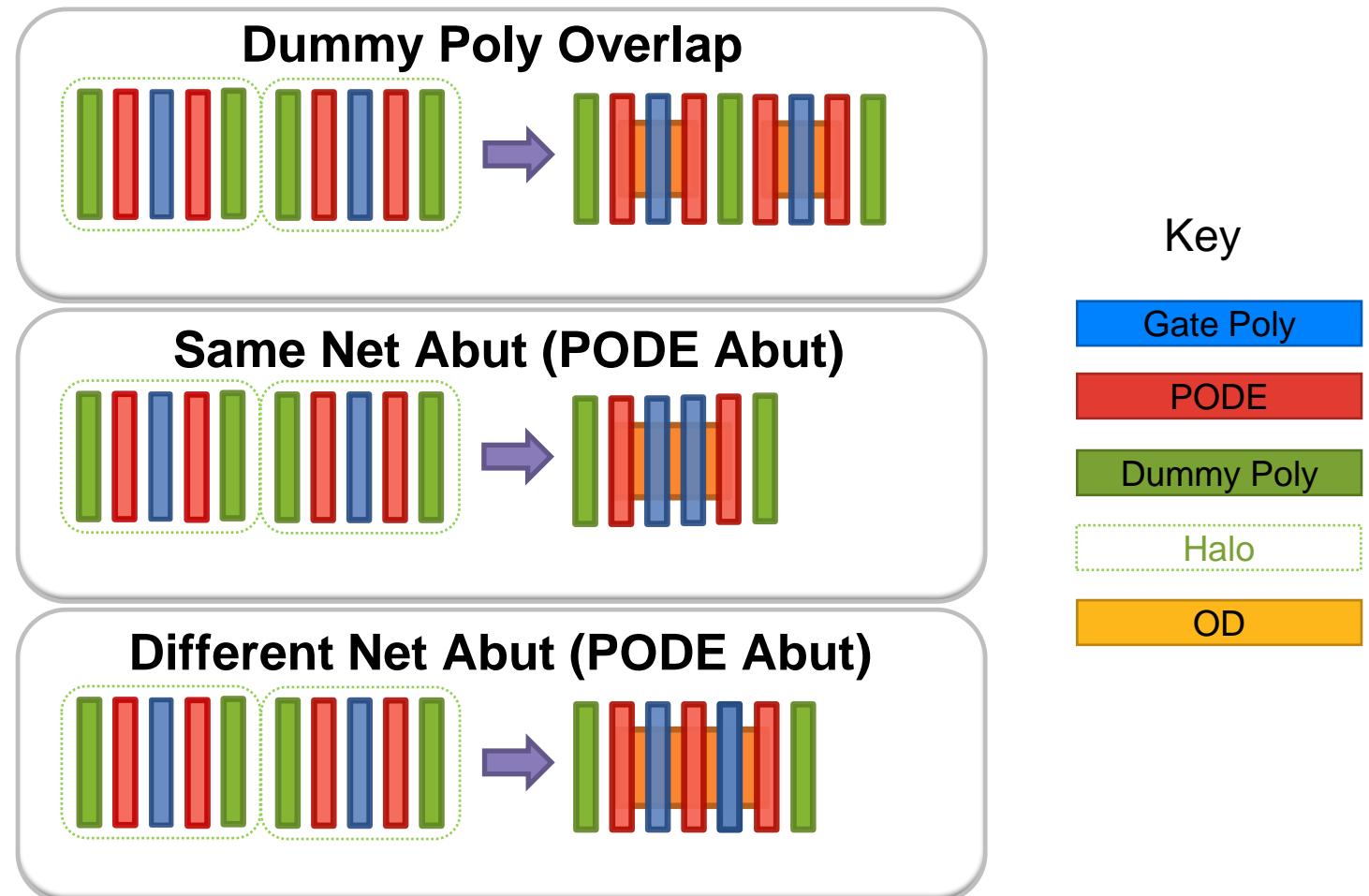
$nFin = 2$
 $L = 10\text{nm}$



$nFin = 4$
 $L = 16\text{nm}$

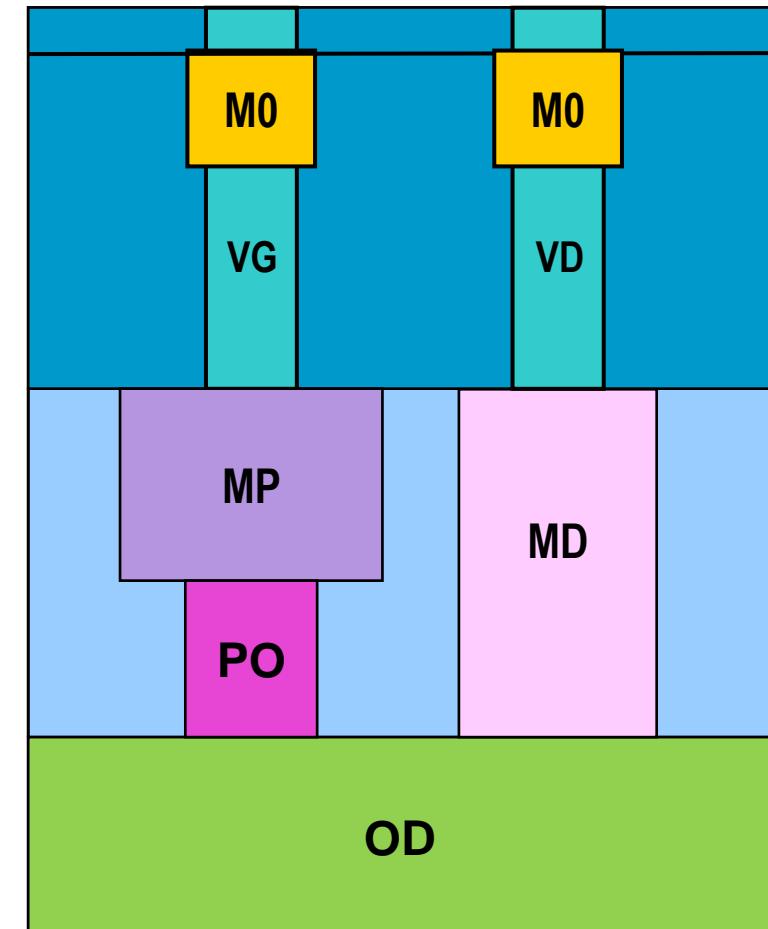
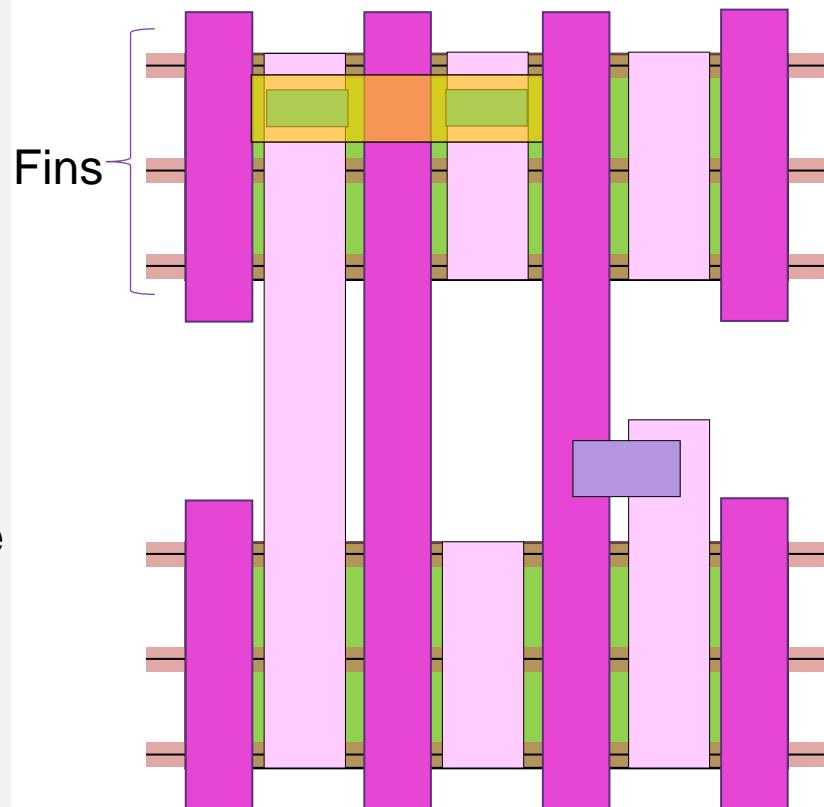
Transition Rules

- **Dummy insertion**
 - Design rules require extensive dummy poly
- **PODE**
 - Poly over diffusion edge
 - Dummy at each diffusion edge to reduce variability
 - Dummy inserted to break continuous diffusion
- **Custom Compiler solution**
 - Easy dummy insertion (will cover later)
 - Transition rules supported in PCell abutment



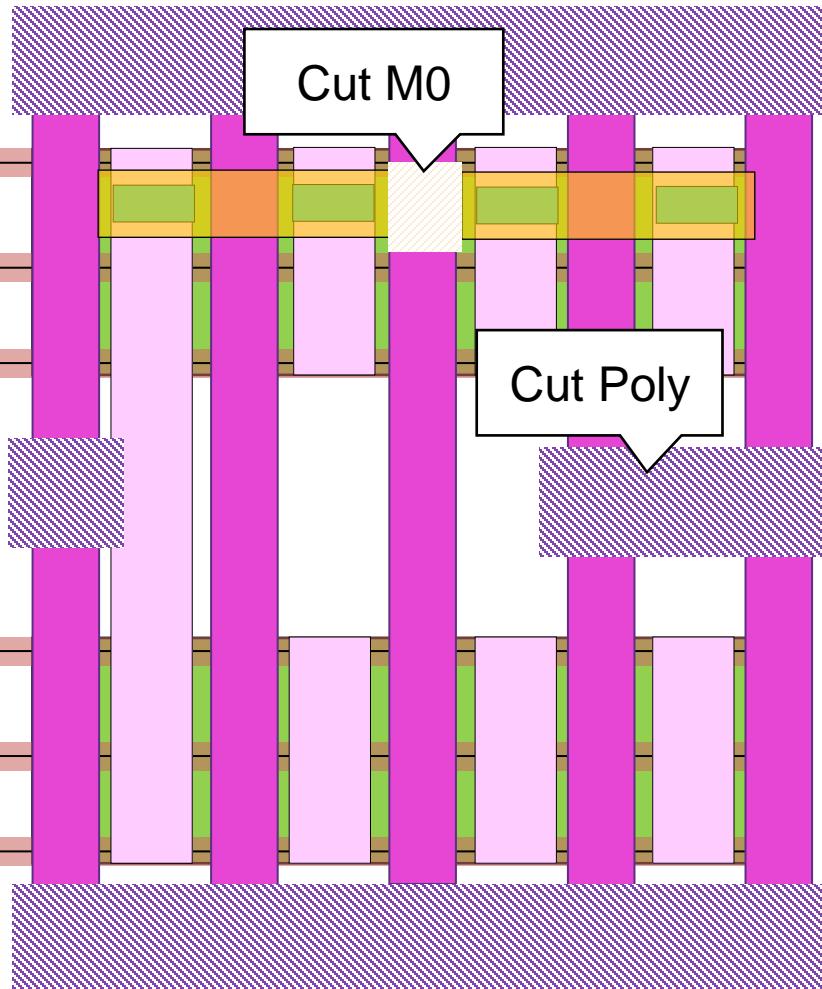
Local Interconnect

- **Very restrictive rules**
 - Length & width restrictions
 - Direction restrictions
- **Contactless connections**
- **Custom Compiler solution**
 - “Create path” command supports width and direction constraints from tech file
 - Spacing, length and direction rule checks
 - Connectivity engine models contactless connections



Cut Layers

- **Tight layout requires many cut layers**
 - Poly, diffusion & some metal layers must be cut
 - Layout can look confusing – especially at 7nm
- **Custom Compiler solution**
 - Schematic driven layout simplifies connectivity tracing
 - Connectivity updated when cut shapes are drawn
 - Cut shapes can be anywhere in layout hierarchy



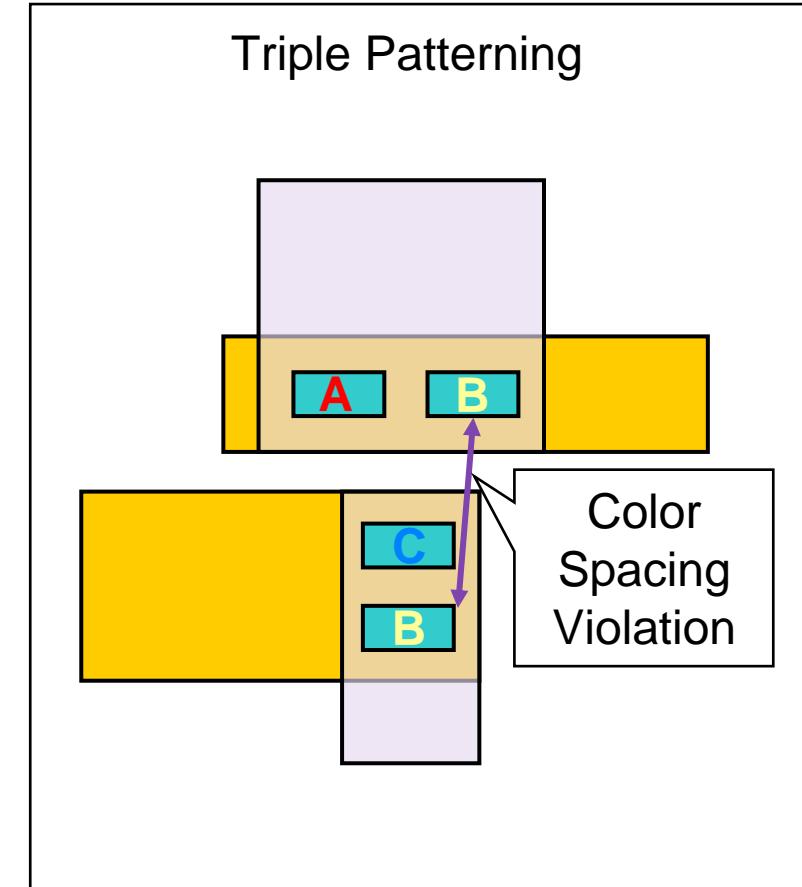
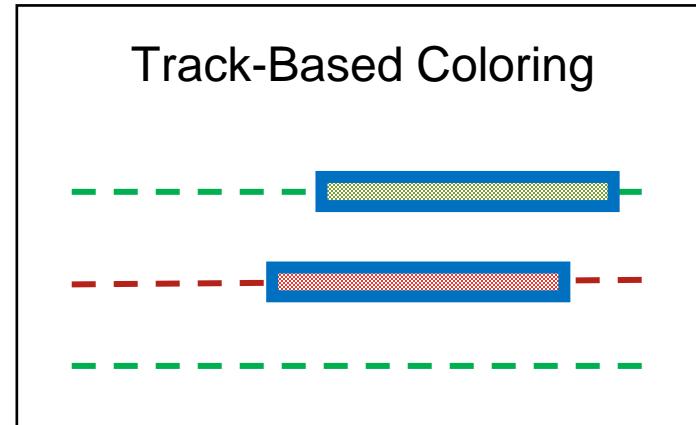
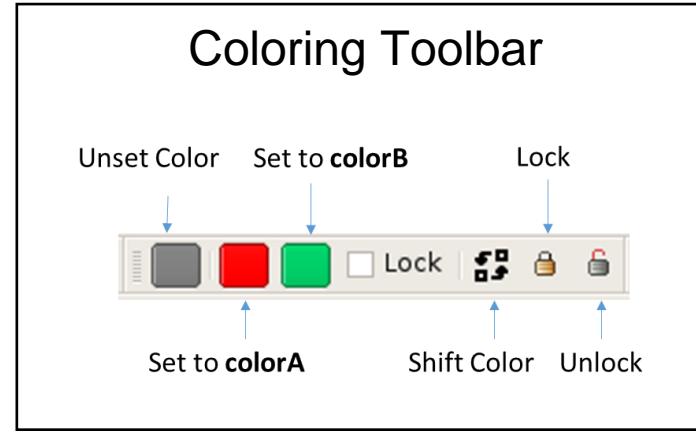
Coloring

- **Coloring**

- Many layers require decomposition into two or more masks
- Custom users need full control over coloring choices
- Automation needed where color choice is not critical

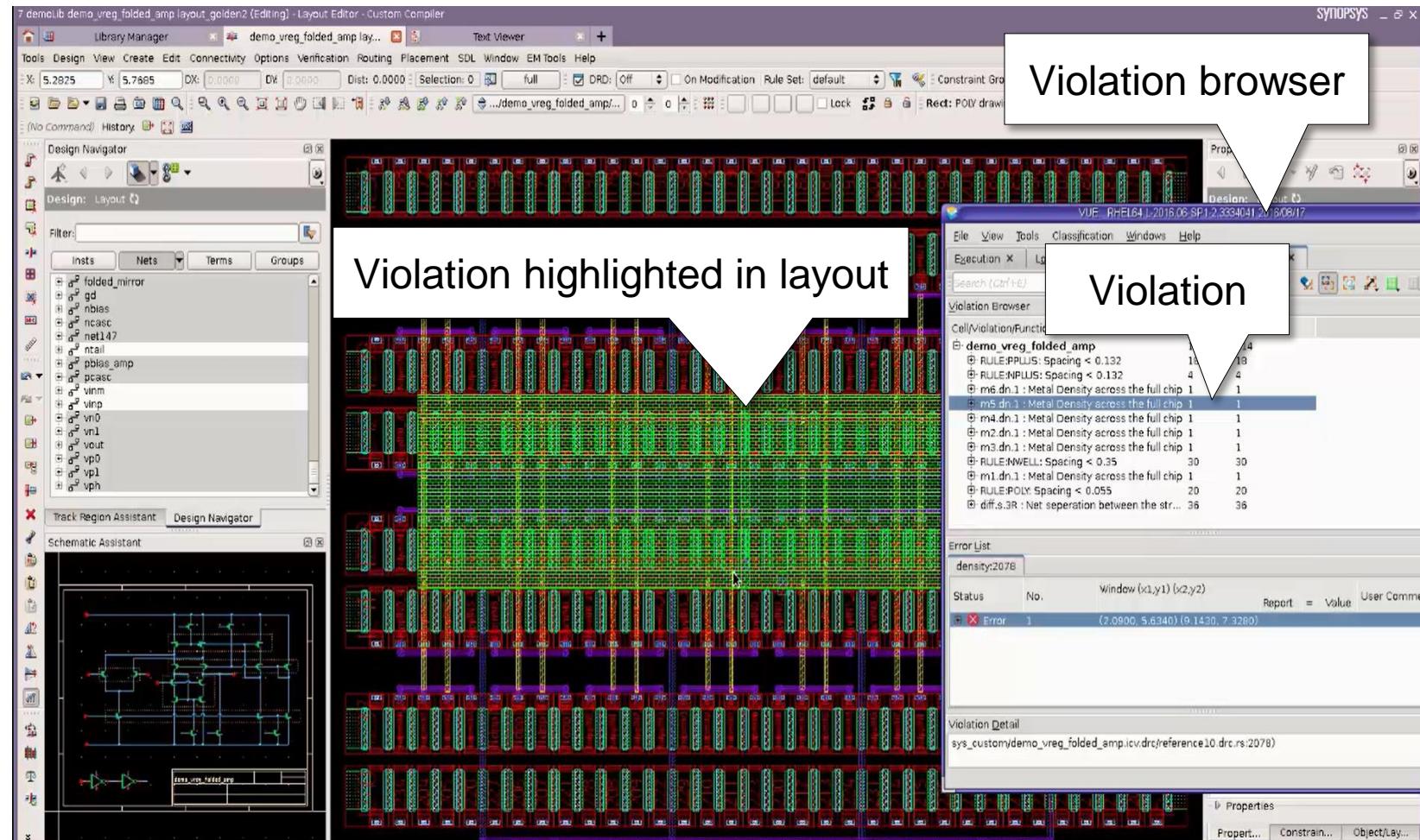
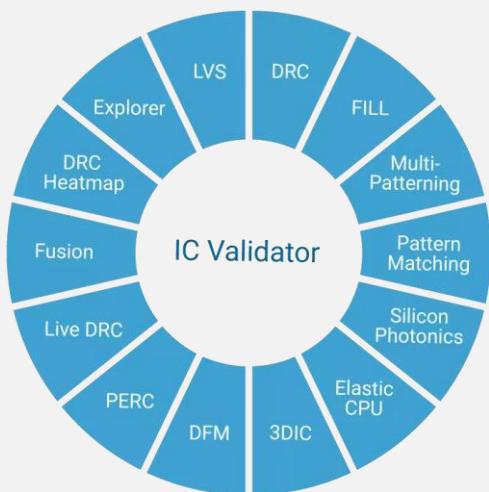
- **Custom Compiler solution**

- Coloring toolbar for manual coloring
- Built-in automatic coloring and color propagation
- Track pattern assistant to assign color by track
- Tool checks for color violations



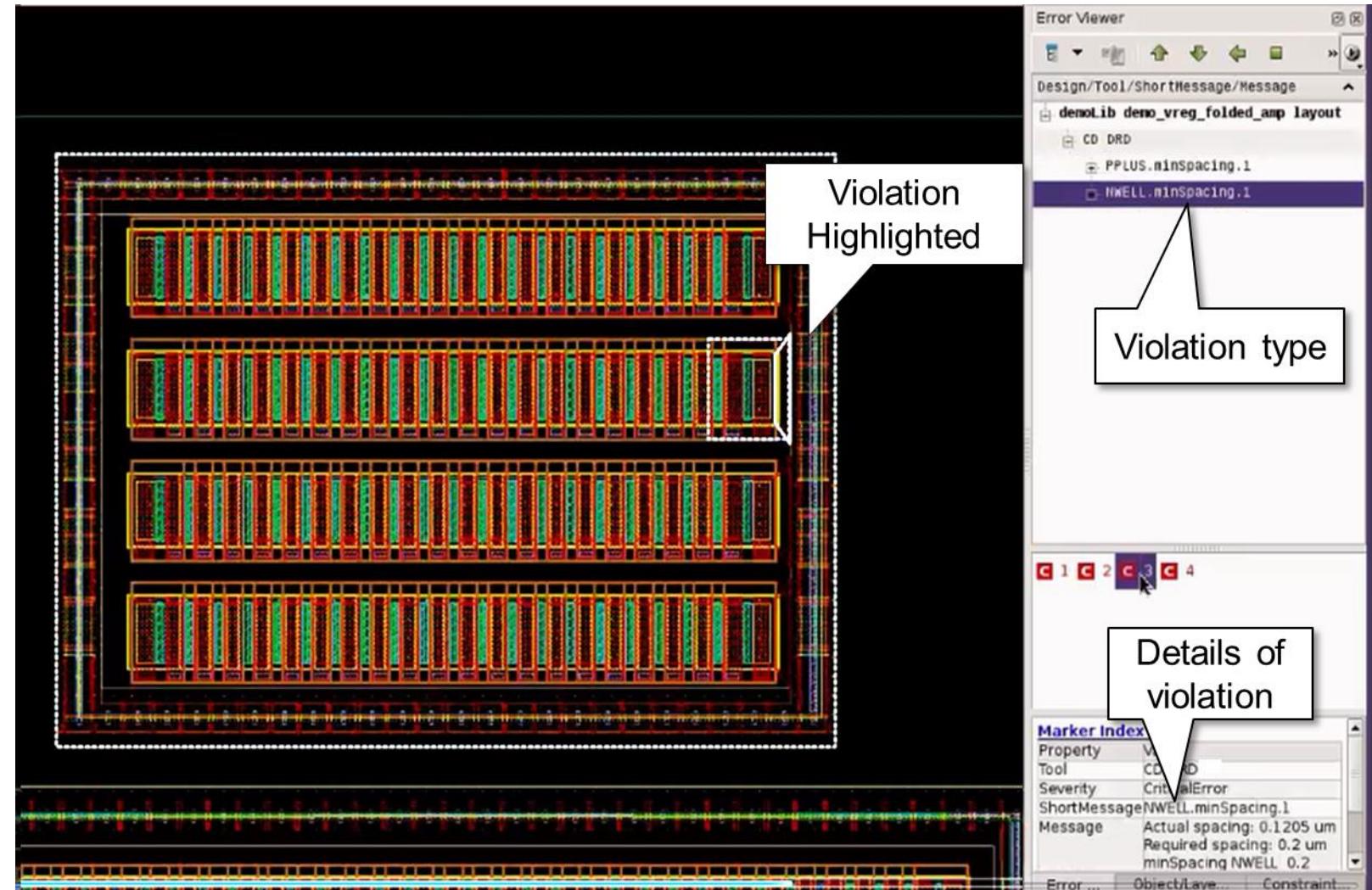
In-Design with IC Validator

- **Sign-off quality DRC/LVS**
 - Trusted engine
 - Foundry certified rule decks
- **Custom Compiler solution**
 - IC Validator integration
 - Cross-probable violation report
 - DRC violations shown directly on layout canvas



Custom Compiler Built-in Checking

- **Layout ECOs are difficult**
 - FinFET layout changes are hard to make
 - Important to avoid design rule errors
- **Custom Compiler solution**
 - Window check
 - Check after shape is created
 - Check only desired rules
 - Fast, built-in engine
 - Provide color guidance



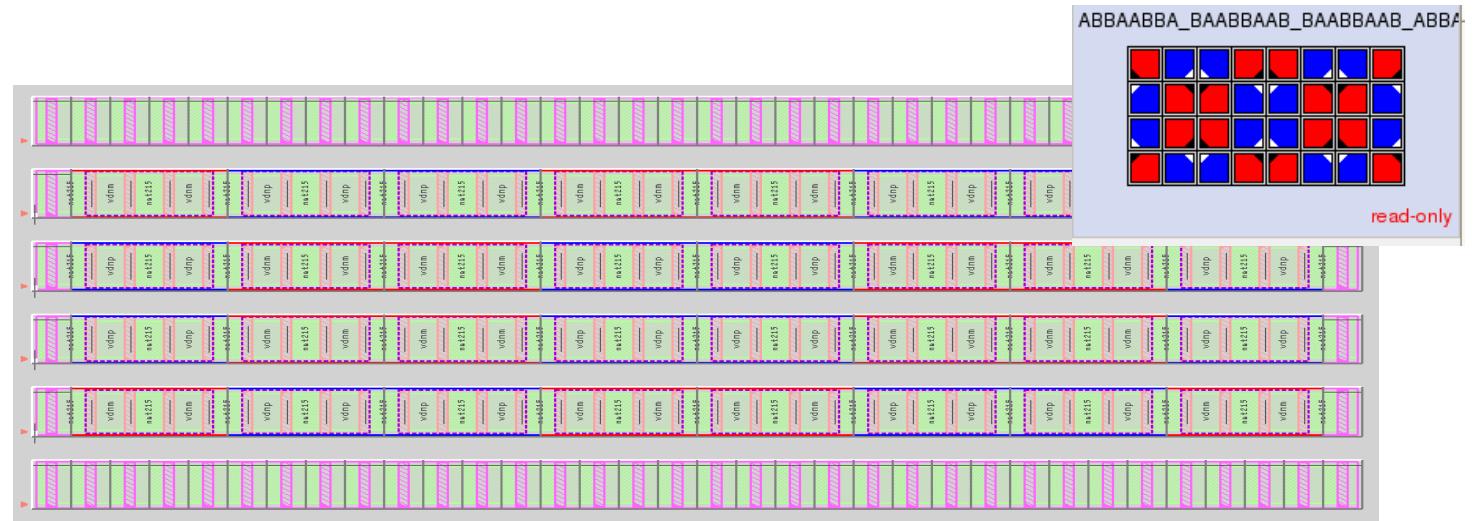
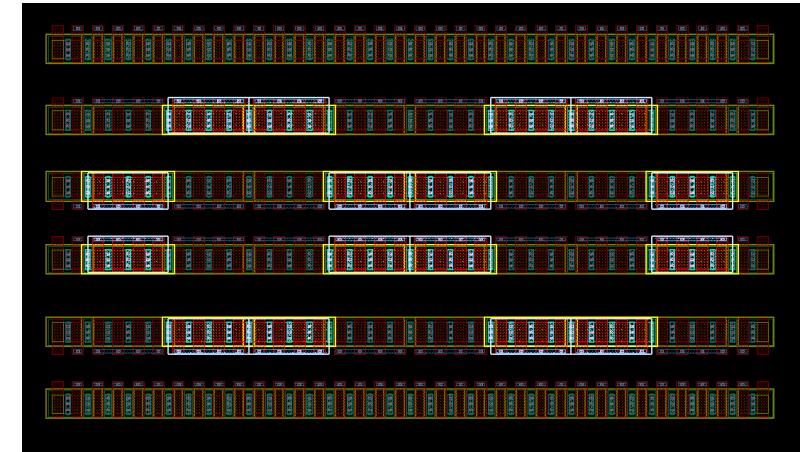
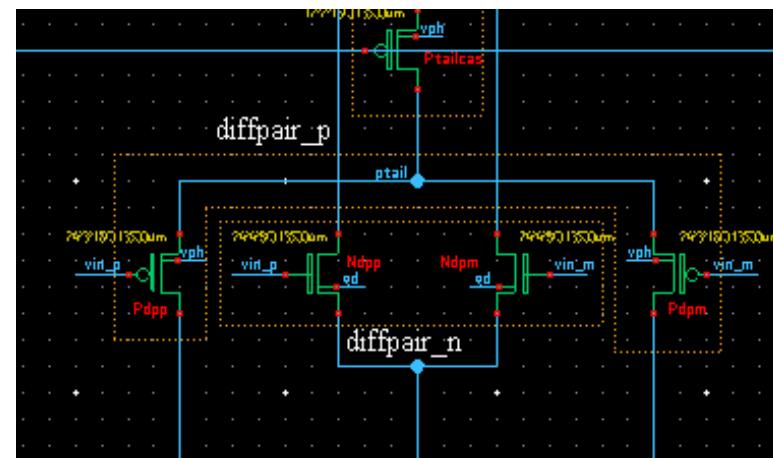
FinFET Device Arrays Placement

- **Matching with arrays**

- Individual transistors can be an array of elements
- Matching requires interdigitating devices from two or more device arrays

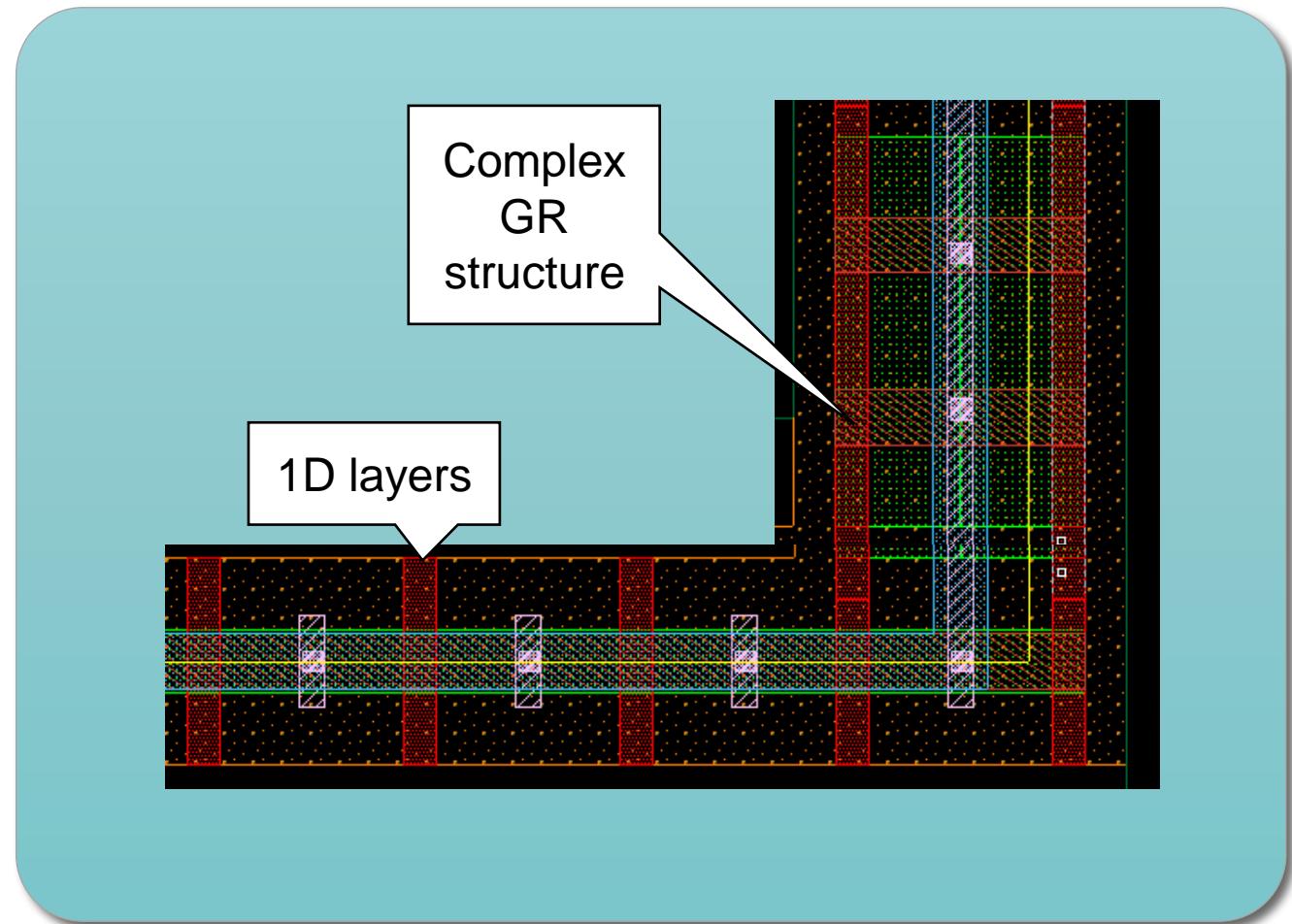
- **Custom Compiler solution**

- Symbolic editor for FinFET device arrays
- Supports multiple transistors, each with multiple fingers and vertically stacked devices



FinFET Guard Rings

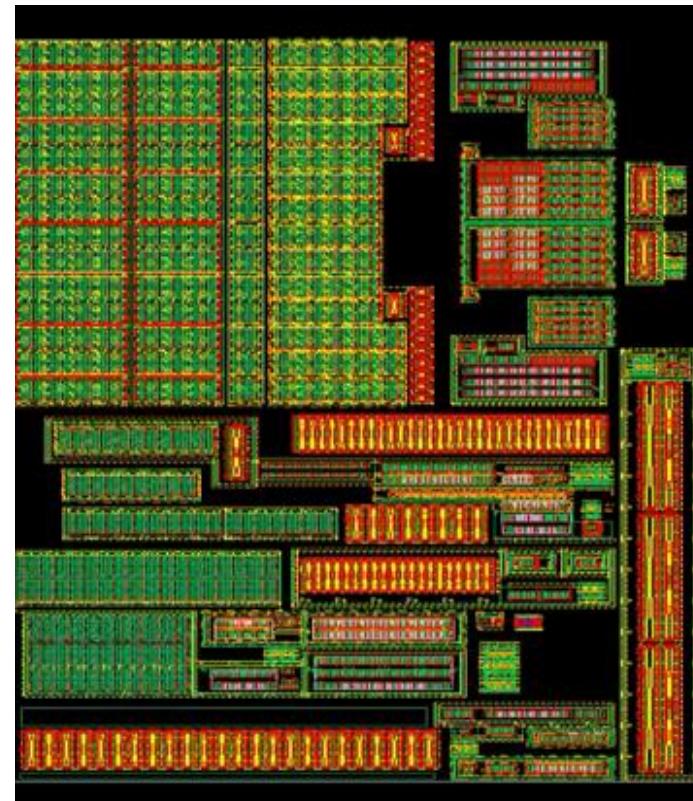
- **Complex layout structure**
 - Shapes on multiple layers
 - 1D routing layers
 - Snap to tracks and fin grid
- **Custom Compiler solution**
 - Editable PCell GR
 - Automatically generate complex shapes
 - Direct editing of guard ring, no stretch handles needed
 - Support stretch, reshape, chop, heal features



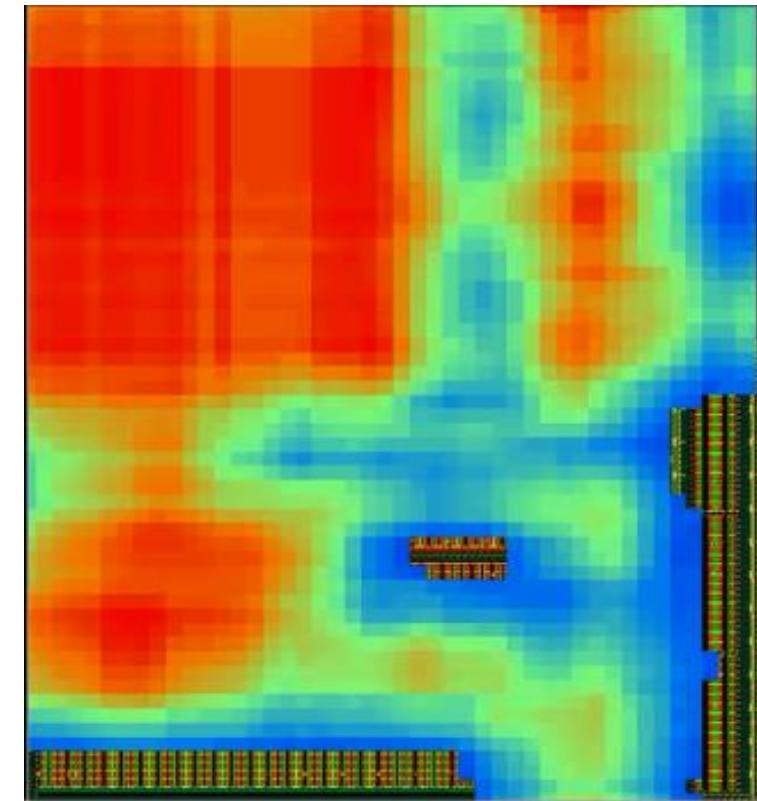
Density Rules

- **More density rules**
 - Metal, poly, diffusion and cut layers have density rules
 - Mask color density rules
 - Difficult to meet these rules with post-processing
- **Custom Compiler solution**
 - Built-in density checker
 - Check by layer and by color
 - Overlay hot-spots in layout

Physical layout



Poly density

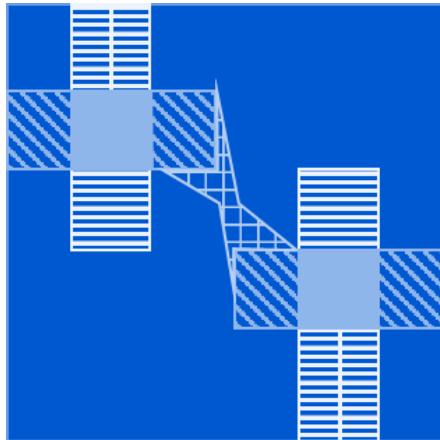


Physical Verification Throughout The Flow

Custom Compiler built-in checking

Fast built-in checks during layout

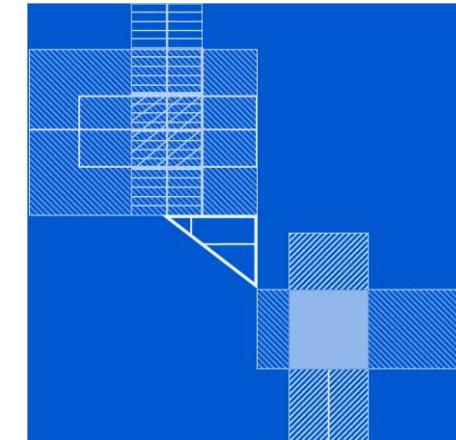
- Design rule checks
 - Full design rule checking engine
 - Window-check and post-commit modes
 - Color and active area density checks



Custom Compiler sign-off checking

Sign-off quality checking

- IC Validator for design rule checks
 - Run ICV from Custom Compiler
 - Review and fix errors
 - Can perform checks on OA database

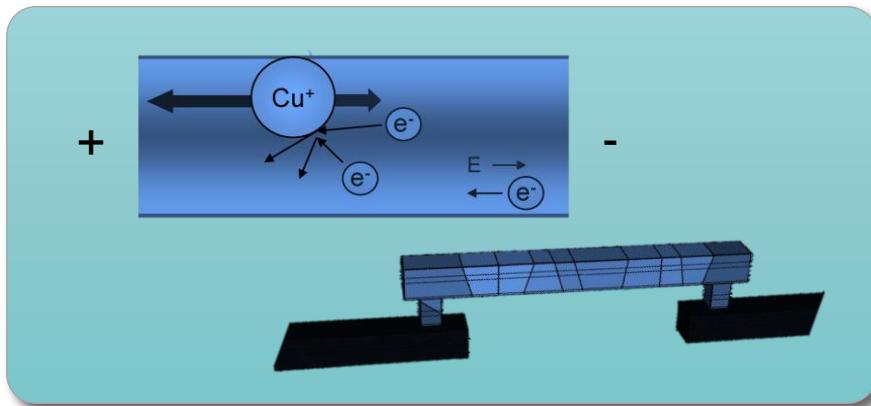


Electrical Verification Throughout The Flow

Custom Compiler built-in checking

Fast built-in checks during layout

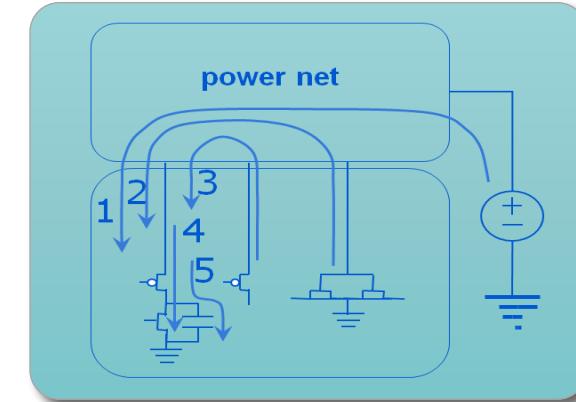
- Electro-migration checker
 - Check for EM issues before layout is finished



Custom Compiler sign-off checking

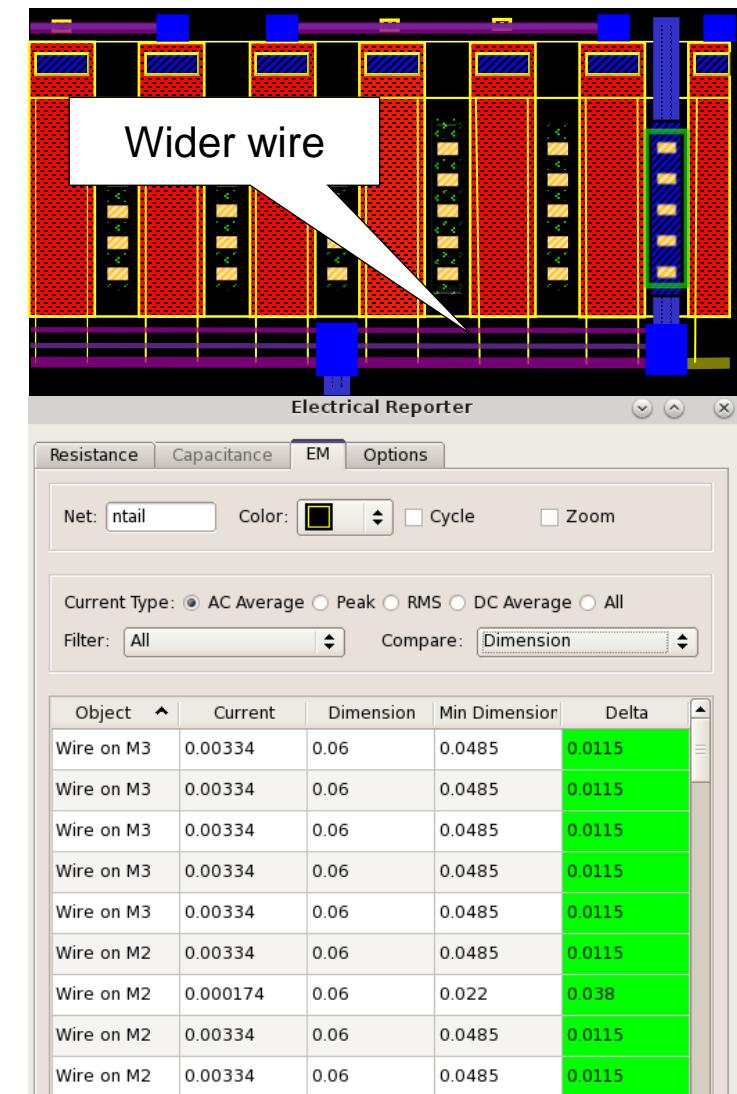
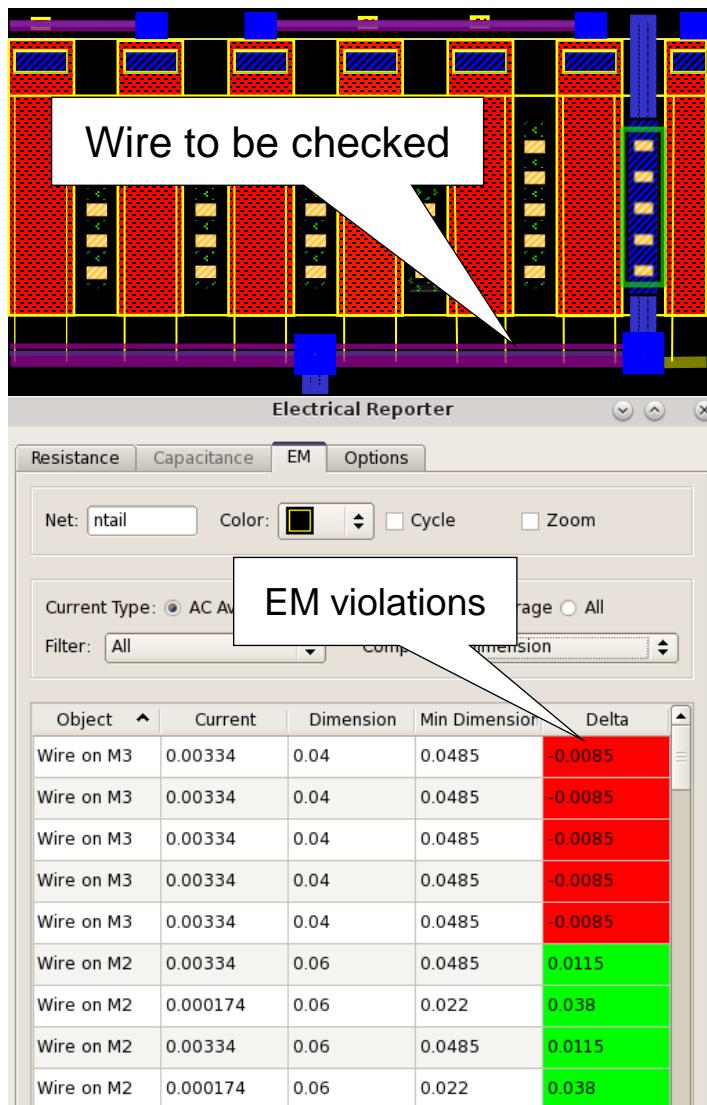
Sign-off quality checking

- CustomSim-RA for EM/IR
 - Run, view errors and perform “what if” analysis



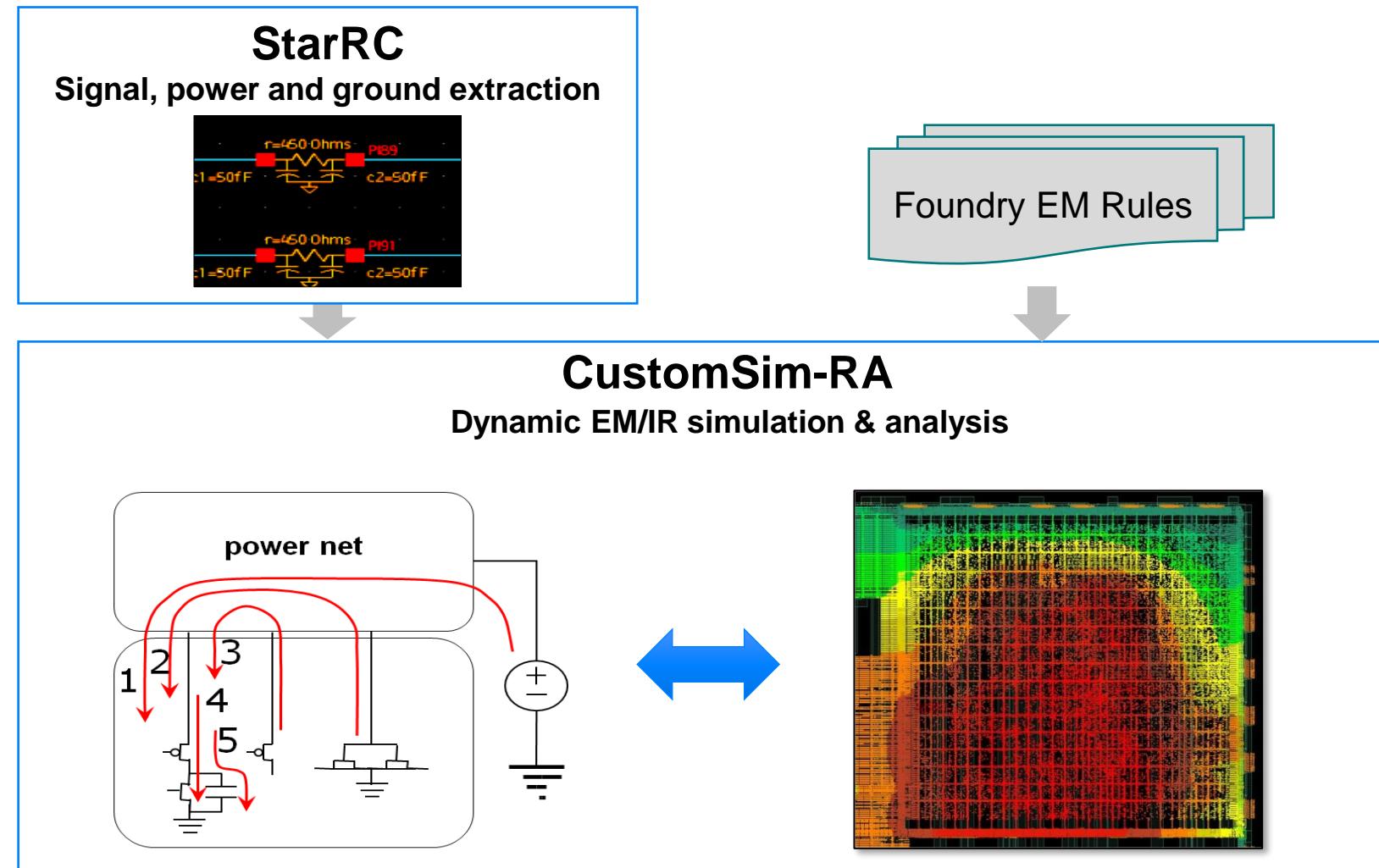
Static EM Checking During Layout

- **Added EM risk with FinFET**
 - Narrower wires
 - Higher currents
- **Custom Compiler solution**
 - Annotate currents from SPICE
 - Built-in electromigration engine
 - Report violations by segment
 - Provide fixing guidance



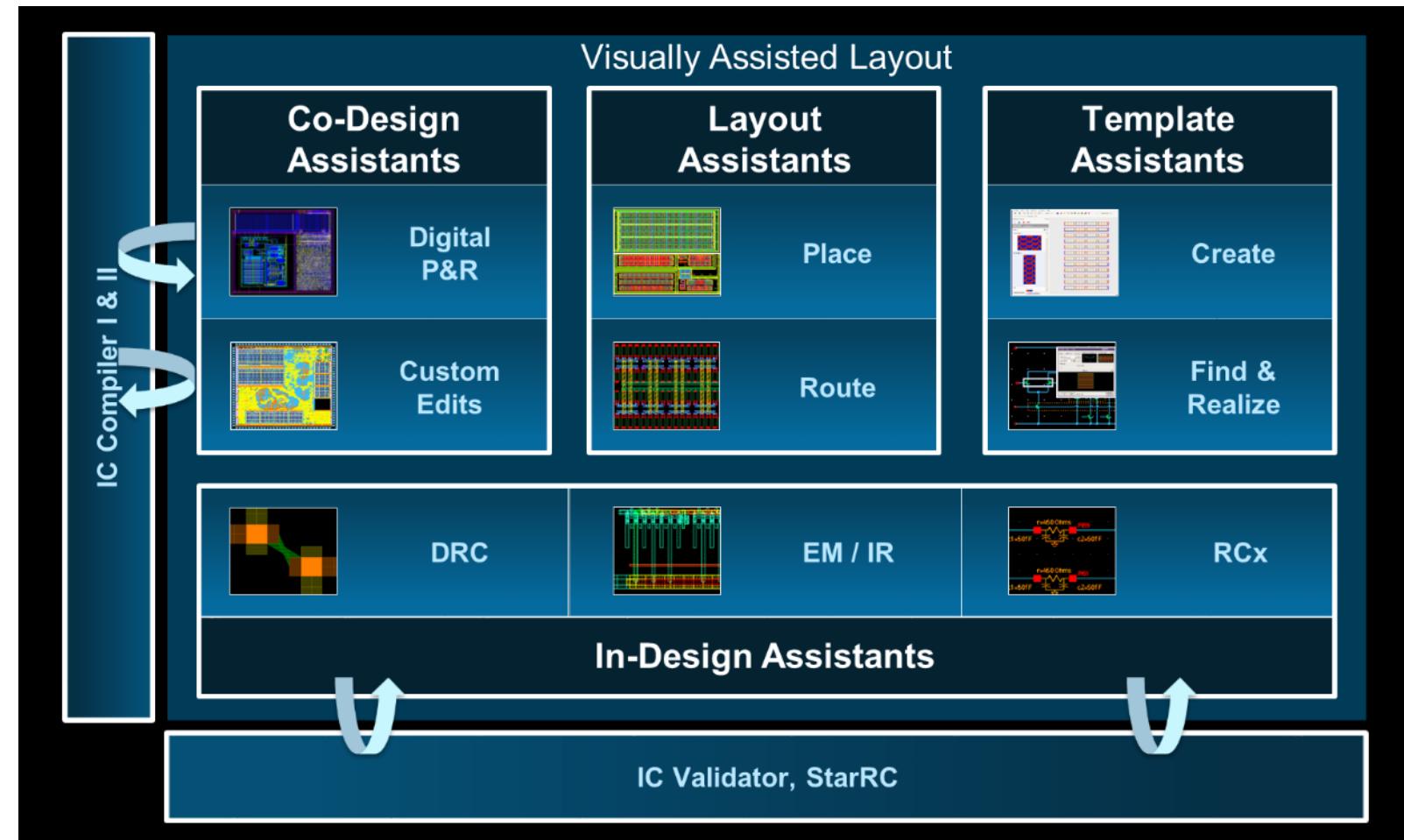
Sign-off EM/IR Analysis

- **Sign-off solution for EM/IR**
 - Optimized P/G extraction in StarRC reduces netlist size
 - CustomSIM-RA dynamic EM/IR analysis
- **Custom Compiler**
 - Integrated with CustomSIM-RA
 - Organizes and filters results for easy analysis
 - Pin-points problems in layout



Custom Compiler Layout

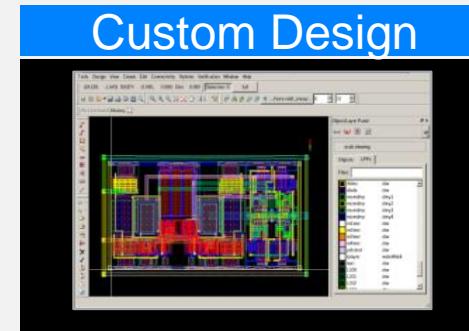
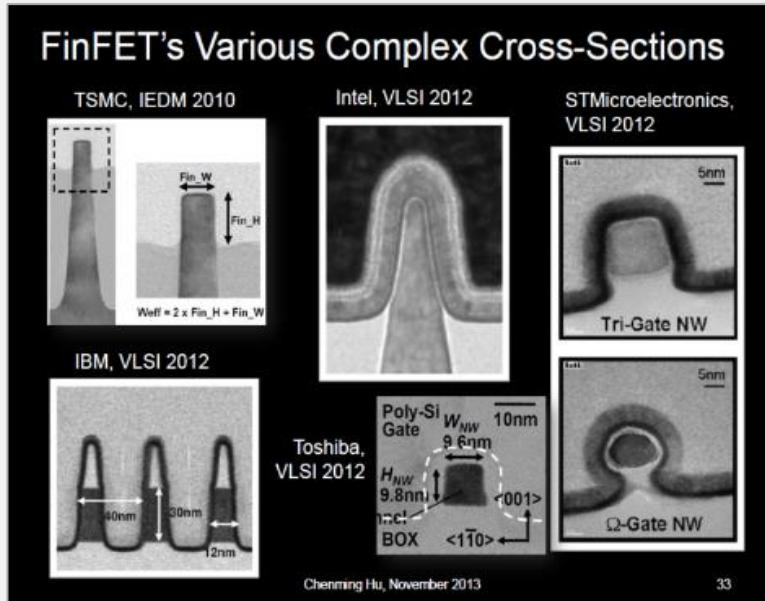
- **Speed layout**
 - Visually assisted automation
- **Re-use know-how**
 - Templates
- **Reduce iterations**
 - In-design analysis
- **Simplify co-design**
 - Unified with digital P&R



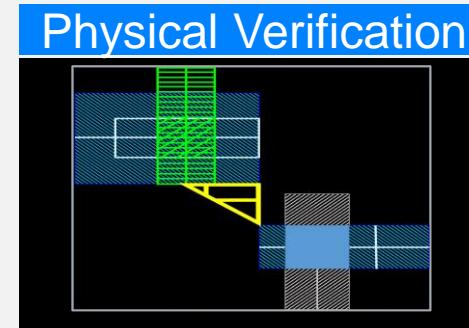
Challenge of Analog & Mixed-Signal Design

Transition to Advanced Technology Nodes

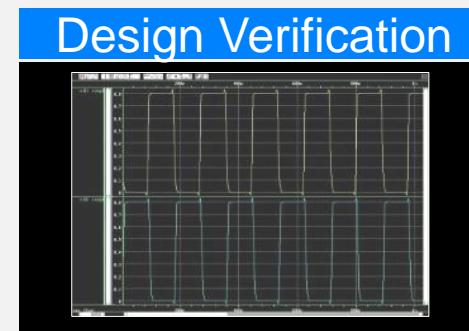
Example: FinFETs Impact Entire Flow



- 2x increase in design rules
- 3x increase in layout effort



- 2-3x more parasitic R/C
- More complex and stringent DRCs

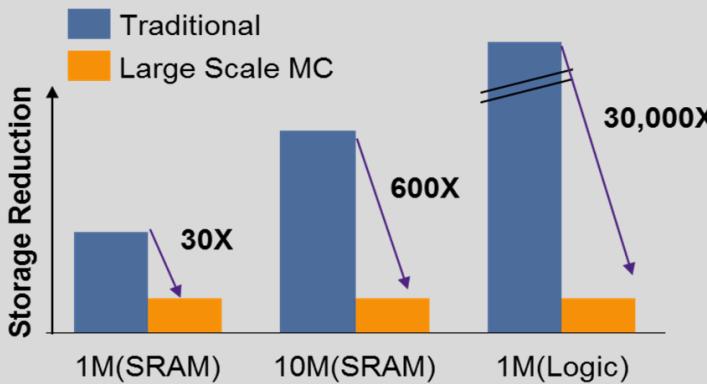


- More complex device models
- Worsening variation, aging, and reliability
- 3-5x increase in corner simulations

Variability Analysis

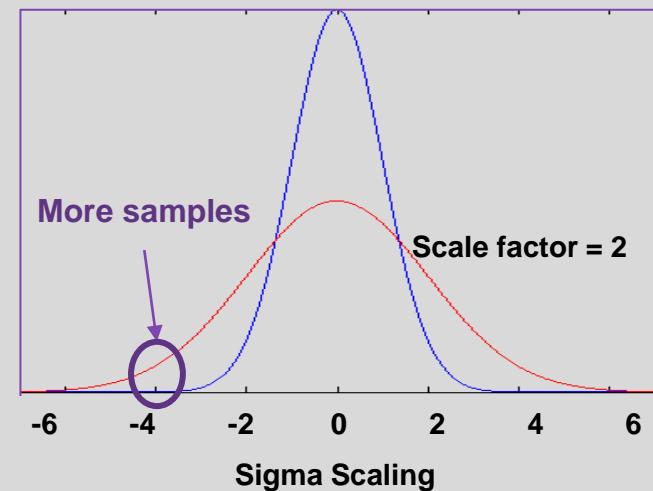
Large scale Monte Carlo PrimeSim HSPICE

- Minimum data set generation
- Massively parallel sim. management environment
- Ideal for high σ Monte Carlo i.e. bit cell, sense amp ...etc.



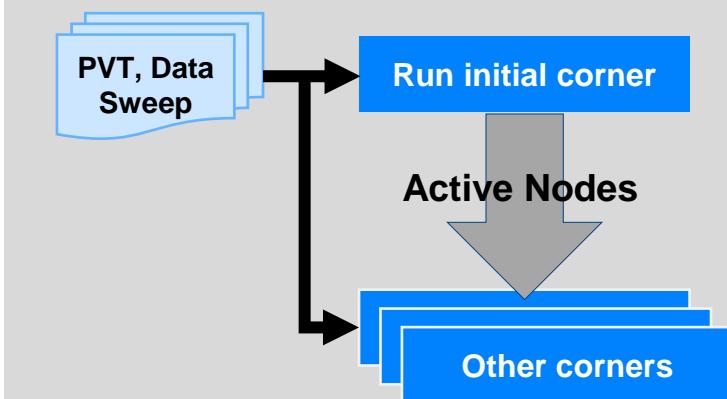
High capacity Monte Carlo PrimeSim XA

- 1M+ transistor capacity
- Block/instance scope control
- Enabled for mixed-signal with VCS
- Outlier visibility with Sigma Scaling



Efficient corner simulation PrimeSim SPICE

- Active-node optimization enables faster corners
- User definable accuracy settings
- Supports parameter and data sweep



Reliability Analysis

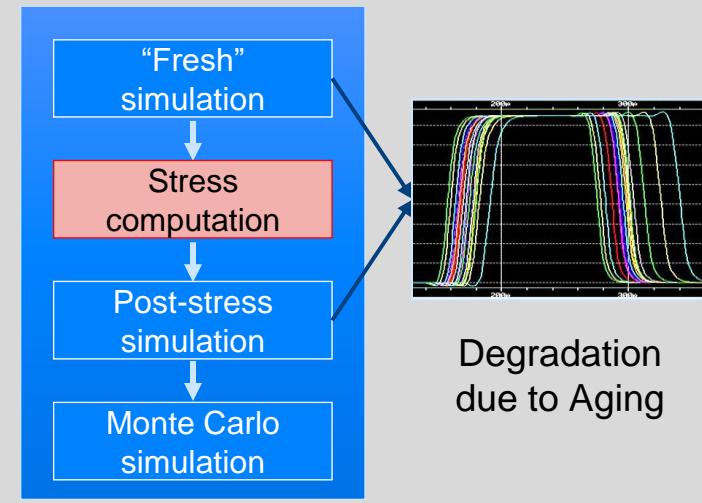
Transistor level EM/IR analysis PrimeSim XA

- Accurate transistor-level analysis
- High performance/capacity
- Optimized StarRC PG extraction
- FinFET certified, self-heating aware



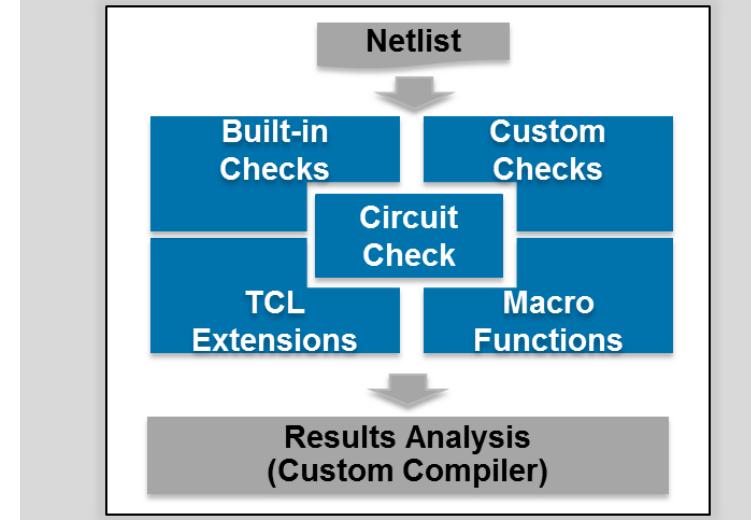
Device aging analysis SPICE, FastSPICE

- Aging simulation with built-in models
- Foundry certified accuracy
- Aging-aware variation analysis
- Certified for Automotive grade flow



Full chip ERC & low power checks

- Comprehensive built-in checks with API for customization
- Find bugs not detectable in simulation
- Full-chip verification in minutes!



How Can Synopsys Help?

Accelerate Robust Custom Design

- >600 R&D engineers
- Leading SPICE, FastSPICE
- Visually-assisted layout
- 1300+ IP designers @ SNPS
- 60+ FinFET Tapeouts

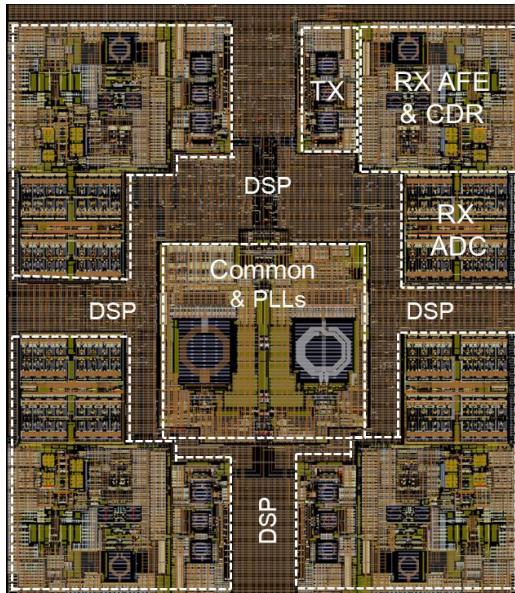


Custom Digital, Standard Library, Memory, Analog, Co-design

Industry-Leading Productivity for Custom Design

Optimized flow used by industry's largest mixed-signal design team

Synopsys DesignWare IP



Analog

Bandgaps,
Regulators

RF

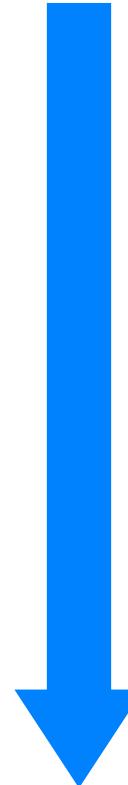
Wide-band
Amplifiers, PLLs

Digital

Serializers,
De-Serializers

Mixed-Signal

High-speed
transmitters



Simulation

PrimeSim

Layout

Custom Compiler

Reliability Analysis

FastSPICE
Reliability Suite

Signoff

StarRC
IC Validator

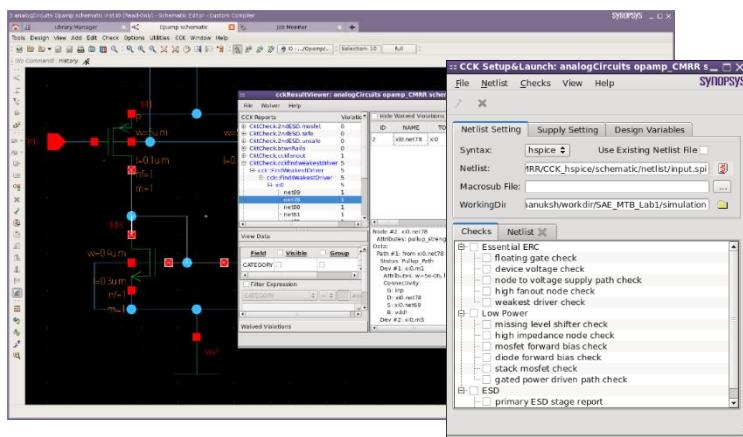
100's of new designs per year

Flow 100% based on Synopsys

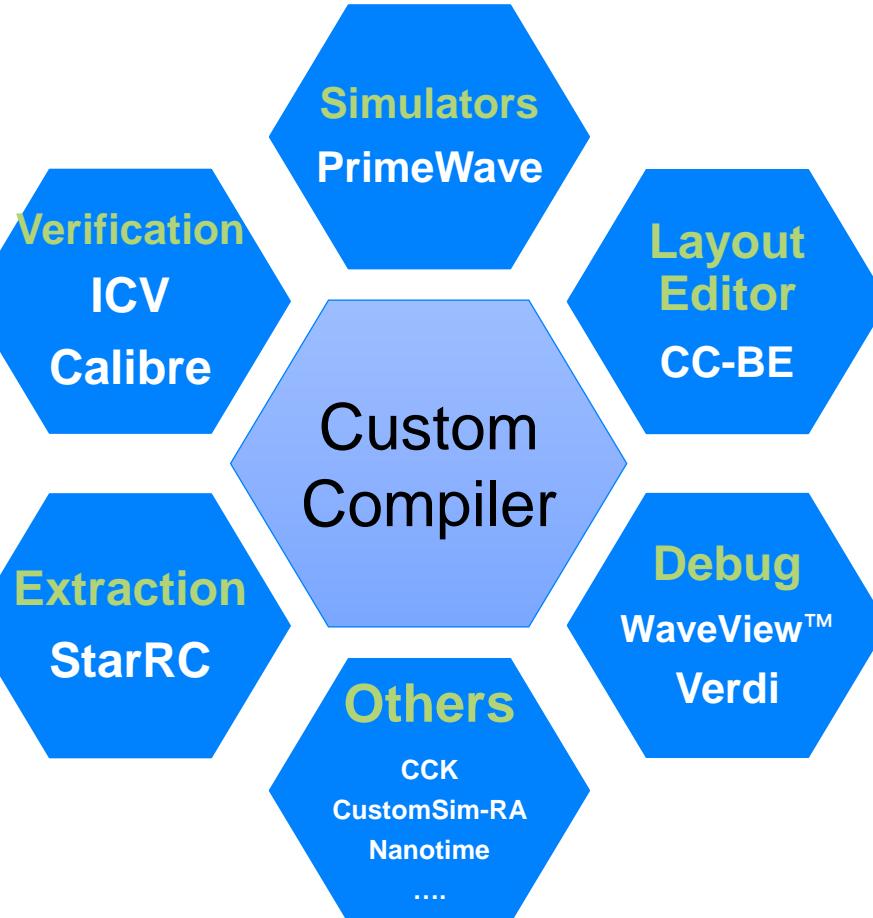
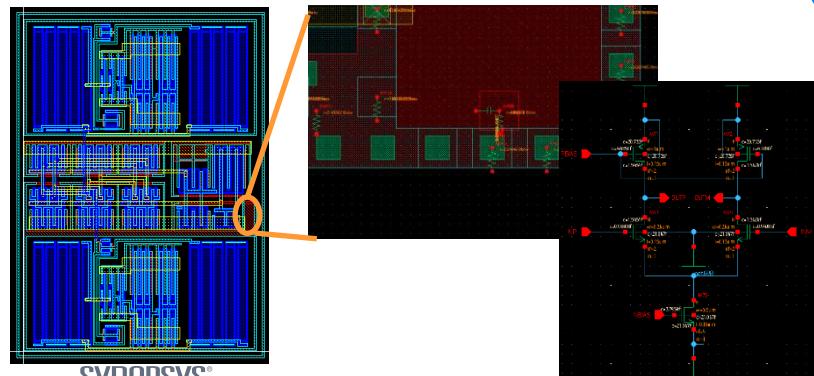
Custom Compiler Front-end Entry (CC-FE)

Platform Integration

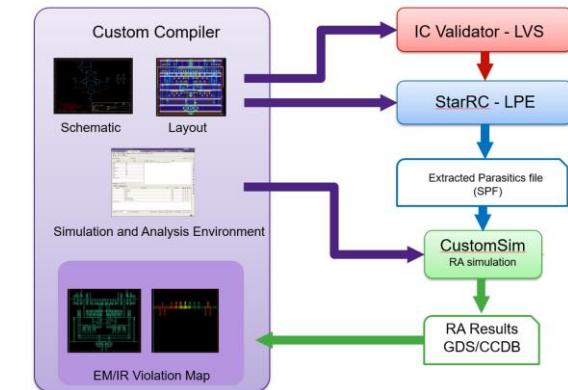
CCK Integration



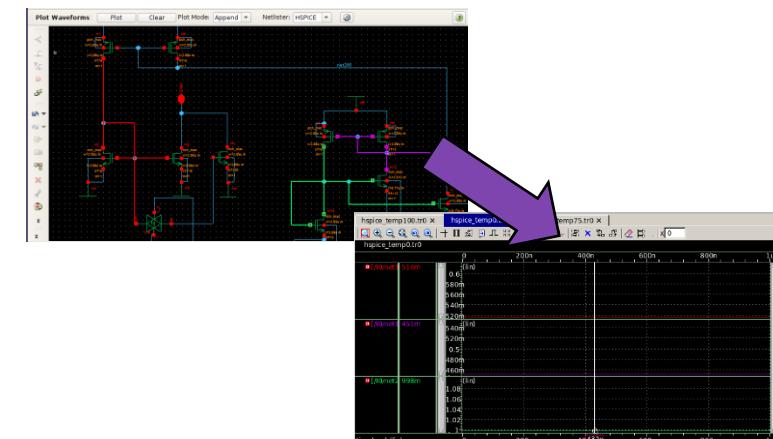
StartRC View Integration



CustomSim RA Integartion



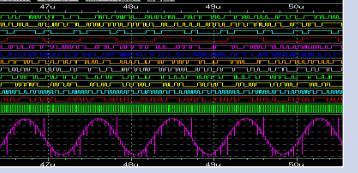
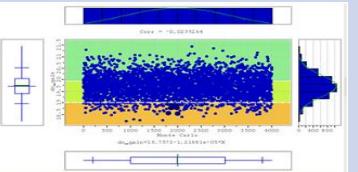
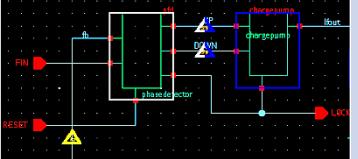
WaveView Integration



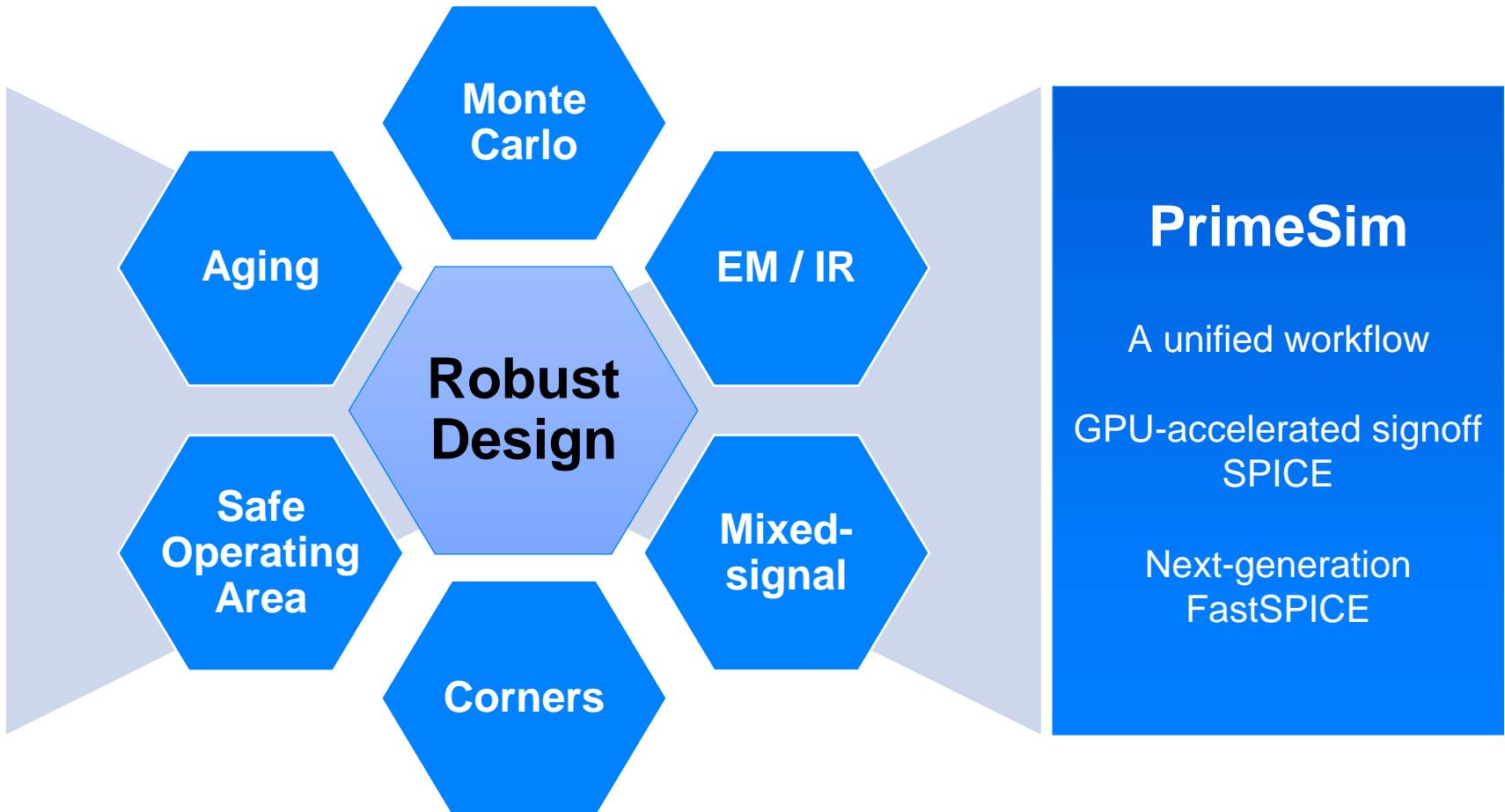
Simulation and Analysis Environment (PrimeWave)

Comprehensive Variability and Reliability Analyses

Custom Compiler



WaveView™



PrimeSim
A unified workflow
GPU-accelerated signoff SPICE
Next-generation FastSPICE

PrimeSim Continuum - Synopsys Circuit Simulation Solution

Common Technologies Across Simulators

GigaScale 

PrimeSim HSPICE
PrimeSim SPICE
(True-SPICE)

PrimeSim XA
PrimeSim Pro
(FastSPICE)

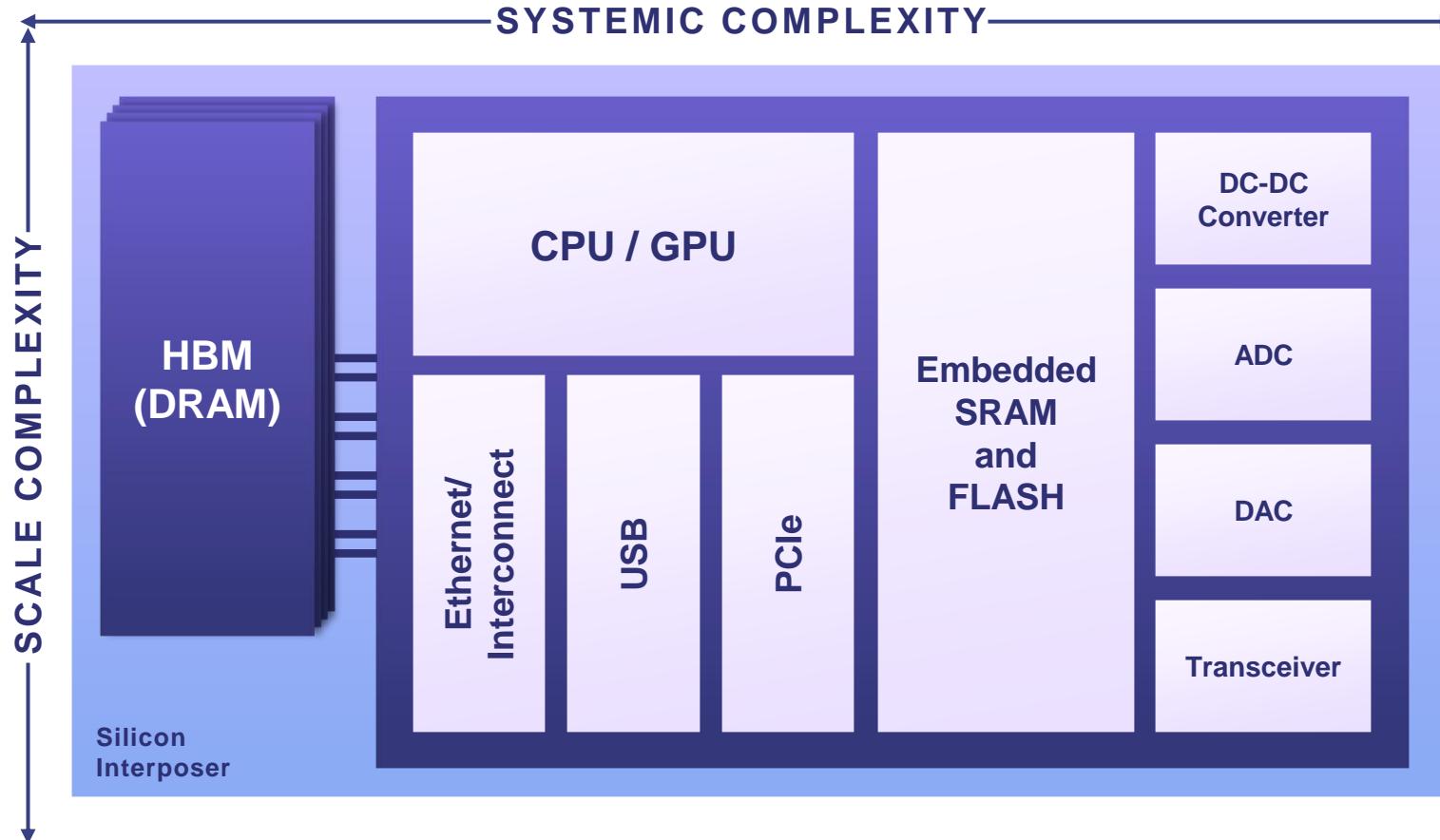
VCS PrimeSim AMS
(Mixed-signal)

Common HSPICE Models, Verilog-A, S-parameter

Common Monte Carlo, Sweep, Aging

Common Reliability Analysis

Hyperconvergence Redefines Circuit Simulation



Systemic Complexity

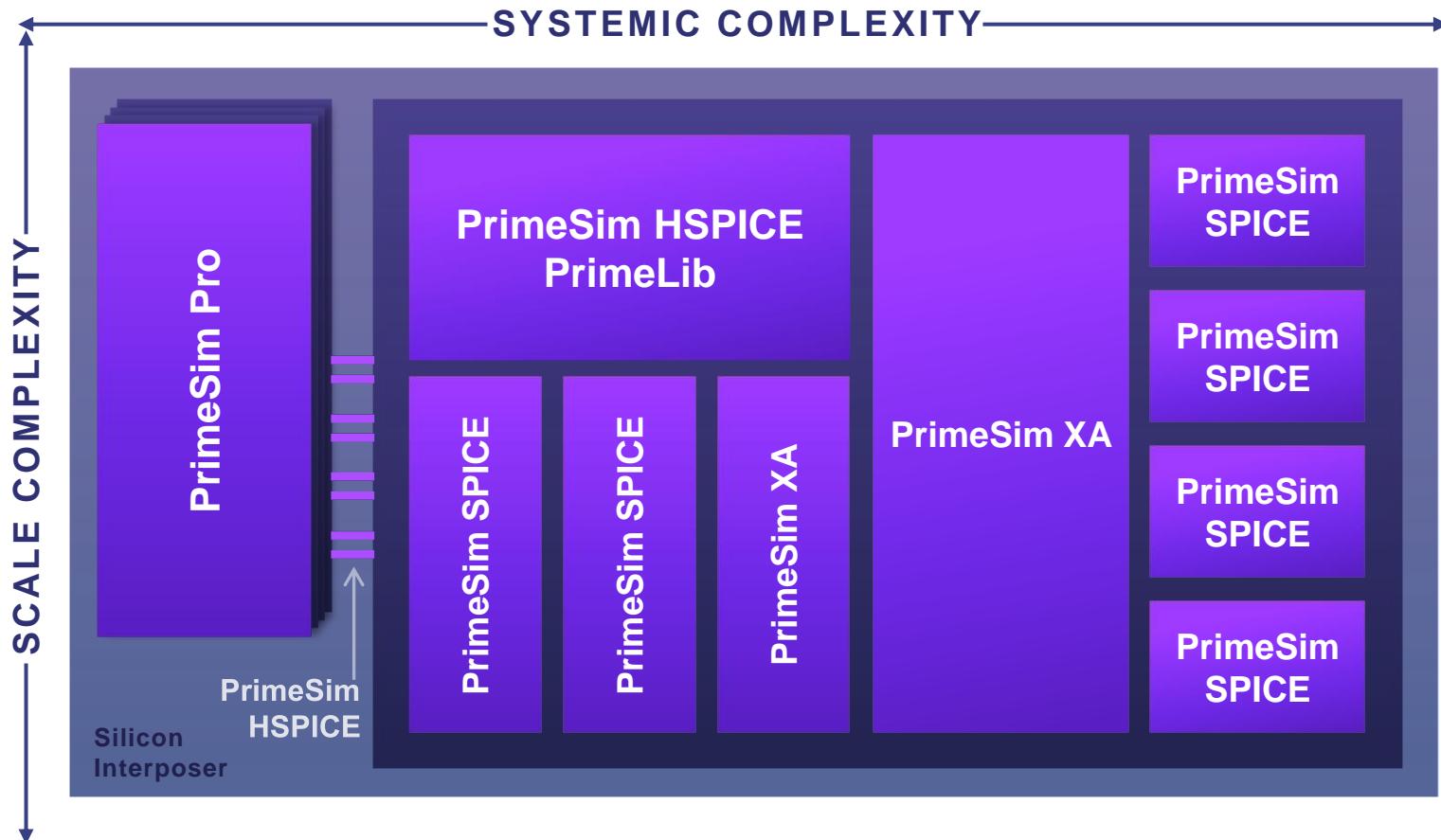
- Hyperconvergence is driving the need for converged workflows around a common circuit simulation solution

Scale Complexity

- Larger and more complex circuits at higher frequencies
- Reduced margins and increased parasitics in advanced nodes
- Need for faster, higher capacity accurate simulators

Introducing PrimeSim Continuum

Addressing Systemic Complexity



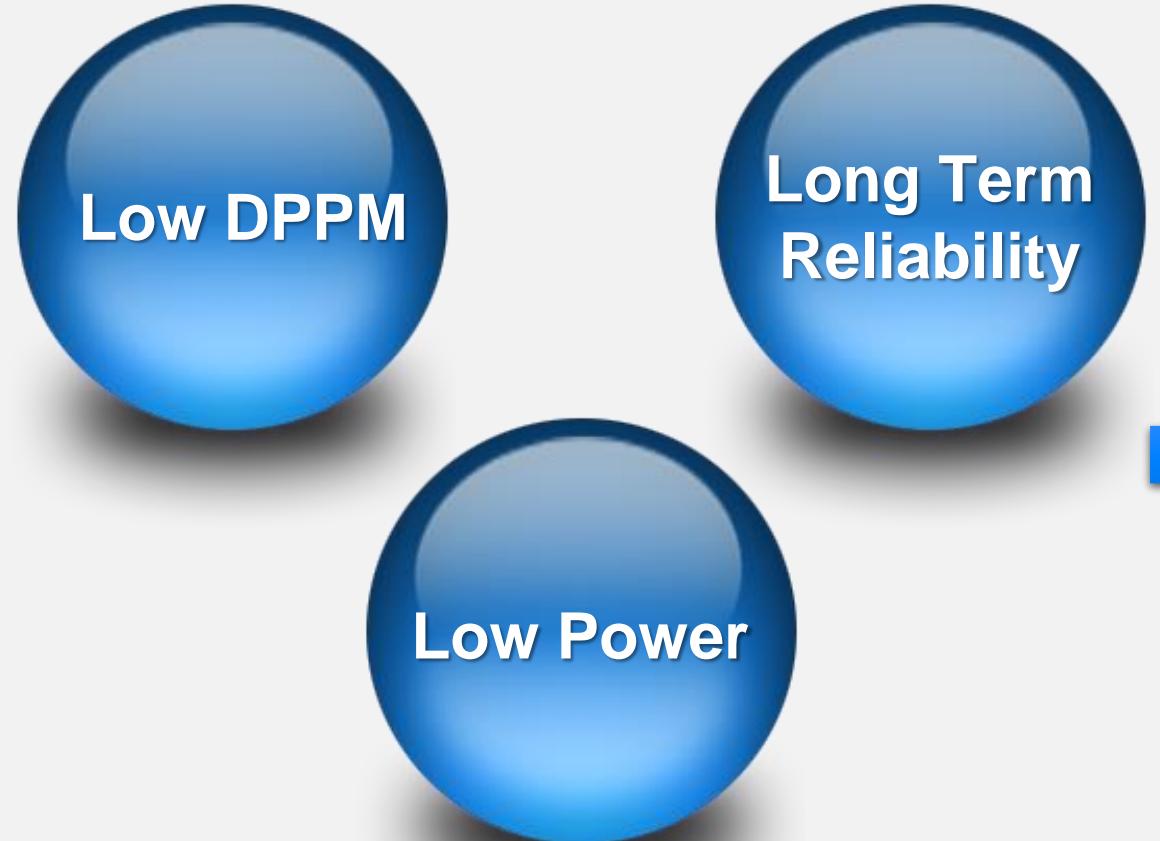
Unified workflow for memory, analog, RF, mixed-signal and custom-digital simulation

Best-in-class Engines

- SPICE and FastSPICE
- Time and Frequency Domain
- Periodic and Transient Noise
- Mixed-signal with VCS
- Unified reliability workflow

Enabling Robust AMS Design

Key Automotive Grade IP Design Requirements



Design Verification Requirements

Verification Method	Synopsys Solution
Corner Analysis	✓
Variation Analysis	✓
Mixed-signal Verification	✓
Aging Analysis	✓
EM / IR Drop Analysis	✓
Circuit ERC Checks	✓

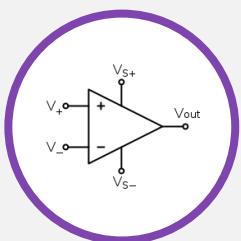
PrimeSim SPICE: Next-Generation SPICE

Addressing Scale Complexity

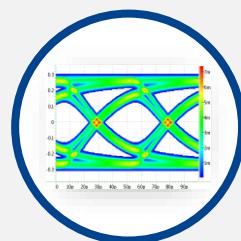
- Superior runtime performance with golden signoff accuracy (3X faster than competition)
- Scalable performance across CPU for time and frequency domain analysis
- 10X faster simulation with heterogenous compute acceleration on CPU and GPU

Comprehensive Analysis

Time domain, frequency domain, noise



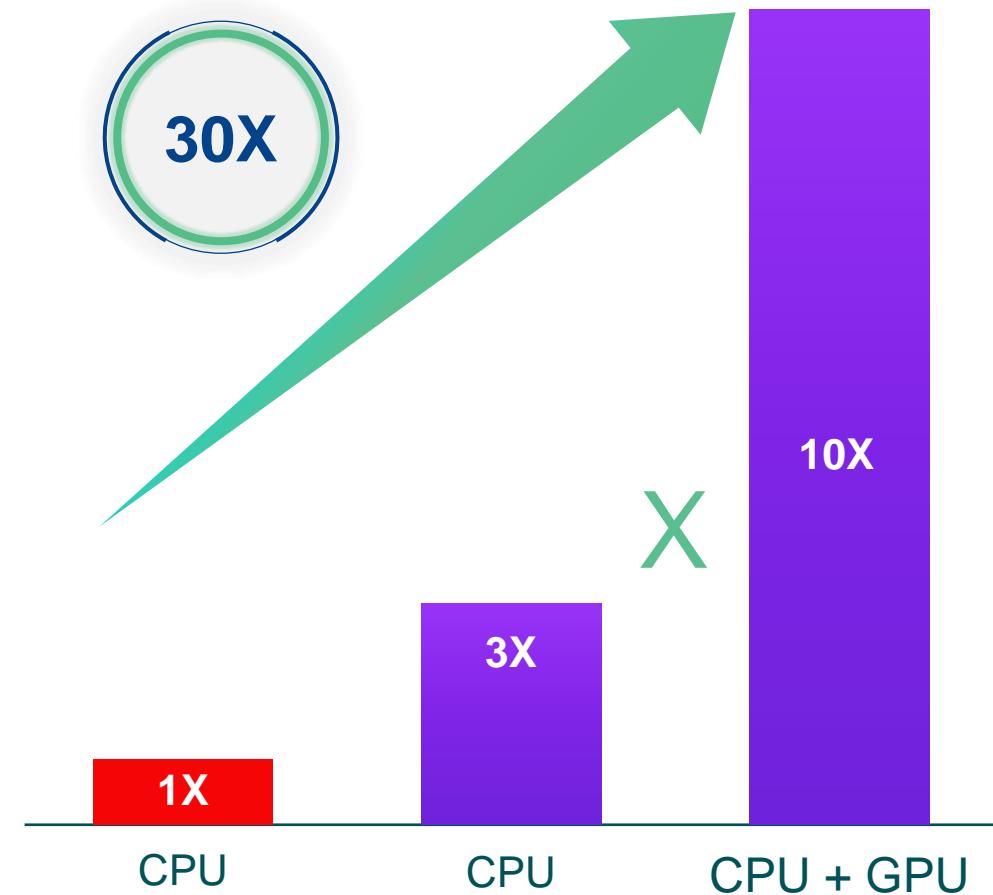
Analog



Signal Integrity

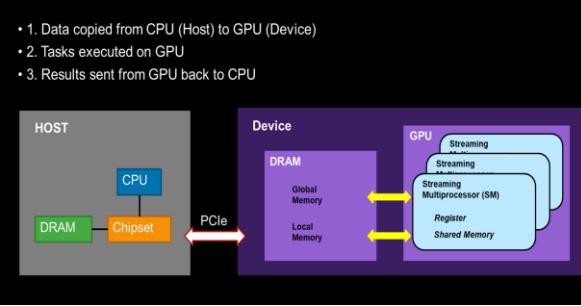


RF



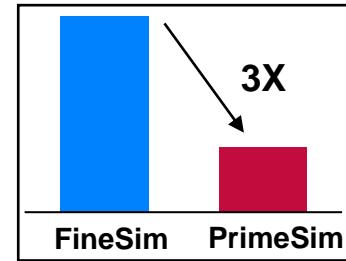
PrimeSim SPICE Key Technologies

GPU Acceleration



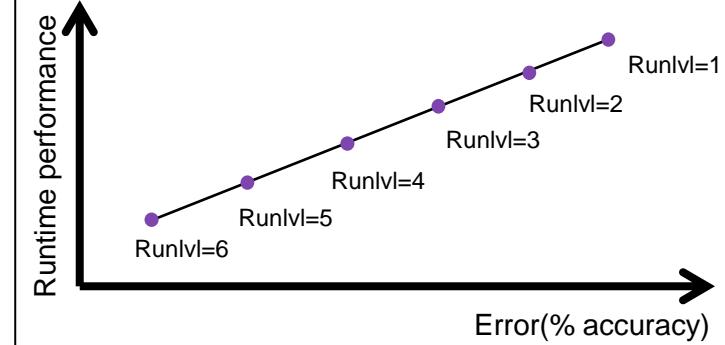
2-5X speedup analog over 8-core CPU

Superior Performance



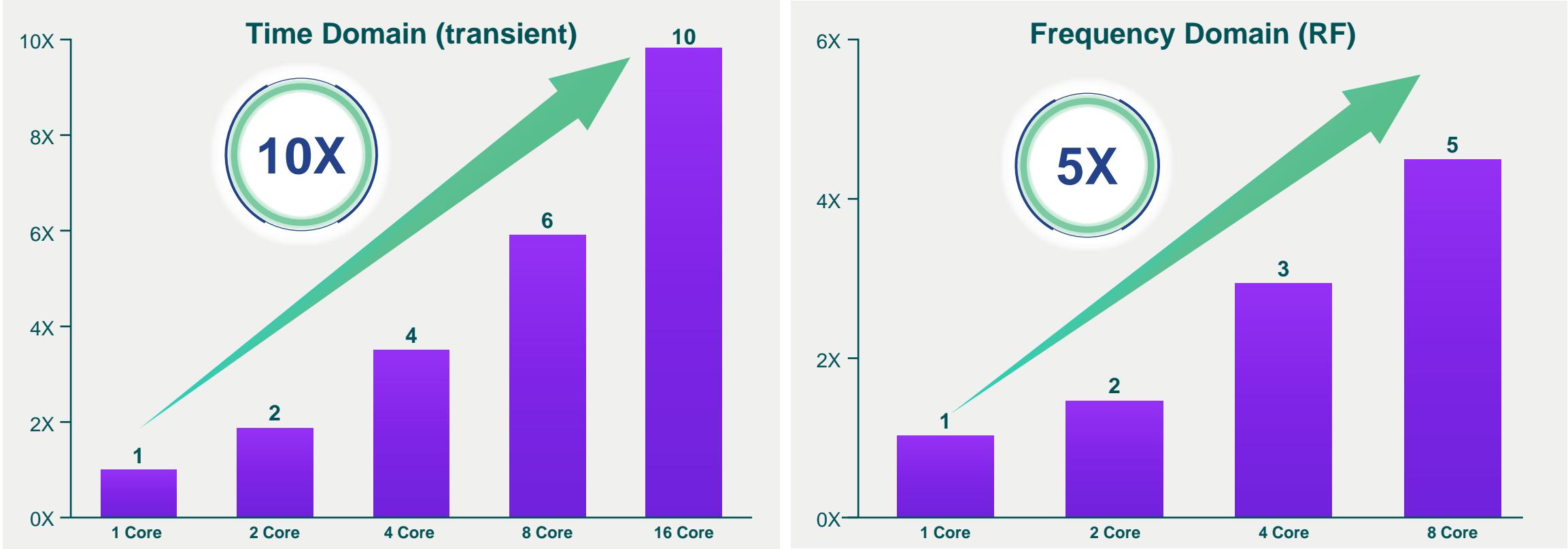
5/3nm: 1.5-3X speedup over 2020.12

Simplified Use Model



EoU based on single control knob

PrimeSim SPICE Scalable Performance Across CPU



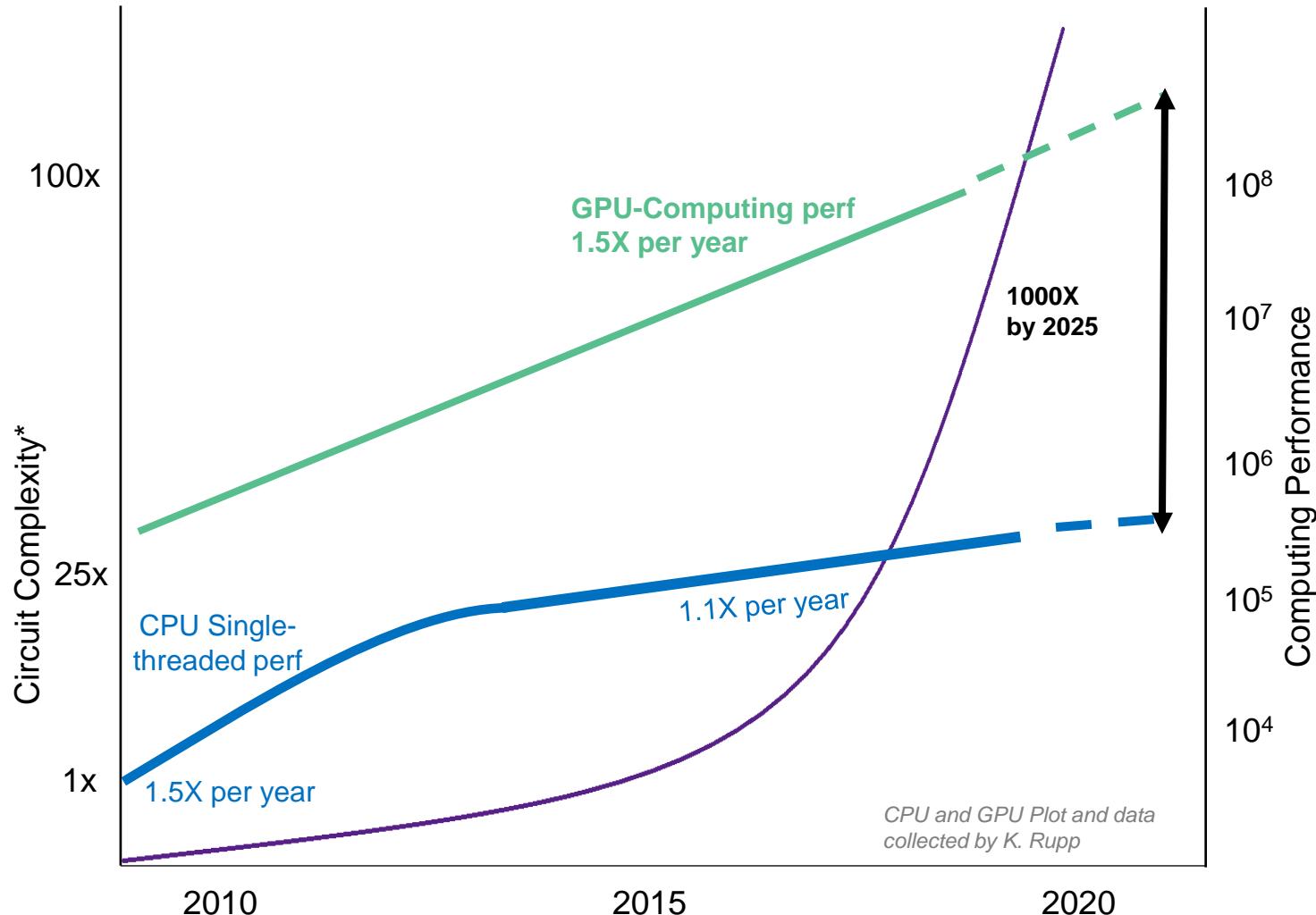
- Scales across multiple cores on the same machines or multiple machines

Heterogenous Compute Acceleration on CPU & GPU

10X faster runtime with golden accuracy for large post-layout designs

Next-Generation Architecture

- CPU-GPU hybrid architecture
- Optimized GPU Matrix Solver
- Device evaluation on the GPU for advanced-node devices
- GPU-friendly data structure to improve bandwidth and latency



PrimeSim GPU Acceleration

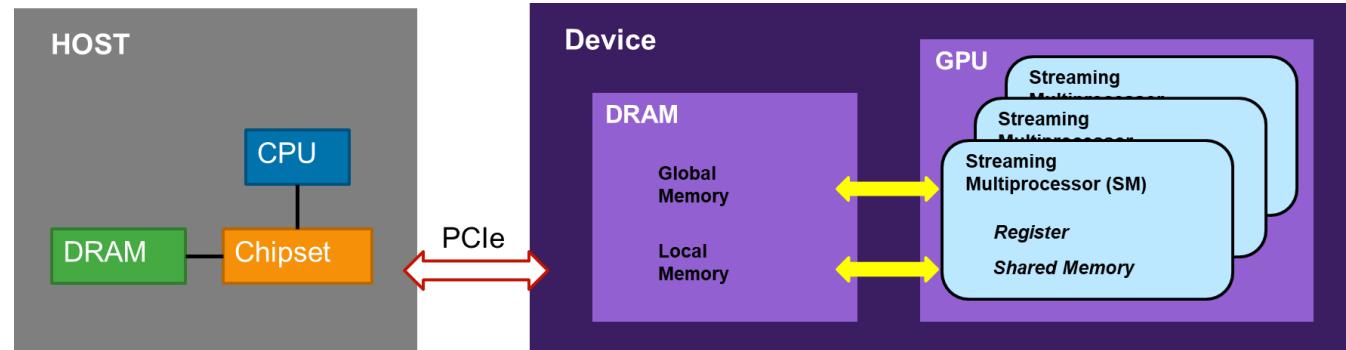
- PrimeSim GPU Technologies

- Advanced direct solver on GPU
- New GPU solutions for connection matrix
- Introduced device evaluation and stamping on GPU
- Optimized GPU flow
 - Improved workload balance
 - Enhanced parallelism

- Multi-GPU boost

- Improved parallelism
- Improved cache/efficiency
- Improved data structure
- Improved load balance

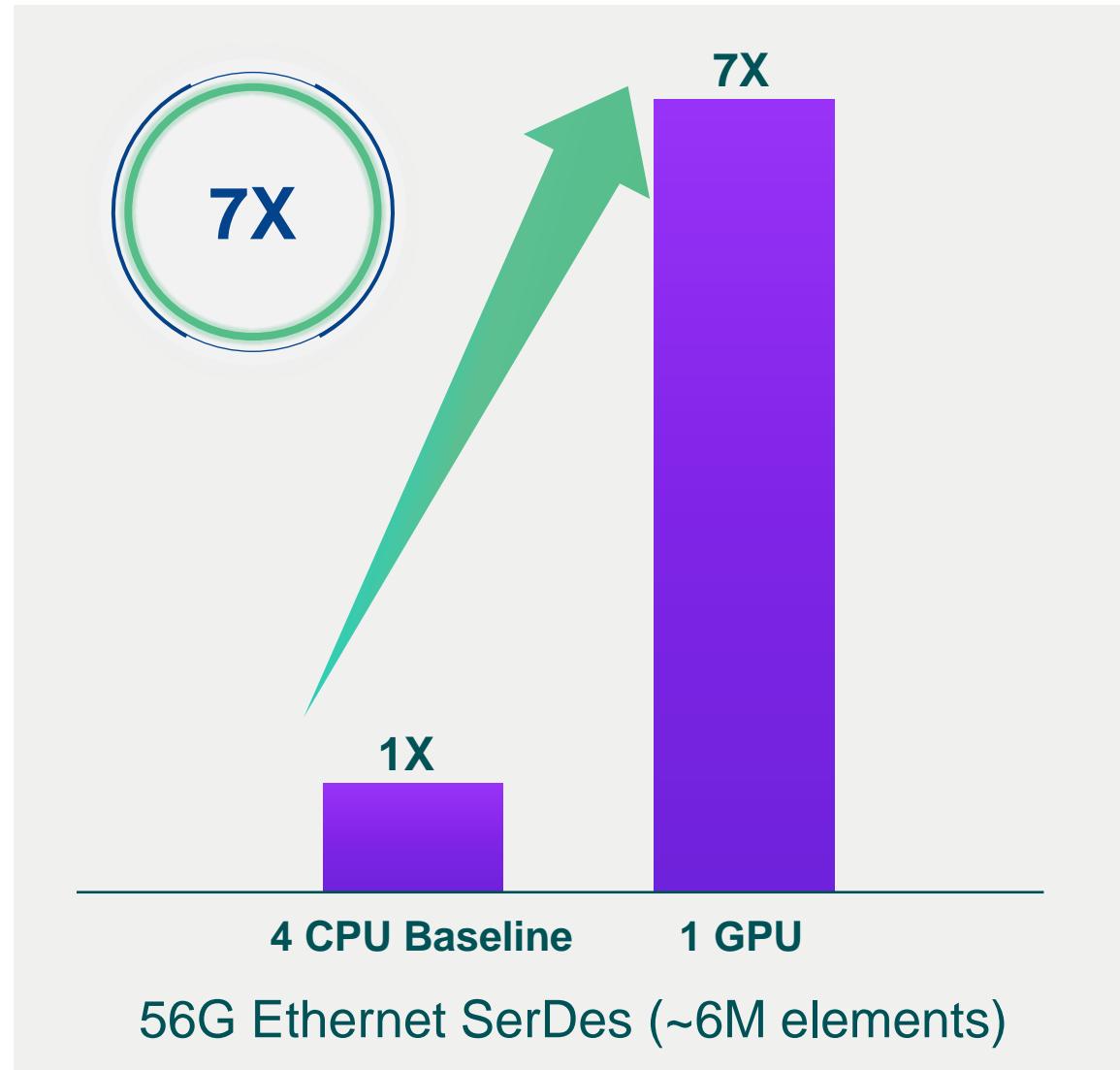
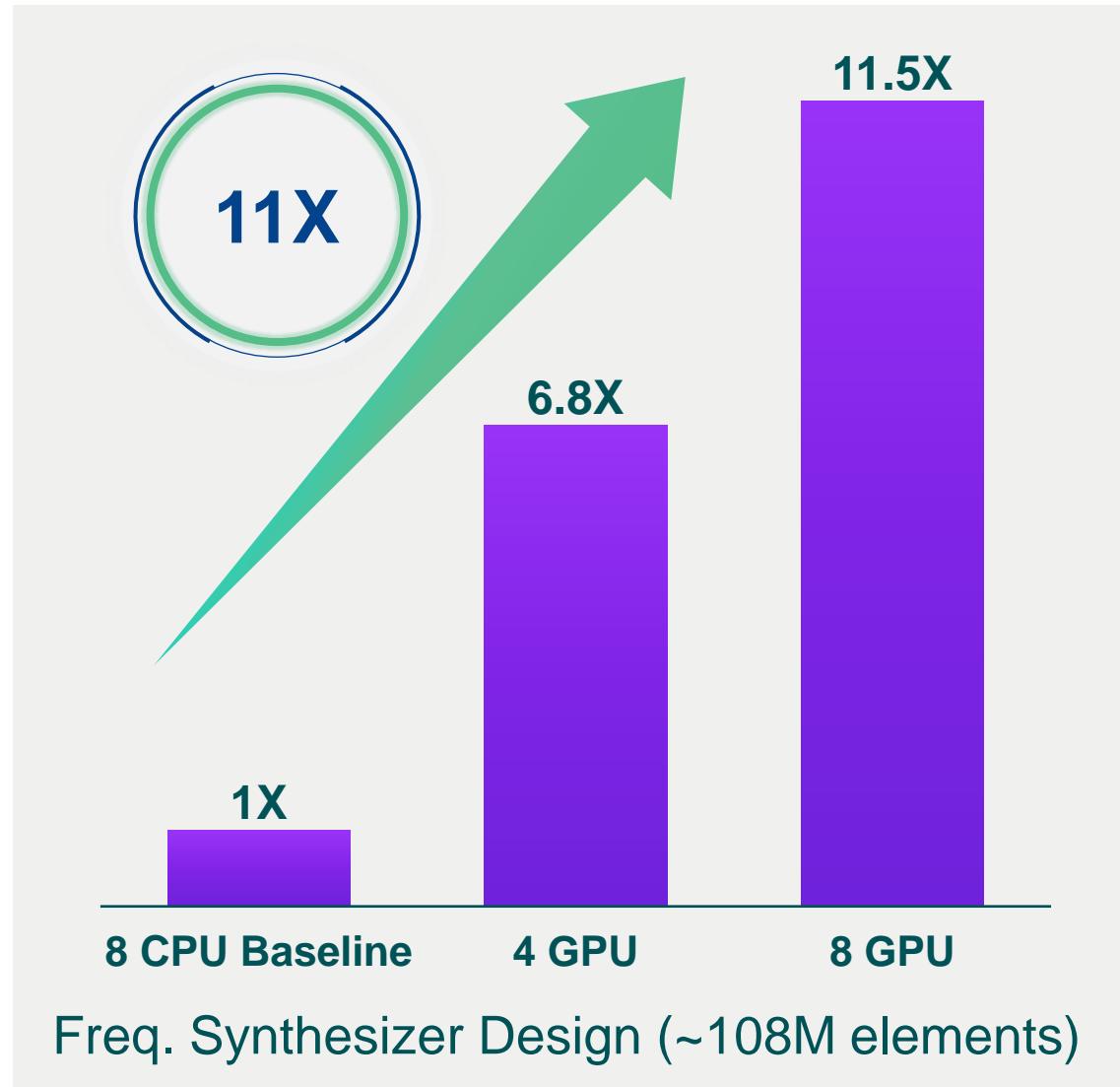
1. Data copied from CPU (Host) to GPU (Device)
2. Tasks executed on GPU
3. Results sent from GPU back to CPU



Circuit nodes	Speedup		
	8 CPU + 1 GPU	8 CPU + 2 GPU	8 CPU + 4 GPU
1.5M	3.03X	4.10X	5.08X
1.4M	2.51X	4.02X	4.71X
650K	2.67X	3.03X	3.23X
160K-600K	1.95 – 2.53X	2 & 4 GPU not needed	

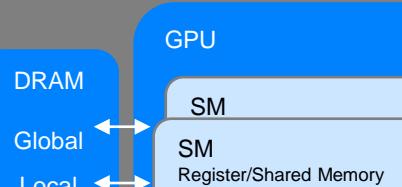
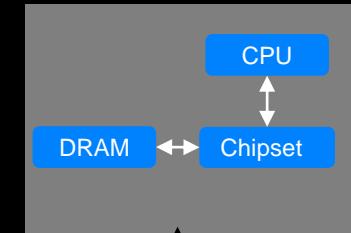
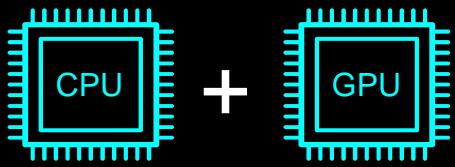
Note: Reference is latest, fast PrimeSim 8 CPU; GPU is NVIDIA V100 32GB

Heterogenous Compute Acceleration on CPU & GPU

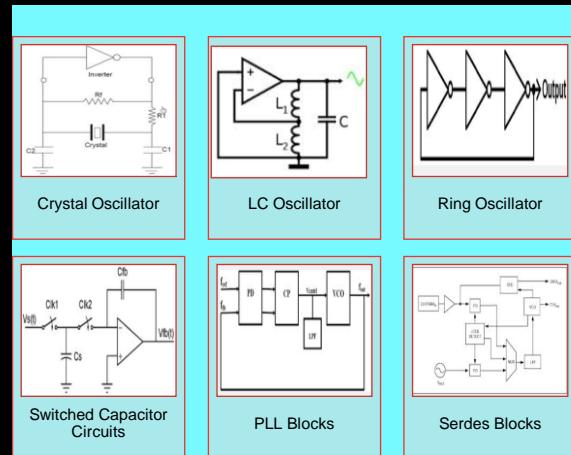
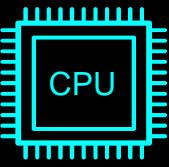


PrimeSim SPICE: Next Generation SPICE Technology

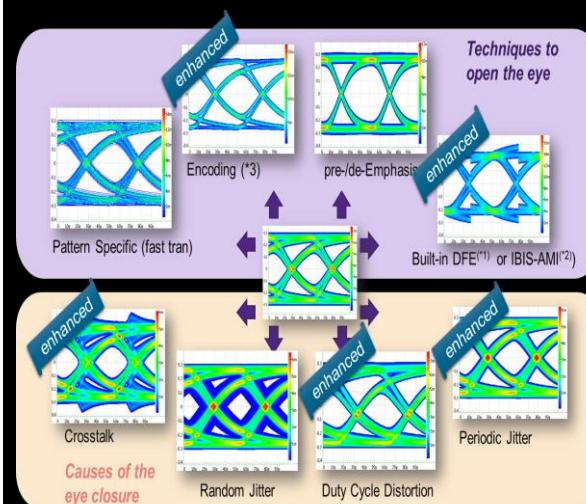
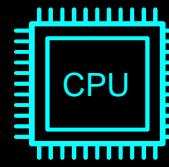
GPU Acceleration



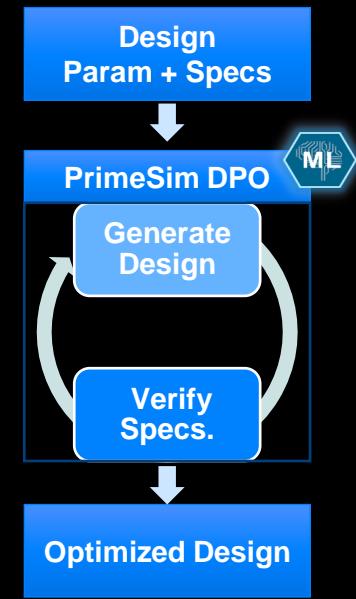
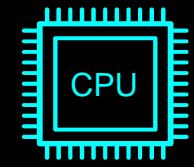
Full Function RF



High Performance SI/PI



ML-based Optimization

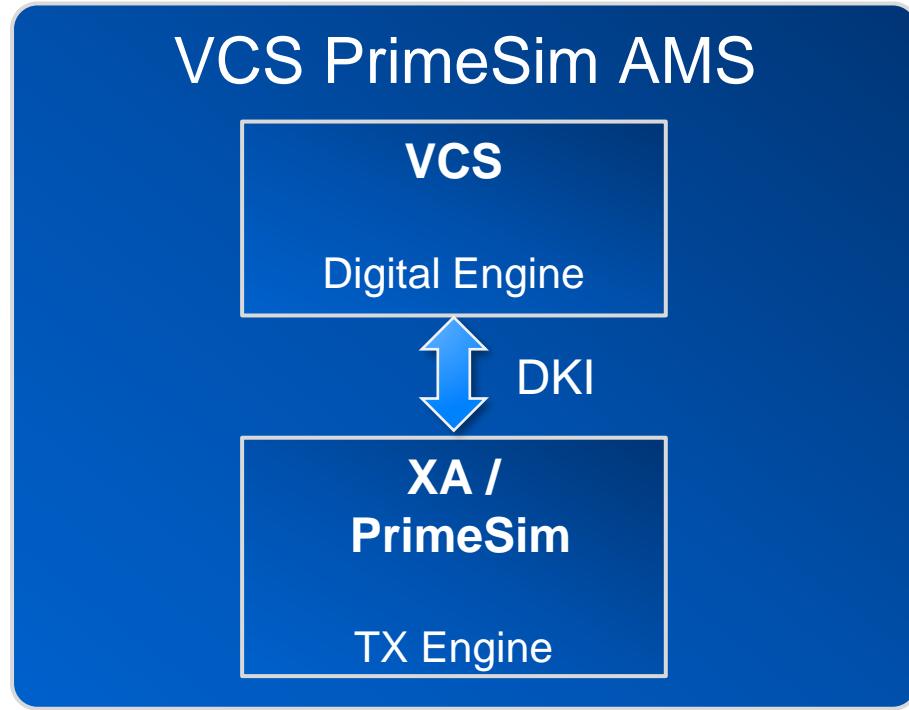


VCS PrimeSim AMS

Digital-Analog Co-Simulation

有些類比的東西用數位做會比較簡單，反之亦然
因此類比與數位終究需要結合

Mixed-signal Solution for Top-Level Simulation



Performance

- Fastest digital / TX-level simulation engines
- Multi-core scalability

Flexibility

- Analog Top, Digital Top, Big-D, Big-A
- Broad language support (SV, V-AMS)

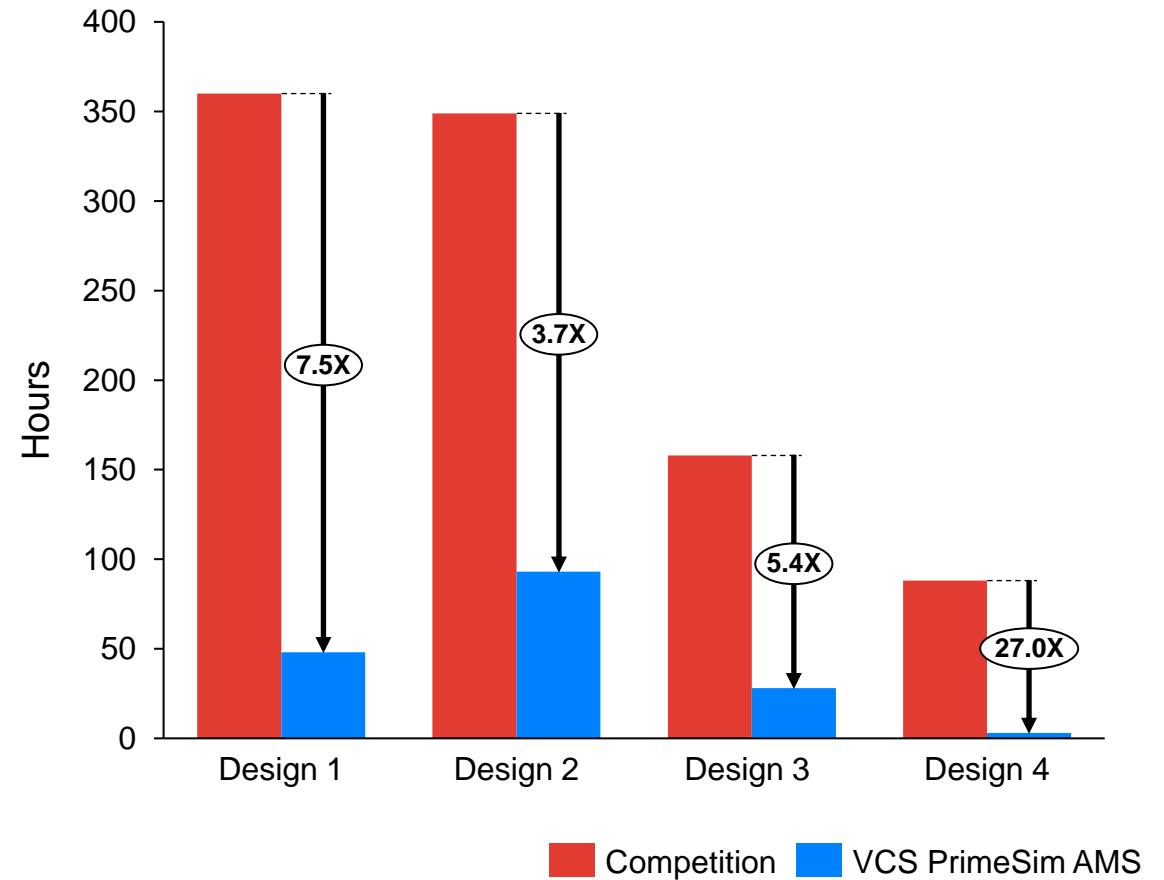
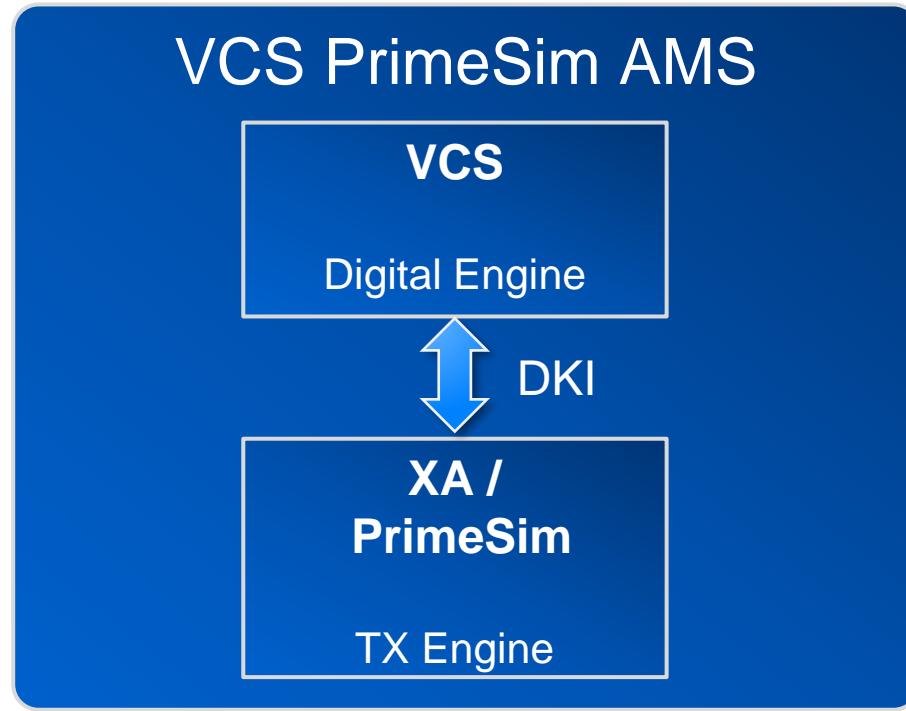
Productivity

- Testbench re-use, UVM in AMS
- Integration with Verdi-AMS for debug

Advanced Analyses

- UPF in AMS
- Monte Carlo in Co-sim, ERC

Fastest Mixed-signal Simulation Performance

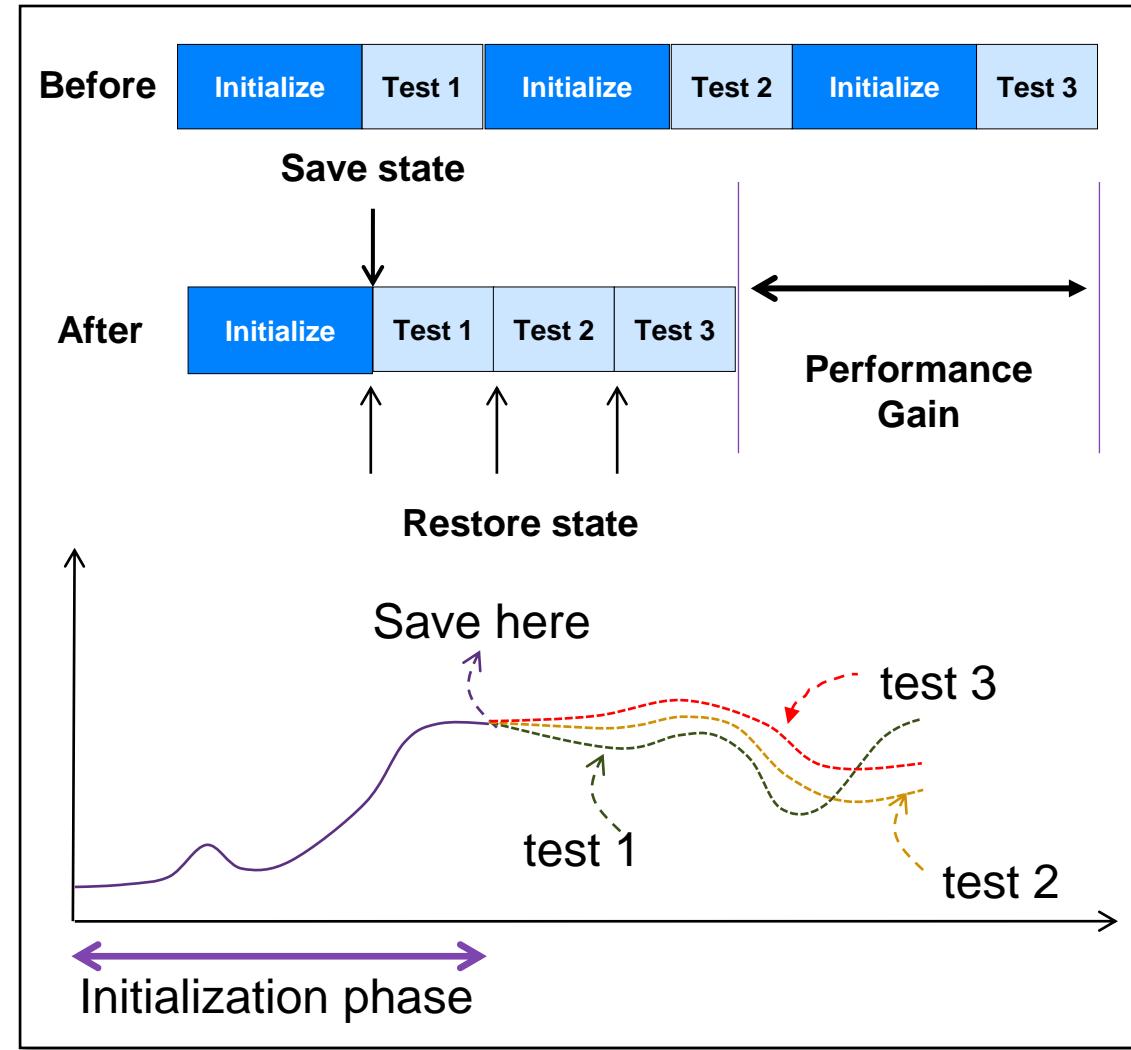


Source : DC-DC converter benchmarks from Synopsys customer

Improving Co-Simulation Throughput with Save and Restore

- Image-based Save and Restore
 1. Run through initialization
 2. Save simulation image
 3. Change vectors / tests
 4. Restore and resume
- Intelligently run post-restore tests
 - Manual or automated
- Delivers significant throughput improvement

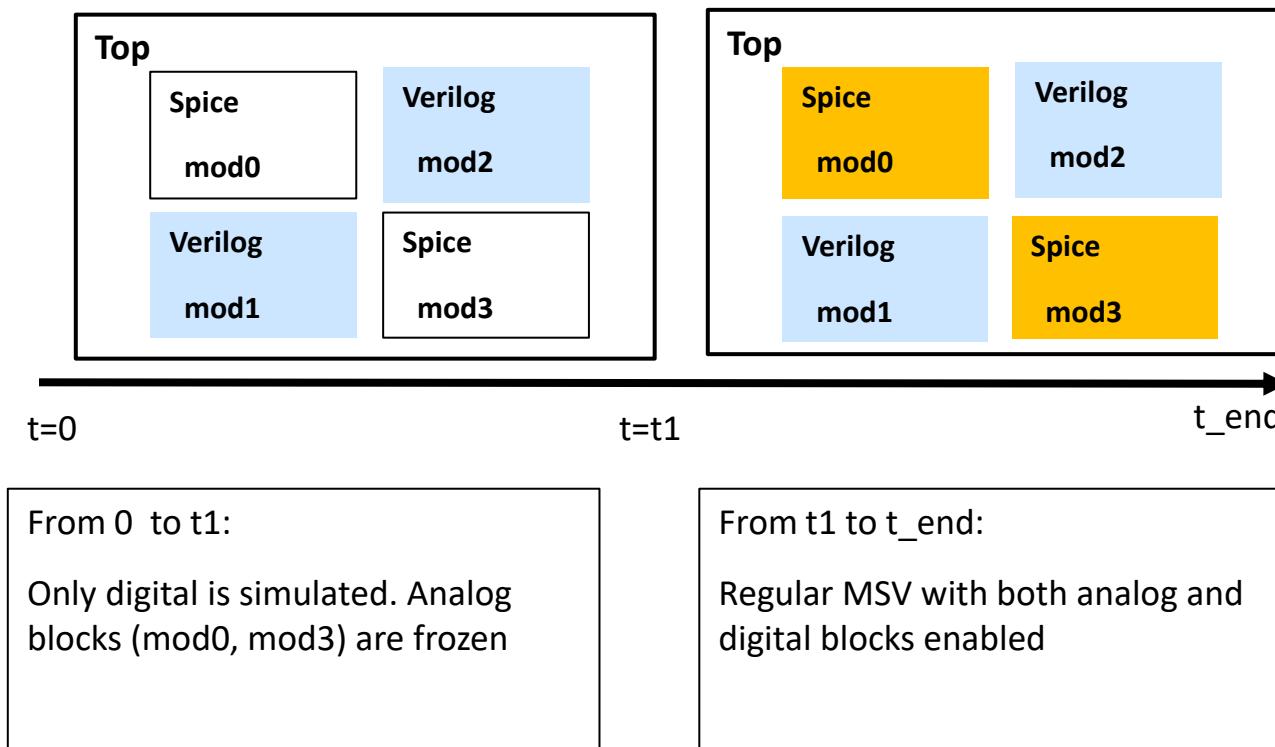
initialization phase其實相對來說也很花時間，因為每次模擬都會經過這段過程，如果可以把這段過程儲存起來給後續的模擬使用便可大幅節省時間



Skipping Analog Simulation during Digital Initialization

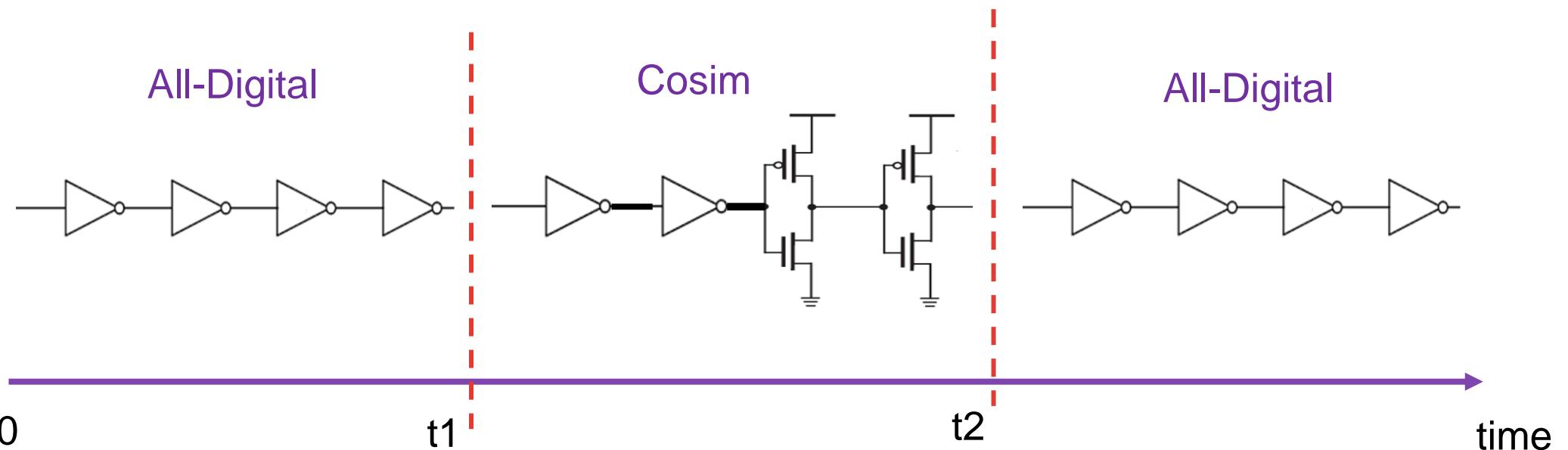
- The goal is to improve the performance of mixed-signal simulation by skipping the simulation of analog when analog results are not needed
- One application would be during the digital initialization when the analog simulation results are “don’t care”

假如現在只需要數位的部分，便可以先把執行類比部分的block先freeze，達到加速的效果

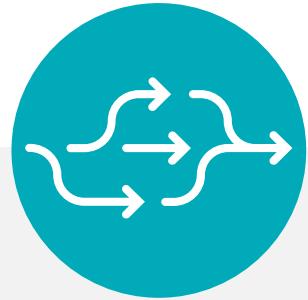


Real Time View Swapping (RTVS)

- The idea of RTVS is to allow dynamically switching of the views between analog and digital views in one simulation
- This allows for parts of the simulation run in all-digital (for performance), and only the accuracy-sensitive periods of the simulation to be simulated in cosim (for accuracy)



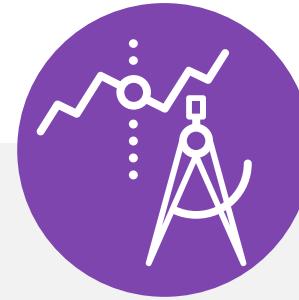
PrimeSim Continuum



A unified workflow
of best-in-class
circuit simulation
technologies



World's fastest
GPU-accelerated
signoff SPICE
10X Faster



Next-generation
FastSPICE
architecture
5X Faster

Circuit Simulation Adopted by Market Leaders

#1 CPU, GPU, Flash, DRAM, Fabless, Foundry

Industry's Favorite



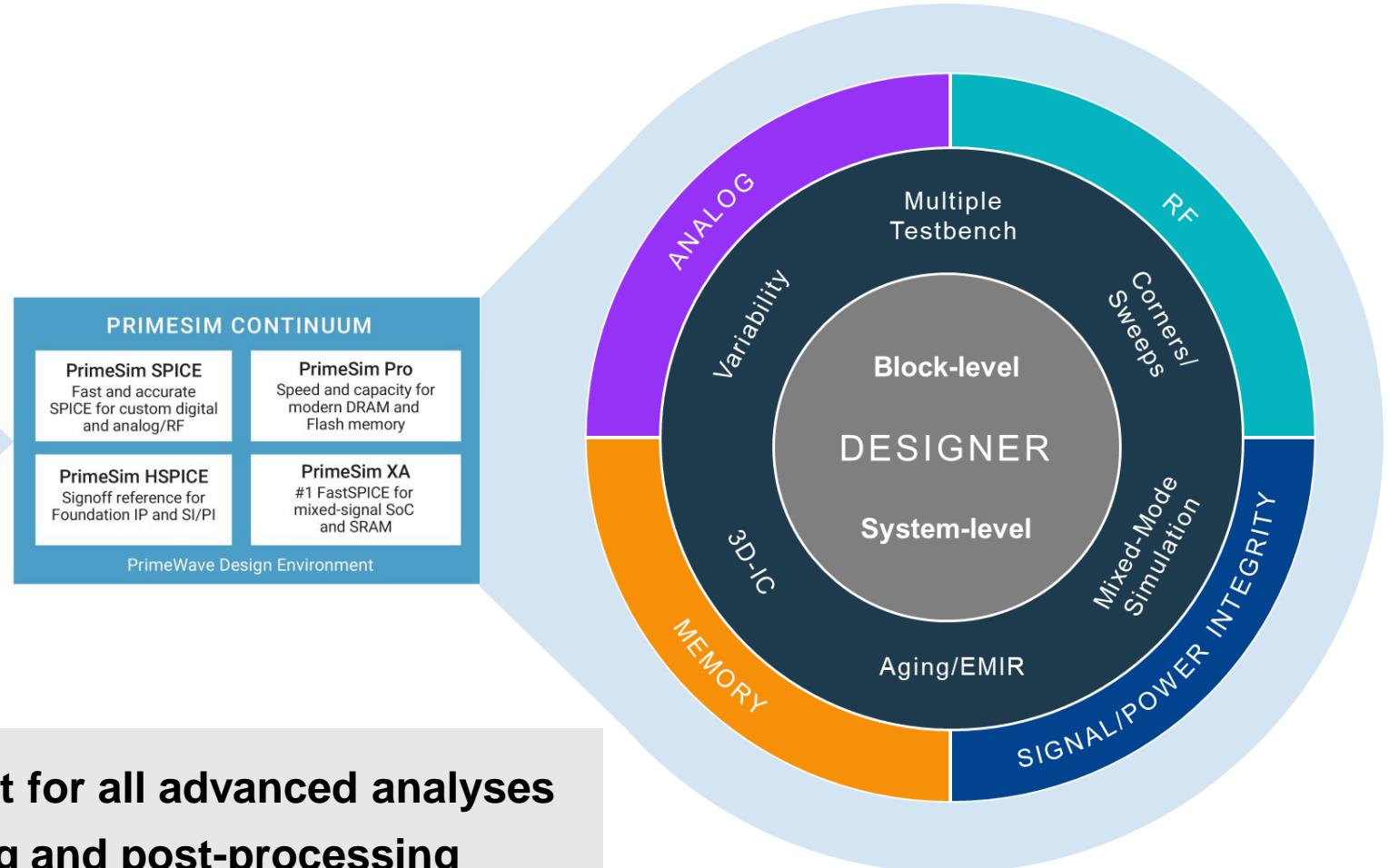
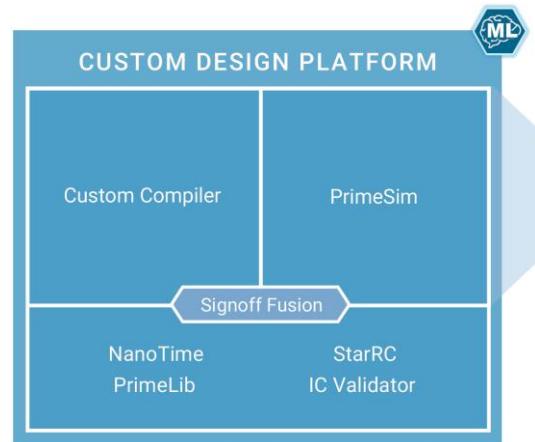
FinFET Leadership



PrimeWave Design Environment

Simulation & Analysis Environment

PrimeWave – Next Generation Simulation Environment

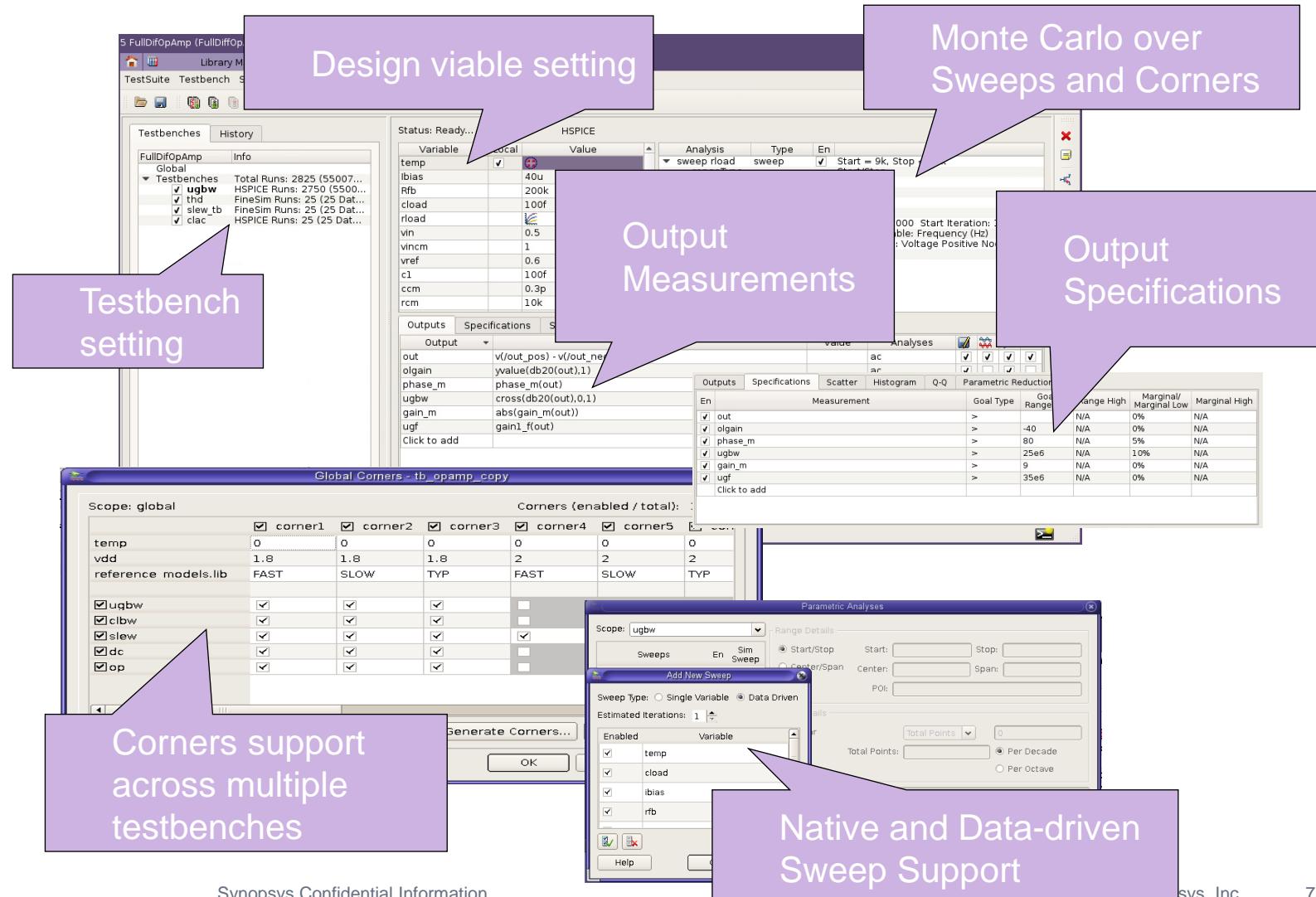


- Comprehensive environment for all advanced analyses
- Integrated Waveform viewing and post-processing
- Flexible and programmable environment

Streamlined Simulation Setup using PrimeWave

Comprehensive Verification using Sweeps and Corners with Monte Carlo

- Circuit Design requires verification of **large number of PVT Corners, Sweeps, and Monte Carlo iterations**
- PrimeWave enables **streamlined setup across multiple testbenches**
- **Global/Local Corners and Sweeps Support**

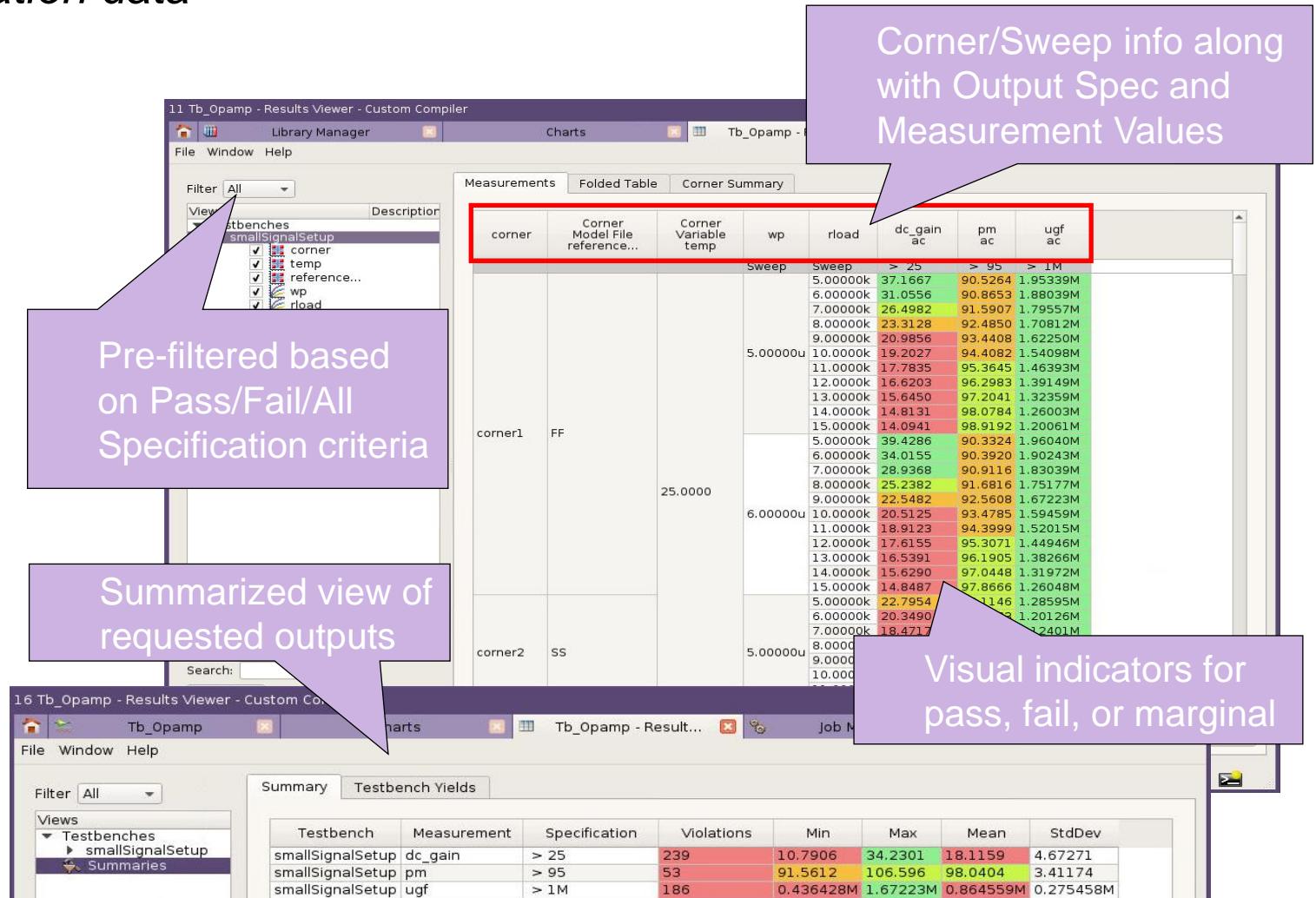


Results Viewer

Analyze extensive amount of simulation data

- **Voluminous data to handle** from Corners, Parametric Sweeps, and Monte Carlo runs
- Results Viewer **enables fast browsing of outputs**
 - Summarized list of outputs across all testbenches
 - Visual indicators for measurements
 - Dynamic filtering to help focus on important regions

方便的使用者介面可以幫助快速分析各種testbench的結果



Identify and Analyze Trouble Areas Against Specs

Review distributions, and view other statistical data

可以在圖表中直接將表現最差的case框選起來，然後便可以得到當時的測試環境等等詳細資料

The screenshot displays three main windows from the Synopsys Custom Compiler:

- 14 Charts - Custom Compiler**: A scatter plot showing failure points (red) against various parameters like rload, reference40, wp, temp, and ugf. A red box highlights a cluster of failure points. A callout box says "Select failure points". Below the plot is a correlation matrix table.
- Variables Table**: Shows variable values for rload, reference40, wp, temp, and # Selected (36). A callout box says "Corner/sweep conditions associated with failures".
- 11 Tb_Opamp - Results Viewer - Custom Compiler**: A detailed table of corner sweep results for various parameters across different testbench configurations. Callouts say "Cross-probe failure points from Charts to Results Viewer for detailed investigation" and "Scatter Charts with correlation coefficients".

Correlation Matrix Table (from 14 Charts window):

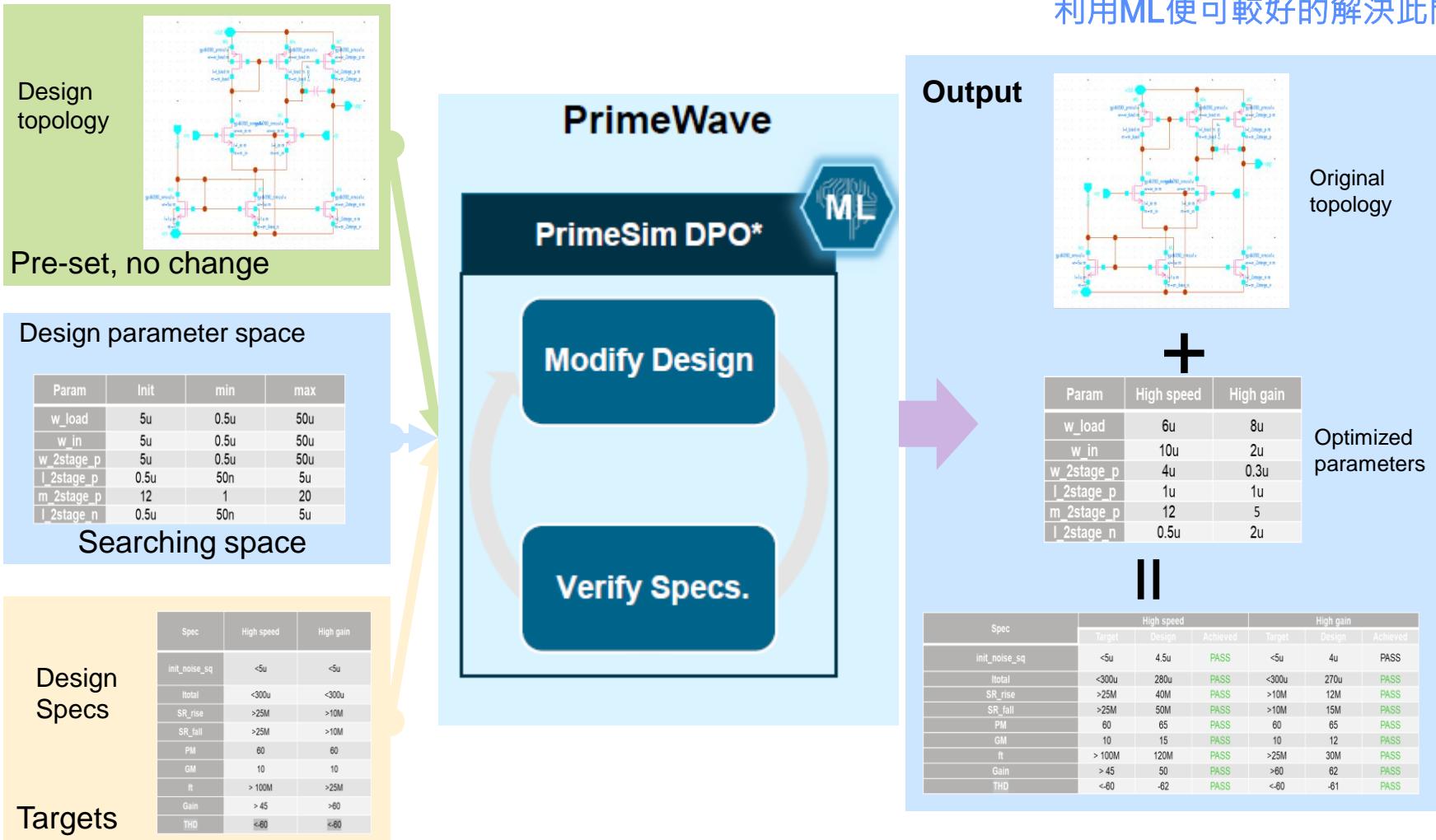
Parameter - 1	Parameter - 2	Corr. Coef	Abs. Corr. Coef
dc_gain	pm	-0.741481	0.741481
reference40_models.lib_(2)	pm	0.292603	0.292603
rload	pm	0.644733	0.644733
temp	pm	-0.0444842	0.0444842
ugf	pm	-0.498368	0.498368
wp	pm	-0.100607	0.100607
dc_gain	ugf	0.0473179	0.0473179

Scatter Charts with correlation coefficients (from 14 Charts window):

Scatter chart showing a negative correlation between dc_gain and another parameter. The correlation coefficient is displayed as -0.741481.

Design Parameter Optimization

ML-based Design Centering and Optimization



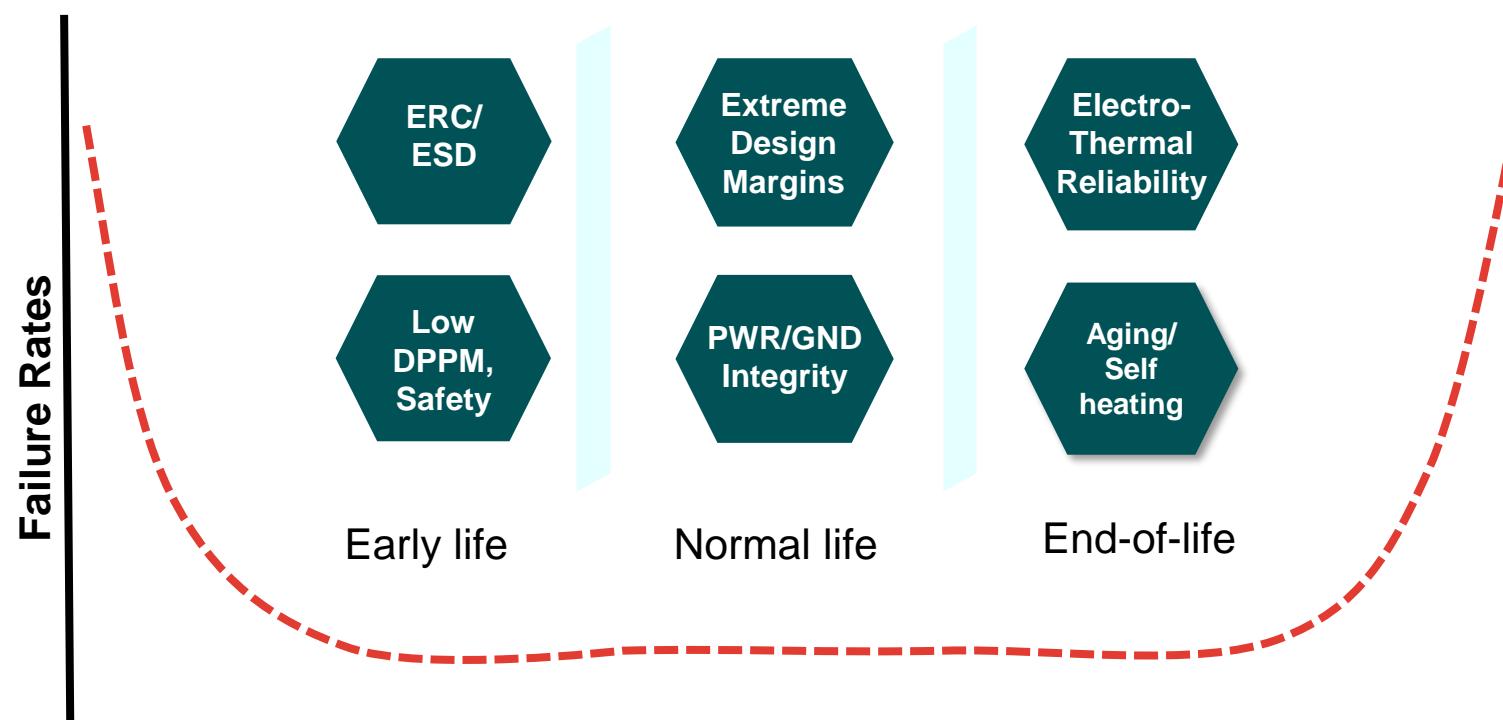
做類比電路時，有些參數以往都需要使用try & error的方式去調校出較好的參數，但是 testcase 數量變多時便會耗時耗力
利用ML便可較好的解決此問題

- Auto-determine optimal design parameters according to specs.
- Free designer from tedious parameter optimizations.
- Overnight auto-optimization to speed up design flow.

PrimeSim Reliability Analysis

Fully Integrated with PrimeWave Reliability Environment

Semiconductor Reliability & Analysis Needs



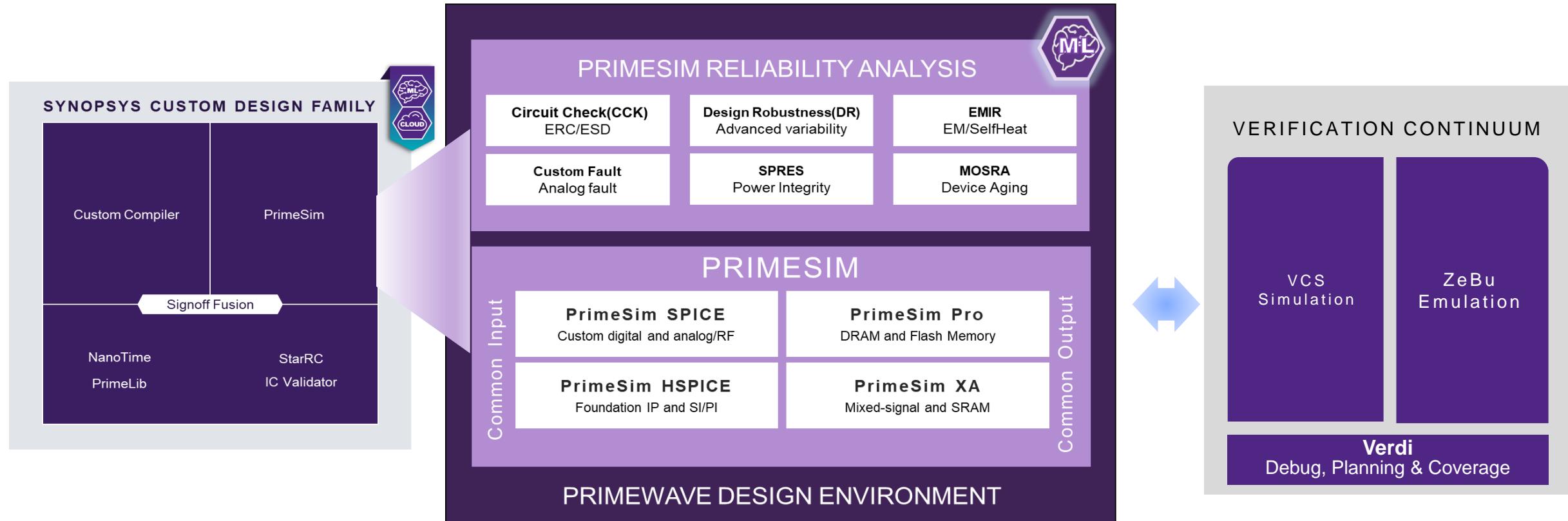
在20nm以下的channel effect非常明顯，會大幅影響電路可靠度

Product Lifetime

EDA Requirements

- Converged workflows around proven solutions
- Comprehensive reliability analysis spanning the full product lifecycle
- Application specific reliability targets
- High performance & QoR with standards compliance
- Ease of setup and analyses

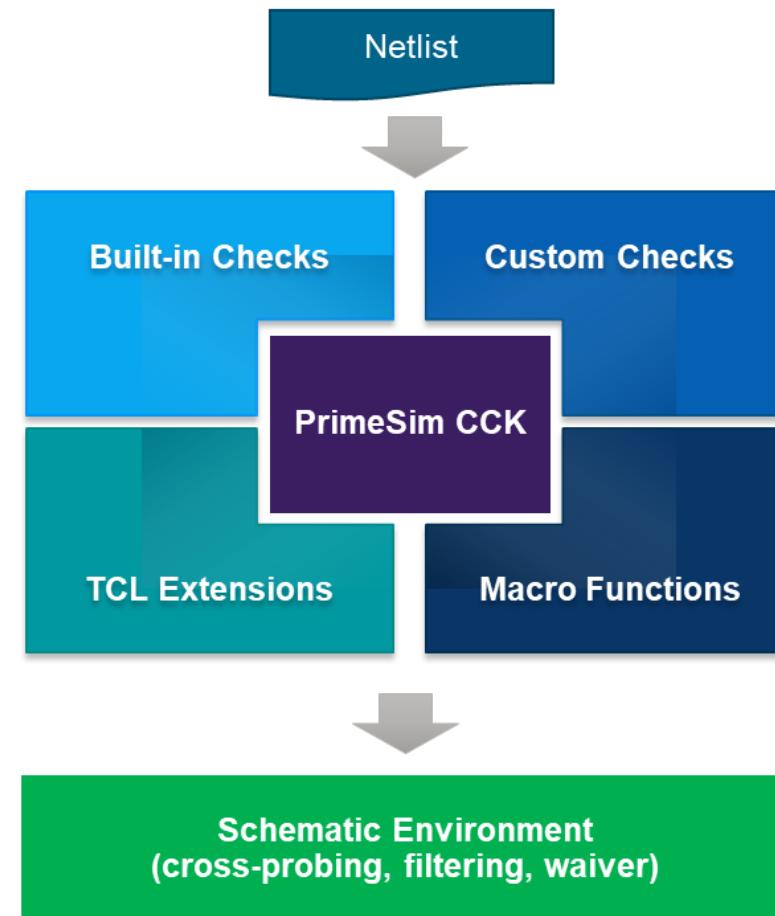
Integral Part of the Custom Design Family



- Integrated with **Custom Compiler** for accelerating analog design
- Integrated with **StarRC** to optimize extraction for reliability analysis
- Integrated with **VCS** for mixed-signal verification
- Integrated with **PrimeLib** for foundation IP characterization

- PrimeSim CCK has flexible and customizable Electrical rule checks is necessary to catch design issues early
- Comprehensive ERC with
 - Customizable checks
 - User defined topology identification
 - Advanced filters/waivers
- Integrated in PrimeWave Design Environment for easier setup and debugging

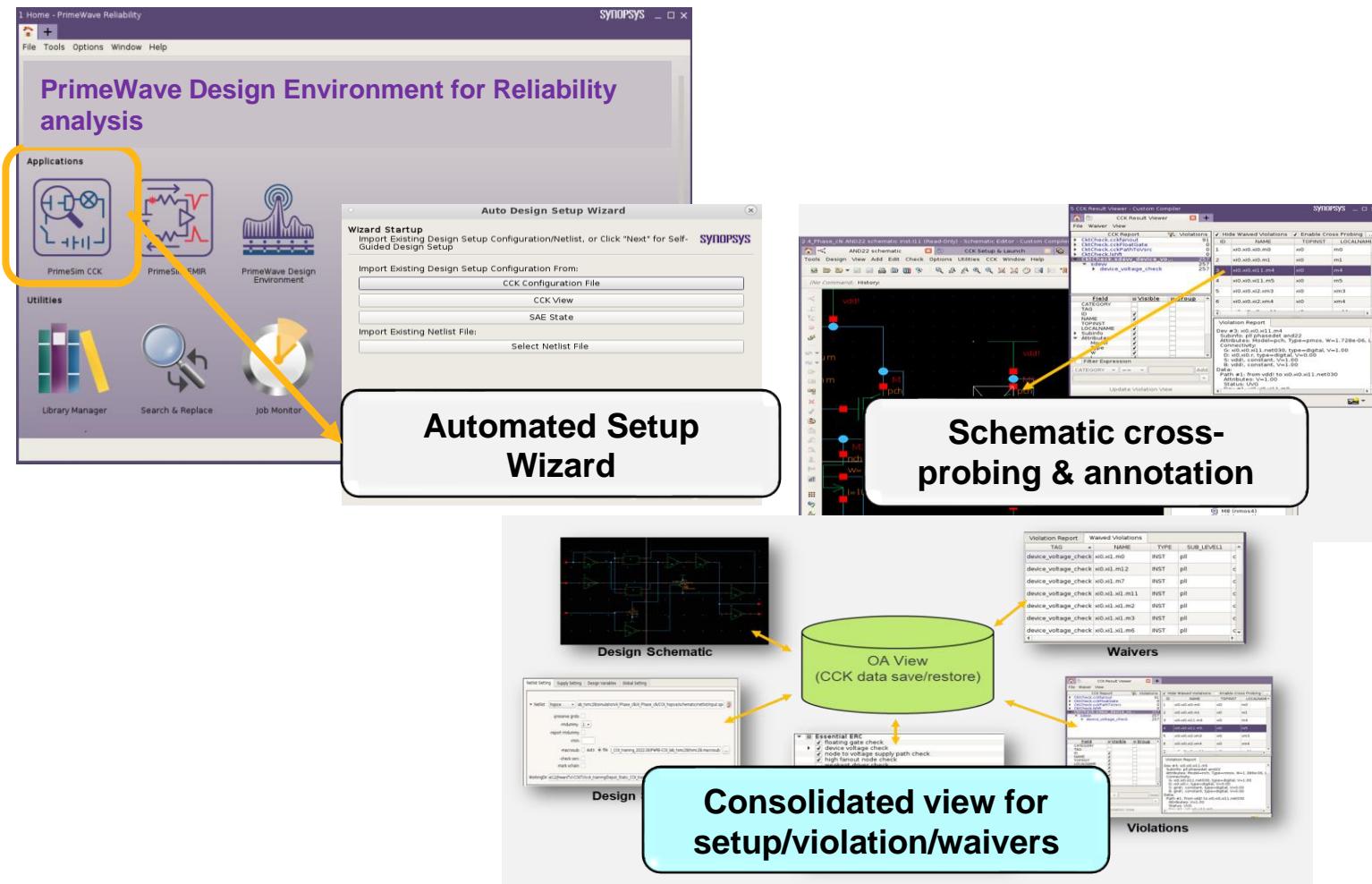
Customizable Circuit Integrity Checks



Advanced Debug with CCK Application

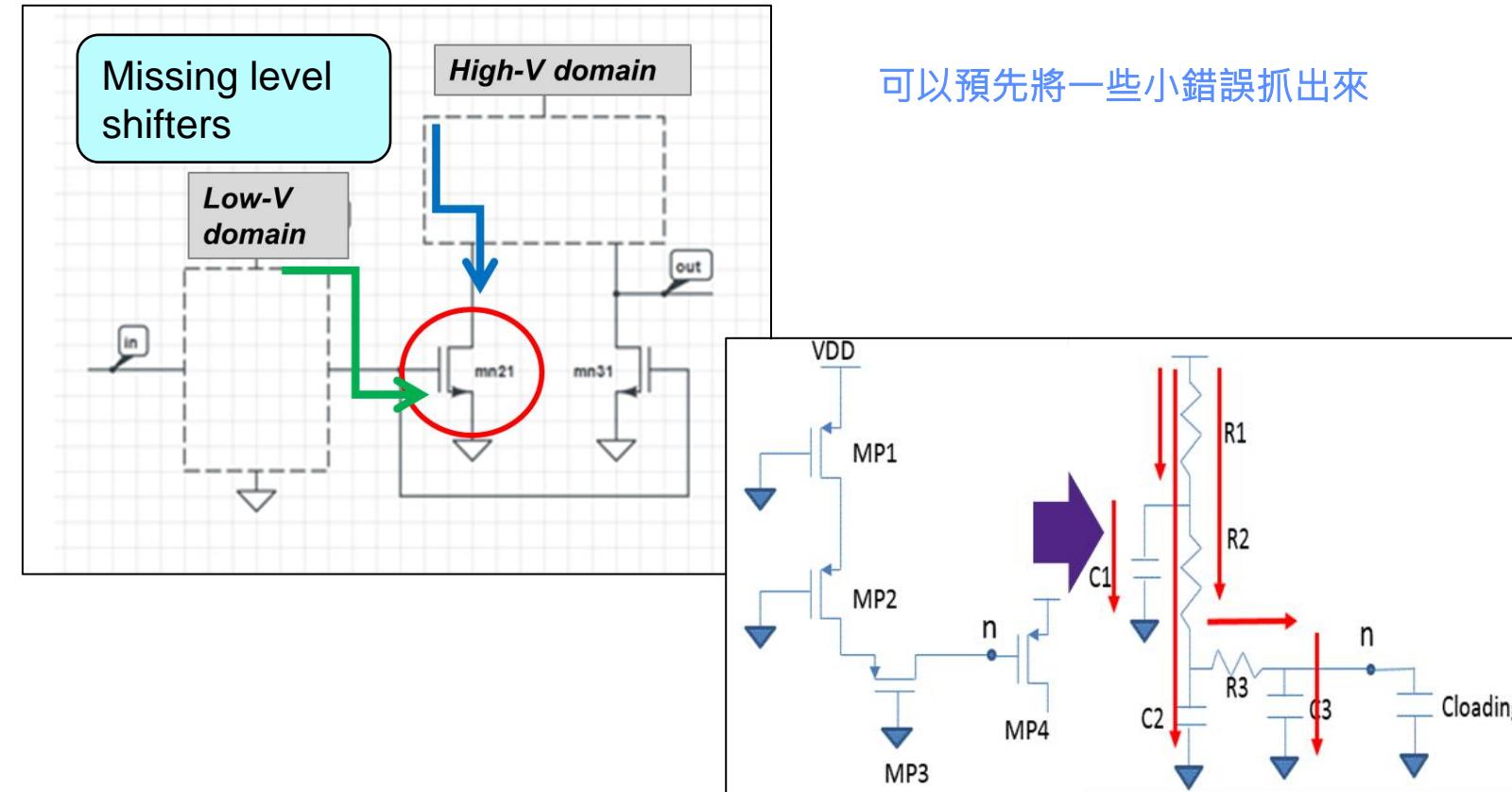
Benefits

- Push button setup, run and validation
- CC or 3rd party schematic viewing
- PDK macro model support
- OA view to save/restore CCK setup/violation/waiver data
- Bottom-up waiver flow support
- Schematic annotations



- Increasing design complexity
 - More FinFETs for similar functionality as planar
 - More custom digital content
 - Complex circuit topologies
 - Lower stress voltage
- More power domains
 - Power Switch, LDO, etc
 - Level shifters
- Increased parasitic
 - Higher interconnect R increasing delay
 - High cross-coupling Increased SI/Cross-talk effects

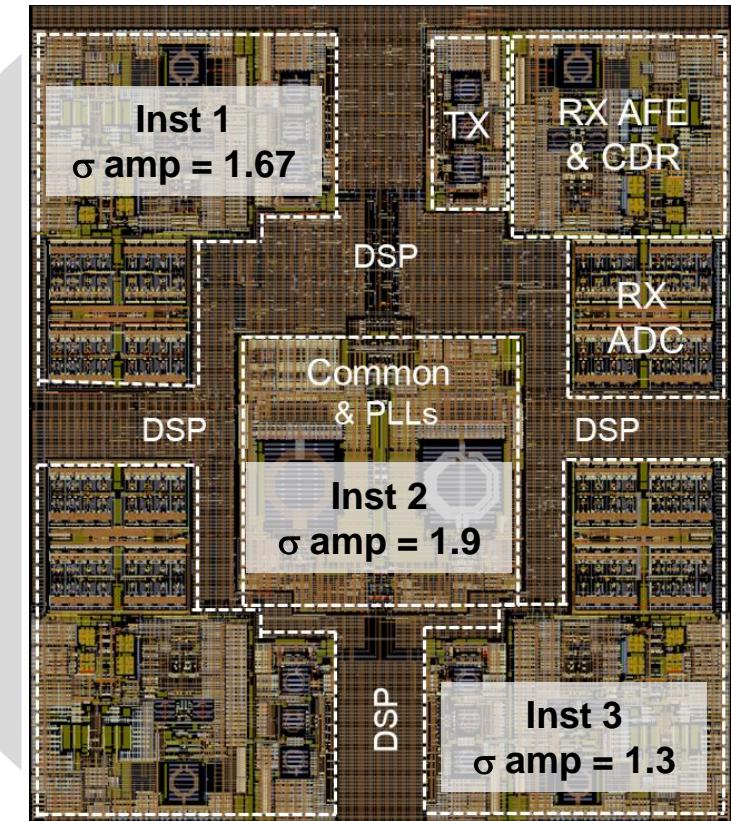
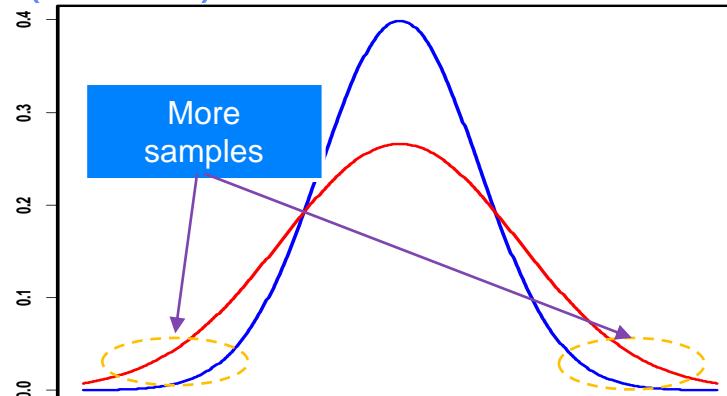
Circuit Integrity Checks for Complex Analog Mixed Signal Designs



Fast & Fine-Grained IP level Monte Carlo Simulation

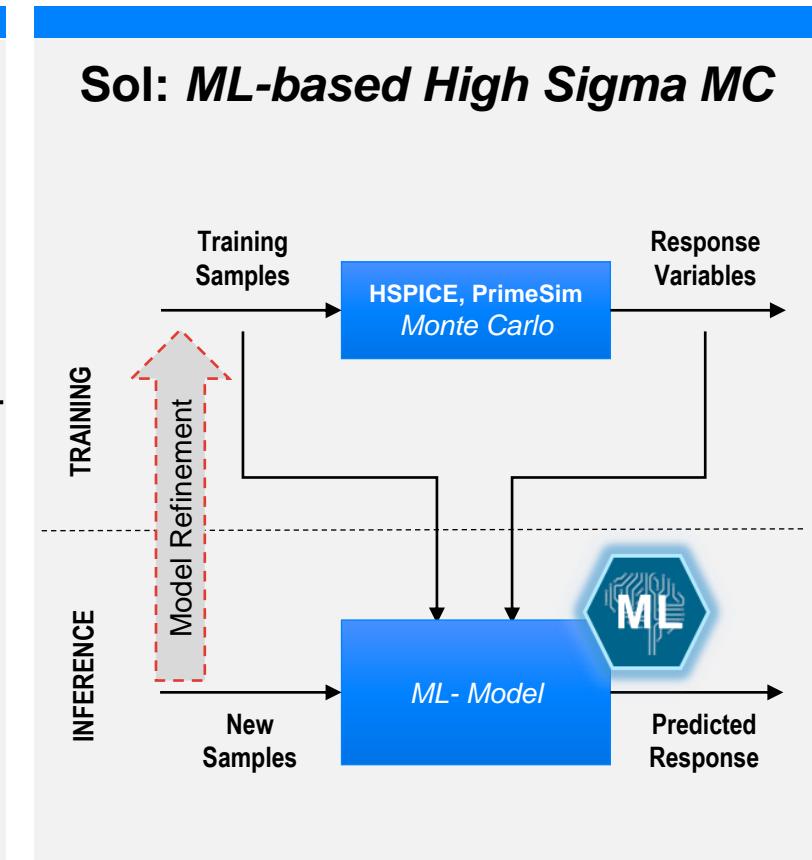
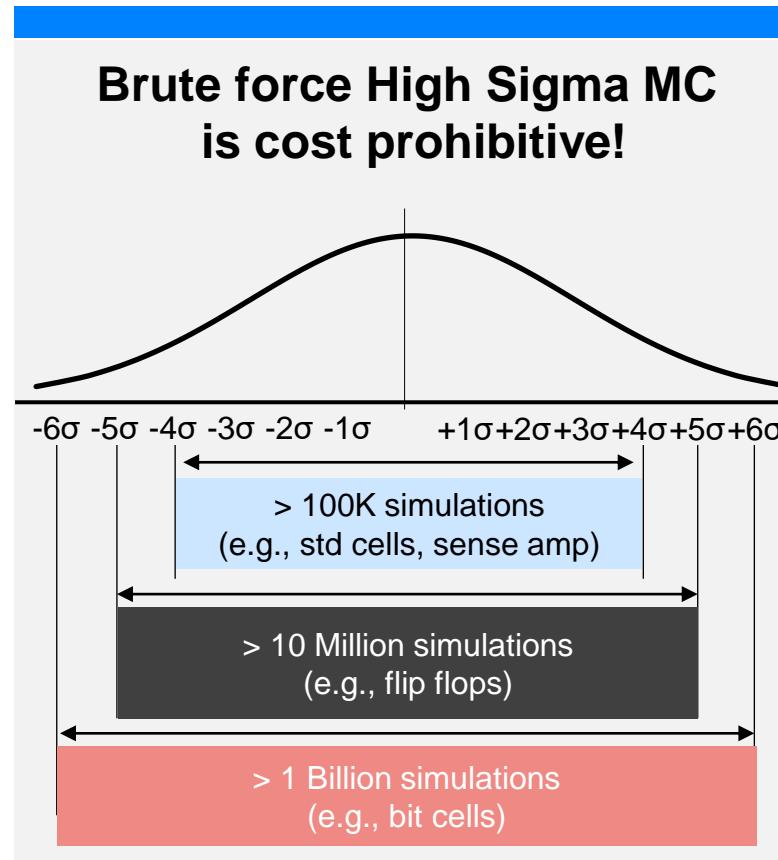
- Full Instance level MC analysis
- Tailor sigma amp. factor based on:
 - Design type
 - No. of instances
 - Target effective sigma
- Improve outlier detection with fewer MC samples
- Supports all PrimeSim Simulators

原本是藍色的高絲分布，但如果我們需要看看更多"比較不好的case"(在 ± 6 sigma附近的值)，可以透過將高斯分布往下壓(紅色的線)從而得到較多的case



Fast High Sigma Monte Carlo Analysis for Logic Libraries

- Advanced Variation Analysis
 - Usually within 1% of HSPICE
- Advanced ML algorithms
 - Adaptive training, refinement
 - Ensemble methods
- Targeted at 3 – 6.5 σ apps
 - Bit cell, std cell, sense amp, mux, flops (< 5K devices)
 - LVF characterization for delay, slew, constraints (with PrimeLib)
- Easy to use, accurate, fast
- Supports all PrimeSim Simulators



100X+ faster High-sigma Monte Carlo for yield and robustness verification

High Sigma MonteCarlo in PrimeWave Design Environment

- Setup testbench and measures with PrimeWave Design Environment
- Intuitive GUI driven setup that supports Sigma Amplification, BSSA, HSMC and PYE flows
- Supports various visualizations(tables, QQ-plots, scatter plots ,etc)
- Supports all PrimeSim simulators

The screenshot shows the PrimeWave Design Environment interface with several dialog boxes open:

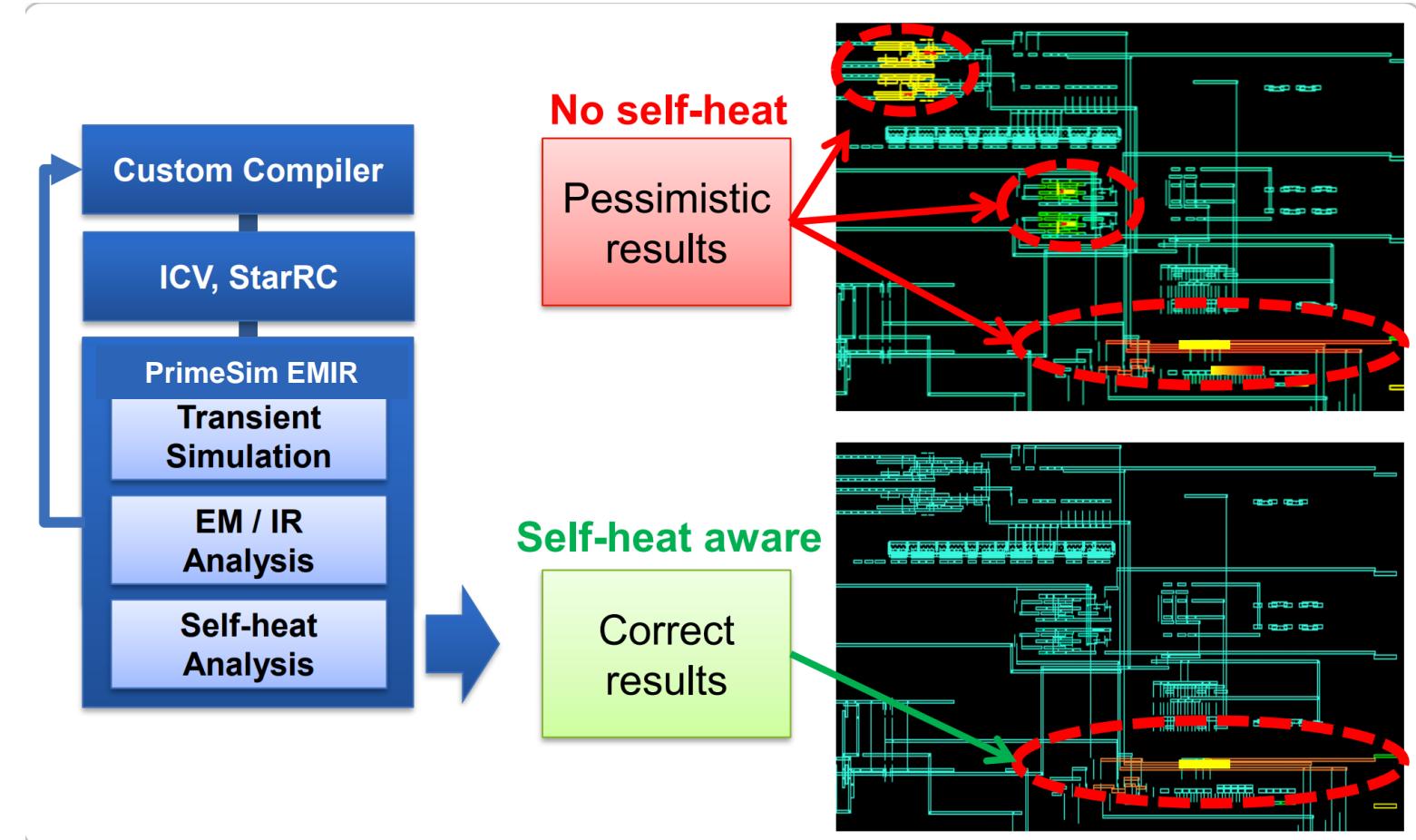
- Tools → MonteCarlo**: A large dialog box containing a table of variables and their values, and a grid of checkboxes for selecting analyses and plotting.
- HSMC Setup**: A dialog box for High Sigma MonteCarlo setup, showing settings for Statistical Variation, Sampling, Iterations, and Data Mining.
- Parametric Yield Estimation setup**: A dialog box for Parametric Yield Estimation setup, showing settings for Input Mode, Sampling, Iterations, and Data Mining.
- Sigma Amplification Setup**: A dialog box for Sigma Amplification setup, showing settings for Input Mode, Sampling, Iterations, and Data Mining.

A callout box on the right lists steps for setting up MonteCarlo:

- Select the relevant Flow
- Set the target Sigma in 'Chip Level Sigma'
- Set the accuracy in 'Uncertainty'
- Set affordable sample size in 'Number'(if applicable)
- Select the outputs that needs to be observed

- Synopsys Custom Design flow provides comprehensive EM sign-off
- In-Design EM with Custom Compiler
- Foundry certified workflow with
 - LVS,LPE from ICV and StarRC
 - Simulation from PrimeSim
 - EM and IR analysis with PrimeSim EMIR
- Certified by various foundries down to 3nm FinFET technology

Dynamic Self-heat Aware EM Analysis



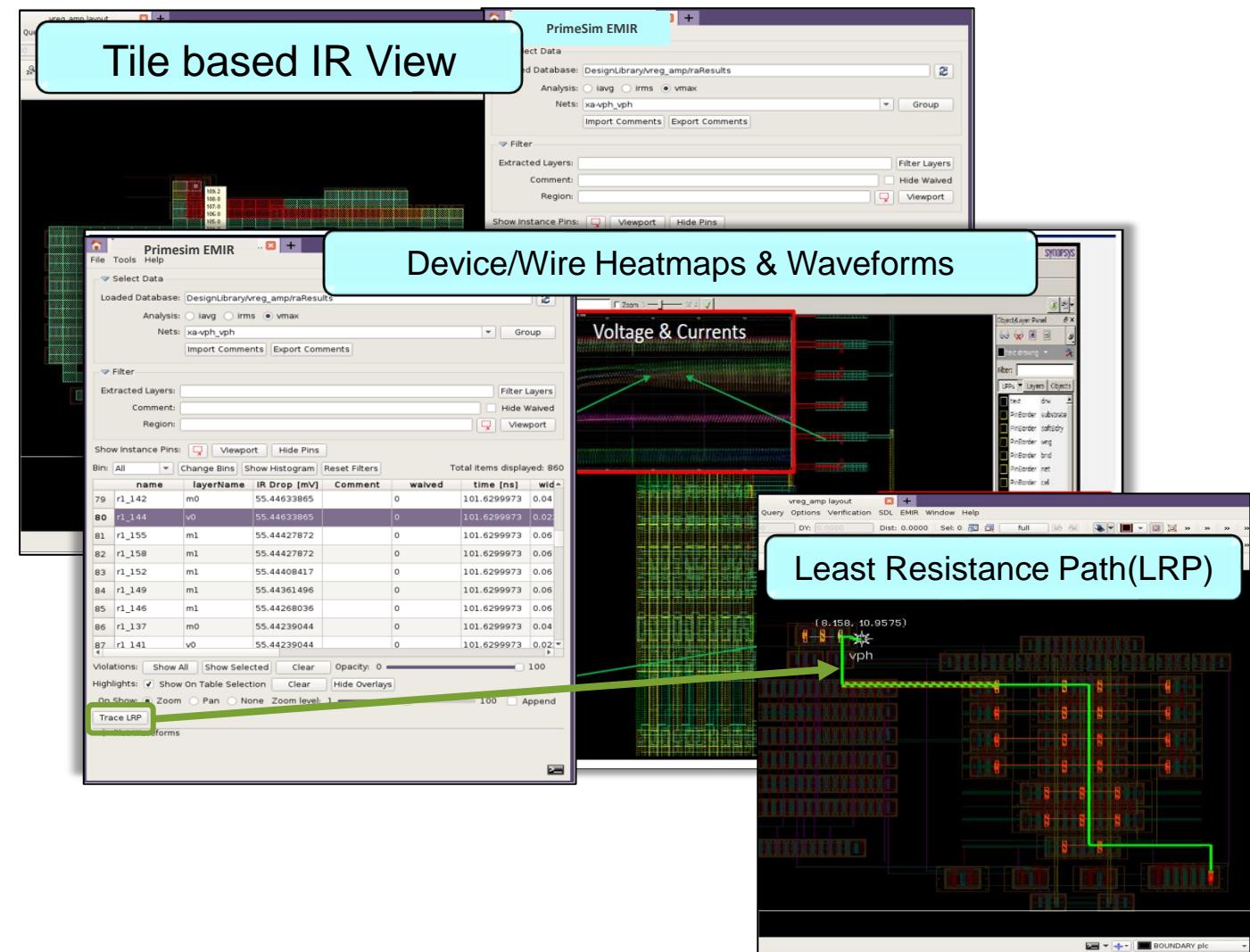
Benefits

- A workflow driven environment for all reliability applications
- Import and visualize schematic/layout views
- Advanced visualization, debugging and root-causing

Key features

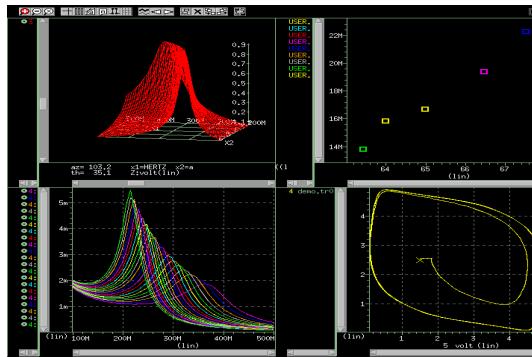
- CC or 3rd party Layout viewing
- RA viewer support
- OA view to save setup/violation/waiver data
- Advanced Visualization and debug
- Support what-if debugging

Advanced Debug with PrimeSim EMIR App



PrimeWave Design Environment

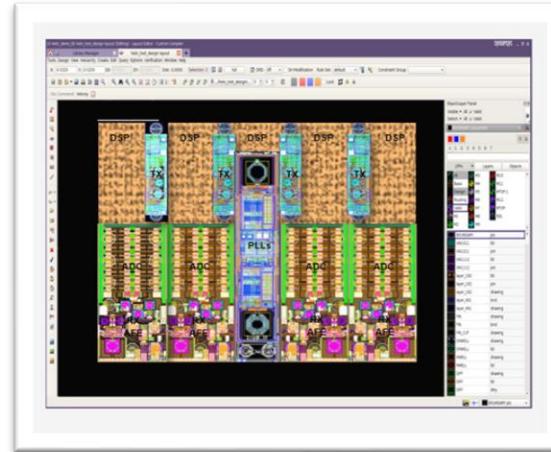
Design



- AI-driven design optimization
- Parasitic analysis to speed parasitic debug
- Design Assistants for faster measurement setup and enhanced coverage

Faster Time to Results

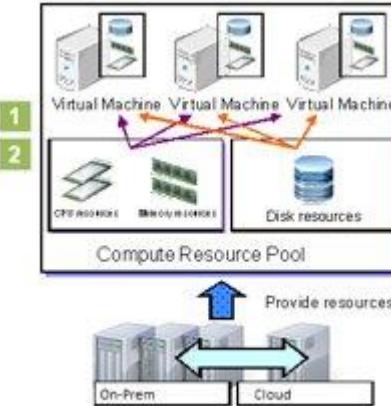
Reliability



- Workflow driven analysis for full life cycle reliability
- Tight handshake with simulation environment for ease of setup
- Schematic & Layout cross probing to debug & root cause reliability issues

Earlier Defect Detection

Regression

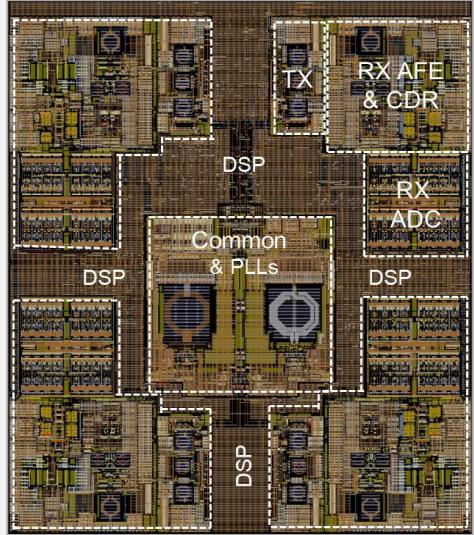


- Scalable and scriptable multi-site verification
- Design snapshot for faster reproduction of golden results
- Compute and Storage Resource Optimization

Lower Cost of Results

Summary

Synopsys Offers a Proven, Modern Alternative for Custom



Used by #1 mixed-signal IP design team

100's of new designs/year

Don't be locked in by legacy analog design tools

Break Free with Custom Compiler

Unlock innovation

synopsys®



Easy to adopt:
Familiar use-model
Simplified licensing

1000's of users at 200+ companies

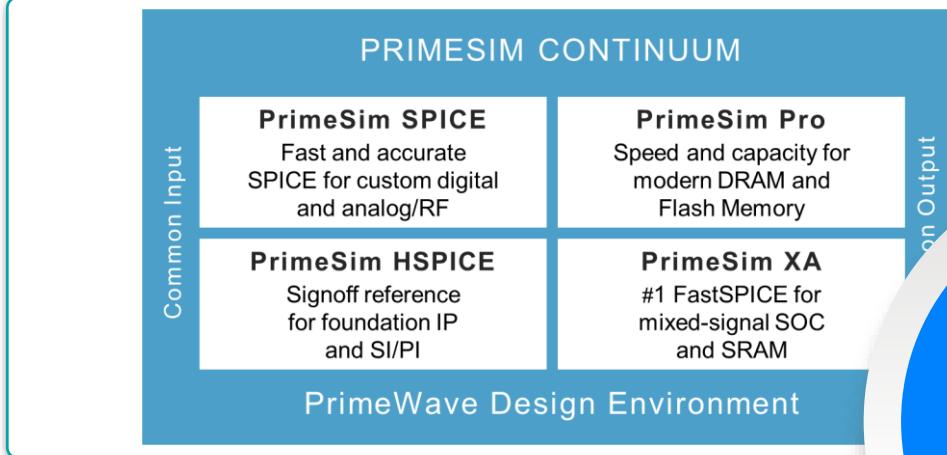


Industry-leading productivity

**2X faster closure
5X faster layout**

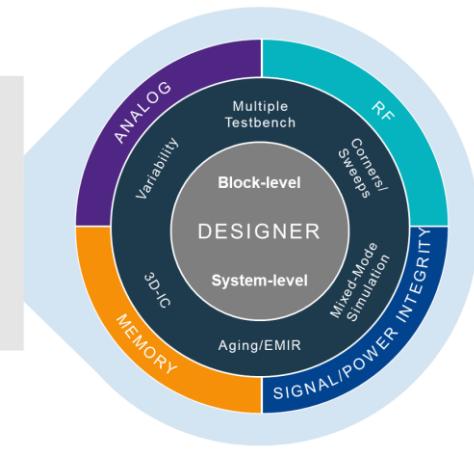
Industry Leading SPICE Engines

Unified Workflow for Analysis and Signoff



PrimeWave: Next-Generation Sim Env

- Comprehensive environment for all advanced analyses
- Integrated Waveform viewing and post-processing
- Flexible and programmable environment



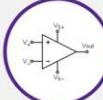
Fastest simulation

PrimeSim SPICE: Next-Generation S

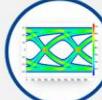
- Superior runtime performance with golden signoff accuracy (3X faster than competition)
- Scalable performance across CPU for time and frequency domain analysis
- 10X faster simulation with heterogeneous compute acceleration on CPU and GPU

Comprehensive Analysis

Time domain, frequency domain, noise



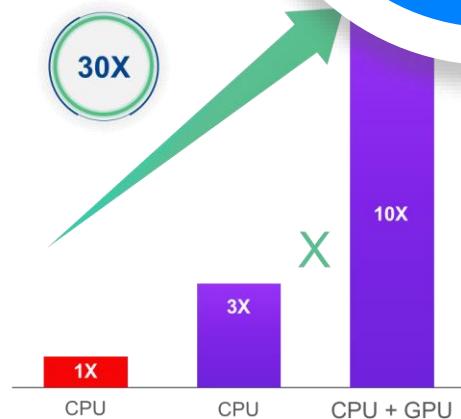
Analog



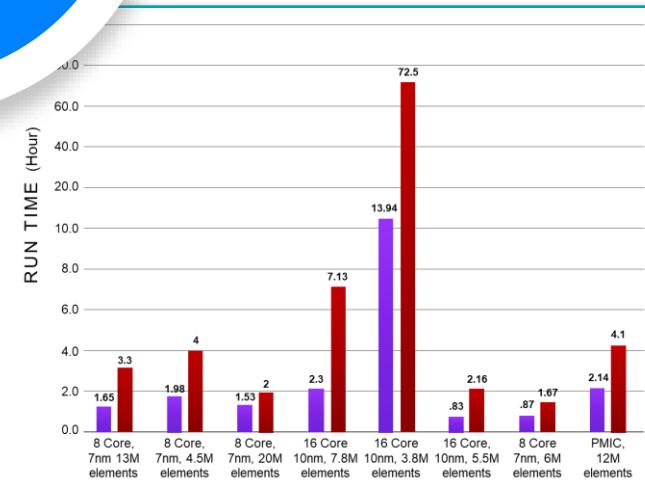
Signal Integrity



RF



PrimeSim SPICE Superior Runtime Performance



PrimeSim SPICE	Other	SPEED-UP
1.65 hrs	3.3 hrs	2X
1.98 hrs	4 hrs	2X
1.53 hrs	2 hrs	1.3X
2.3 hrs	7.13 hrs	3.1X
13.94 hrs	72.5 hrs	5.2X
0.83 hrs	2.16 hrs	2.6X
0.87 hrs	1.67 hrs	1.9X
2.14 hrs	4.1 hrs	2X

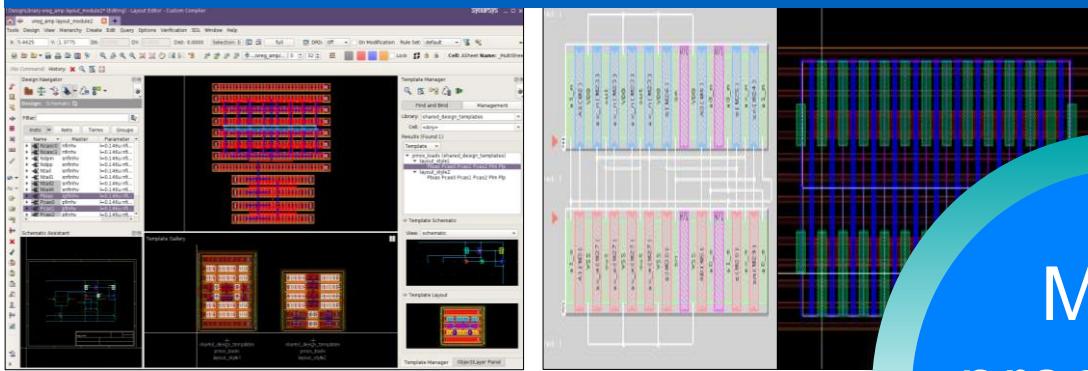
* Recent benchmark results from customers

Custom Layout Differentiating Technologies

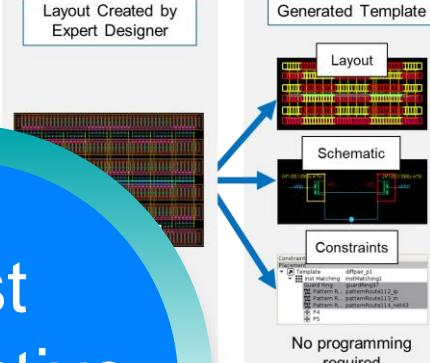
Visually Assisted Layout Automation

Analog Layout Reuse with Templates

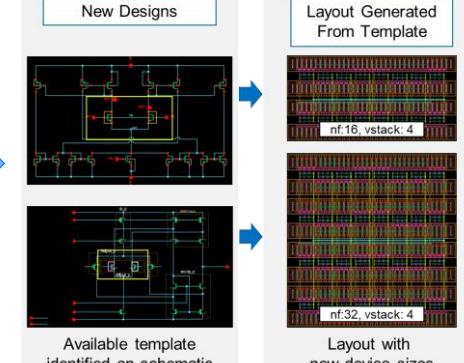
Graphical guidance and real-time feedback



Create Template



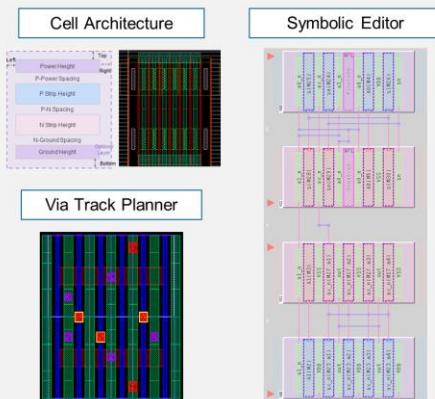
Use Template



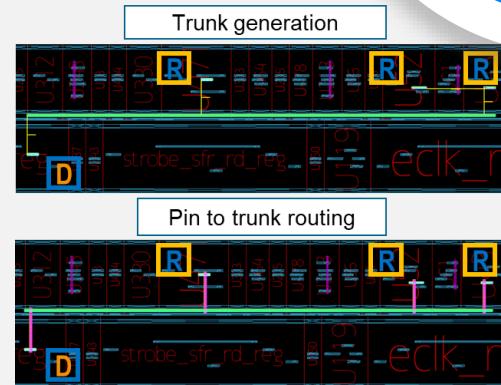
Most productive layout

Custom Digital Automation

Digital Cell Layout



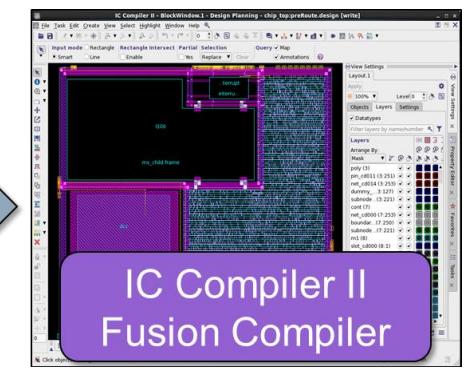
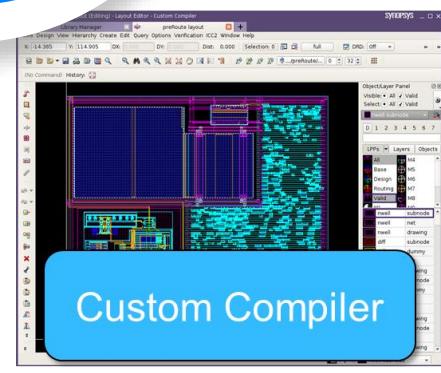
Custom Digital P&R



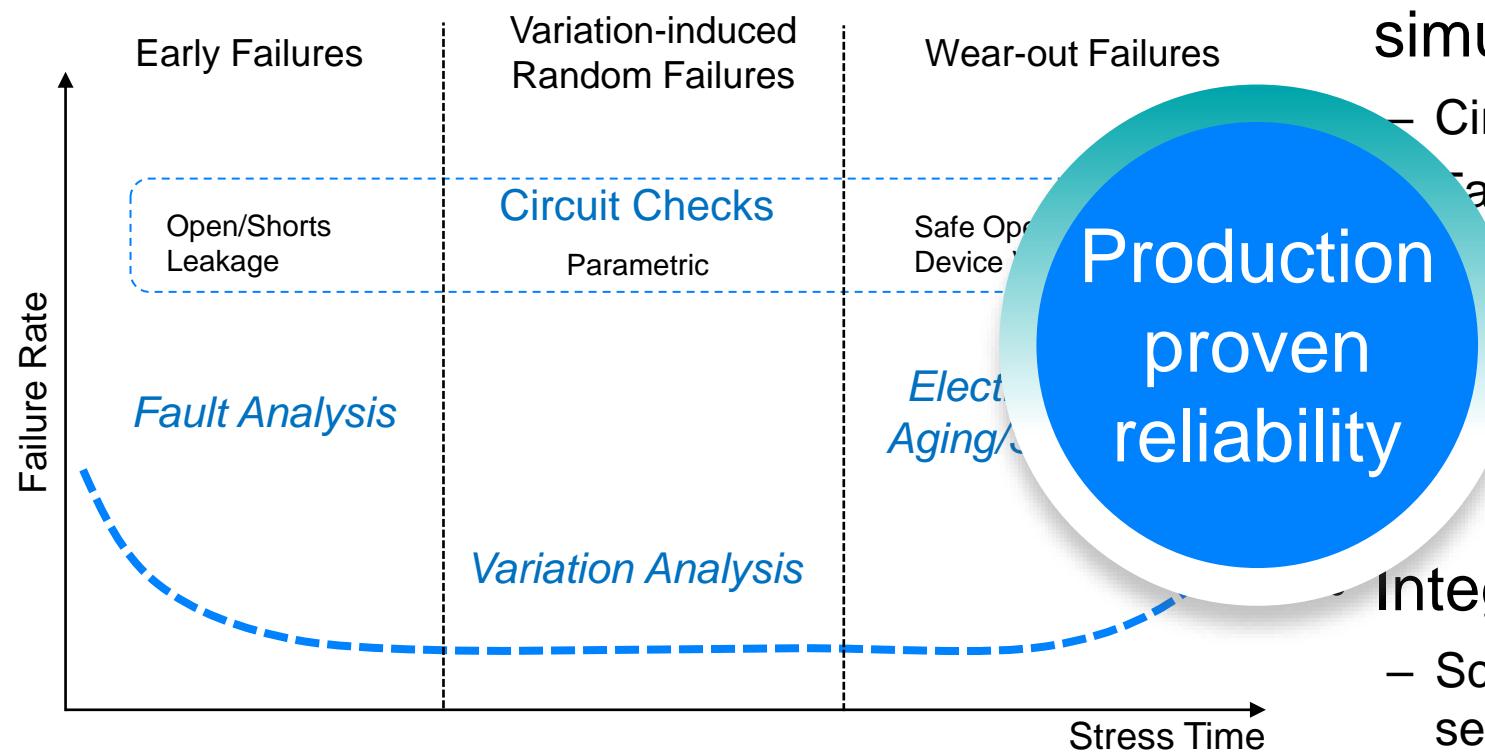
Unified Analog and Digital Co-Design

Lossless bi-directional connection

Custom Compiler



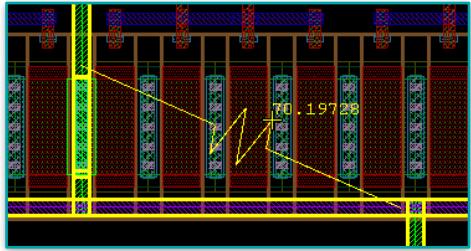
Reliability Solution for the Entire Product Life Cycle



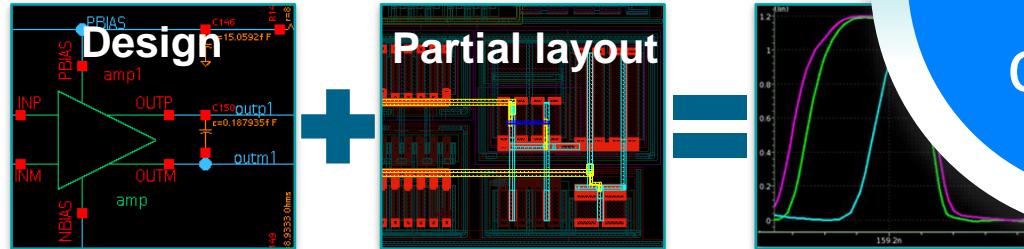
- Comprehensive analysis across all simulators
 - Circuit checks
 - Fault analysis
 - Large-scale & High-Sigma Monte Carlo Analysis
 - Electromigration/IR Drop
 - Aging/self-heating
- Integrated environment
 - Schematic/layout visualization with interactive setup, results exploration and what-if analyses
- Production-proven and foundry certified

Custom Design Signoff Solutions

Fusion Technology for Early Analysis

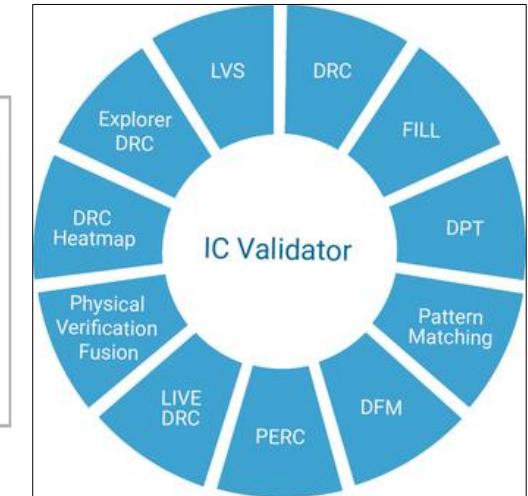
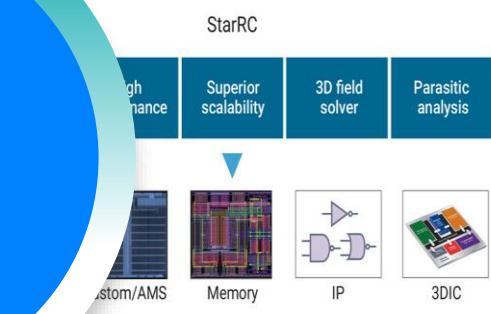


Partial layout extraction and simulation



On canvas electrical and DRC checking with StarRC, IC Validator and CustomSim-RA

Signoff Checks



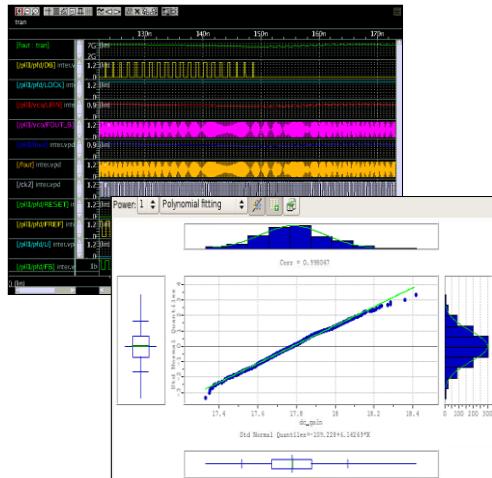
Faster
design
closure

Industry gold standard with leading performance and scalability

Complete Analog/Mixed-Signal Design Flow

Easy to adopt, familiar use-model, differentiated features

Simulation



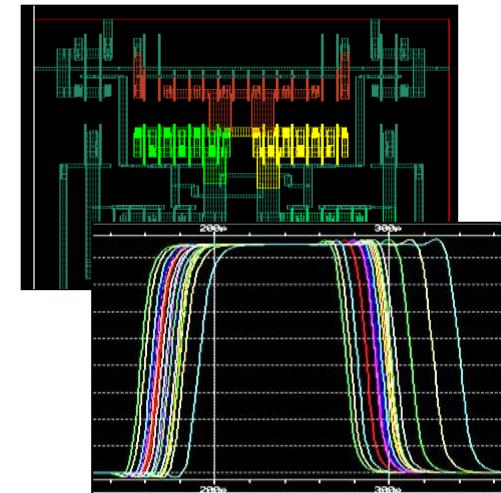
- Leading performance
- Golden accuracy

Layout



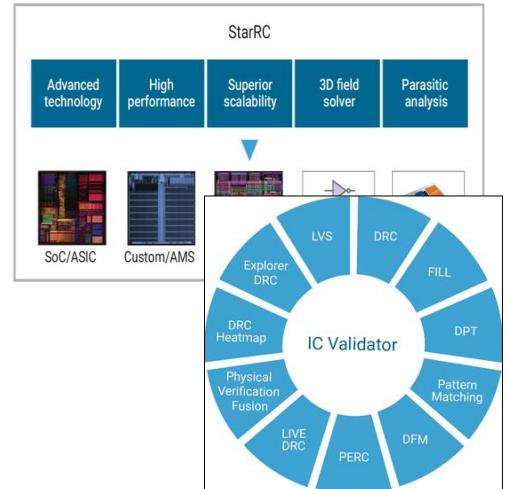
- Fast and productive
- Intuitive automation

Reliability



- Comprehensive
- Spans full life cycle

Signoff



- Golden reference
- Fusion technology

Synopsys Custom Design Platform Delivers Productivity

Fastest simulation

Most Productive layout

Production proven reliability

Faster design closure



Q&A

SYNOPSYS®

Thank You

Reference

- Article

- [FinFET Technology Considerations for Circuit Design](#)
- https://www.komatsu.jp/en/company/tech-innovation/report/pdf/180330_04e.pdf
- [IEDM 2017: Intel's 10nm Platform Process](#)
- [TSMC Talks 7nm, 5nm, Yield, And Next-Gen 5G And HPC Packaging](#)
- [TSMC FINFLEX™ – Ultimate Performance, Power Efficiency, Density and Flexibility - Taiwan Semiconductor Manufacturing Company Limited](#)
- [平平都是7nm 性能、製程大不同！](#)
- [The truth of tsmc 5nm](#)

- Video

- [Lam Research: Multiple Patterning Enables Feature Shrink](#)
- [Lam Research: Extending Moore's Law - Self-Aligned Quadruple Patterning](#)
- [What ASML Has Next After EUV](#)
- [How Does a MOSFET works](#)
- [EUV | Technology | Samsung Semiconductor Global](#)