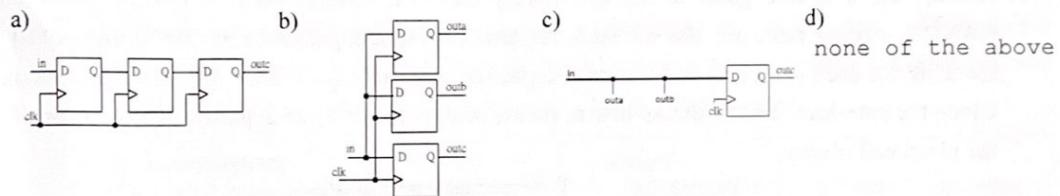


Special Topics in Computer-Aided Design (IEE6661)

1. (5%) Given the Verilog code shown right, which one is most likely the corresponding circuit after synthesis?
Please briefly explain your reasons.

```
input in;
output outa, outb, outc;
always @(posedge clk) begin
    outa = in;
    outb = outa;
    outc = outb;
end
```



2. (5%) For an always statement with multiple edge-triggered signals, how to determine its clock pin and asynchronous control pins?

3. (a) Given a Boolean function $F(A,B,C,D) = \sum(4,5,8,10,12,13,14)$ with don't care $d(A,B,C,D) = \sum(0,2,9,15)$. If we would like to use Quine-McCluskey method to optimize this Boolean function, the first step is to sort all possible minterms. Please show the sorting results for this function F. (3%)
 (b) During the optimization, $C1=A'BC'$, $C2=A'C'D'$, $C3=ABC'$ are three possible cubes. Please use the positional cube representation to represent the three cubes. (3%)
 (c) In (b), please use positional cube representation to test whether $C1$ and $C2$ can be merged to become a larger cube. Please also test the merging possibility for $C1$ vs $C3$. (4%)
 (d) Finally, there are 4 possible prime implicants, $P1=AB$, $P2=AD'$, $P3=BC'$, $P4=C'D'$. Please find the minimum cover of this function by using column covering method. (8%)
 (e) If ESPRESSO heuristic approach is adopted, why the complexity of logic optimization can be reduced? Does it always find the best result? (5%)

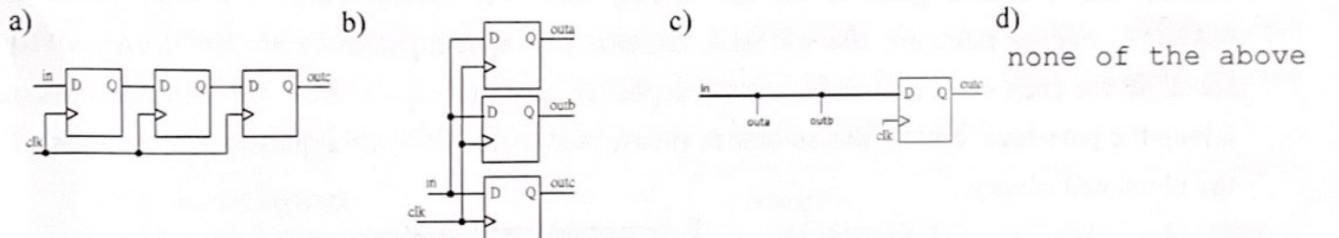
4. Consider the logic network defined by the following expressions:

$$x = ab'c + ace + bcd + b'd + de, \quad y = ac + d$$

- (a) How can we know if some part of function x can be substituted by function y ? Please show your calculation process and explain your result. (8%)
 (b) In (a), do we really get improvement with the possible substitution in terms of the total number of literals? (3%)
 (c) After substitution, the two-level circuit is converted to a multi-level circuit. What are the possible advantages and disadvantages of this change? (5%)

1. (5%) Given the Verilog code shown right, which one is most likely the corresponding circuit after synthesis? Please briefly explain your reasons.

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2. (5%) For an always statement with multiple edge-triggered signals, how to determine its clock pin and asynchronous control pins?

當有多個 edge-trigger signals. 不會在執行運算中使用到的是 clk pin. 其它是 asynchronous control pins.

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(a)

QM:

0	00000
2	00100
4	01000
8	10000
10	10100
12	11000
13	11010
14	11110

0	00000
5	01010
9	10010
10	10100
12	11000
13	11010
14	11110
15	11111

0	00000	CD
2	00100	B'D'
4	01000	BC'
8	10000	AC'
10	10100	AD'
12	11000	AB
13	11010	
14	11110	
15	11111	

minterm

$$\begin{matrix} 0100 \\ 0100 \end{matrix}$$

(b).

$$C_1: 10\ 01\ 10\ 11 \quad \phi: 00$$

$$C_2: 10\ 11\ 10\ 10 \quad 1: 01$$

$$C_3: 01\ 01\ 10\ 11 \quad 0: 10$$

 $\Rightarrow \{4, 5\}$

$$C_1 \cup C_2 \rightarrow \{0, 4\}$$

 $C_1 \cup C_2$ 非空

$$C_1 \cup C_2 = 10\ 11\ 10\ 11 \quad \Rightarrow \text{check on set.}$$

$$\begin{matrix} 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{matrix} \quad \{0, 1, 4\}$$

1不在。
→不能合併

 $\Rightarrow \{4, 5\}$

$$C_1 \cup C_3 \rightarrow \{12, 13\}$$

 $\begin{matrix} 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 \end{matrix}$

$$C_1 \cup C_3 = 11\ 01\ 10\ 11 \quad \{4, 5, 12, 13\}$$

C_1 and C_3 可 merge.

(d)

	4	5	8	10	12	13	14
AB	12 14	13 15			✓	✓	✓
AD'	8 12	10 14		✓	✓	✓	
BC'	4 12	5 13	✓	✓	✓	✓	
CD'	0 12	4 12	✓	✓	✓		
	$\Rightarrow F = AD' + BC'$						

(e) - ESPRESSO

i the complexity can be reduced. because it avoid generation of all prime implicant and use iteratively to find alternative covers.

ii No. 可能找到的點數法 optimiza by 舊值。

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$$x = ab'c + ace + bcd + b'd + de \quad y = ac + d$$

(a). by weak division,

(b) before, lit = 13 + 3 = 16

$$U = ac + ac + d + d + d$$

after

$$x = (b'e)y + bcd$$

$$y = ac + d$$

$$V = b' + e + bc + b' + e$$

literal = 9

$$Var = \underline{b'} + e$$

$$\Rightarrow f = b' + e, \text{ remainder } = bcd$$

$$Vd = bc + \underline{b'} + e$$

$$\Rightarrow x = (b'e)(ac + d) + bcd$$

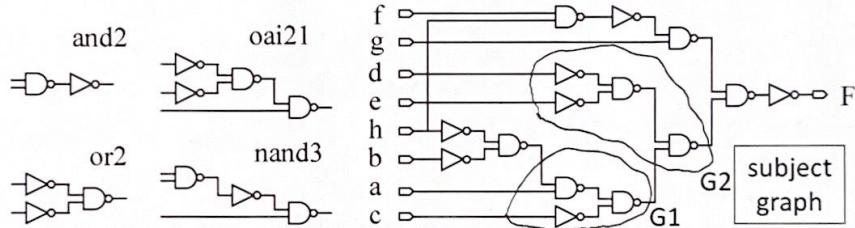
\Rightarrow improvement.

(c). two level \rightarrow multi-level

adv. 可用 gate \uparrow Area \downarrow disadv. delay \uparrow . (critical path \uparrow)

Special Topics in Computer-Aided Design (IEE6661)

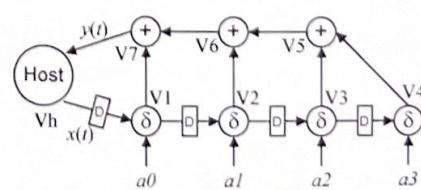
5. (a) In timing optimization, what are the key factors that need to be considered? Please briefly explain your reasons. (5%)
 (b) There is a timing optimization technique called “timing decomposition”. Why can it improve the overall delay time? What is the possible cost of using this technique?? (5%)
6. Assume the available gates in the cell library are INV, AND2, OR2, NAND2, OAI21 and NAND3. Inverter pairs are also allowed. Assume the input capacitance of OAI21 and NAND3 are 0.5fF for each input pin, and the input capacitance of other gates are 0.3fF for each input pin. Given the gate-level circuit shown below, please answer the following questions after mapped to the given cell library.



- (a) For group G1, how many choices do you have to implement this area? What is the related cost in terms of the number of gates? Please redraw every possible implementation results for group G1 on your answer sheet. (5%)
 (b) For group G2, you can implement the final node as NAND2 or OAI21. In terms of the total capacitance on each signal net (including the input pins to this area), which selection is better for low power purpose? Please explain your reasons. (5%)
7. (a) Why dual V_t design technique is able to reduce the overall power consumption? What is the possible overhead of this technique? (5%)
 (b) If dual V_t technique is applied in a single gate, it is called a mixed- V_t gate. Please explain the pros and cons of adopting mixed- V_t gates to implement digital circuits. (5%)

8. For the circuit shown right:

- (a) Given a retiming ($r_h=0, r_1=-1, r_2=-1, r_3=-2, r_4=-2, r_5=-1, r_6=-1, r_7=0$), please redraw the new circuit after retiming. (8%)
 (b) Since the adders and comparators are not changed, what is improved by the retiming technique? In which situation will you obtain more speedup through retiming? (5%)



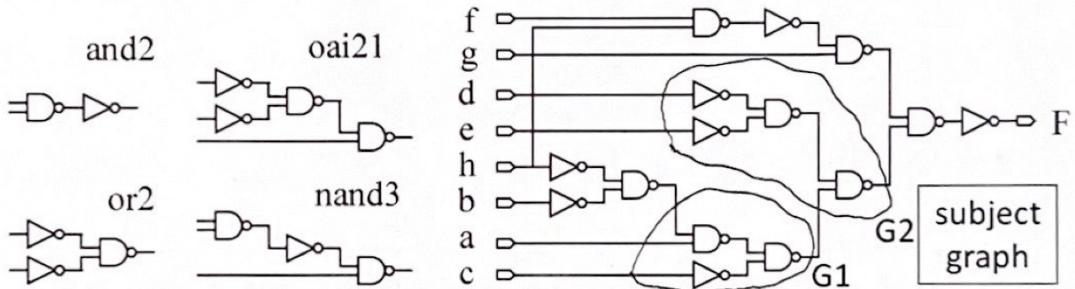
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(a). delay . too早 delay 過早會 timing violation.

(b). approve timing by reconstructing the logic network to minimize arrival time.

drawback : Area may increase.

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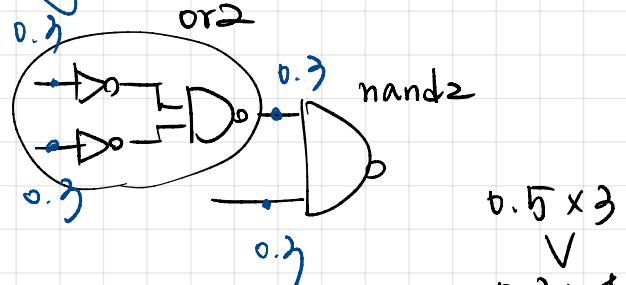
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(a).
G1
① and2 + or2 \Rightarrow 2 gates

② 2nand2 + inv \Rightarrow 3 gates

③

(b).
G2.
OAI21
0.9
0.5
0.5



③ is better since lower load.

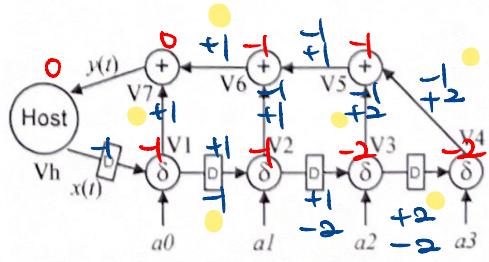
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(a) i only deploy the fast, leaky V_f on path that needs to improve timing.
 ii support for another library is an extra cost.

(b). adv. preserve delay while decreasing leakage.
 disadv. 不同 V_f layout \nrightarrow well $\xrightarrow{\text{exp}}$ Pd
 \Rightarrow area \uparrow . cap \uparrow

8. For the circuit shown right:

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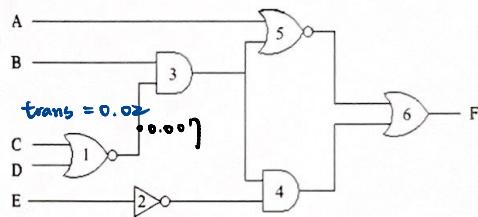
P.2

critical path became short.

clk period can be lower

Special Topics in Computer-Aided Design (IEE6661)

9. (8%) Assume the delay time and input capacitance of each gate can be determined by the following lookup table in liberty format. But the delay time of an inverter is only a half of the value obtained from the table. In order to simplify the calculation, the rising delay and falling delay are assumed to be the same. The delay values from different inputs are assumed equal, too. Rising time and falling time are also obtained from the same table. Assume the initial input transition time is 0.02 ns, and the output loading are 3fF at node F. What is the delay of gate 3 in this case?



```
lu_table_template(table10){
    variable_1 : total_output_net_capacitance; // pF
    variable_2 : input_transition_time; // ns
    index_1 ("0.002,0.003,0.006,0.013,0.025,0.050,0.100");
    index_2 ("0.020,0.035,0.060,0.120,0.210,0.420,0.830");
}
cell (NANDX1) {
    pin(A1) {
        direction: input;
        capacitance: 0.007;
    }
    pin(A2) {
        direction: input;
        capacitance: 0.007;
    }
    pin(ZN) {
        direction: output;
        capacitance: 0.0;
    }
    internal_power() {...} // power omitted in this example
}
```

```
timing() {
    cell_rise(table10) { // cell delay at output rising
        value("0.013,0.016,0.020,0.023,0.030,0.040,0.050",
        "0.015,0.019,0.023,0.026,0.037,0.047,0.060",
        "0.019,0.022,0.028,0.033,0.046,0.060,0.077",
        "0.026,0.030,0.033,0.043,0.055,0.080,0.104",
        "0.040,0.041,0.046,0.059,0.076,0.099,0.147",
        "0.066,0.069,0.073,0.084,0.108,0.144,0.189",
        "0.122,0.124,0.129,0.139,0.160,0.209,0.279");
    }
    cell_fall(table10) // cell delay at output is falling
    value(...); // assume the same with rising
    rise_transition(table10) // output rising time
    value(...); // values are the same with cell_rise
    fall_transition(table10) // output falling time
    value(...); // values are the same with cell_fall
} // end timing
} // end pin
} // end cell
```

$$\text{cell rise delay} = 0.02 \times \frac{1}{7} \times 0.003 = 0.0024 \text{ ns}.$$

rise trans is the same as cell rise.

$$\text{gate 3 . output load} = 0.014. \quad 0.024 + \frac{1}{12} \times 0.004 \\ \text{trans} = 0.0204 \quad = 0.0244 \\ = 0.0244 \quad 0.024 + \frac{1}{12} \times 0.004 \\ = 0.0268$$

$$0.0244 + \frac{0.0004}{0.014} \times (0.0268 - 0.0244) \\ = 0.0237$$