C1 - Introduction

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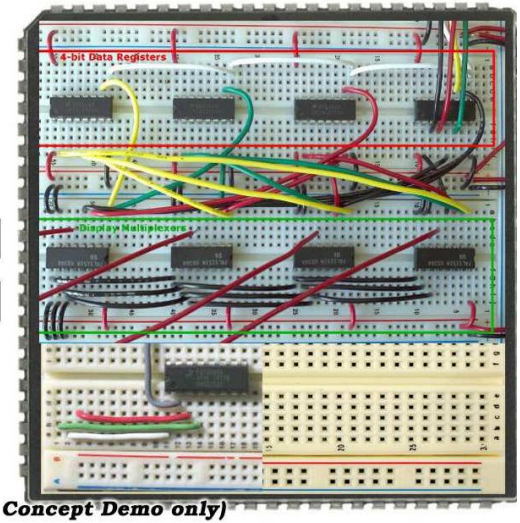
VHDL

VHDL = LOGIC DESIGN

- ***Just Like Building a Circuit on Your Breadboard!!***
- ***Also known as a "Hardware Description Language"***

```
 5  LIBRARY ieee;
 6  USE ieee.std_logic_1164.all;
 7
 8  ENTITY LabExCG4 IS
 9      PORT(   u, v, w, x, y : IN BIT;
10              s       :   IN STD_LOGIC_VECTOR(2 DOWNTO 0);
11              m : OUT BIT);
12  END LabExCG4;
13
14  ARCHITECTURE Behavior OF LabExCG4 IS
15  BEGIN
16  PROCESS(s)
17  BEGIN
18      CASE s is
19          WHEN "000" => m <= u;
20          WHEN "001" => m <= v;
21          WHEN "010" => m <= w;
22          WHEN "011" => m <= x;
23          WHEN "100" => m <= y;
24          WHEN OTHERS => m <= y;
25      END CASE;
26  END PROCESS;
27  END Behavior;
```

=



(NOT Actual equivalent Circuit - For Concept Demo only)

什么是VHDL?

- VHDL : VHSIC Hardware Description Language
- VHSIC : Very High Speed Integrated Circuit
- VHDL：硬件描述语言，描述了数字电路的结构和行为。

- 语言标准描述电路或用于以下方面的数字系统:
  - **电路系统的建模（仿真）**
  - **数字电路的综合（自动生成）**
  - 测试程序说明（testbench）
  - 层次类型的描述 (**netlist**)

历史

- 1981 - 由美国 DoD（国防部）发起，以解决物资生命周期危机。
- 1983-85 - Intermetrics、IBM和TI开发语言库。
- 1986 - 所有权利转让给 IEEE（电气和电子工程师协会）
- 1987 - 发布 IEEE 标准 1076-1987
- 1994 - 修订标准 VHDL-1076-1993（所需的一切，被 90% 的设计师使用）
- 2002 – VHDL标准 IEEE 1076-2002
- 2009 – VHDL 2008 标准 IEEE 1076-2008

https://www.doulos.com/knowhow/vhdl_designers_guide/a_brief_history_of_vhdl

其他类似语言

- 其他类似语言
- Verilog较旧。 语法接近于C语言，在美国和亚洲广泛使用
- VHDL-AMS混合数字模拟建模语言 IEEE.1076.1-1999。 它与VHDL 完全兼容。 仅用于建模。

- System C
- System Verilog

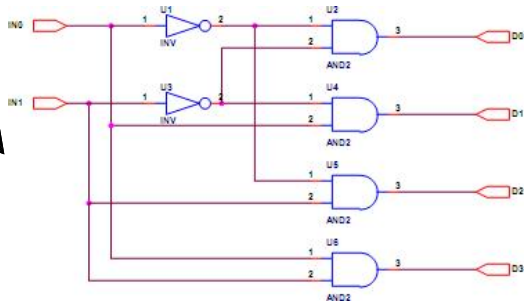
建模还是综合?

- 建模
  - 所有的语言。 逻辑+时间
  - 模型可以是行为，结构或数据流类型。
- 综合
  - 综合VHDL是通用VHDL的子集
  - 综合需要对电路和技术有充分的 了解。

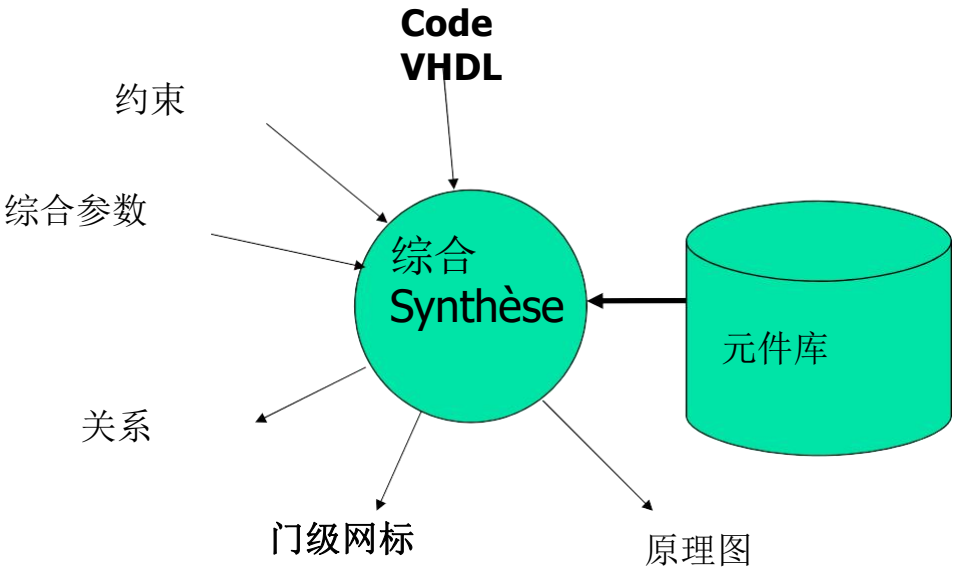
综合(1)

```
entity DECOD1_4 is
     port(IN0, IN1: in std_logic;
          D0, D1, D2, D3: out std_logic);
end DECOD1_4;
```

Synthèse



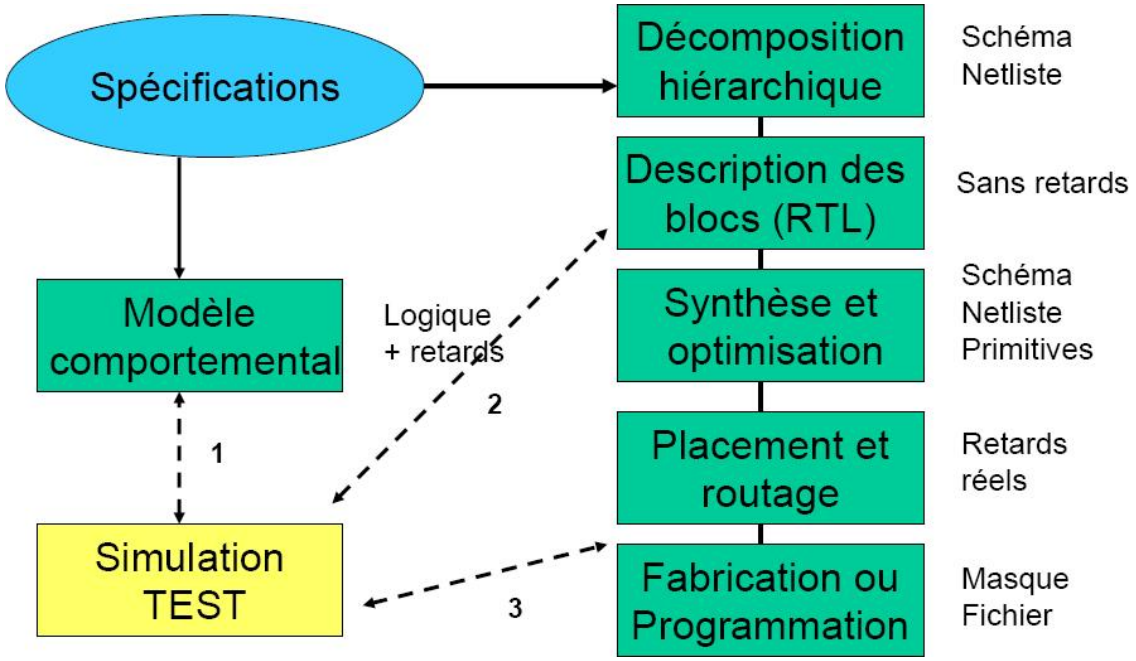
综合(2)



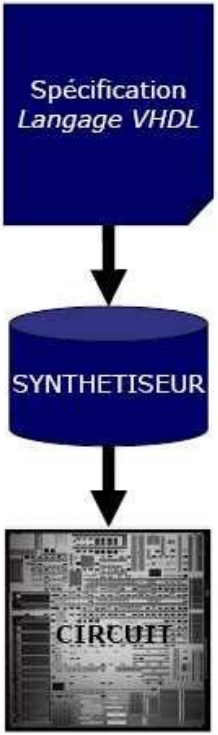
警告摘要

- 综合对于VHDL的编写方式非常敏感。
- 对于综合，必须遵守某些编码规则。
- 一个好的设计只能来自一个好的VHDL代码（该工具无法解决奇迹）
- 综合不能替代人类的专业知识。
- " Le VHDL de synthèse est un sous-ensemble du VHDL généraliste "

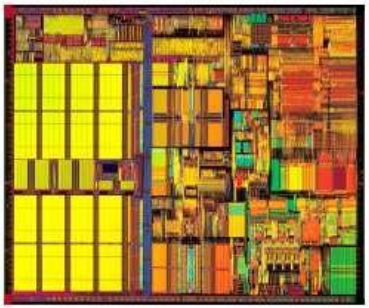
设计流程

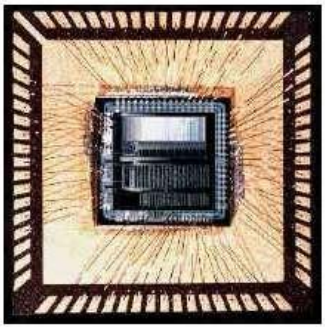

Spécifications
Décomposition hiérarchique
Schéma Netliste
Description des blocs (RTL)
Sans retards
Modèle comportemental
Logique + retards
Synthèse et optimisation
Schéma Netliste Primitives
2
1
Placement et routage
Retards réels
Simulation TEST
3
Fabrication ou Programmation
Masque Fichier

专用集成电路ASIC

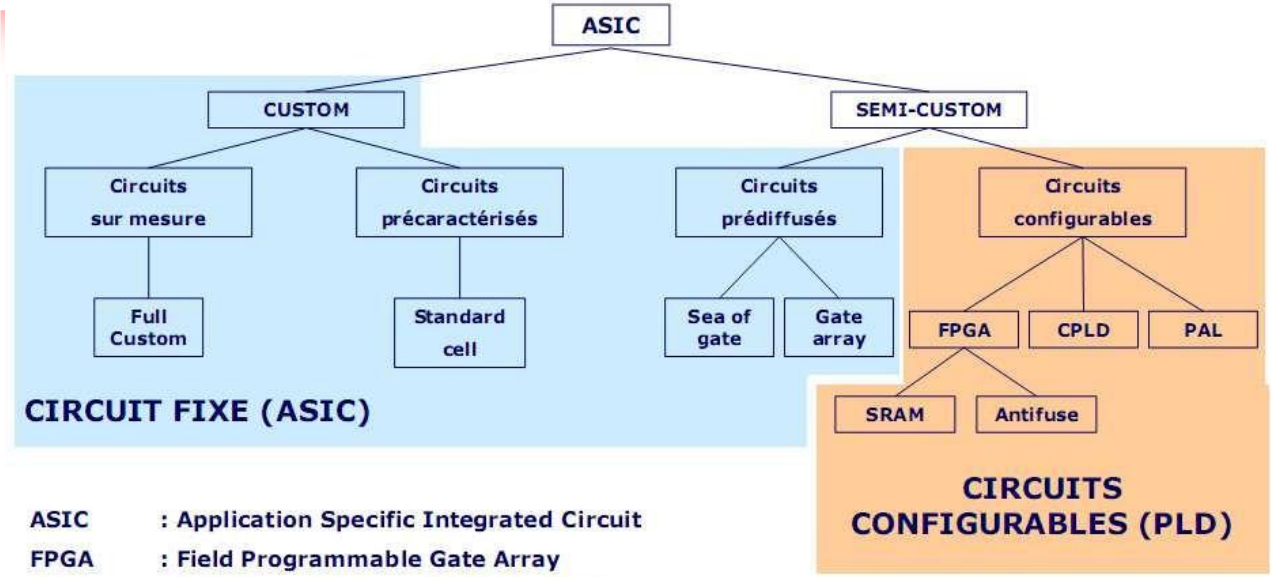


- ASIC : Application Specific Integrated Circuit
  - 数字、模拟和混合（通信领域）
  - 专用功能
  - 实现复杂 (从高级规范到物理综合)
  - 极高的性能:专用+并行实现+先进技术
  - 电路 = 规格



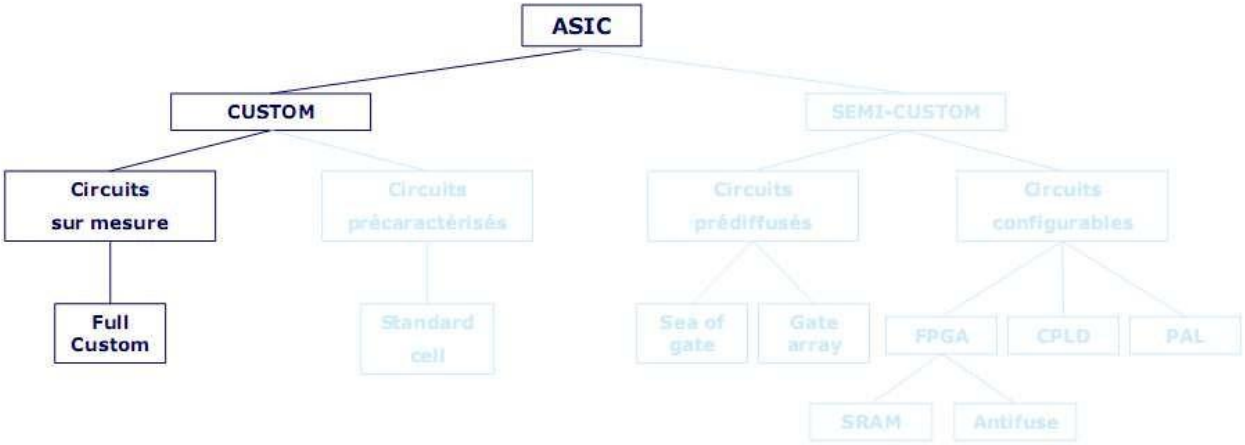


不同硬件特点



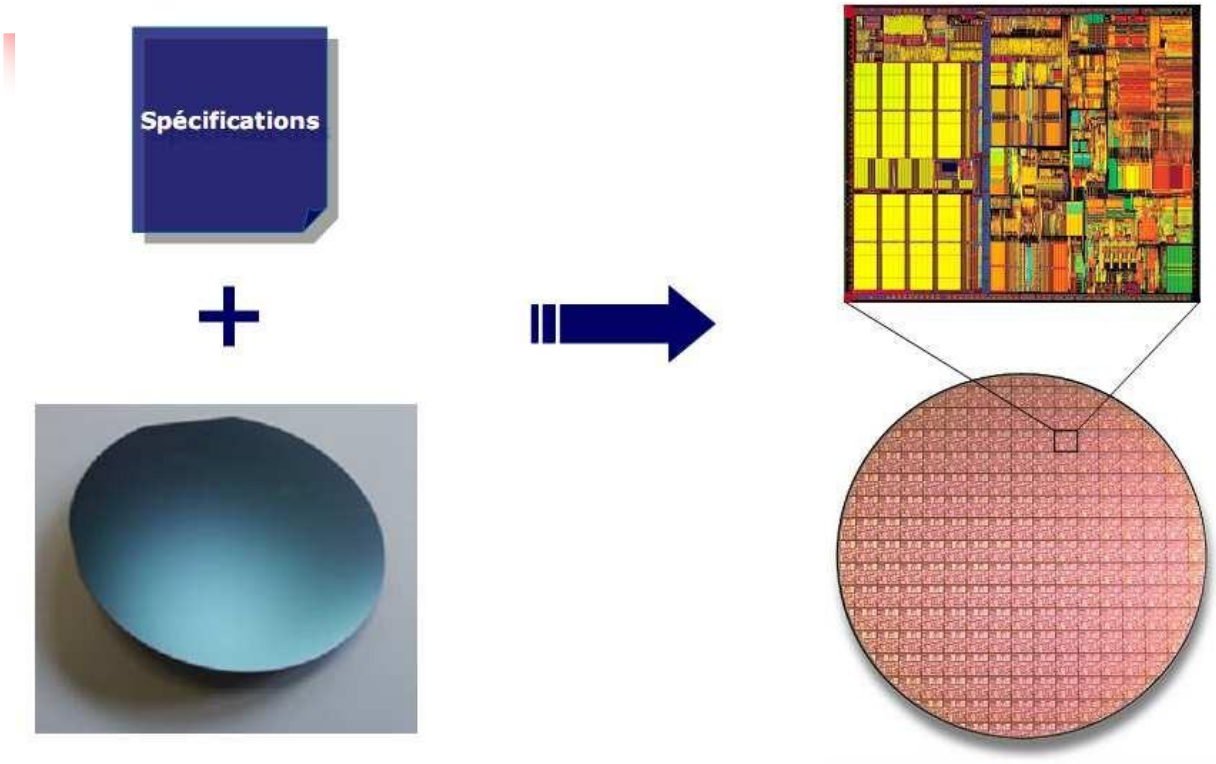
ASIC	: Application Specific Integrated Circuit
FPGA	: Field Programmable Gate Array
CPLD	: Complex Programmable Logic Device
PAL	: Programmable Array Logic
GAL	: Generic Array Logic = PAL
SRAM	: Static Random Acess Memory

ASIC 全定制

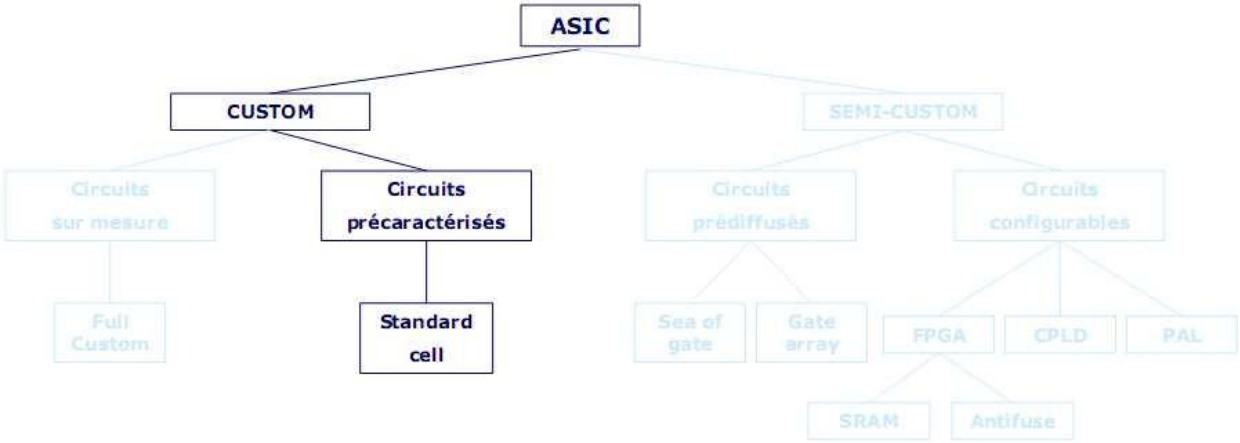


ASIC : Application Specific Integrated Circuit

ASIC Full Custom

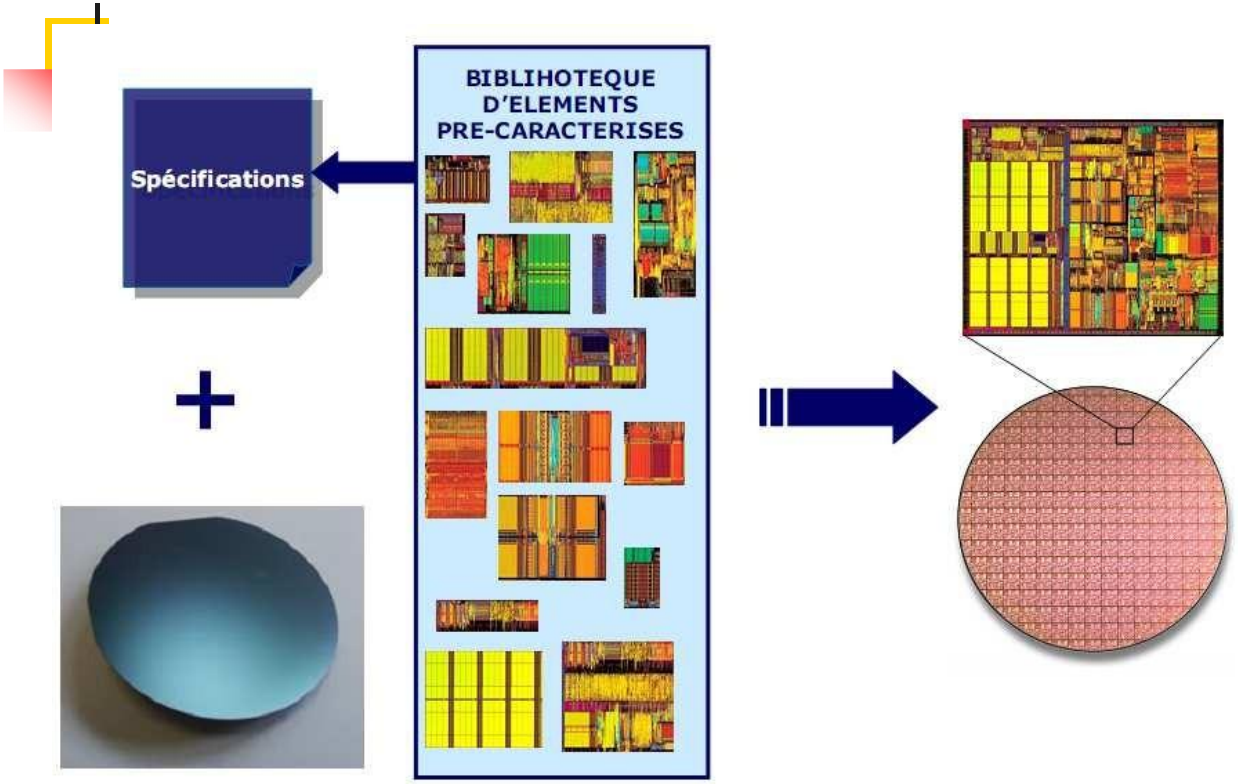


ASIC 标准单元

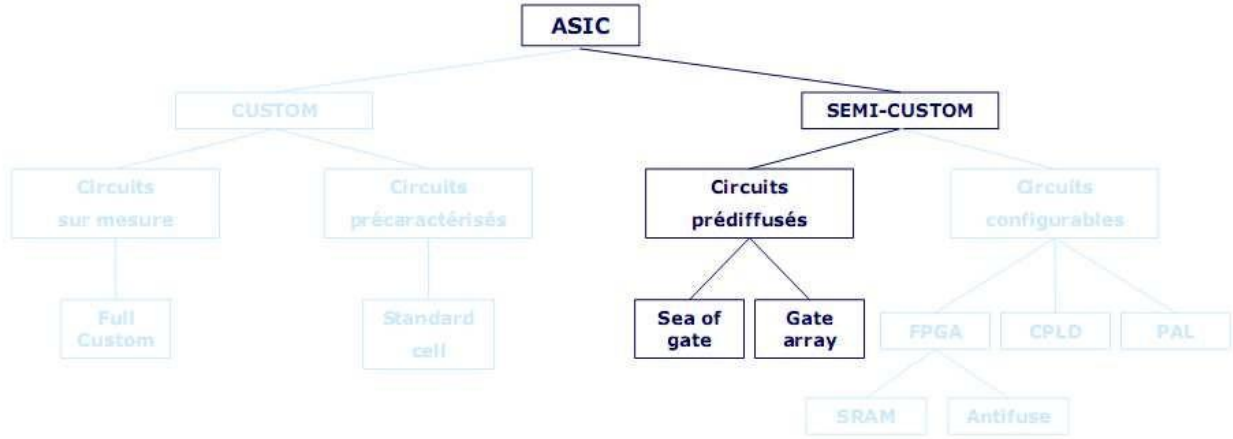


ASIC : Application Specific Integrated Circuit

ASIC标准单元

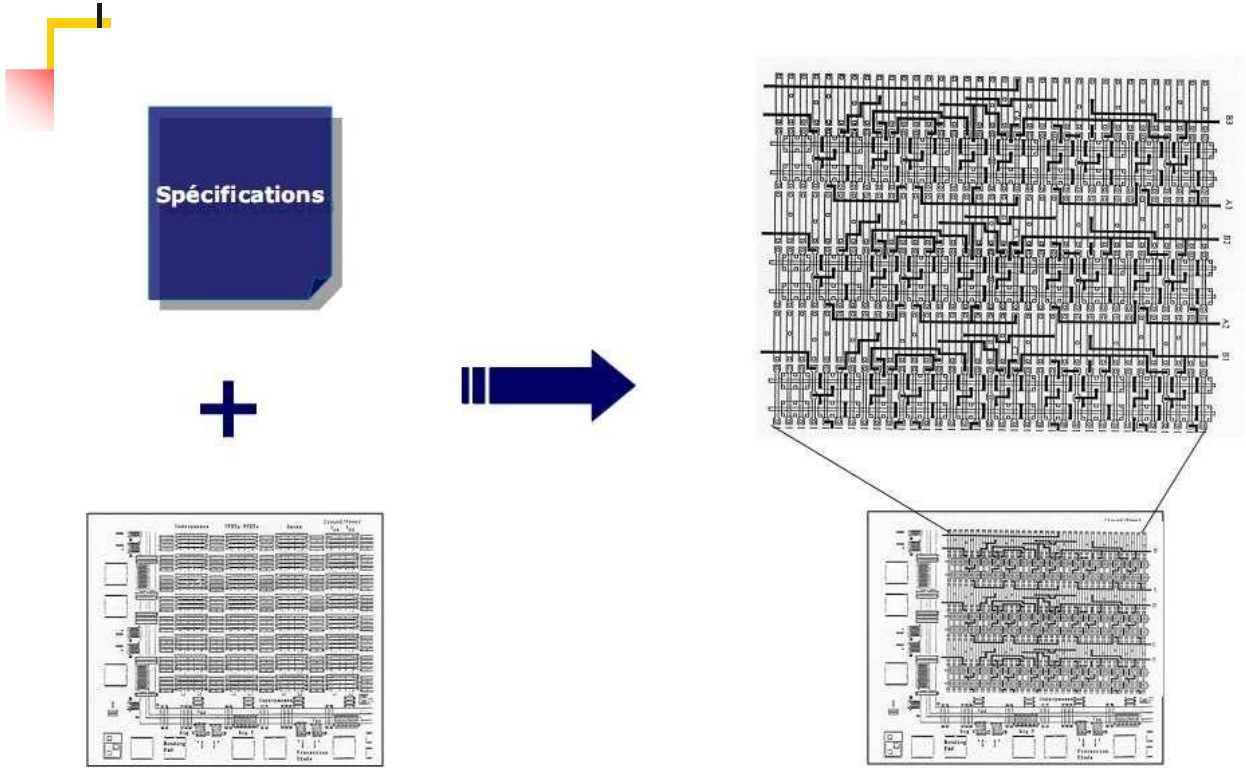

Spécifications
BIBLIHOTEQUE
D'ELEMENTS
PRE-CARACTERISES

ASIC 门阵列

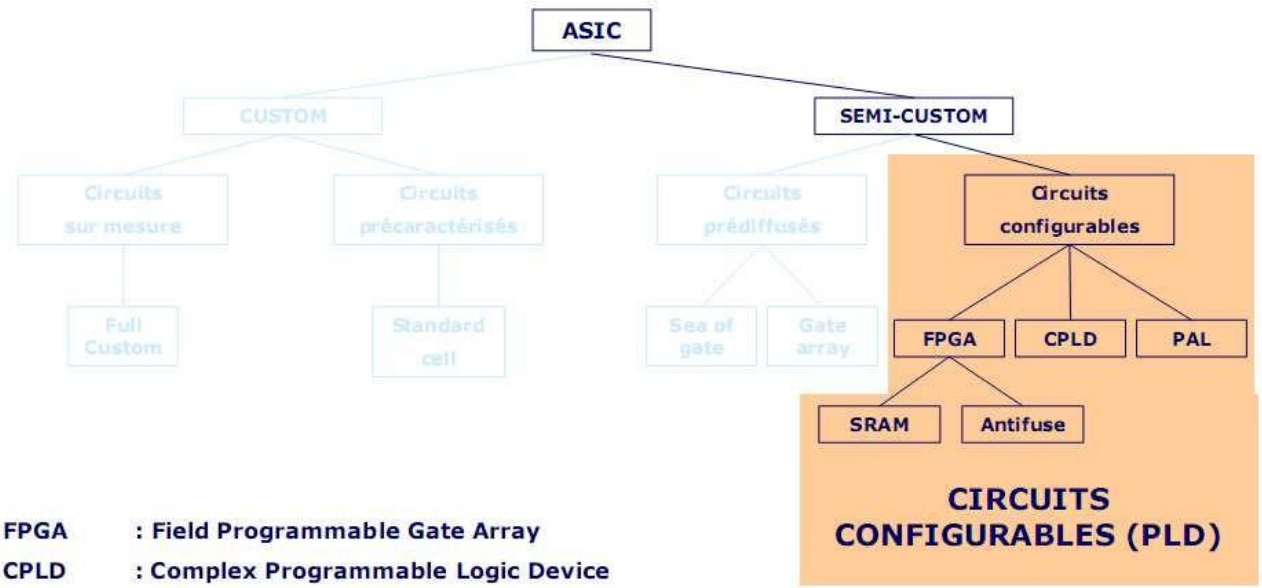


ASIC : Application Specific Integrated Circuit

ASIC门阵列



可配置电路



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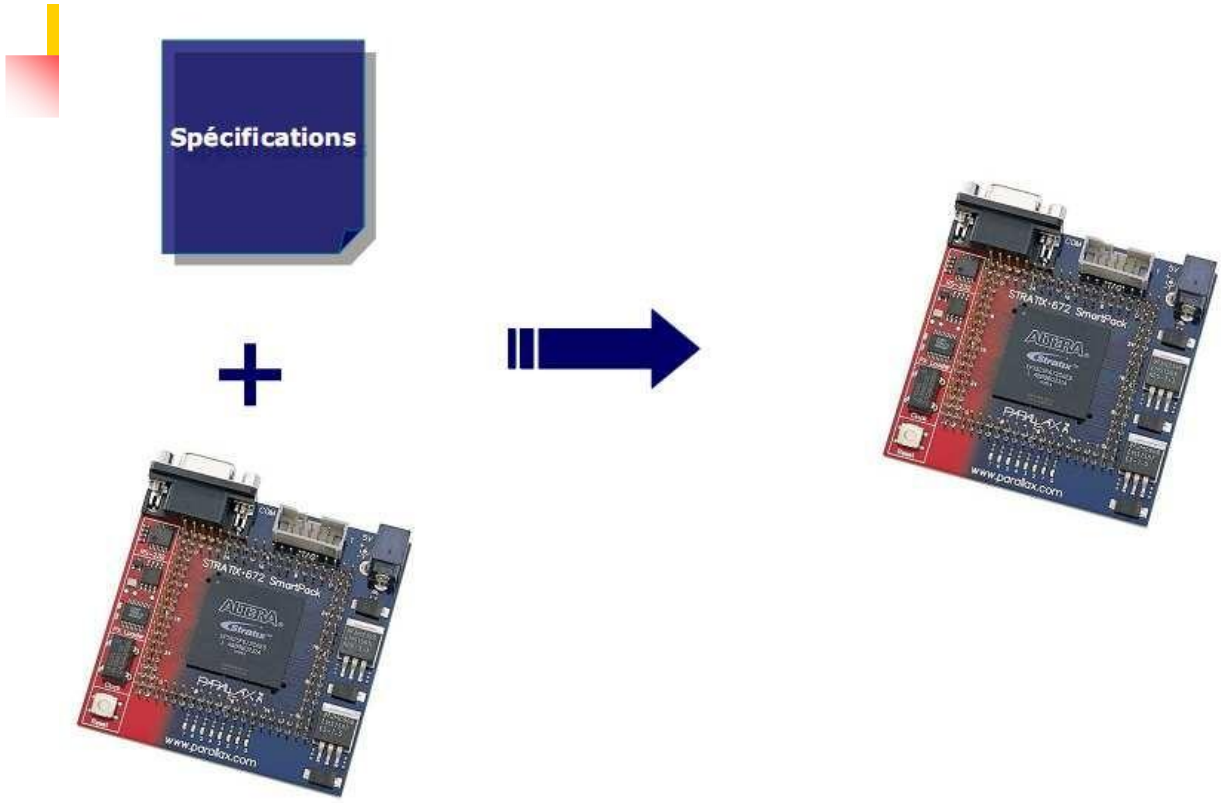
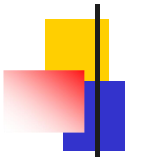
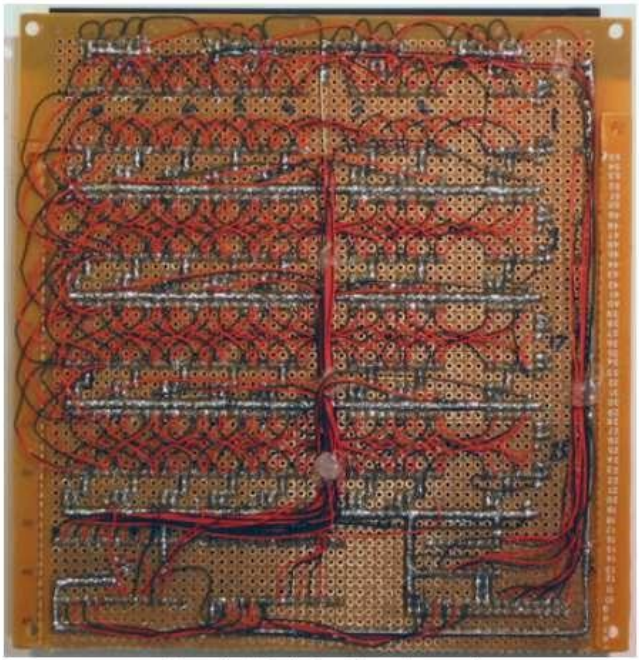
可配置电路

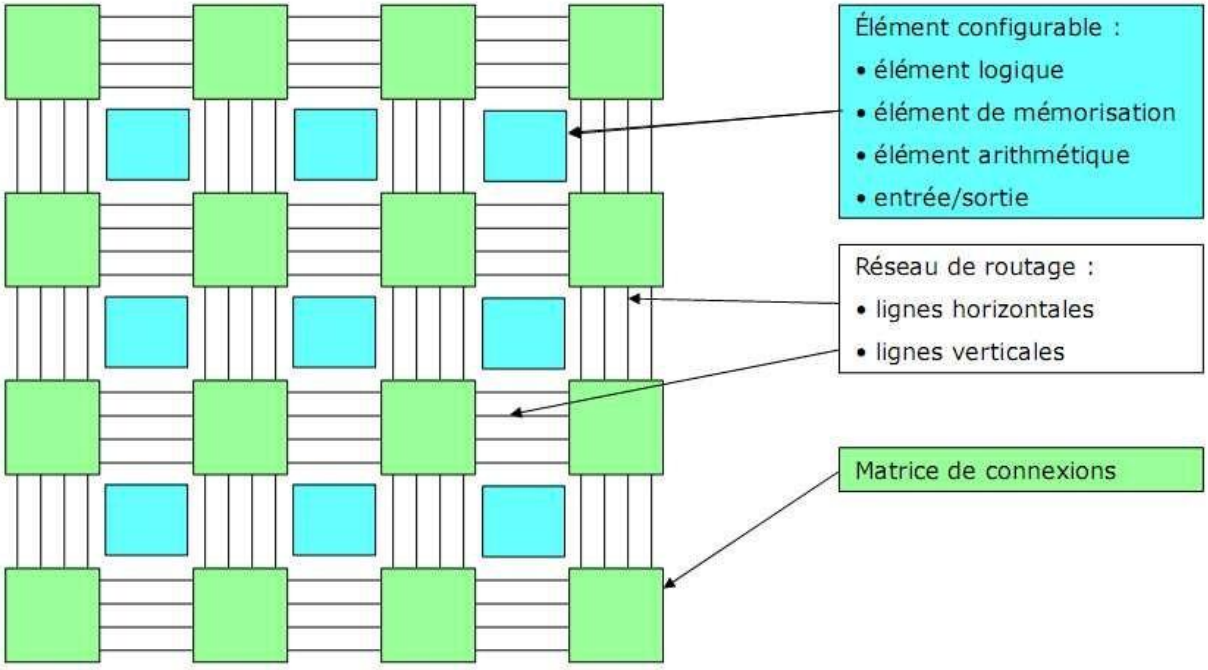

Spécifications
STRATIX-672 SmartPack
ALTERA
Stratix
PARALAX
www.parallax.com



FPGA：设计!

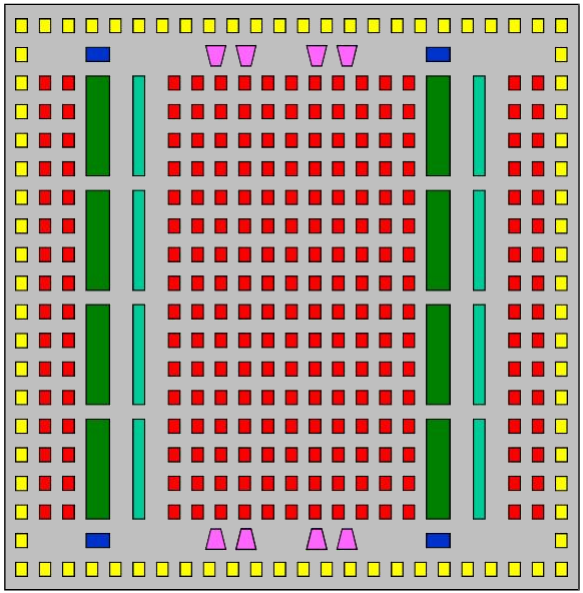


FPGA


Élément configurable :
• élément logique
• élément de mémorisation
• élément arithmétique
• entrée/sortie
Réseau de routage :
• lignes horizontales
• lignes verticales
Matrice de connexions

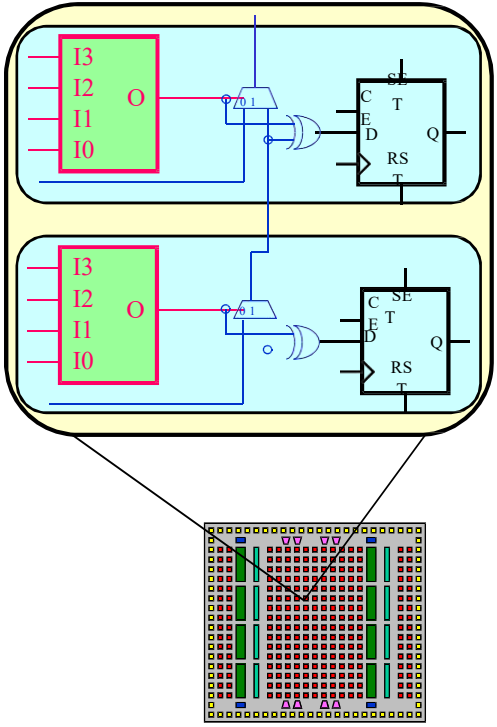
FPGA 结构

- Logic Fabric
  - Gates and flip-flops
- Embedded Blocks
  - Memory
  - DSP/Multipliers
  - Clock management (PLL)
  - High speed serial I/O
  - Soft/hard processors
- Programmable I/Os
- In-system programmable

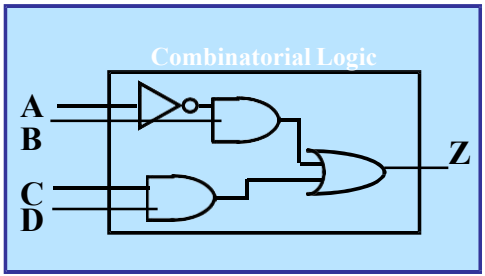


逻辑结构

- Logic Cell (Xilinx) / Logic Element (Altera)
  - 查找表Lookup table (LUT)
  - 触发器Flip-Flop
  - 进位逻辑Carry logic
  - 数据选择器 (not shown)
- Slice
  - Two Logic Cells/Element



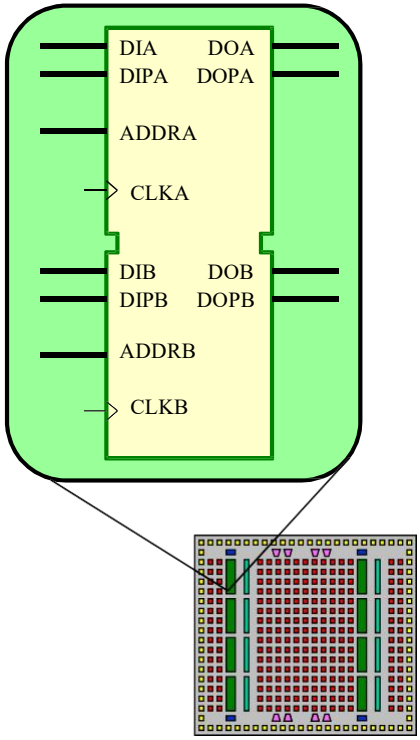
查找表Look-Up Table (LUTs)



A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
	.	.	.	
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

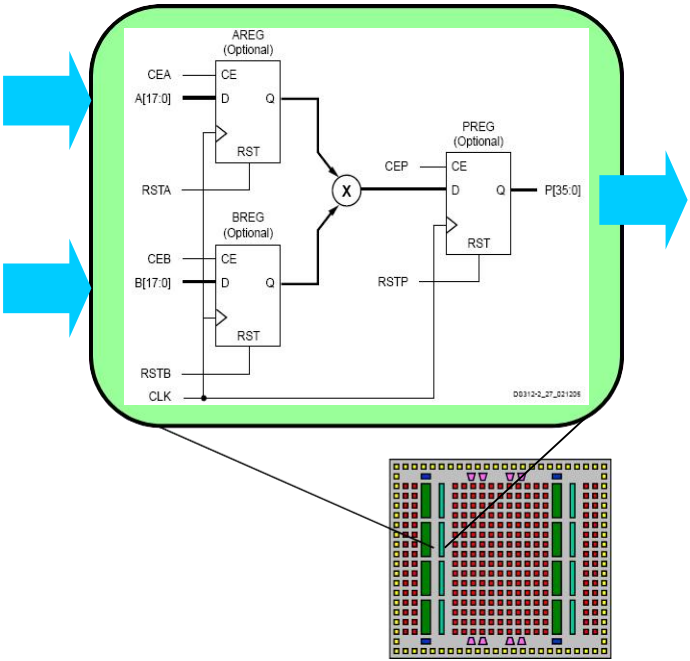
存储块
Blocs Memory

- **Block RAM**
  - RAM or ROM
  - True dual port
    - Separate read and write ports
  - Independent port size
    - Data width translation
  - Excellent for FIFOs



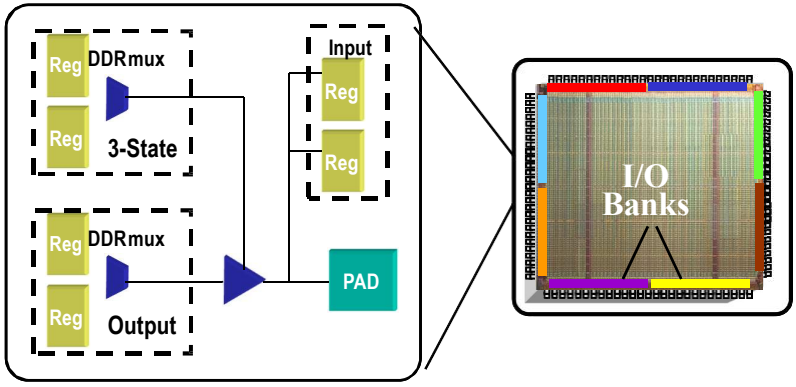
乘法器
Multipliers

- **Multipliers**
  - Signed or unsigned
  - Optional pipeline stage
  - Cascadable



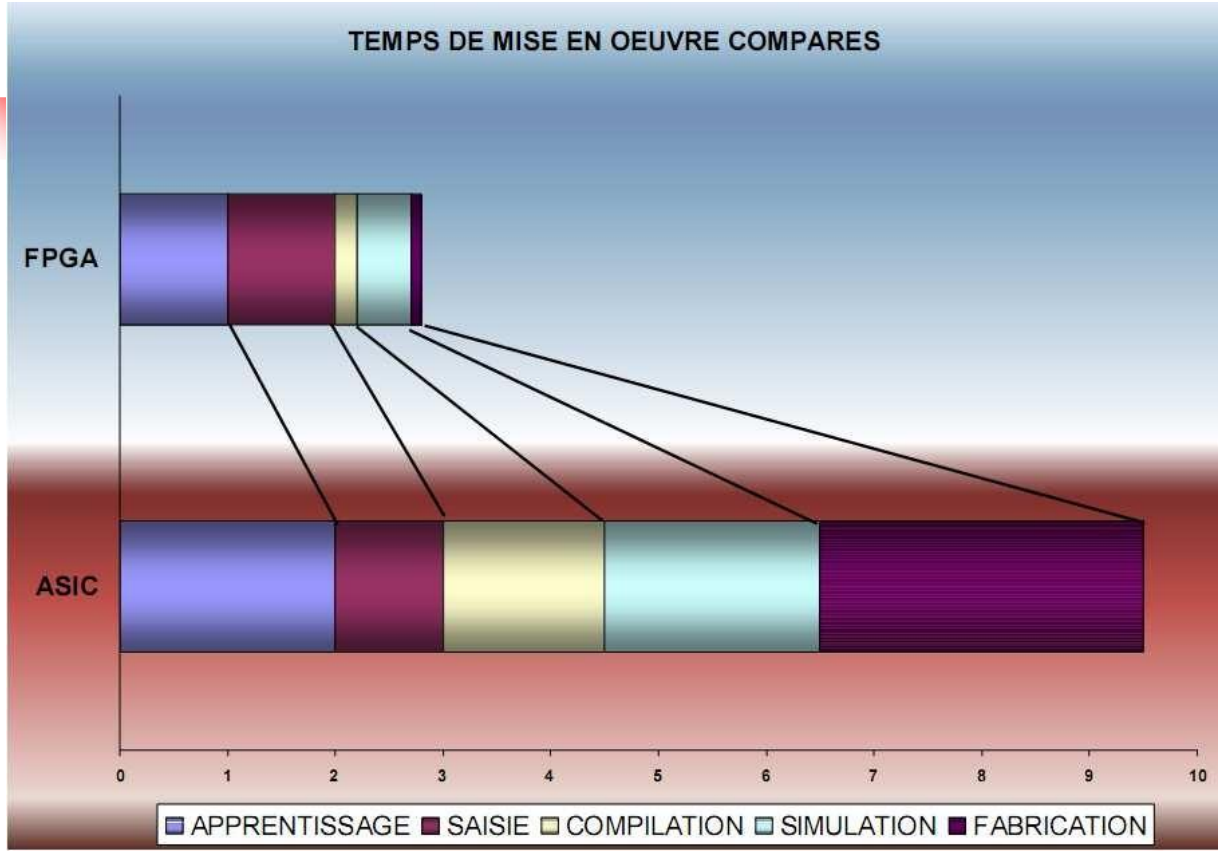
可编程Programmable I/Os

- Single ended
- Differential / LVDS
- Programmable I/O standards
  - Multiple I/O banks



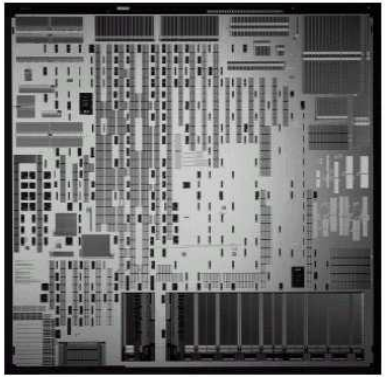
	Standard	Output V_{CCO}	Input V_{REF}
Single ended	LVTTL	3.3V	--
	LVCMOS33	3.3V	--
	LVCMOS25	2.5V	--
	LVCMOS18	1.8V	--
	LVCMOS15	1.5V	--
	LVCMOS12	1.2V	--
	PCI 32/64 bit 33MHz	3.3V	--
	SSTL2 Class I	2.5V	1.25V
	SSTL2 Class II	2.5V	1.25V
	SSTL18 Class I	1.8V	0.9V
	HSTL Class I	1.5V	0.75V
	HSTL Class III	1.5V	0.9V
	HSTL18 Class I	1.8V	0.9V
	HSTL18 Class II	1.8V	0.9V
	HSTL18 Class III	1.8V	1.1V
	GTL	--	0.8V
	GTL+	--	1.0V
Differential	LVDS2.5	2.5V	--
	Bus LVDS2.5	2.5V	--
	Ultra LVDS2.5	2.5V	--
	LVDS_ext2.5	2.5V	--
	RSDS	2.5V	--
	LDT2.5	2.5V	--

设计周期的持续时间

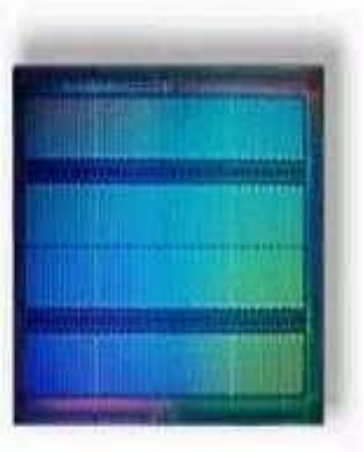

TEMPS DE MISE EN OEUVRE COMPARES
FPGA
ASIC
0
1
2
3
4
5
6
7
8
9
10
APPRENTISSAGE
SAISIE
COMPILATION
SIMULATION
FABRICATION

专用集成电路
ASIC

- 优点
  - 高集成度
  - 高性能（速度，低功 耗）
  - 批量生产成本低
  - 定制化
  - 工业安全
- 缺点
  - 第一份副本的价格
  - 没有可能的错误
  - 不灵活
  - 上市时间长
  - 专为专家（创始人）制造



可编程门阵列
FPGA



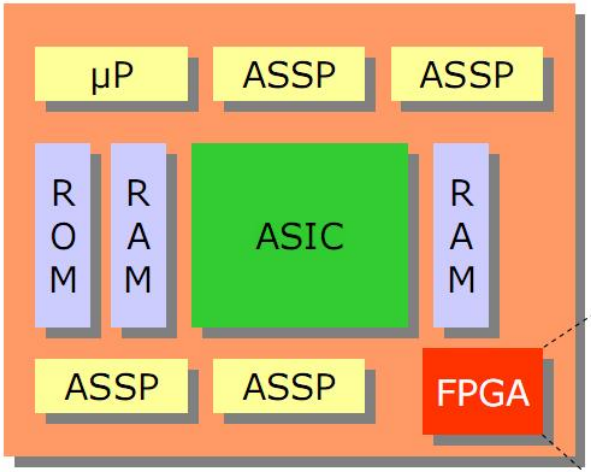
- 优点
  - 原型制作的可能性
  - 上市时间短
  - 适应未来发展重构
  - 柔韧性
- 缺点
  - 集成受到路径资源的限制
  - 性能
  - 大量生产的单价高

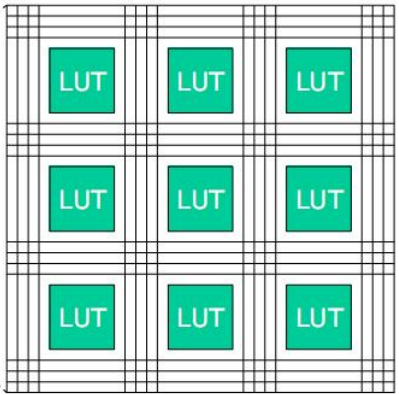
设计方法的演变

- 总是更多集成(SoC)
- FPGA越来越高效，越来越便宜，因此越来越多地被使用
- FPGA正在慢慢取代ASIC电路.
- 示例...

1990：FPGA = 简单的逻辑堆叠

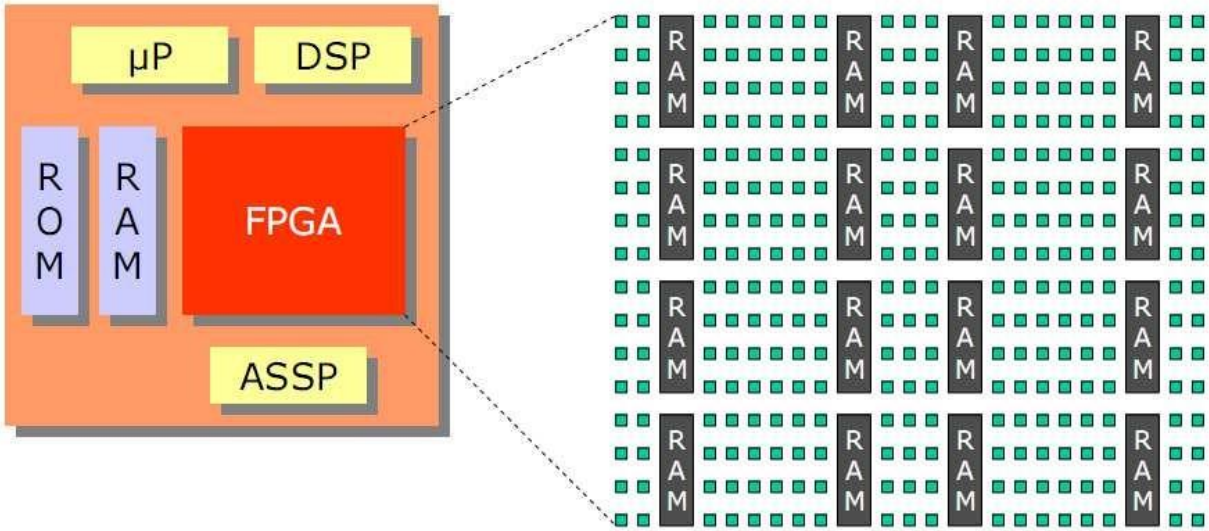
- ASIC : Application Specific Integrated Circuit
- ASSP : Application Specific Standard Product
- FPGA : Field Programmable Gate Array
- RAM : Random Acess Memory
- ROM: Read Only Memory



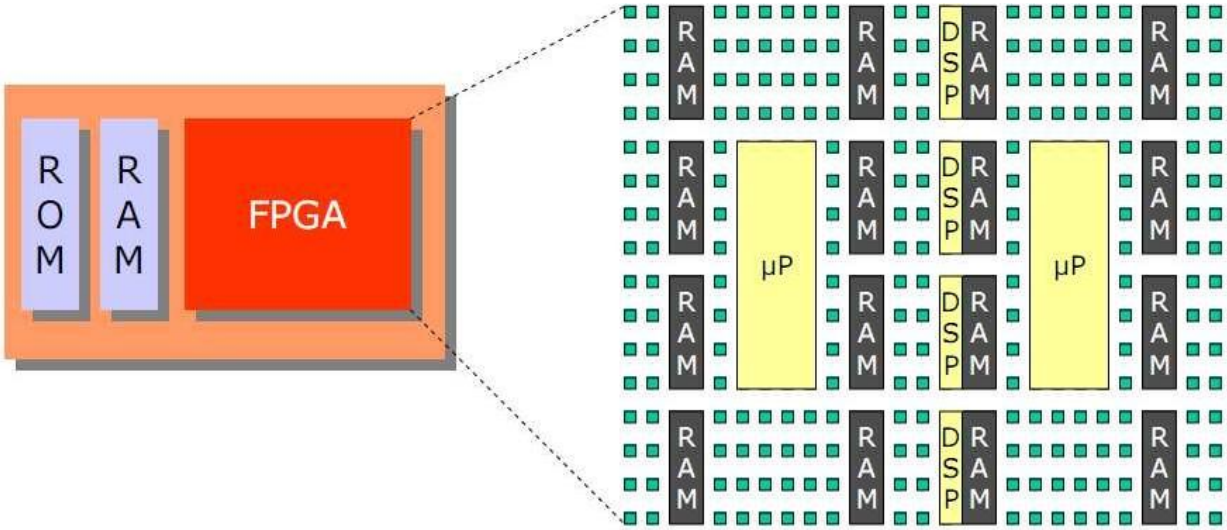


2000：FPGA = ASIC的替代品

(扩展容量)



自2005年以来：FPGA+处理器内核

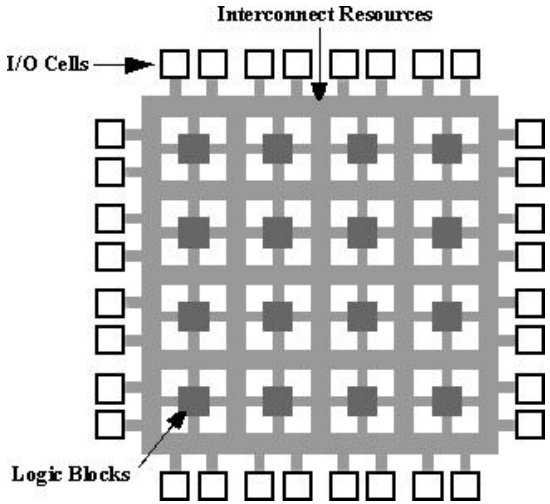


关于硬件目标的结论

- 优点Avantages
  - 高性能：功耗和工作频率
  - 并行，流水线……
  - 实时处理的可能性
  - 应用电路专用化
  - 具有灵活组件的可能性: FPGA
  - Choix large de techno, boitier, gamme …
- 缺点Inconvénients
  - 相对复杂和长期的设计
  - 设计成本可能很高(ASIC et FPGA de taille importante)
  - 需要严格的设计方法
  - 需要更多专业知识

FPGA主要厂商

- **Xilinx**
- **Altera**
- Lattice Semiconductor
- Actel (microsemi)
- Cypress
- Atmel
- QuickLogic



区别μC 和 FPGA

- μC微处理器（单片机）：
  - 顺序执行程序的指令。
- FPGA：
  - 系统的硬件描述。
  - FPGA可以包含一个或多个μC或μP，这称为SoC或SoPC。

什么是IP?

- IP (知识产权)
  - 虚拟组建
  - HDL语言描述的功能
- 供应商Vendeur d'IPs :
  - ARM
  - www.design-reuse.com
- Ips开源 open source :
  - www.opencores.org

VHDL WWW

- VHDL sur Internet
  - http://vhdl33.free.fr/
  - https://www.doulos.com/knowhow/vhdl_designers_guide/
  - http://www.opencores.org/
    - Composants RTL open source (IPs)
  - http://www.freemodelfoundry.com/
    - Composants behaviour (modélisation) pour la simulation.