C5 – Fichiers et Librairies

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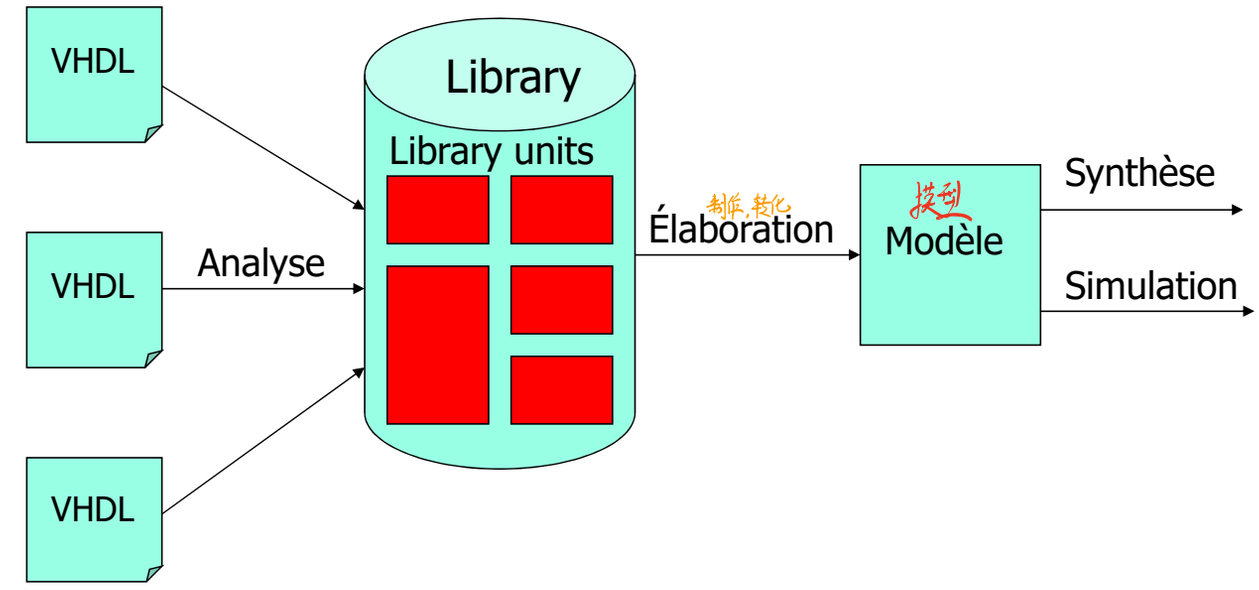
VHDL

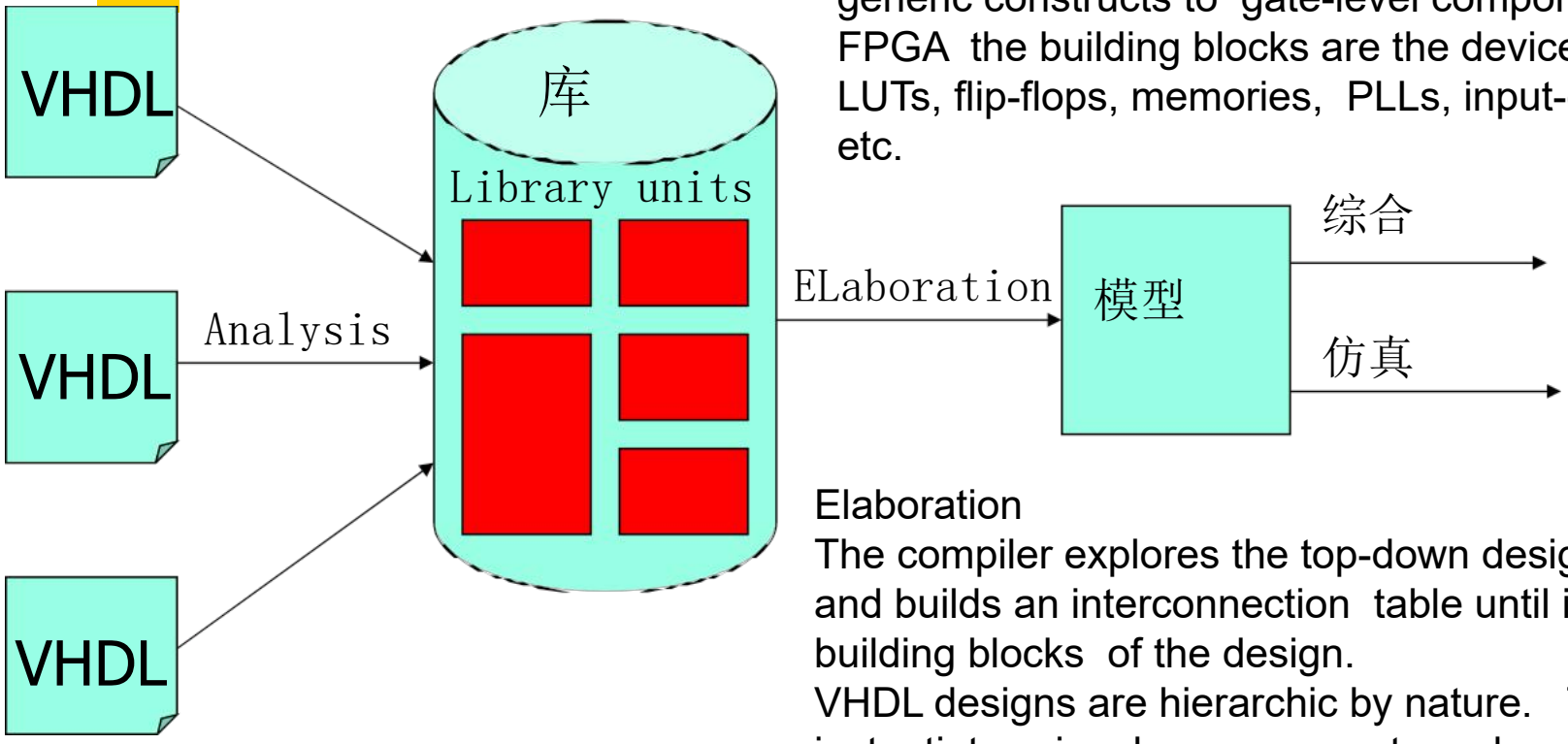
Compilation

Fichiers VHDL contenant
des « design units »



编译

包含“设计单元”的VHDL文件



Analysis

Analysis is the process where the design files are checked for syntactic and semantic errors. The syntactic rules are dictated by the language.

Synthesis

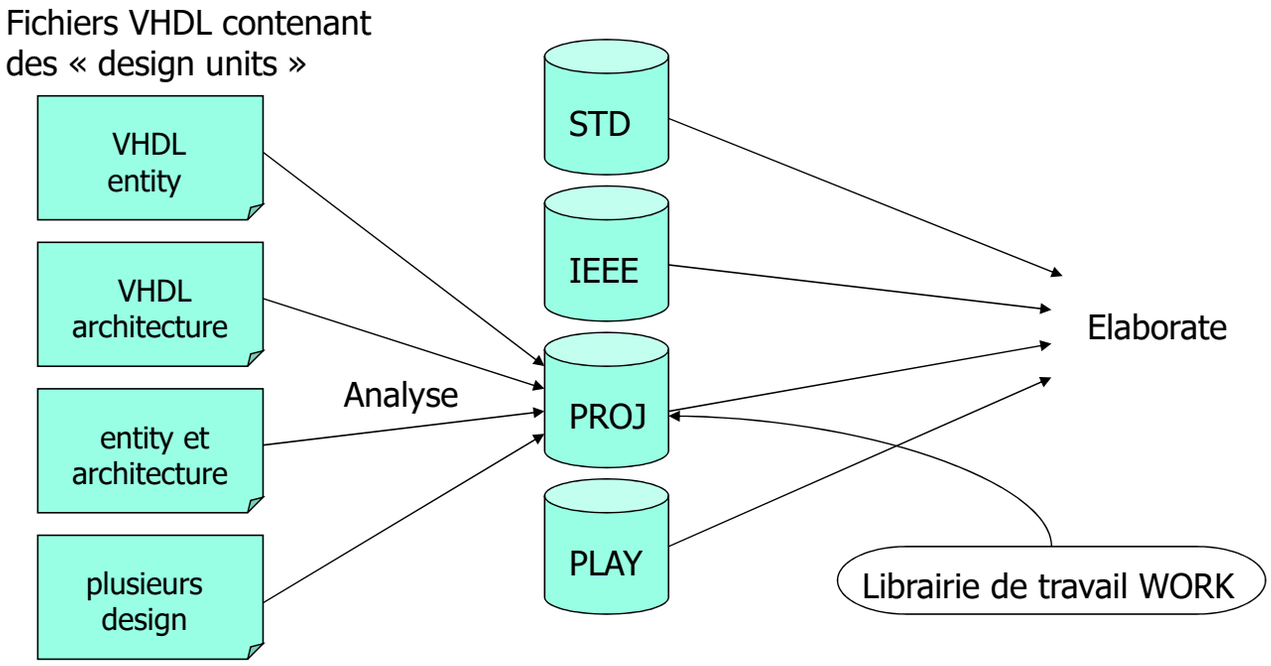
During Synthesis, the design is mapped from RTL generic constructs to gate-level components. On an FPGA the building blocks are the device primitives: LUTs, flip-flops, memories, PLLs, input-output pins, etc.

Elaboration

The compiler explores the top-down design hierarchy and builds an interconnection table until it reaches the building blocks of the design.

VHDL designs are hierarchic by nature. The top entity instantiates signals, components and processes. Each component instantiates additional signals, components and processes. At this step the building blocks are still generic RTL constructs: Logic gates, registers, memories, etc.

Librairie de travail



La clause de contexte

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity TEST_BENCH1 is
end entity;

architecture TB of TEST_BENCH1 is
  ...
end architecture;

library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity ENTITY2 is
  port( ... );
end entity;

architecture RTL of ENTITY2 is
  ...
end architecture;
```

Entité vide => la clause de contexte se reporte devant l'architecture

Chaque entité/ package/ configuration nécessite une clause de contexte

Clause de contexte implicite

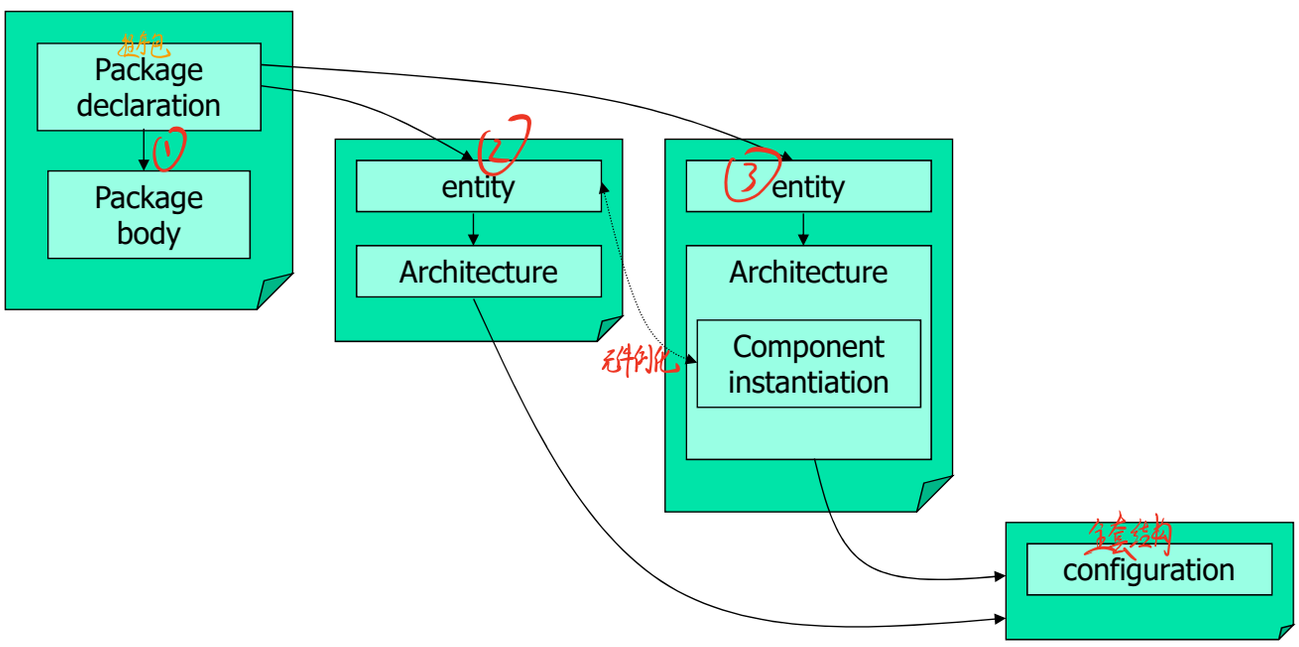
```
library STD, WORK;
use STD.STANDARD.all;
```

Inclut par défaut

```
INTEGER   0  1  99
BIT       '0'  '1'
BOOLEAN   FALSE  TRUE
STRING    "Hello World"
TIME      10 NS
```

Types du package STD.STANDARD

Ordre de la compilation



Style Recommandé

VHDL 93

Indentation

Instanciation directe

```
architecture BENCH of NOR2_TB is


  signal A, B, F: STD_LOGIC;

begin
  stimulus: process is
  begin
    A <= '0';
    B <= '0';
    wait for 10 NS;
    B <= '1';
    wait;
  end process stimulus;

  UUT: entity work.NOR2 port map (
        A => A,
        B => B,
        F => F);

end architecture BENCH;
```

Alignement

Des espaces

Des labels compréhensibles

Association par nom

Noms des labels

Identifiant = lettres, nombres et underscores

```
G4X6     Gate_45     \extended!"£$%^&*()\
TheState      The_State
```

Noms différents

La casse est ignorée pour les identifiants

```
INPUT    Input    input
```

mêmes noms

Beaucoup d'identifiant son des mots réservés

```
And   buffer   bus   function   register   select
```

Identifiants illegaux ...

```
4plus4   A$1   V-3   The__State   _State_
```

Double underscore