Lab 4: FPGA-DE2 實作練習

1. 實驗目的

   本次實驗是藉由 VerilogHDL，設計一燈號顯示器並且熟悉 DE2 的操作方法

2. 實驗器材

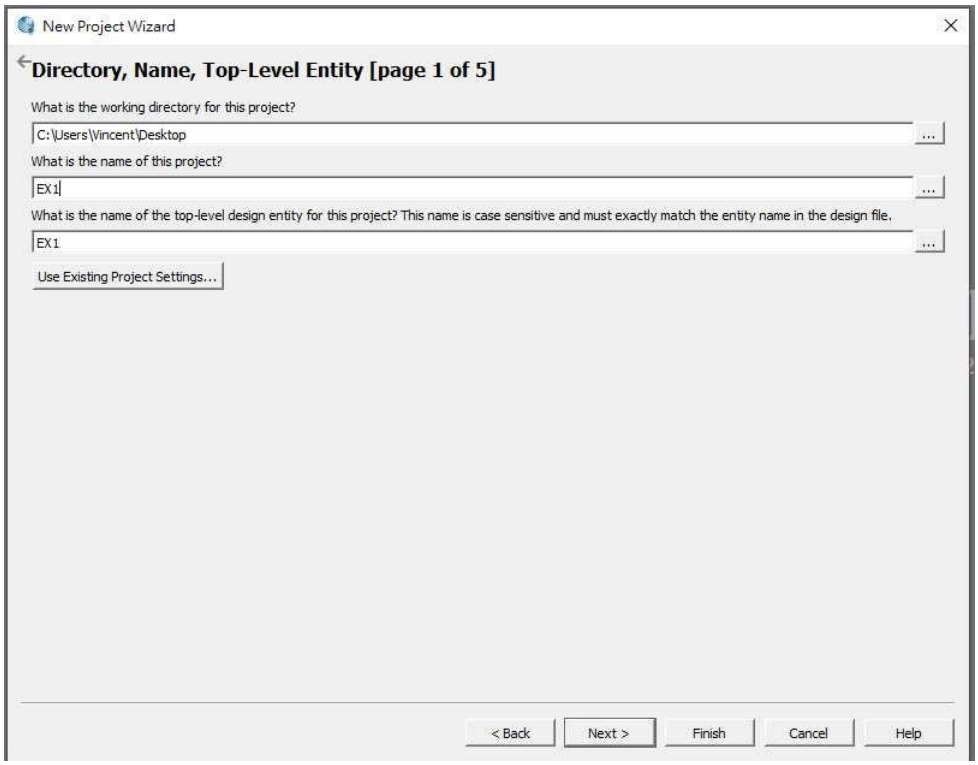
   Quartus Ⅱ (CAD tools)、DE2

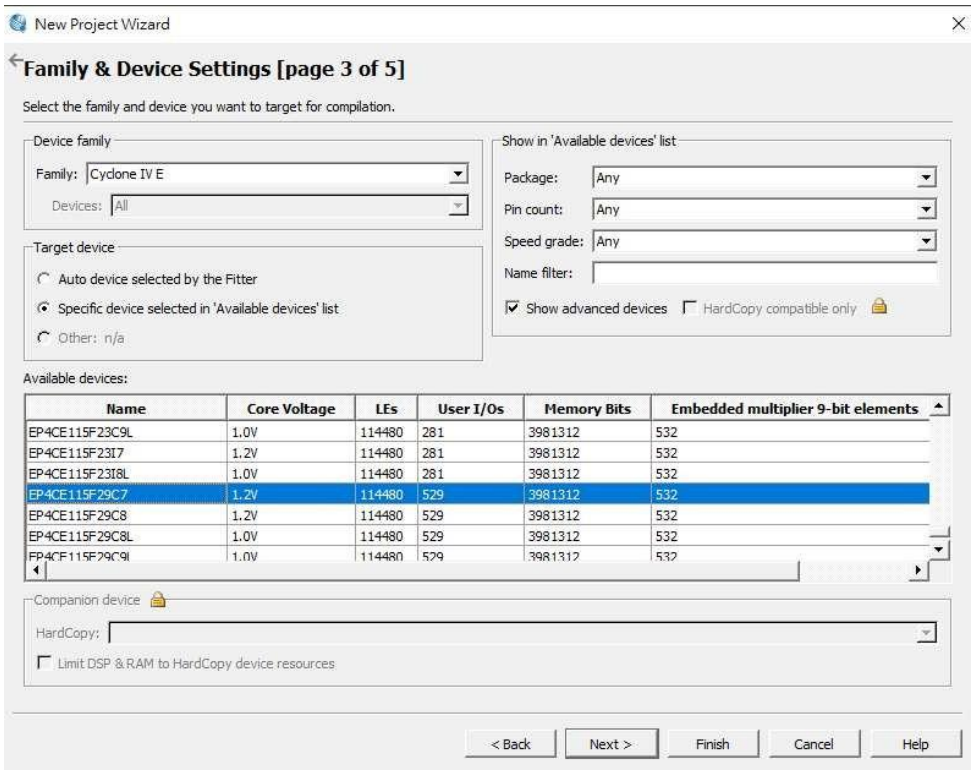
3. 實驗內容

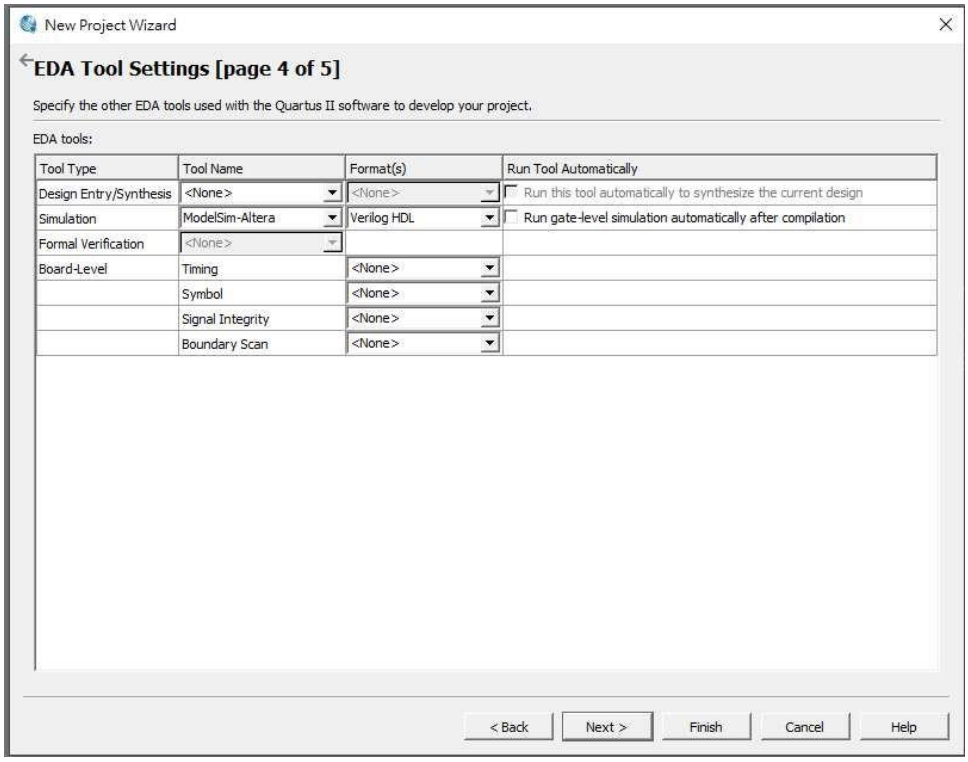
   請使用 Verilog HDL 描寫出：簡易邏輯電路，再利用 DE2 實驗板上的 FPGA 晶片 CycloneIV 系列 EP4CE115F29C7N，將其指撥開關作為輸入，並將結果輸出LED 加以驗證結果。(以下圖例皆以 CycloneIV 系列為例)

4. 實驗步驟

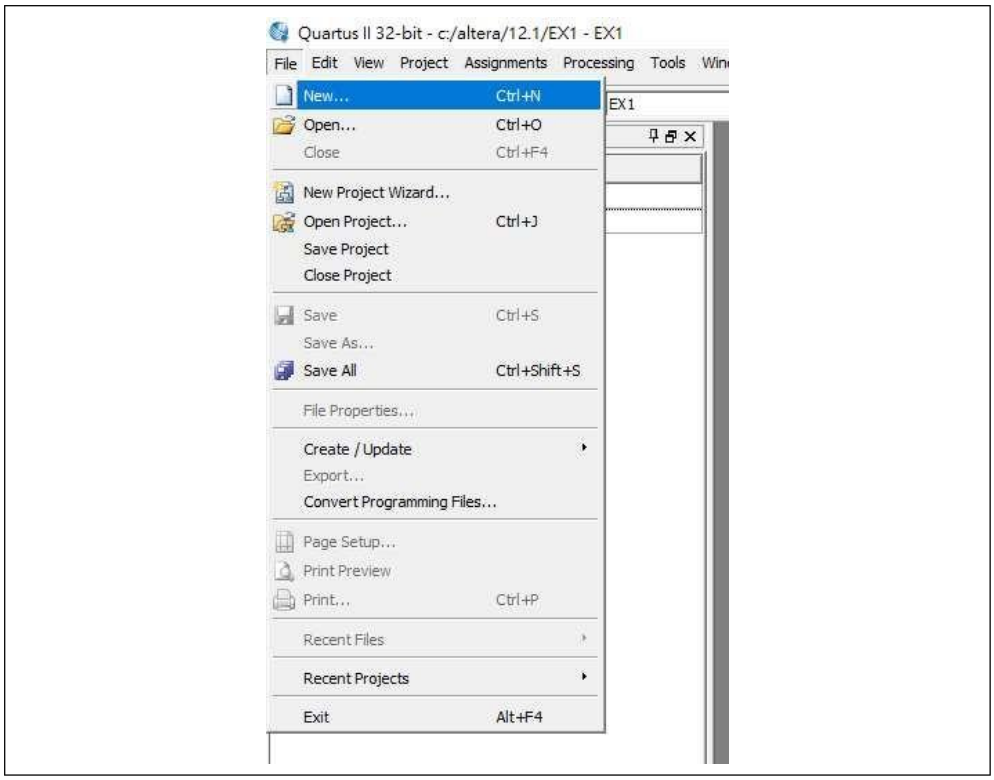
   A. 開啟Quartus II 12.1 sp1(64-bit)並選擇Create a New Project，Project Name 請輸入本次實驗的名稱，此次為Lab3。

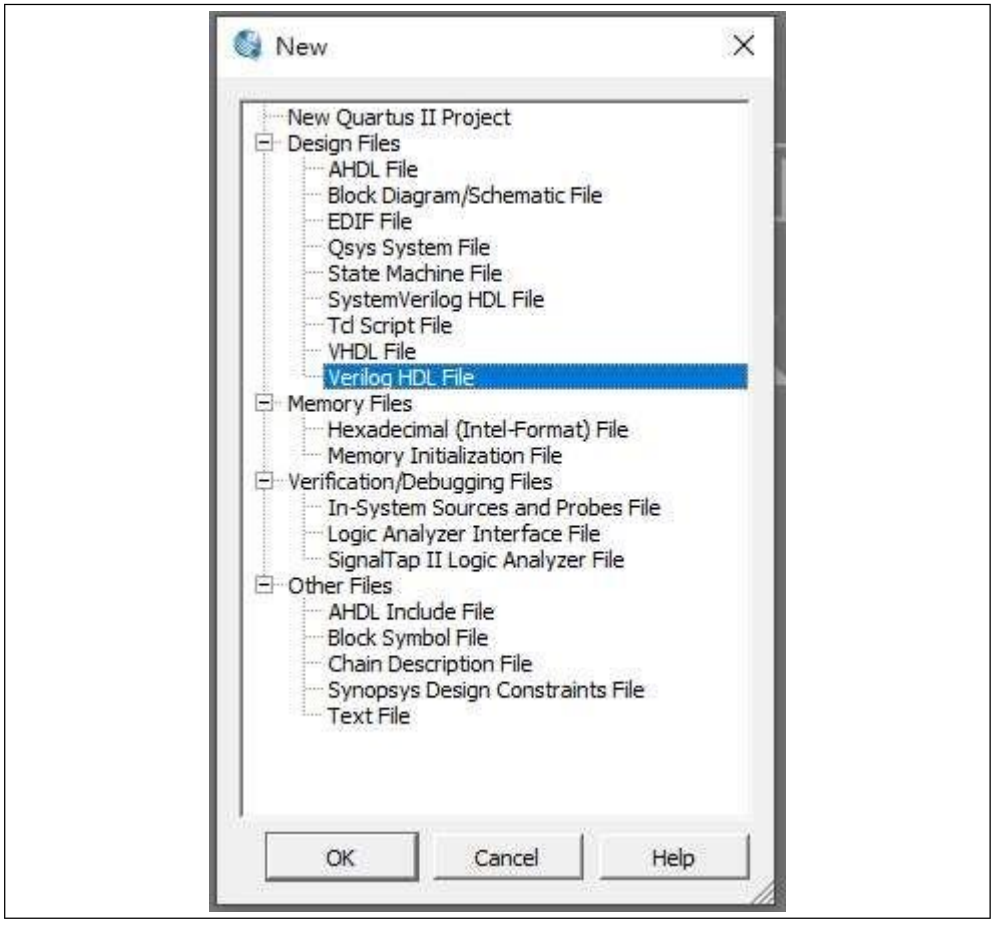



New Project Wizard
Family & Device Settings [page 3 of 5]
Select the family and device you want to target for compilation.
Device family
Family: Cyclone IV E
Devices: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any
Name filter:
Show advanced devices
HardCopy compatible only
Available devices:
Name | Core Voltage | LEs | User I/Os | Memory Bits | Embedded multiplier 9-bit elements
EP4CE115F23C9L | 1.0V | 114480 | 281 | 3981312 | 532
EP4CE115F23I7 | 1.2V | 114480 | 281 | 3981312 | 532
EP4CE115F23I8L | 1.0V | 114480 | 281 | 3981312 | 532
EP4CE115F29C7 | 1.2V | 114480 | 529 | 3981312 | 532
EP4CE115F29C8 | 1.2V | 114480 | 529 | 3981312 | 532
EP4CE115F29C8L | 1.0V | 114480 | 529 | 3981312 | 532
Companion device
HardCopy:
Limit DSP & RAM to HardCopy device resources
< Back
Next >
Finish
Cancel
Help


New Project Wizard
EDA Tool Settings [page 4 of 5]
Specify the other EDA tools used with the Quartus II software to develop your project.
EDA tools:
Tool Type | Tool Name | Format(s) | Run Tool Automatically
Design Entry/Synthesis | <None> | <None> | Run this tool automatically to synthesize the current design
Simulation | ModelSim-Altera | Verilog HDL | Run gate-level simulation automatically after compilation
Formal Verification | <None>
Board-Level | Timing | <None>
Symbol | <None>
Signal Integrity | <None>
Boundary Scan | <None>
< Back
Next >
Finish
Cancel
Help

B. 建立新的文件


Quartus II 32-bit - c:/altera/12.1/EX1 - EX1
File Edit View Project Assignments Processing Tools
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4
EX1

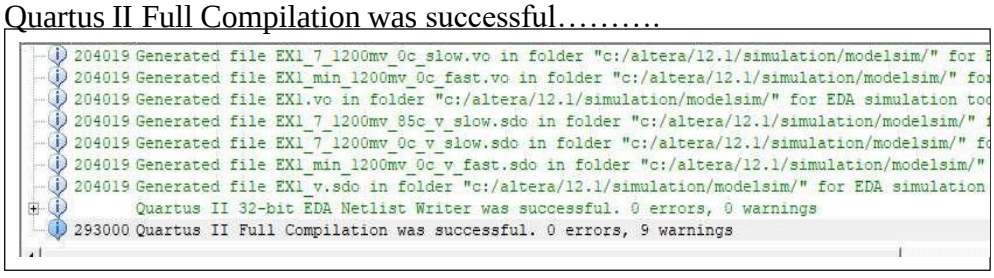

New
New Quartus II Project
Design Files
AHDL File
Block Diagram/Schematic File
EDIF File
Qsys System File
State Machine File
SystemVerilog HDL File
Tcl Script File
VHDL File
Verilog HDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and Probes File
Logic Analyzer Interface File
SignalTap II Logic Analyzer File
Other Files
AHDL Include File
Block Symbol File
Chain Description File
Synopsys Design Constraints File
Text File
OK
Cancel
Help

C. 輸入程式碼

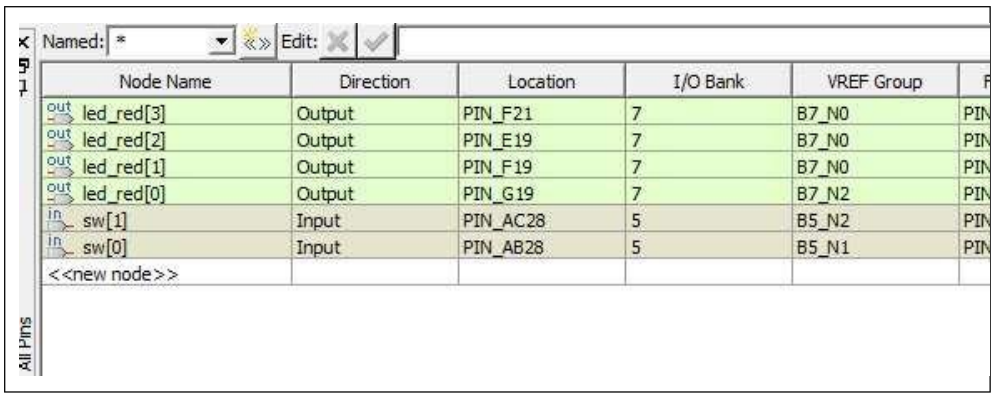
```
module EX1 (sw,led_red);

input[1:0]sw;
output[3:0]led_red;
reg led;

assign led_red[0] = sw[0]?1'b1:1'b0;
assign led_red[1] = sw[1]?1'b1:1'b0;
assign led_red[2] = (sw[0]==sw[1])?1'b1:1'b0;
assign led_red[3] = led;

always@(sw)

begin
    if(sw[0])
        if(sw[1])
            led=1'b1;
        else
            led=1'b0;
    else
        led=1'b0;
end

endmodule
```

D. 編譯 Processing　Start Compilation 等待編譯完成，會顯示如下圖

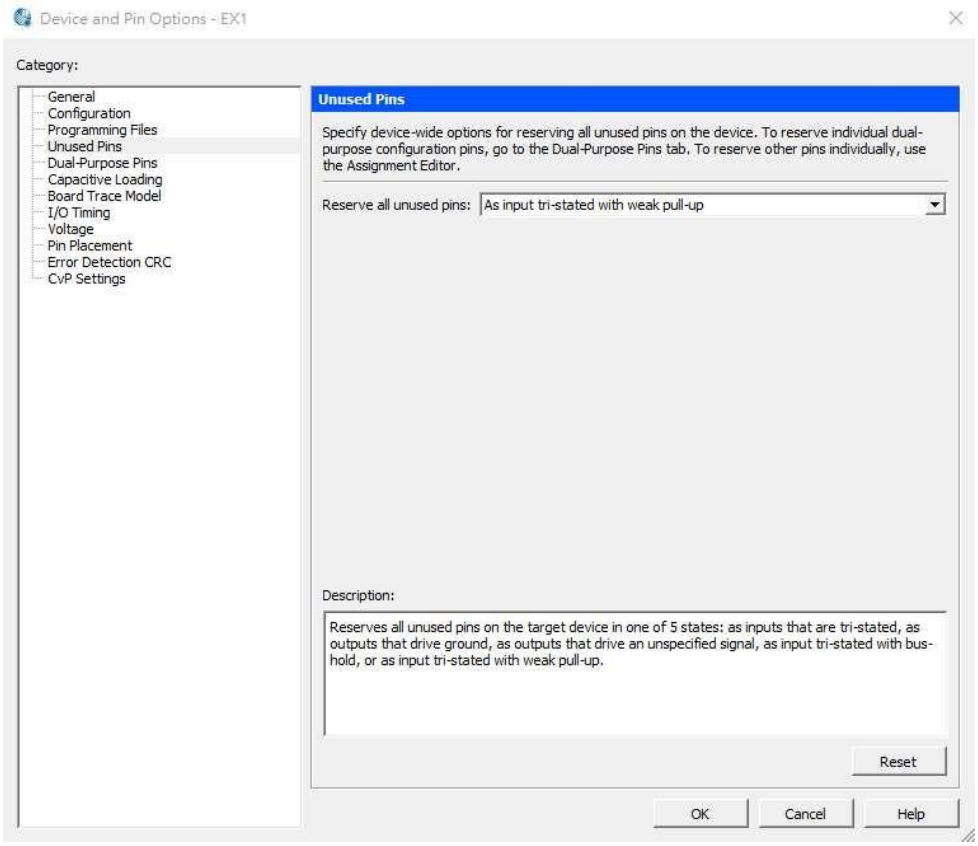
Quartus II Full Compilation was successful…….



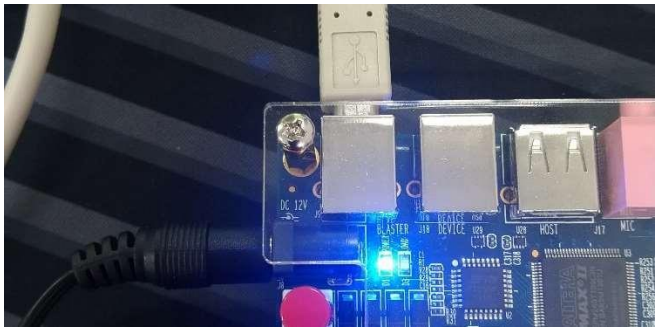
E. 設定PIN 角位 Assignments　　Pin Planner 在Location 處點兩下輸入角位名稱。



在Assignments　　Device…，在Device and Pin Options…選擇如下圖



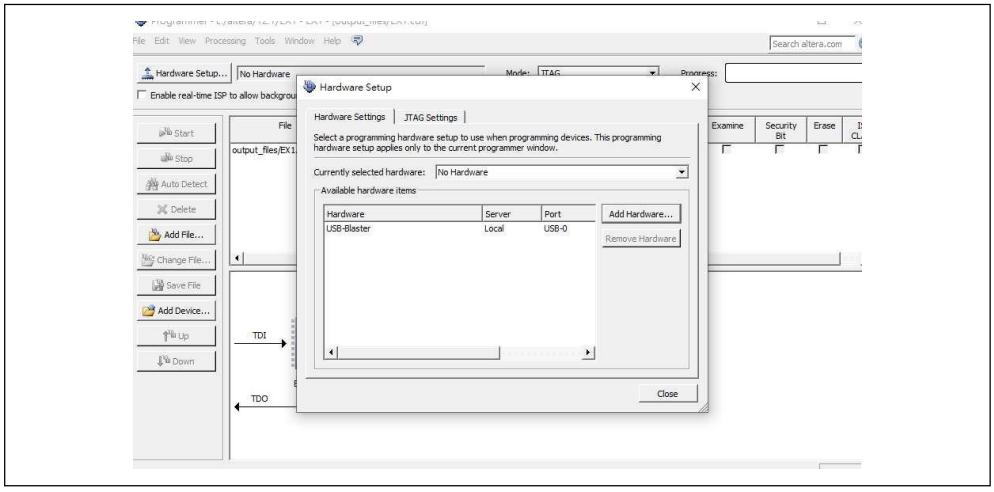
F. 燒錄至FPGA 板子當中，插入USB 孔如下所示



進入裝置管理員

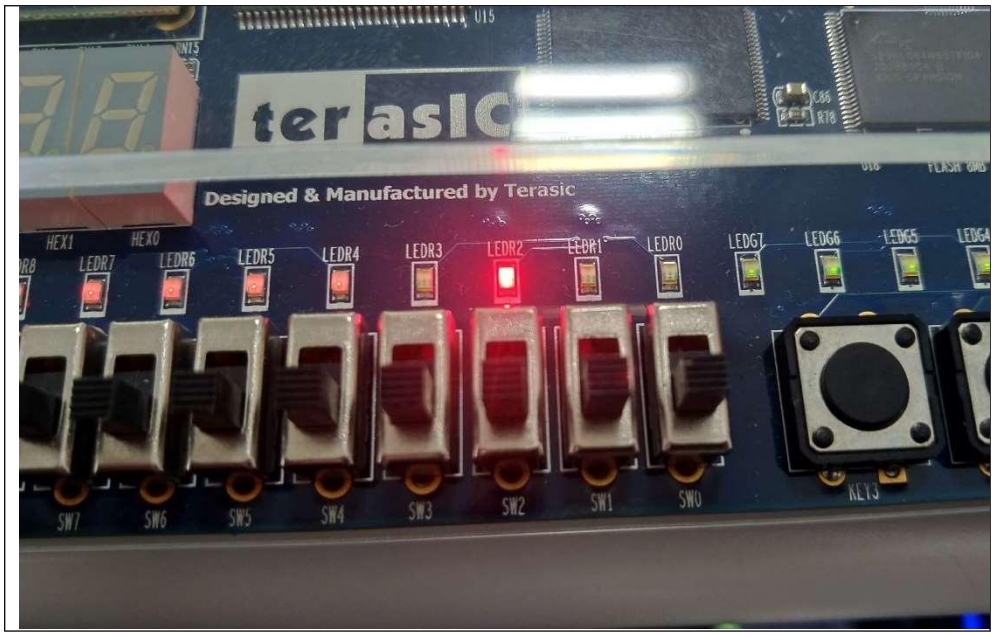
選擇瀏覽驅動程式位置

進入Tools　　Programmers 點選Hardware setup 可以選擇我們剛剛所安裝的DE2 板子

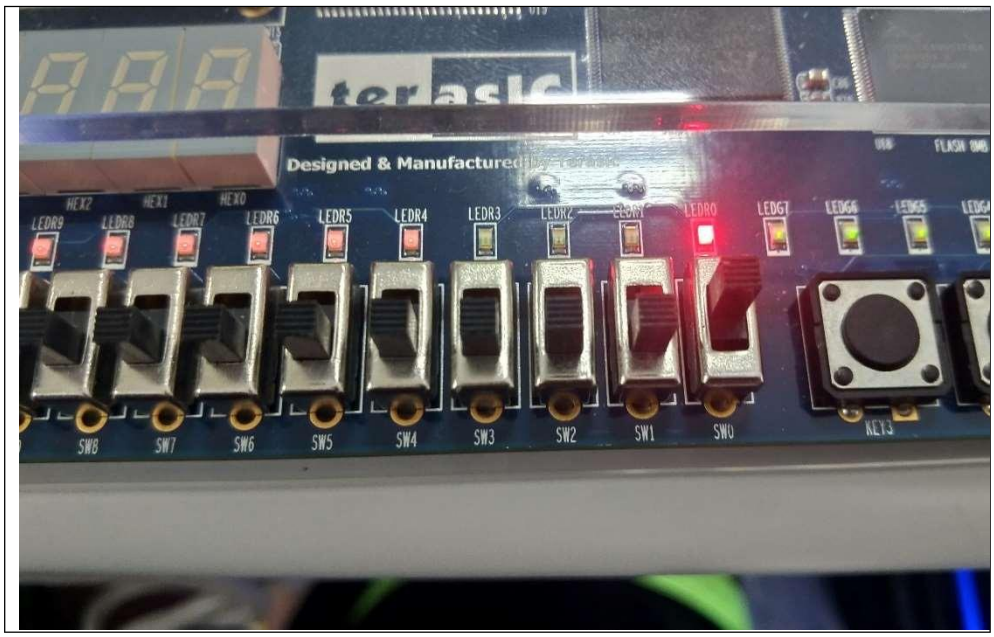


將板子上SW19 撥到run 的位置並點選START 燒入至FPGA 板子。 所得結果應如下：

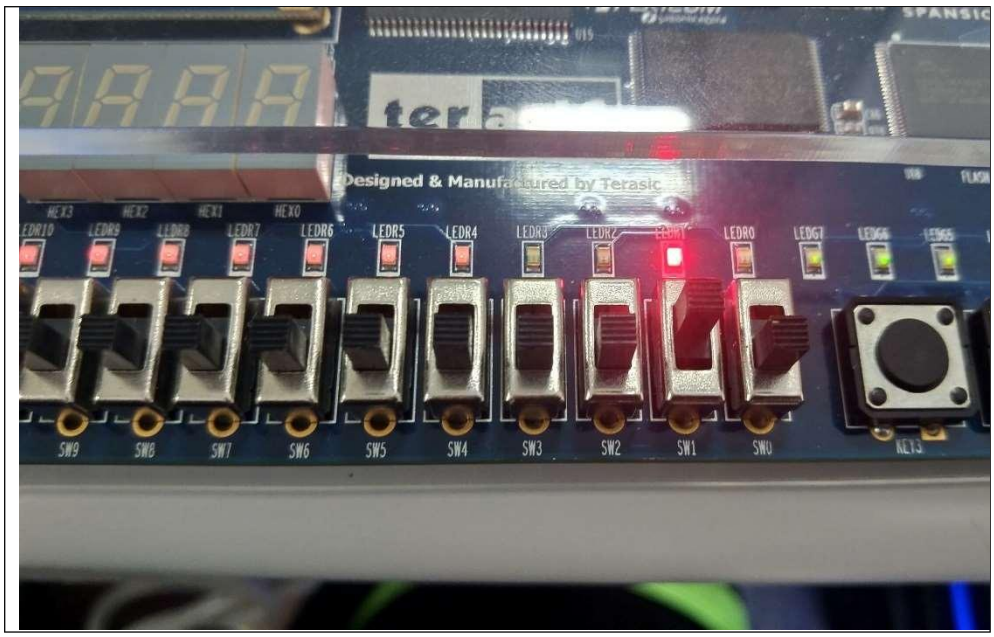
1. sw0 = 0 , sw1 = 0, ledr2 =1



2. sw0 = 1 , sw1 = 0, ledr0 =1



3. sw0 = 0 , sw1 = 1, ledr1 =1



4. sw0 = 1, sw1 = 1, ledr0,1,2,3 =1

5. 本週題目，修改此程式碼使 SW0=0，
SW1=1 時LEDR0 與LEDR2 亮起。 SW0=1，
SW1=0 時LEDR1 與LEDR2 亮起。 SW0=0，
SW1=0 時LEDR1 與LEDR0 亮起。 SW0=1，
SW1=1 時LEDR3 亮起。