Yuean Gu

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Education

University of Chinese Academy of Sciences **Sept. 2019 – Jun. 2023(excepted)**
Electronics and Information Engineering; GPA: 3.87/4.0 *Beijing, China*

University of California, Berkeley **Jan. 2022 – May. 2022**
Electrical Engineering; GPA: 4.0/4.0 *Berkeley, U.S.*

Academic Performance

Overall GPA: 3.87/4.0 Ranking: 4/43 Major GPA: 3.98/4.0
Toefl: 108 (R29, L28, S23, W28)

Research Experience

64baud/s Optical Transmitter Driver Chip Tapeout **Aug. 2022 – Now**
Institute of semiconductors, Chinese Academy of Sciences(CAS), supervised by Prof. Nan Qi *Beijing,China*

- Working on designing a silicon photonic micro-ring based 64baud/s based optical transmitter with 2-tap Feed-Forward Equalization(FFE) and nonlinear equalization in 45nm SOI CMOS.
- Currently focusing on designing Cherry-Hooper structure continuous-time linear equalizer (CTLE) stage and 2-stage variable gain amplifier(VGA). Expected to realize 15dB boost and 12 dB gain within the bandwidth of 35G. Modeled CTLE in Advanced Design System and wrote verilog-A model in Virtuoso to optimize circuit design.
- Expected to tapeout in November.

45RFSOI Mosfet Modeling Down to Cryogenic Temperatures **Mar. 2022 – Aug. 2022**
Berkeley Wireless Research Center, UC Berkeley, supervised by Prof. Vladimir M. Stojanovic *Berkeley, U.S.*

- Evaluated DC characteristics of transistors in the commercial 45nm PD-SOI process down to 2.5K on different types of devices and introduced an effective temperature formulation to capture the effects of the band tail states.
- Extracted key design parameters including threshold voltage, effective mobility and saturation velocity, presented a modified verilog-A compact model within industry-standard Berkeley short-channel IGFET model (BSIM) framework.
- Introduced polynomial functions to replace the original threshold voltage expression in BSIM model, which has discontinuity points at cryogenic temperatures. Modelled id-vd curve and id-vg curve with a wide temperature range and mean absolute percentage error is smaller than 0.1 percent.

High-Speed PCB Design and Layout **July 2021 – Sept. 2021**
State Key Laboratory of semiconductor superlattices, CAS, supervised by Prof. Nan Qi *Beijing, China*

- Designed high-speed evaluation boards for 4×25Gb/s De-Serializer with Baud-Rate Sampling CDR in Altium Designer.
- Signal integrity: Designed differential coplanar waveguide on board, calculated characteristic impedance of transmission line to decrease reflection using SI9000 and simulated its performance using Advanced Design System.
- Power integrity: Used multiple decoupling capacitors to depress the current ripple and magnetic bead to suppress high-frequency noise and spike interference.

Optical Ising Machine Design **Mar. 2021 – May 2021**
State Key Laboratory on Integrated Optoelectronics, CAS, supervised by Prof. Ming Li *Beijing, China*

- Read literature about optoelectronic oscillator(OEO) and summarized recent progress in the field of OEO.
- Assisted in the design of an optical Ising machine, which is based on OEO and can be used to solve some optimization problems. Added an optical fiber of proper length to keep the feedback signal in the same phase with the forward signal and used Matlab to process experiment data.

Manuscripts

[1] Bozhi Yin, Yuean Gu, and Vladimir M. Stojanovic "Characterization of 45RFSOI Transistor for cryogenic applications."

Technical Skills

EDA Tools: Cadence(Virtusuo, Spectre), Advanced Design System, Sentaurus Device, Altium Designer, Multisim
Other Tools: Matlab, Code Composer Studio, Vivado
Languages: C, C++, Verilog, Python, Latex

Awards

UCAS Overseas Graduate Studies Fellowship **Sept. 2022**
University of Chinese Academy of Sciences *Beijing, China*

Outstanding Academic Research and Innovation Award **Oct. 2022**
School of Electronic, Electrical and Communication Engineering, University of Chinese Academy of Sciences *Beijing, China*