Yuean Gu

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Education

University of Chinese Academy of Sciences **Sep. 2019 – Jun. 2023(excepted)**
Electronic and Information Engineering; GPA: 3.87/4.0; Ranking:4/43 *Beijing, China*

University of California,Berkeley **Jan. 2022 – May. 2022**
Electrical Engineering; GPA: 4.0/4.0 *Berkeley, U.S.*

Academic Performance

Overall GPA: 3.87/4.0 Major GPA: 3.98/4.0
Core Courses: Principles of Electric Circuits(90/100) Nonlinear Electronic Circuits(91/100)
Linear Electronic Circuits(96/100) Integrated Circuits Devices(A+)
Digital Signal Processing(93/100) Programming Fundamentals and Experiments(95/100)
Toefl: 108 (R29, L28, S23, W28)

Research Experience

University of California, Berkeley **March 2022 – August 2022**
Berkeley Wireless Research Center, supervised by Prof. Vladimir M. Stojanovic *Berkeley, U.S.*

- Evaluated DC characteristics of transistors in the commercial 45nm PD-SOI processfor down to 2.5K cryogenic temperatures on different types of devices. Extracted key design parameters and analyzed them with the corresponding low-temperature effect.
- Introduced an effective temperature formulation to capture the effects of the band tail states and presented a compact model that corrects the low-temperature threshold voltage for the band-tail states, Fermi–Dirac statistics, and interface traps.
- Used Cadence Virtuoso and Matlab to model the experimental data of 45nm PDSOI CMOS from room temperature down to cryogenic temperatures.

Institute of semiconductors, Chinese Academy of Sciences **July 2021 – September 2021**
State Key Laboratory of semiconductor superlattices, supervised by Prof. Nan Qi *Beijing, China*

- Designed a testboard system for a clock-data-recovery chip using Altium Designer.
- Calculated the characteristic impedance of transmission line to decrease the reflection and increase the transmission of the high frequency signals.
- Modeled and simulated the differential coplanar waveguide on board, using Advanced Design System.
- Chose a kind of low dropout regulator for the powerboard according to key parameters and used multiple decoupling capacitors to depress the current ripple.

Institute of semiconductors, Chinese Academy of Sciences **March 2021 – May 2021**
State Key Laboratory on Integrated Optoelectronics, supervised by Prof. Ming Li *Beijing, China*

- Read literature regarding optoelectronic oscillator(OEO) and summarized recent progress in the field of OEOs,with particular attention to new mode control and selection methods, as well as chip-scale integration of OEOs.
- Assisted in the design of a optical Ising machine, which is based on optoelectronic oscillator and can be used to solve some optimization problems. Calculated the length of optical fiber which was added in the feedback loop of Ising machine in order to keep the forward signal and feedback signal in the same phase, operated pratically and used Matlab to process the experimental data.

Manuscripts

[1] Bozhi Yin, Yuean Gu, and Vladimir M. Stojanovic "Characterization of 45RFSOI Transistor for cryogenic applications."(Submitted)

Technical Skills

EDA Tools: Altium Designer, Cadence Virtusuo, Advanced Design System, Multisim, SI9000
Other Tools: Matlab, Code Composer Studio, Vivado, Filter Solution
Languages: C, C++, Verilog, Python, Latex

Awards

Triple-A Student **June 2021**
University of Chinese Academy of Sciences *Beijing, China*

Outstanding Academic Research and Innovation Award **August 2022**
School of Electronic, Electrical and Communication Engineering, University of Chinese Academy of Sciences *Beijing, China*