# Yugal Kithany

yugalkithany@gmail.com | linkedin.com/in/yugalkithany | yugalkithany.github.io

## Education

**University of Illinois at Urbana Champaign,** Bachelor of Science in Computer Engineering Aug 2021 – Dec 2024

Undergraduate Thesis: *Control Algorithms for Vision-Based Navigation.* Advisor: Sayan Mitra

Coursework: Computer Architecture, Operating Systems, FPGA Systems Laboratory, Control Systems, Parallel Programming, Distributed Systems, Green Power, Algorithms, Data Structures, Discrete Math, Computer Systems Programming.

## Experience

**Research Assistant, Prof. Dong Kai Wang's Computer Architecture Lab** Sep 2023 – Present

- Writing synthesizable SystemVerilog code and conducting simulations using QuestaSim.
- Developing hardware in RTL libraries for RISC-V 1.0-compliant and composable vector processors.
- Evaluating open-source L1/L2 parameterized caches for vector processors and simulate in existing RTL code base.

**Software Developer, Prof. Sayan Mitra's Reliable Autonomy Group** Sep 2023 – Present

- Developing PID controller to optimize drone velocity and safety for gate-based racing with RRT to guarantee stability.
- Designed and simulated MPC algorithms on Microsoft Airsim to execute vision-based UAV tracking algorithms.
- Increased drone velocity by 20% with 75% reduction in collisions in comparison to baseline design.

**Firmware Engineering Intern, Milwaukee Tool** May – Aug 2024

- Designed data acquisition system effectively integrating with product line, providing live monitoring of performance.
- Ensured high-quality system design through collaborative processes and iterative development methodologies.
- Conducted comprehensive unit testing of C++ classes and functions using Google Test and various DUT methods.

**Operating Systems Course Assistant, UIUC** Aug 2023 – Aug 2024

- Discuss key-note ideas about complex OS design topics for 200+ students. Grade exams and project submissions.
- Help debug x86 and C driver-code for Unix-Based OS projects to improve students' learning experience.

**Software Developer Intern, Federated Hermes Global Trading and Technology** May – Aug 2023

- Developed, tested, optimized SQL packages for Oracle database in sprint-oriented Software Development Life Cycle.
- Designed a Power App simulating the trading environment and modeled impact on downstream systems.
- Converted SQL report of investment portfolio to real-time, improved refresh time by 20%, added user-form function.

## Projects

**Speculative Out-of-Order RISC-V Processor**

- Designing and verifying ERR out-of-order processor, implementing RV32IM ISA with FP and Mult/Div extensions.
- Developed arbiter, stride prefetchers, and cache-line adapter for efficient two stage cache-DRAM integration.
- Optimizing design with early branch recovery, Perceptron branch predictor with BTB, and split load-store queue.

**RTL Projects on DE10-Lite FPGA board**

- Developed three-stage (fetch, decode, execute) SLC3 processor and created CPU with integrated memory (SRAM, IR).
- Implemented the design and functionality in SystemVerilog and compiled on Quartus Prime with SystemVerilog.
- Designed and built digital systems with TTL and FPGAs. Debugged on Model Sim and Signal Tap Logic Analyzer.

**Single Core Unix x86 Kernel**

- Designed paging-based virtual memory, context switching, read only file system, round-robin scheduler.
- Introduced compatibility for Linux commands on Posix style shell with keyboard comparability.

**Convolution Neural Network for Image Classification**

- Optimized forward-pass of convolution layers with Nvidia Cuda Platform, evaluated performance on Nsight Systems.
- Implemented modified LeNet5 architecture for working with Fashion MNIST dataset.

## Skills

**Languages**: SystemVerilog, RISC-V, C++, C, x86 Assembly, CUDA-C, Python, Linux, SQL, Java, Matlab, Simulink, ROS.
**Tooling**: Synopsys VCS, Verilator, Quartus, ModelSim, ADO, Git, Bitbucket, MS Office Products, Jama Cloud, Jira.