2020 Digital IC Design Homework 5: Sobel

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| NAME | |  | | | | | | |
| Student ID | |  | | | | | | |
| **Simulation Result** | | | | | | | | |
| Functional simulation | Level | | Gate-level simulation | Level | | | Gate-level simulation time | simulation time (ns) |
| (your pre-sim result) | | | | | | (your post-sim result) | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | |  | | | |
| Total memory bit | | | | |  | | | |
| Embedded multiplier 9-bit element | | | | |  | | | |
| (your flow summary) | | | | | | | | |
| **Description of your design** | | | | | | | | |
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*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (gate-level simulation time in ns)*