Unit - 7

Field effect transistor

A Bipolar Junction Transistor (BJT) is a current control device while a Field Effect Transistor (FET) is a voltage control device. Similarly, the BJT is bipolar i.e. the current flows due to both charge carriers [electrons and holes], while the FET is a unipolar device since, the current flows due to either electrons [in the N- channel] or holes [in the P-channel]. The field effect transistor gave an extremely high input impedance which is the most advantage over BJT devices.

Field Effect Transistors (FETs) are of several types such as Junction Field Effect Transistors (JFETs) and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs).

# Junction Field Effect Transistor (JFET)

On the basis of majority change carriers, JFETs are of two types:

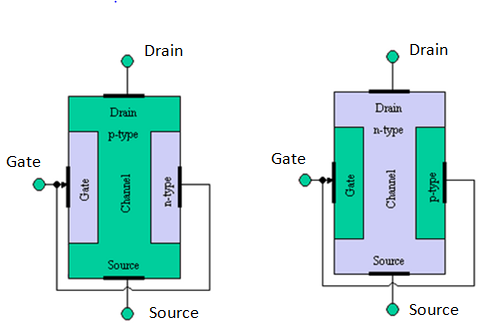
1. N-channel JFET with electrons as the majority charge carriers.
2. P-channel JFET with holes as the majority charge carriers.

N-channel JFETs are preferred over the P-channel JFETs because the movability of electrons is higher than that of holes.

# Construction of JFET

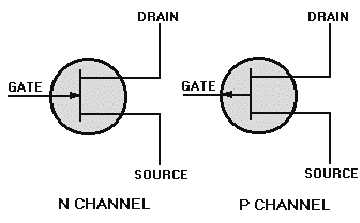
In an N-JFET, N-type silicon bar has two smaller pieces of P-type silicon material diffuse on the opposite side of its middle part, forming a P-N Junction. The two PN Junctions forming diodes or gates is connected internally and the common terminal is called the gate.

Ohmic contacts are made at the two ends of channel which are called the source and drain.



*Figure: P-channel JFET (left) and N-channel J-FET (right)*

The schematic symbols of NJFET and PJFET are:



**Source:** The terminal through which the majority carriers enter the channel is called the source terminal and the conventional current entering the channel at S is designated as IS.

**Drain:** The terminal though which the majority carries leave the channel is called the drain terminal (D) and the conventional current leaving the channel at D is designated as Id.

The drain to source voltage is called VDS and it is positive if D is more positive than S.

**Gate:** There are two internally connected heavily doped impurity regions formed by alloying by diffusion or by any other methods available to create two P-N Junctions. These impurity regions are called the gate (G). The voltage VGS is applied between the gate and source in the direction to reverse bias the PN Junction. Conventional current entering the channel at G is designated as IG.

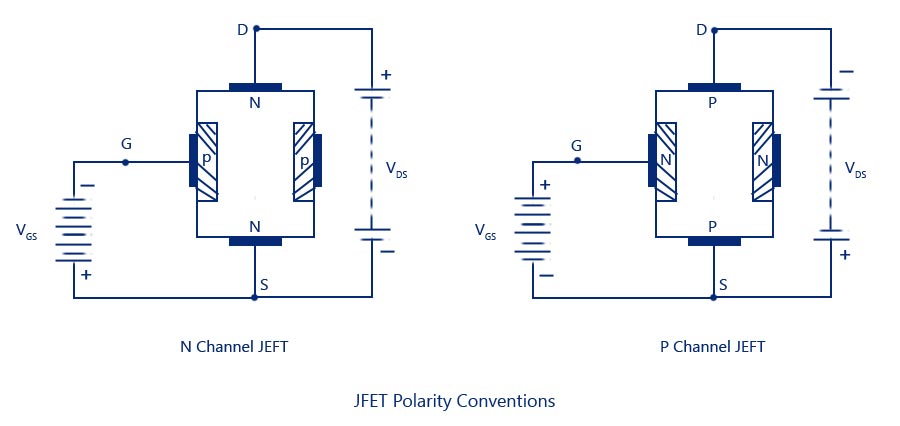
**Channel:** The region between source and drain sandwiched between the two gates is called the channel and the majority carrier moves from source to drain through this channel.

# Operation of JFET

To operate the JFET as an amplifier, the gate must be reverse biased with respect to the source and drain to source also must be reverse biased.

Thus, for NJFET, the gates are provided with the negative voltage and a positive voltage is given to the drain.

Similarly, for the PJFETs, a positive voltage is connected to the gate and a negative voltage to the drain.



# Operation of NJFET

In the NJFET, the channel N-type silicon bar has two P-type silicon materials diffused on the opposite sides of its middle part. The two PN junction forming the diodes are internally connected and the common terminals is called the gate. The two ends of the channel are the drain and the source.

## Case A

When V­GS = 0V i.e. no voltage is applied to the gate as well as drain with respect the source, the depletion region around the PN junction are of equal thickness and symmetrical as shown in figure above. There is no drain current with VGS = 0V and VDS = 0V.

## Case B

VGS = 0V and VDS is applied. Due to the VDS, there exists more reverse voltage near the drain end compared to the source end, so a wedge shaped depletion layer is formed.

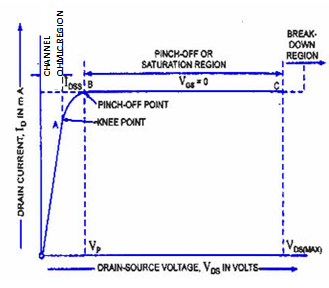
The size of the depletion width determines the width of the channel and the magnitude of current flowing through its channel.

The drain current ID increase linearly with VDS up to a certain voltage, VDS (pinch-off voltage) and after this drain current ID remain constant. The region where ID current increase linearly with the VDS is called the Ohmic region. At the pinched off point, ID becomes maximum and is called the IDS (i.e. the drain to source saturation current). The region where the ID remains almost constant even though VDS is increased is called the pinch-off or saturation region.

## Case C

VGS = -1V, -2V, -3V etc. and VGS > 0V.

Due to the reverse biased voltage at the gate, the pinch-off occurs earlier (i.e. to a lower value of VDS). The gate to source voltage at which the drain current becomes completely zero is called V­GS off or pinch-off voltage i.e. VGS .off = VP.



# Advantages of JFET over BJT

1. JFET is similar to fabricated. Its efficiency is high and it has a longer life compared to BJT.
2. The JFET has better thermal stability than BJT.
3. It has a higher power again.
4. It has sequence less charactersitices. So, it is useful in the tuner of radio and TV receiver.

# Disadvantages of JFET

1. The JFET has a relative small gained bandwidth product.
2. It has greater susceptibility to damage in its handling.
3. It has a low voltage gain due to a gm.
4. Its cost is higher than BJT

# Applications of JFET

1. JFET are used in RF amplifiers in FM tuning circuit.
2. JFETs are used in digital circuits, LST and memory circuits.
3. JFETS can be used as analog switch and an amplifier.

# MOSFET (Metal Oxide Semiconductor field Effect Transistor)

The metal oxide semiconductor field effect transistor(MOSFET) is one of the mostly used electrons devices particularly in digital circuits because of the relatively small size and its easy febrications technique where thousands of devices is fabricated in a single chip.

Since, it is constructed with the gate terminal insulated from the channel, it may be refferred to as Insulated Gate Fixed Effect Transistor(IGFET).

Both IFET and MOSFET are voltage controlled unipolar devices becauses their channel conductively is only one charge carries, so these are unipolar devices. However, BJTs are bipolar devices becauses the current flows due to both electrons and holes.

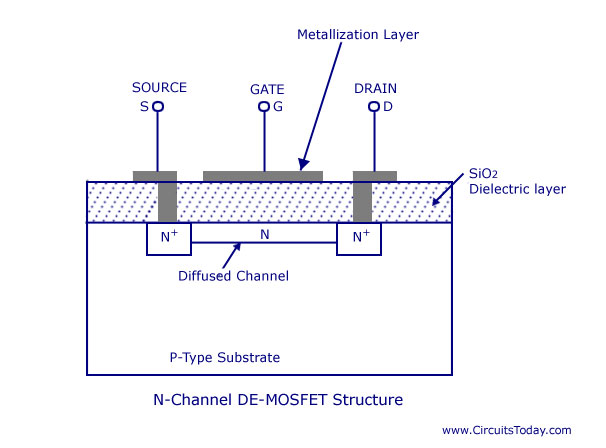
The principal feature that distinguishes a MOSFET from JFET is the fact that the gate terminal in a MOSFET is insulated from its channel region. So, a MOSFET is also called IGFET.

There are two types of MOSFET:

1. Depletion-type MOSFET (DMOSFET)
2. Enhancement- type MOSFET (EMOSFET)

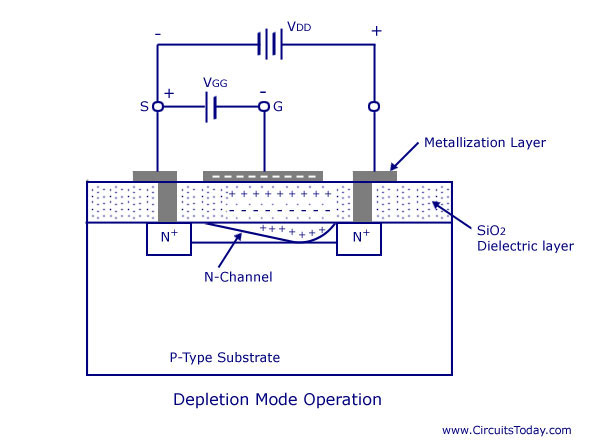
# Depletion type MOSFET

A basic construction of N-channel depletion type MOSFET is shown below:



A slab of P-type materials is formed from a silicon base and is referred to as substrate. The source and the drain terminals is linked by N-channel. The gate is also connected to a metal contact surface but remains insulated from n-channel by a thin size layer. It is the insulating layer of SiO2 in MOSFET that account for very high desirable high input impedance. There is no direct electrical connection between the gate terminal and the channel of MOSFET.

# Operation of MOSFET



There exists a lightly doped n-channel between the heavily doped drain and source as shown in figure. So, the ID flows even at V­GS = 0V, if the VDS is applied.

## Case A

VGS = negative voltage and VDS is applied

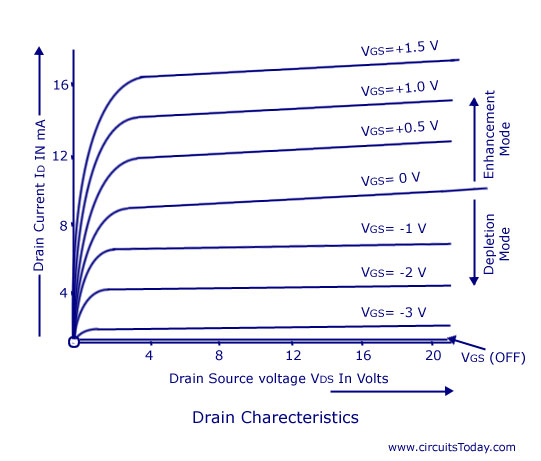
With VGS = negative voltages, the channel width reduces due to electromagnetic induction; i.e. the negative charge on the gate repels electrons from the channel to P-substrate. Thus, the drain current reduces. This mode of operation is termed the depletion mode.

## Case B

VGS = positive voltage and VDS is applied

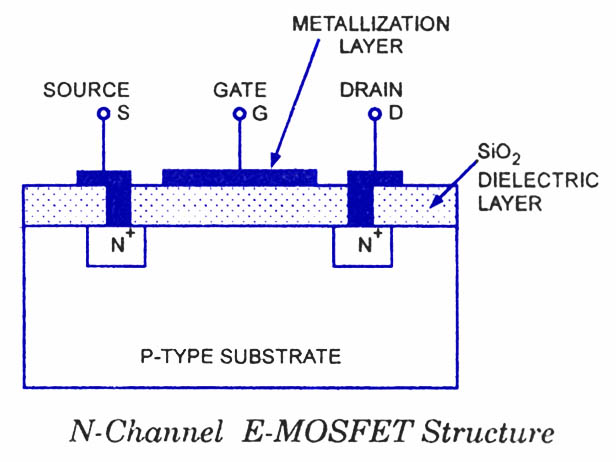
When V­GS has the positive voltage, the charge on the metal attracts electrons from the P-substrate and thus, the channel width increases and the drain current increases. This mode of operation is termed the enhancement mode.

The drain characteristics curve for both the depletion region and enhancement mode is shown in the figure.



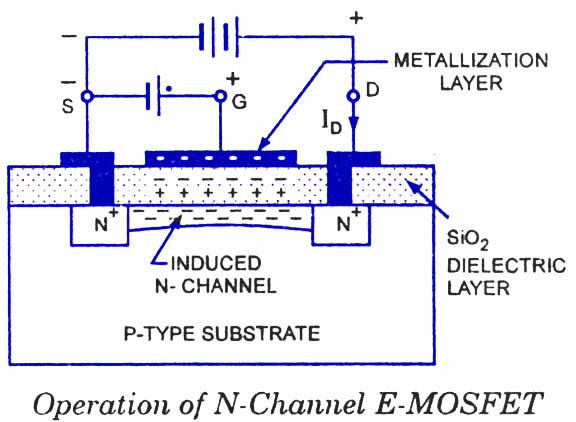
Thus, the DMOSFET operates in the depletion mode as well as in enhancement mode.

# Enhancement-type MOSFET



A slab of P-type material is formed from a silicon base and it is referred as substrate. The source of drain terminal are connected through metallic contact to N-doped region in the absence of the channel between two ends of difference between DMOSFET and EMOSFET.

# Operation of EMOSFET



In the EMOSFET, initially there is no channel between the drain and source as shown in figure.

## Case A

VGS = 0V and VDS > 0V

For VGS = 0V and V­DS increasing, there will be no drain current since there is no conducting path (channel) between the drain and source.

## Case B

VGS = positive voltage and VDS > 0V

With a positive voltage at the gate, the channel forms between the drain and the source. The minimum gate-to-source voltage at which significant drain current flow, is called the threshold voltage (VTR).

If VGS > VTR, then drain current ID is given as:

Where, k is constant, V­TR is threshold voltage.

It is the minimum voltage that should be applied to the gate that significant drain current start to flow.

The transfer characteristics curve for the EMOSFET is shown in the figure:

