# ECS404 Computer Systems and Networks

Computer Architecture
Week 4 Pt 2: CPU Registers and SRAM

#### Aims

• Show how SRAM, the memory used for cpu registers, works.

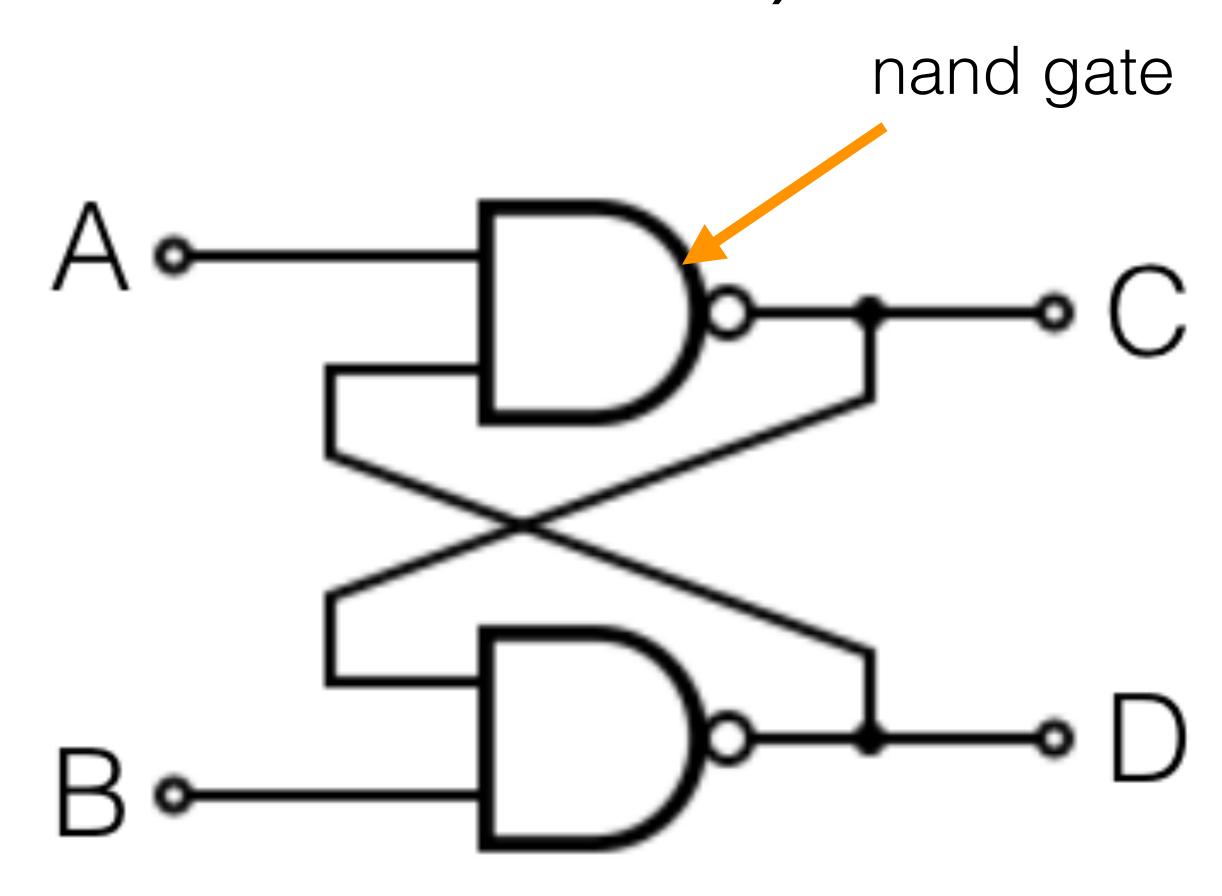
### Learning Objectives

 Understand the construction of a flipflop, and understand how these are used to implement high-speed memory, for example in cpu registers and high-speed caches

# Logic Gates

- In week 3 we looked at how to build logic gates.
- Gates have inputs and they produce outputs.
- In the jargon they are combinational circuits: their state depends only on the current inputs.
- Memory cells incorporate feedback and their state depends on past inputs as well as the current ones. They are **sequential** circuits (state depends on sequence of inputs).

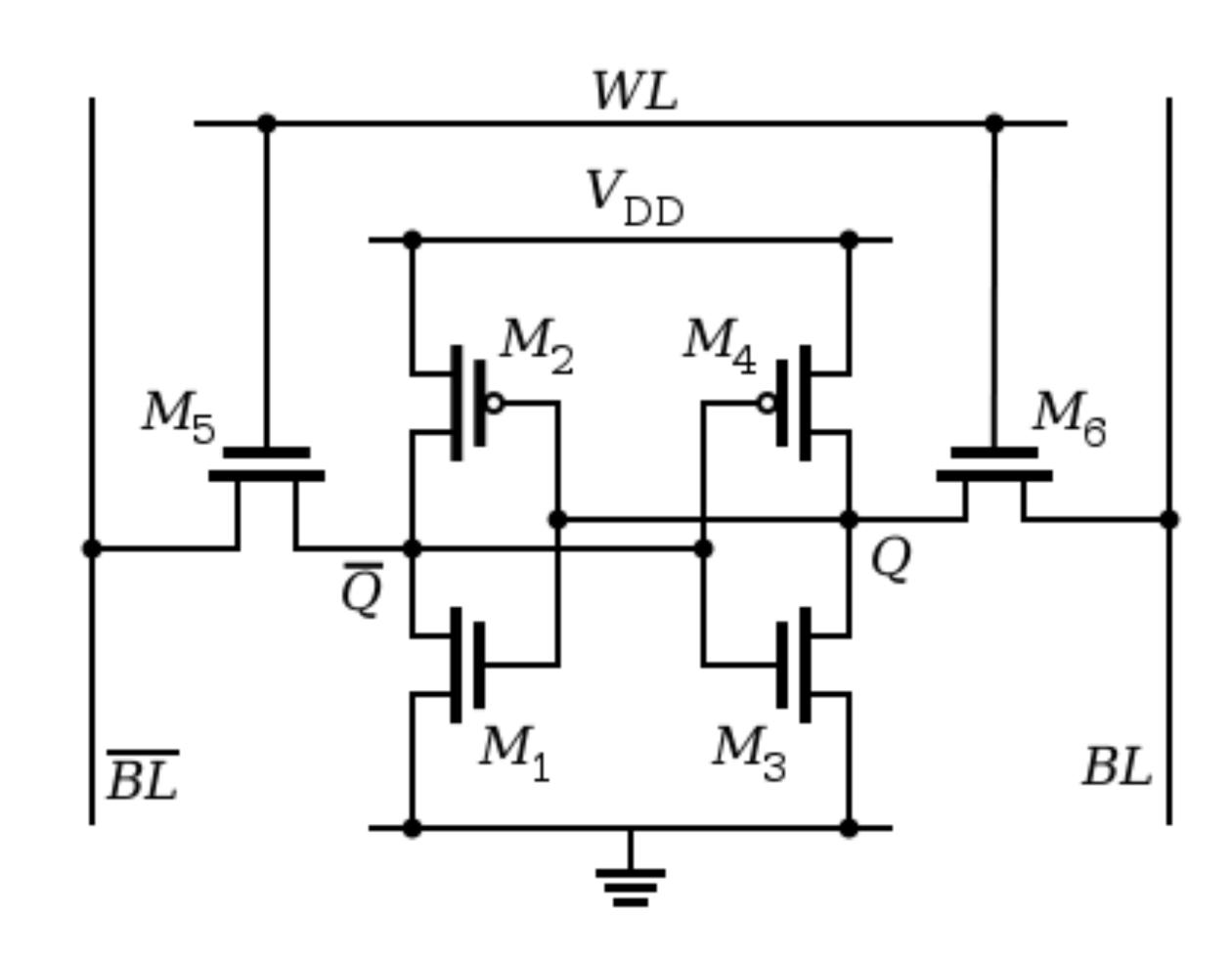
# Basic Flip Flop (see lecture notes)



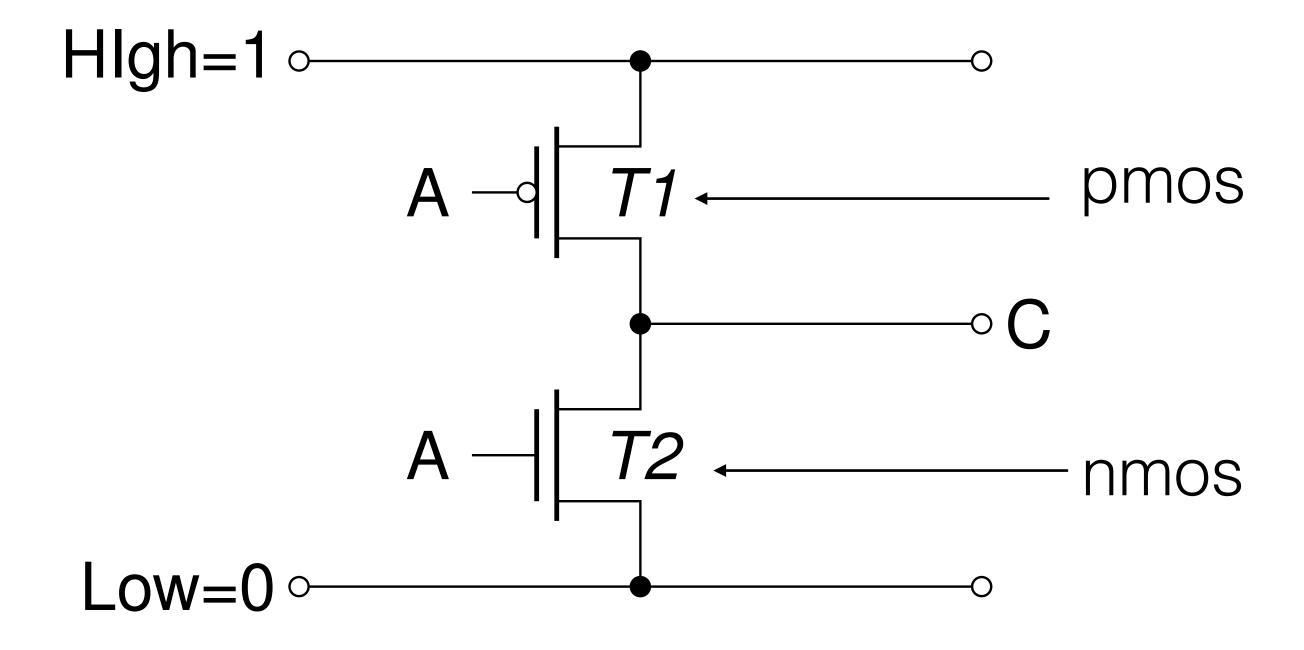
### Memory

- .. and that is enough.
- If we can store one bit, then we can build whole computer memories.

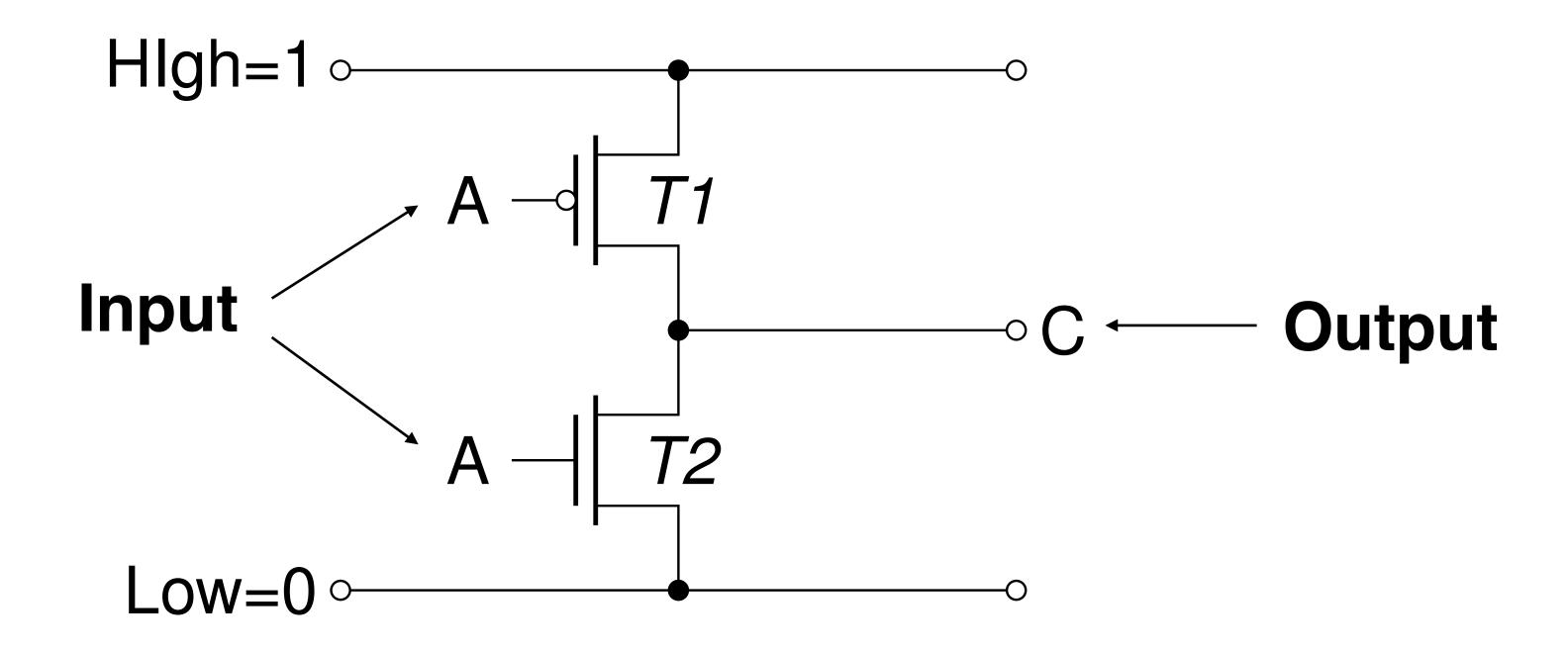
# An actual SRAM

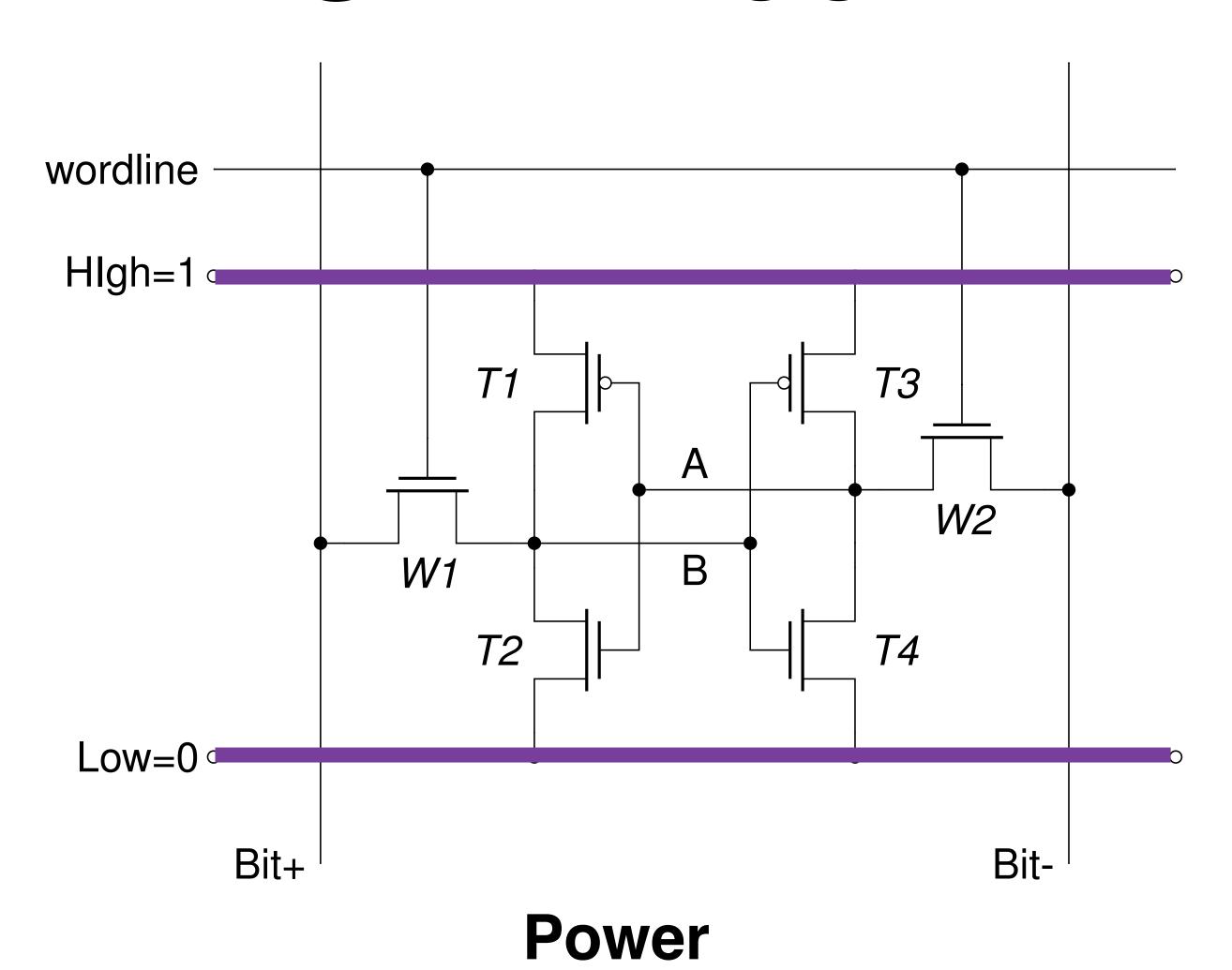


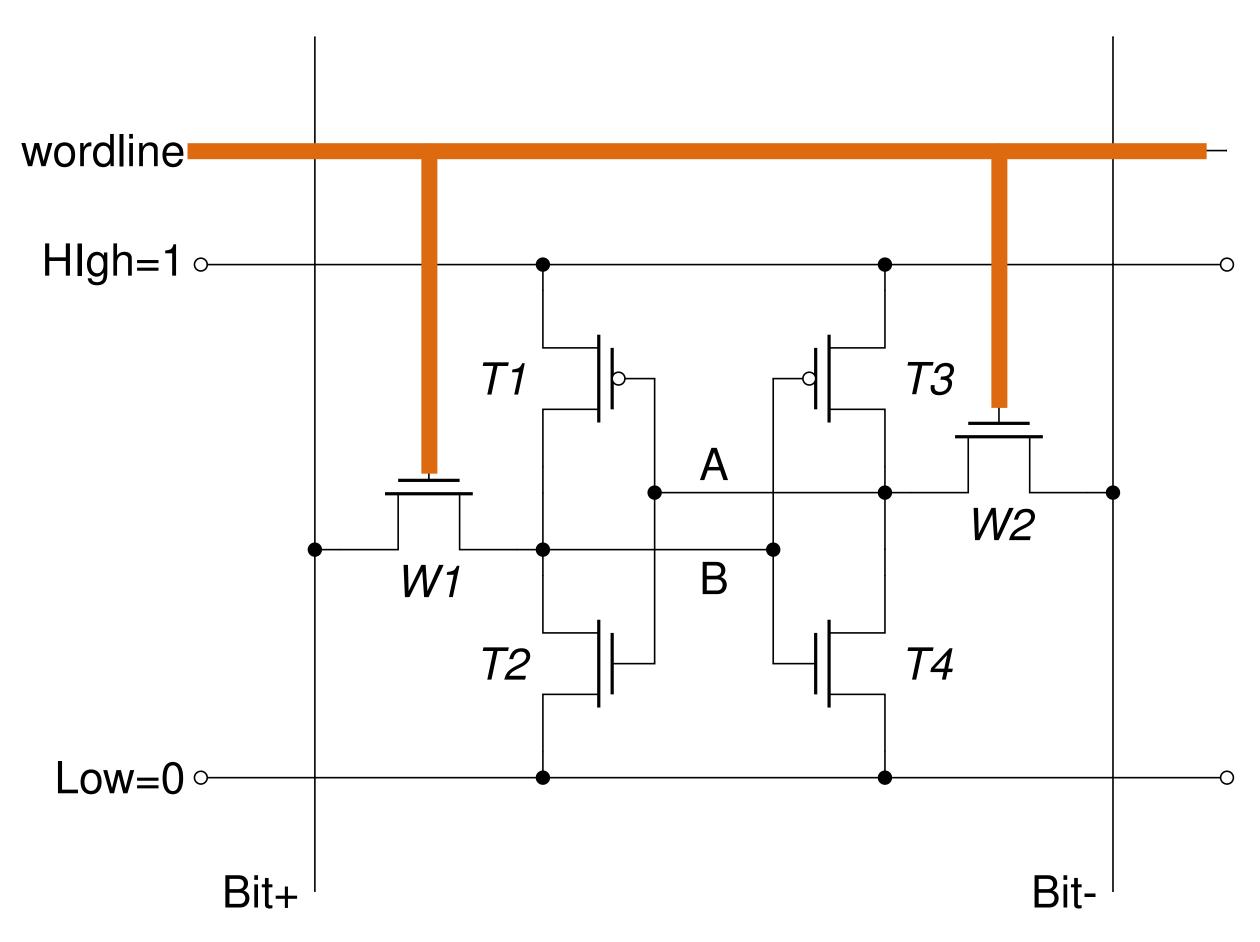
# Inverter or not gate



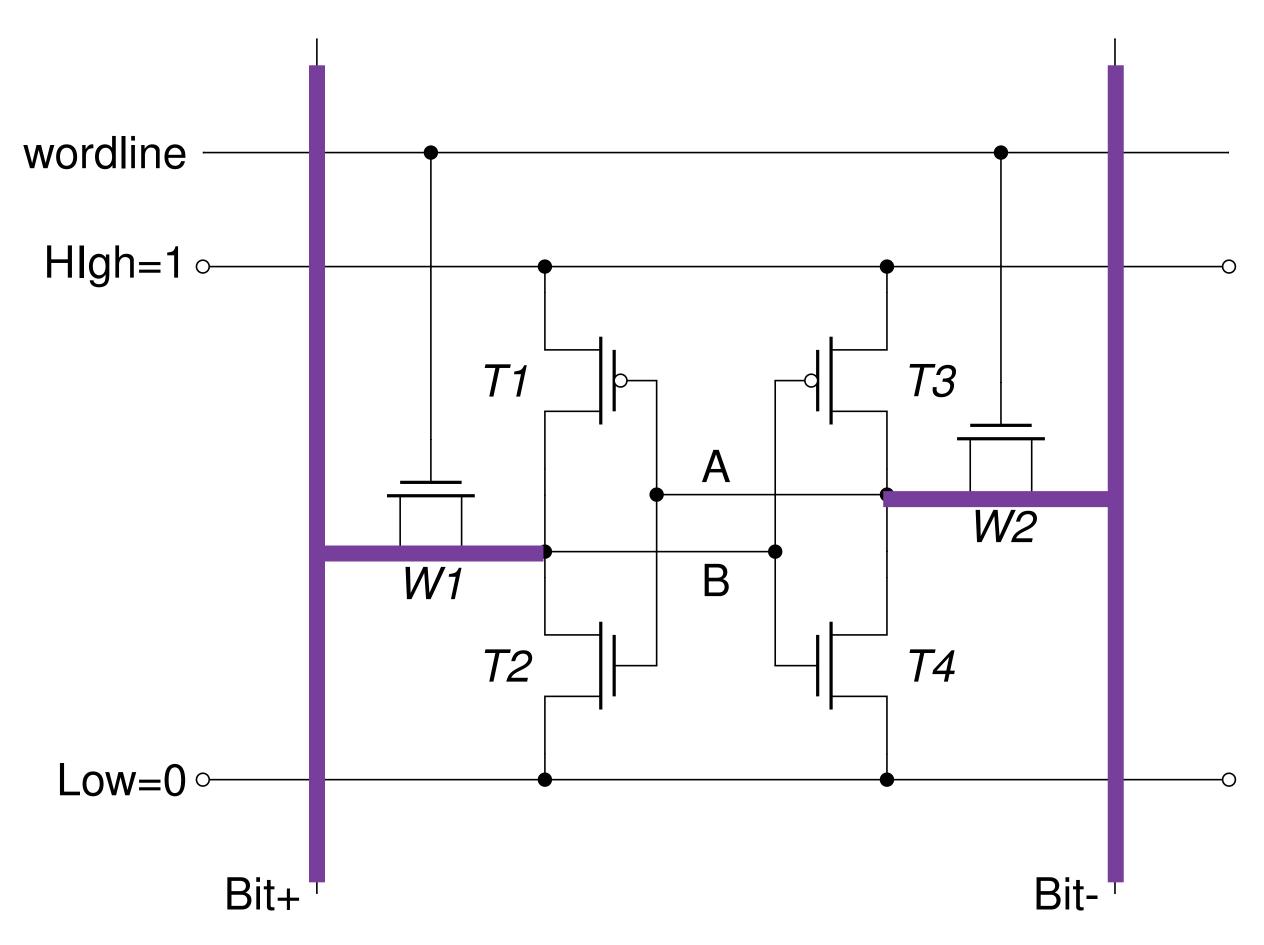
# Inverter or not gate



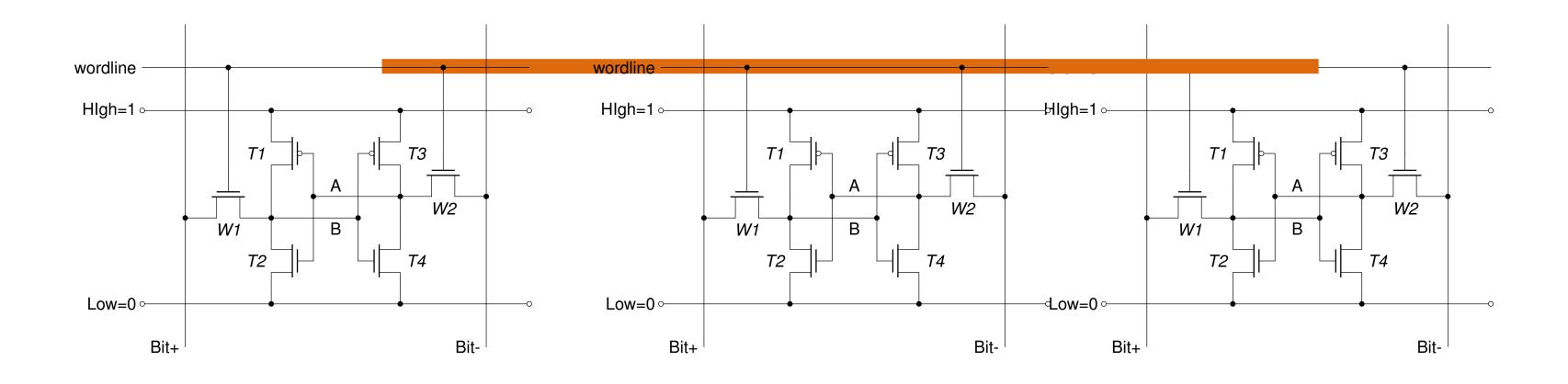




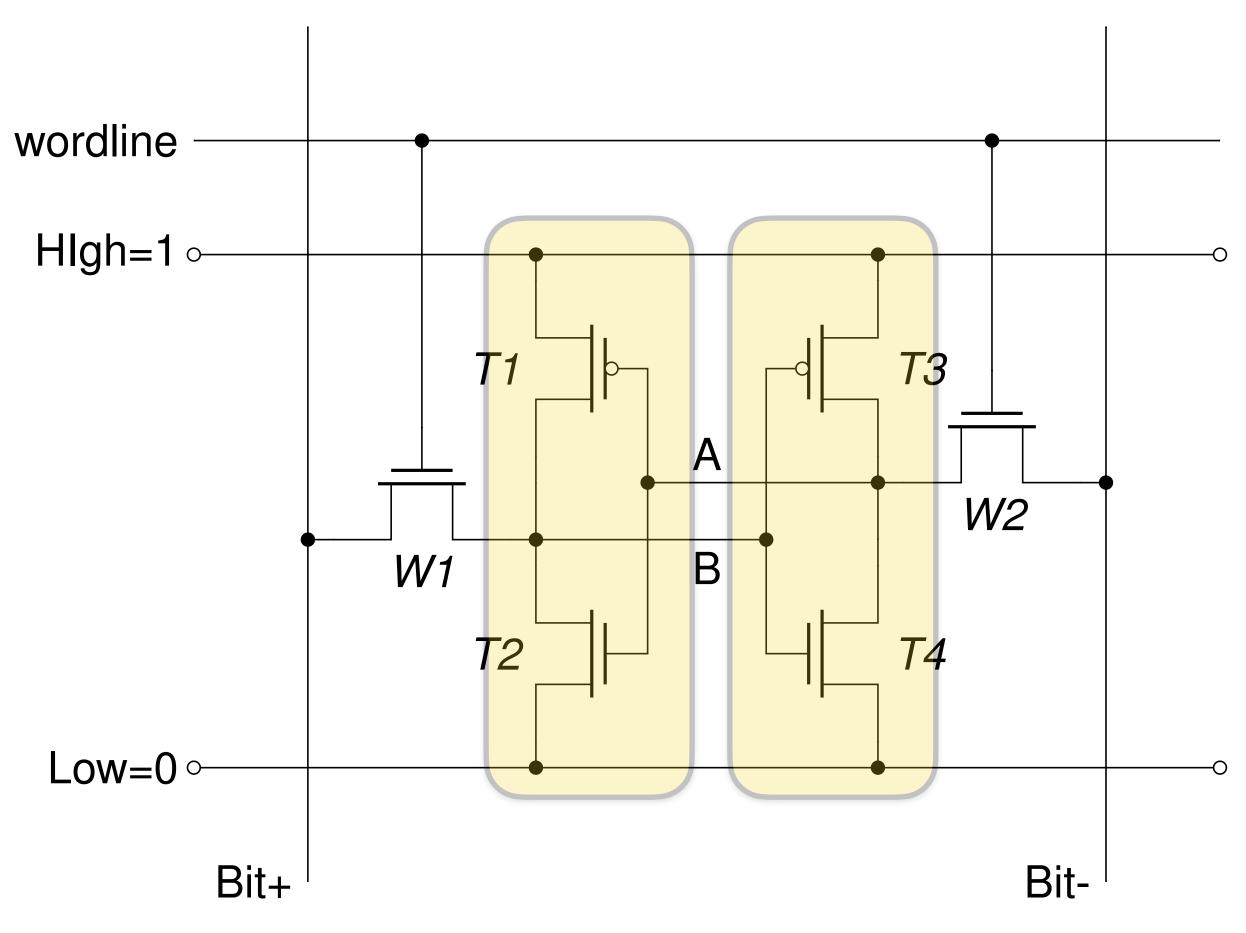
Access control



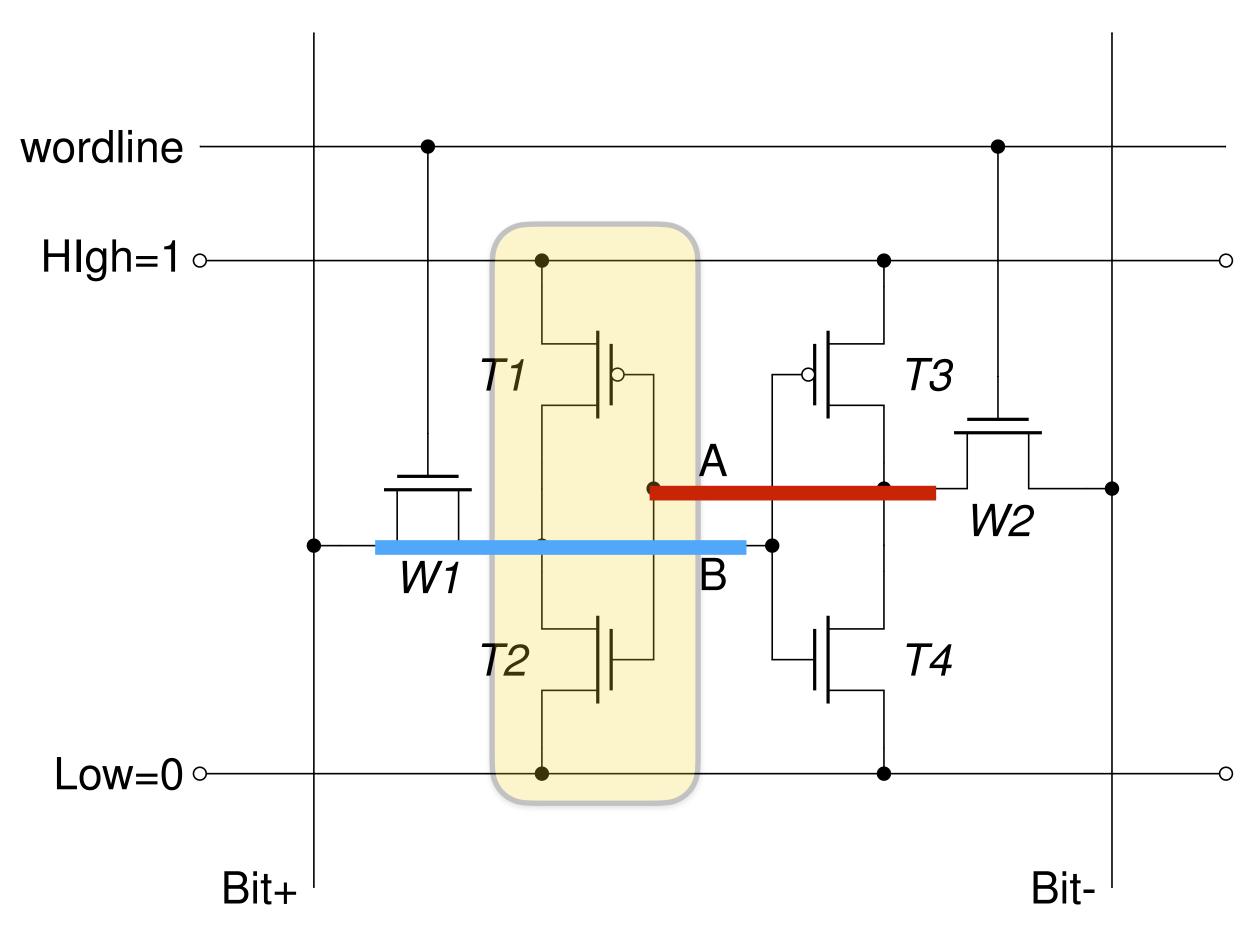
Data input and output



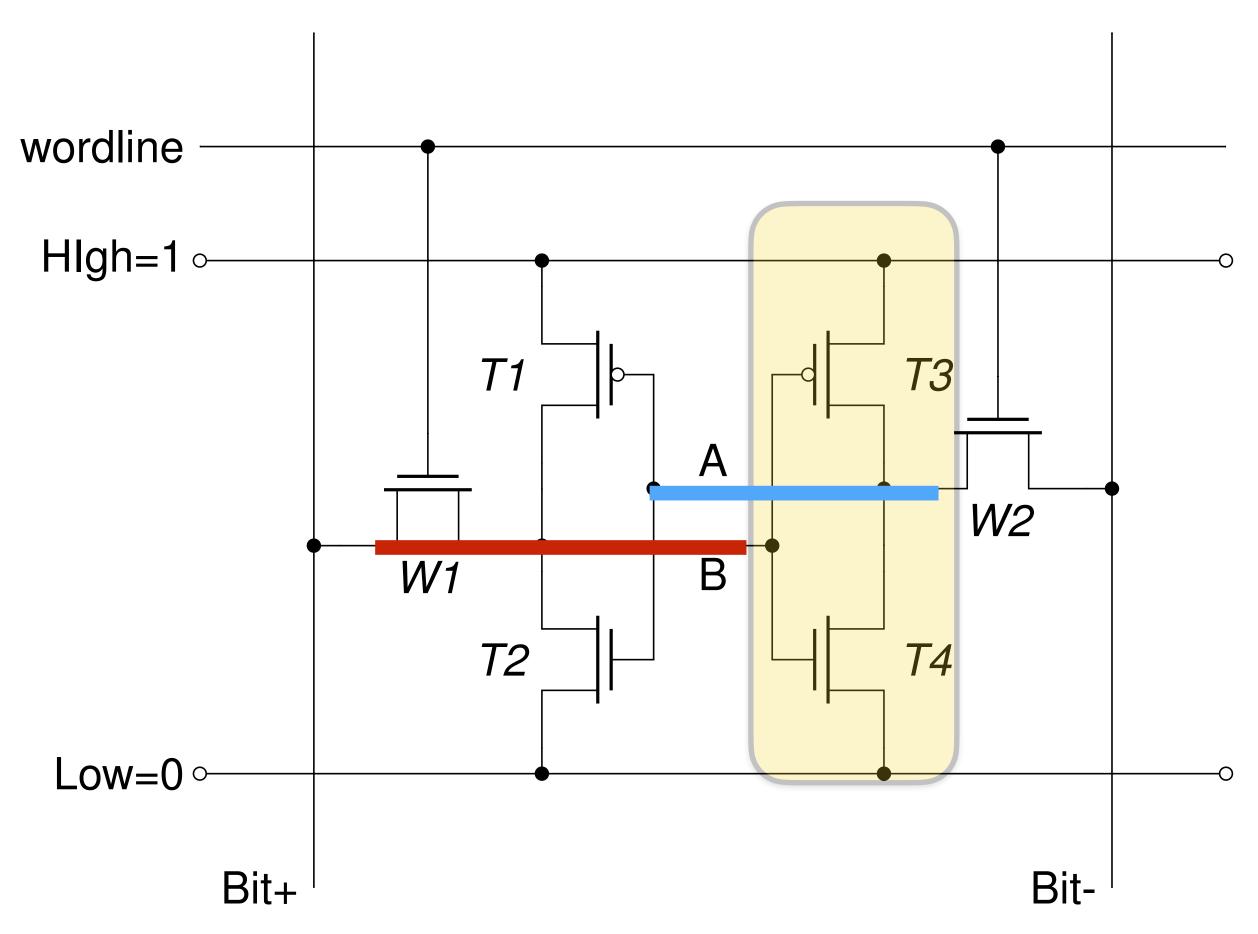
#### Access control



Inverters

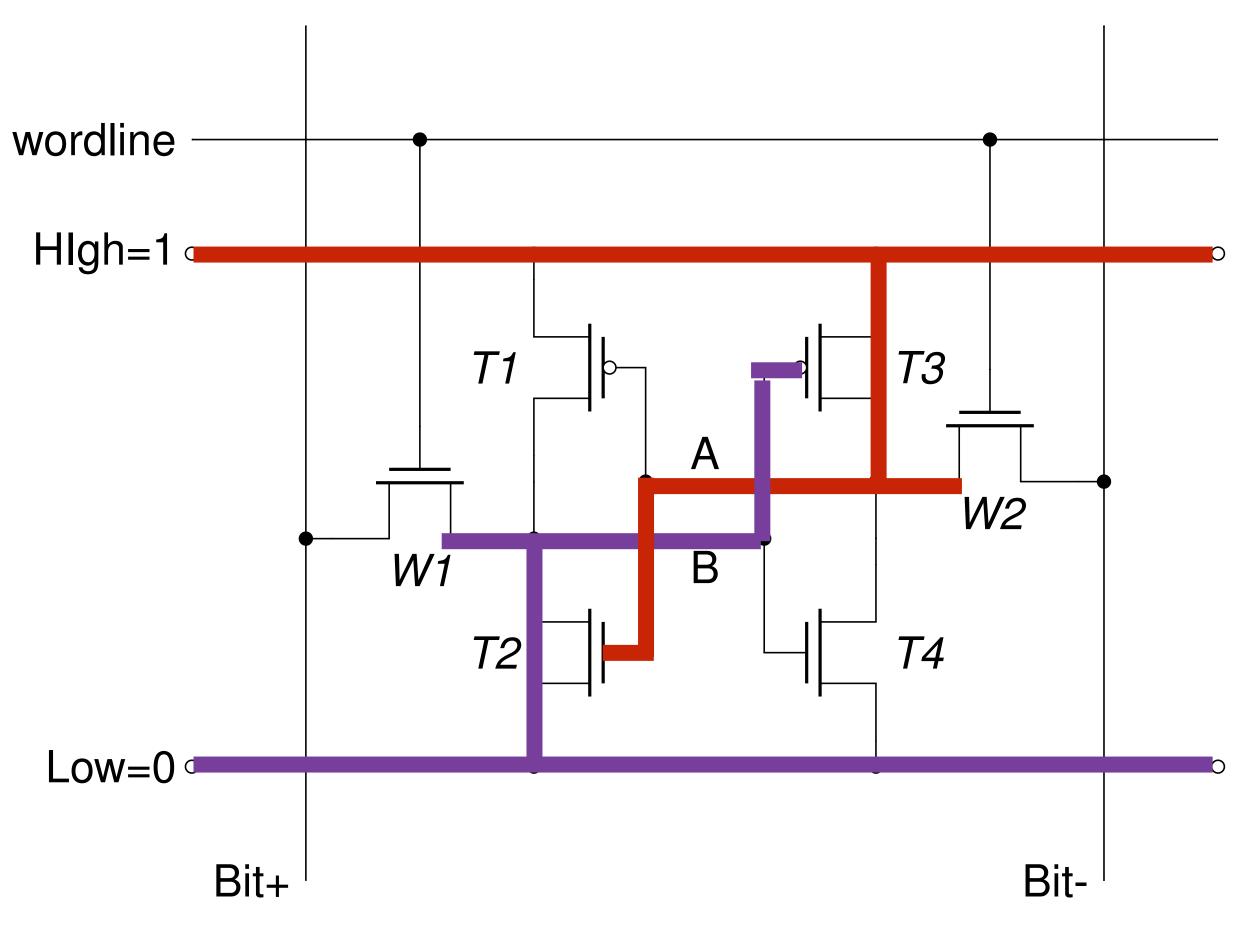


Inverter 1: input and output

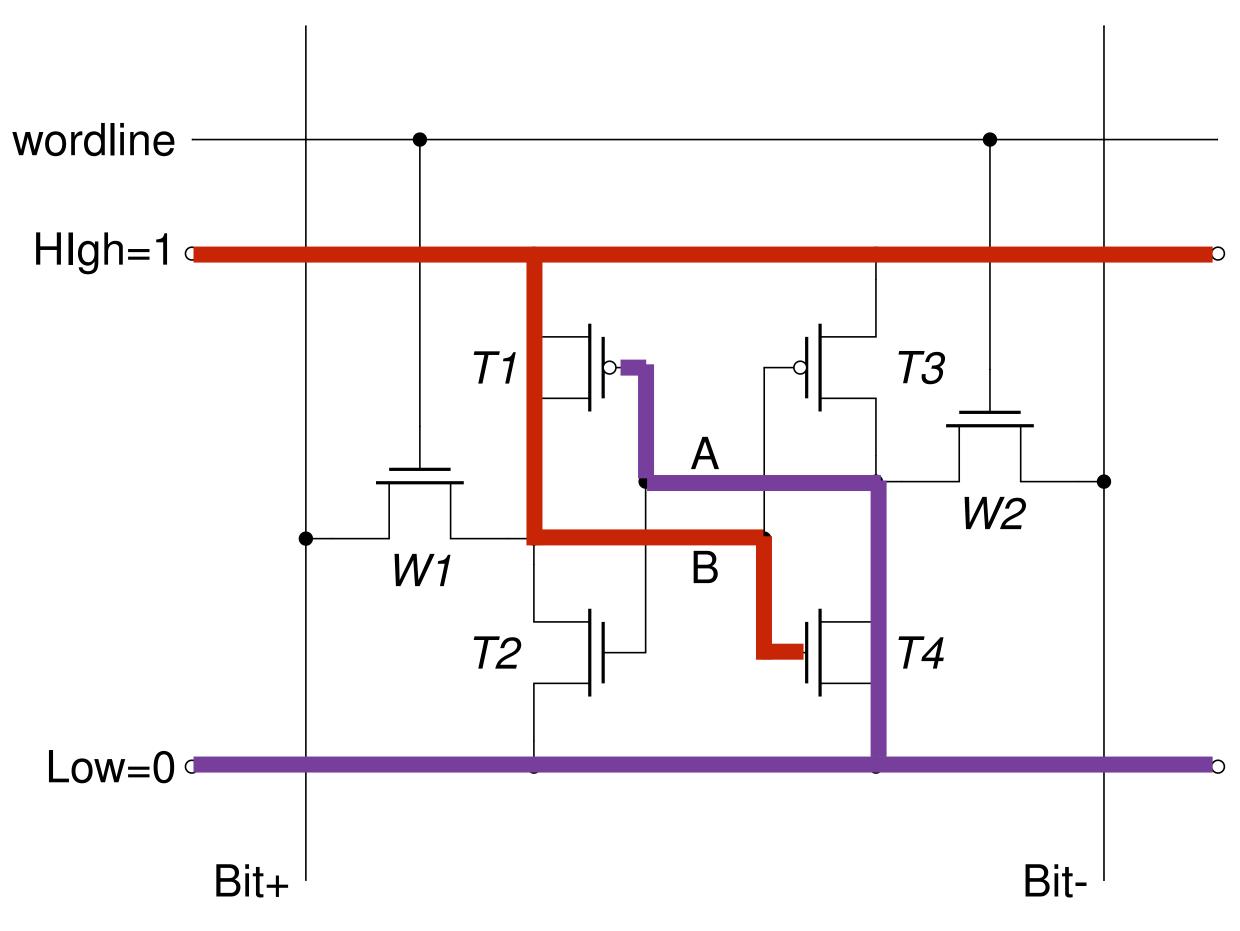


Inverter 2: input and output

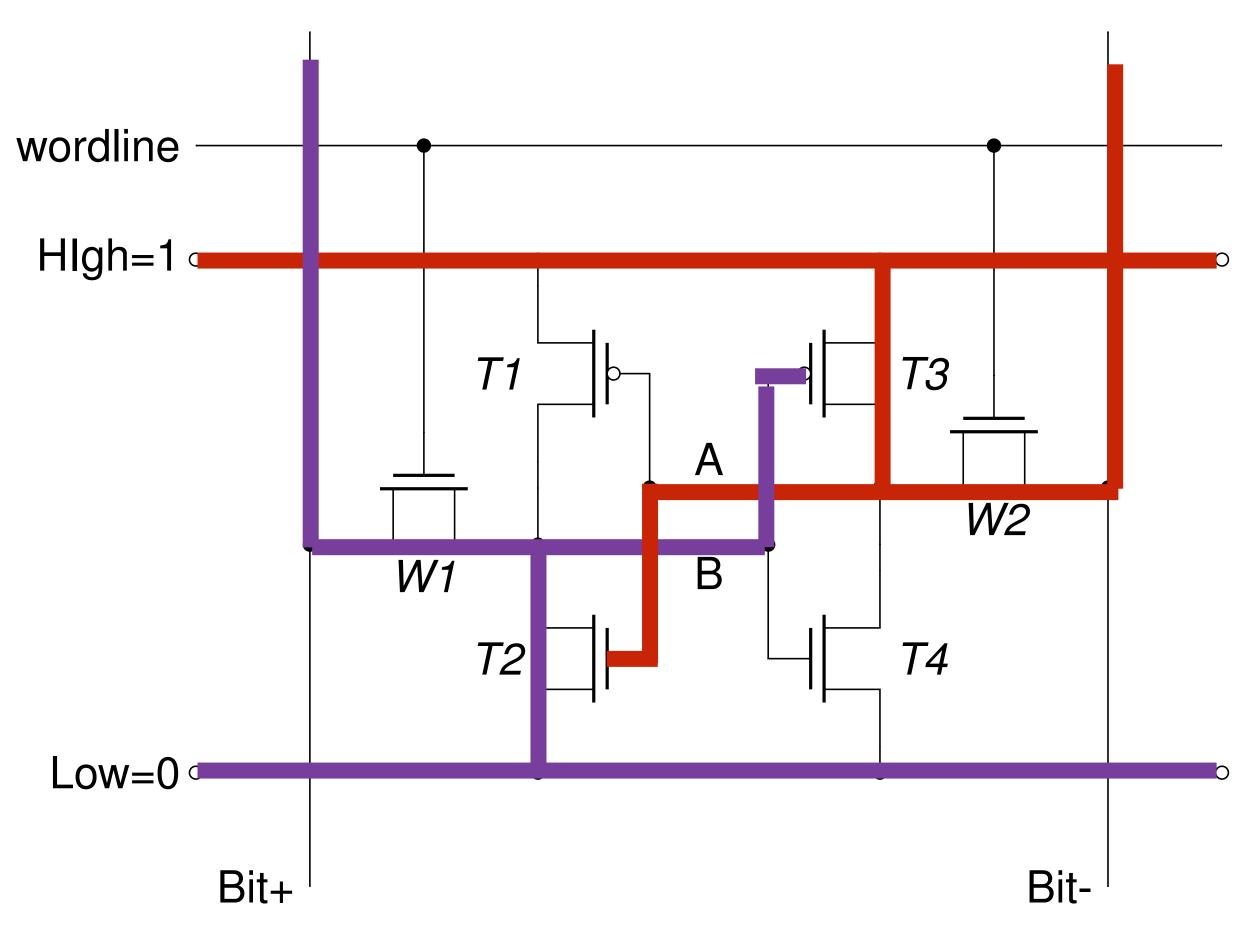
- Input of each inverter is output of other.
- So we can have
  - A=1 and B=0
  - Or A=0 and B=1
- We can't have
  - A=1 and B=1
  - A=0 and B=0



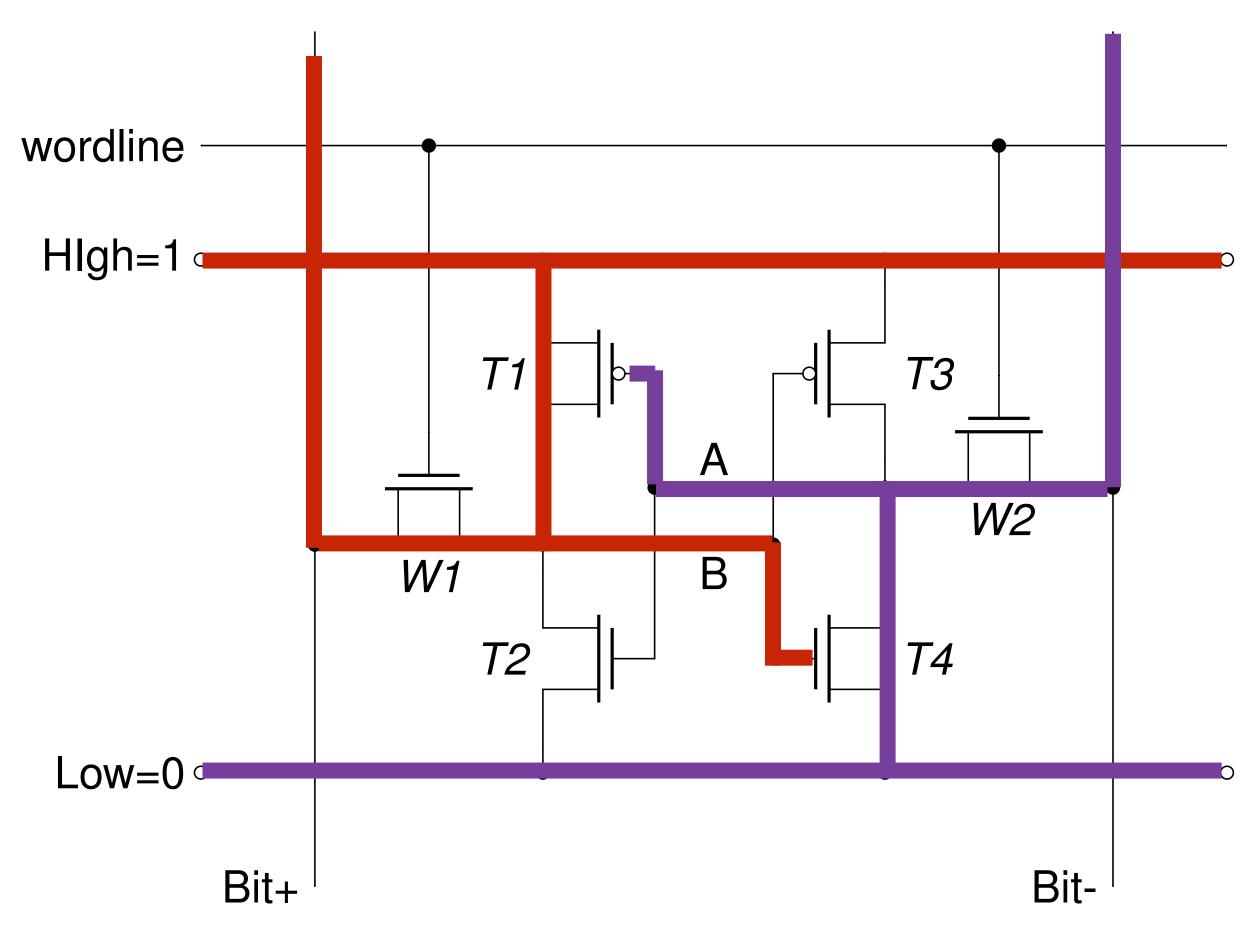
**A=1** and **B=0** 



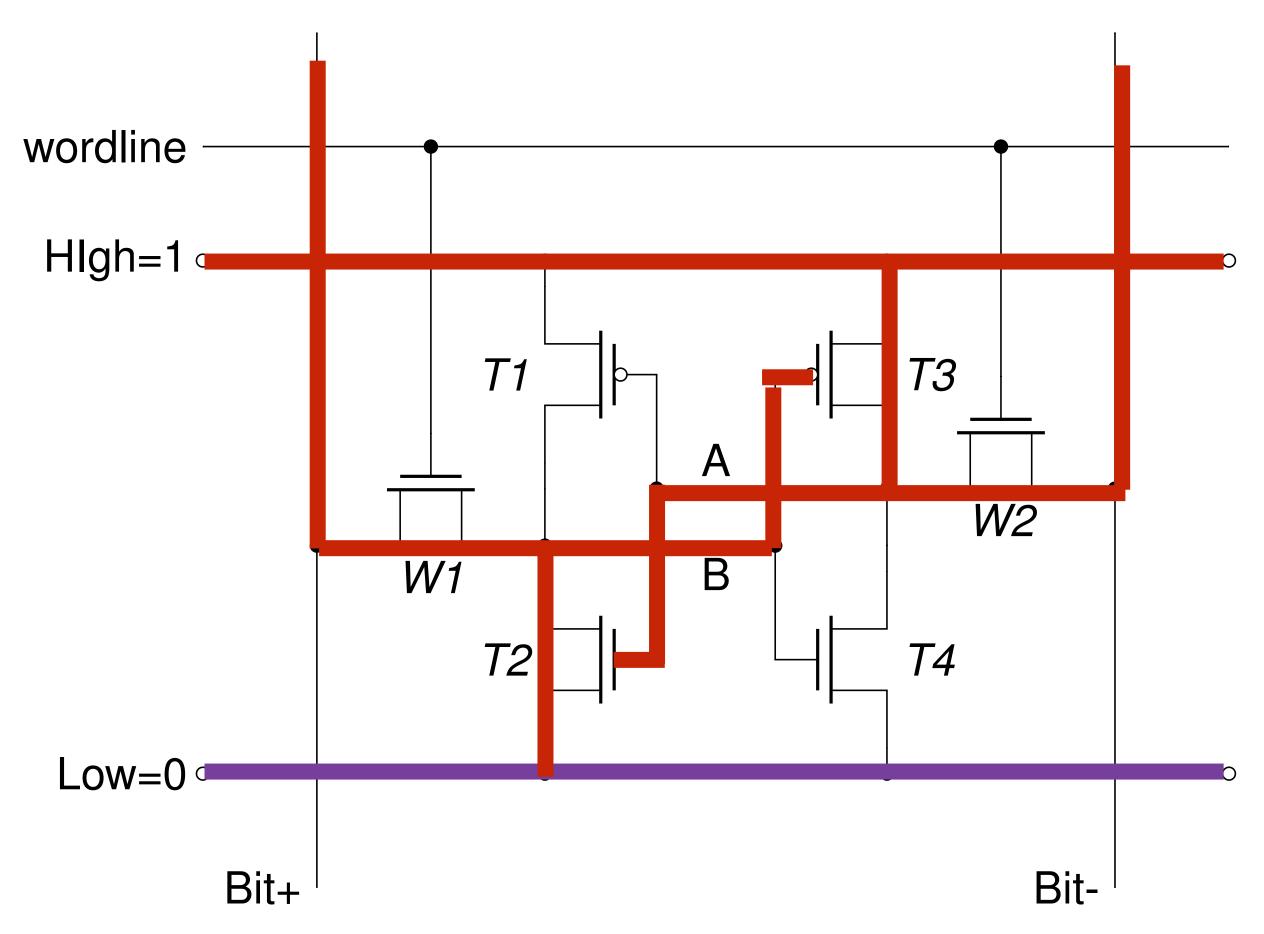
**A=0** and **B=1** 



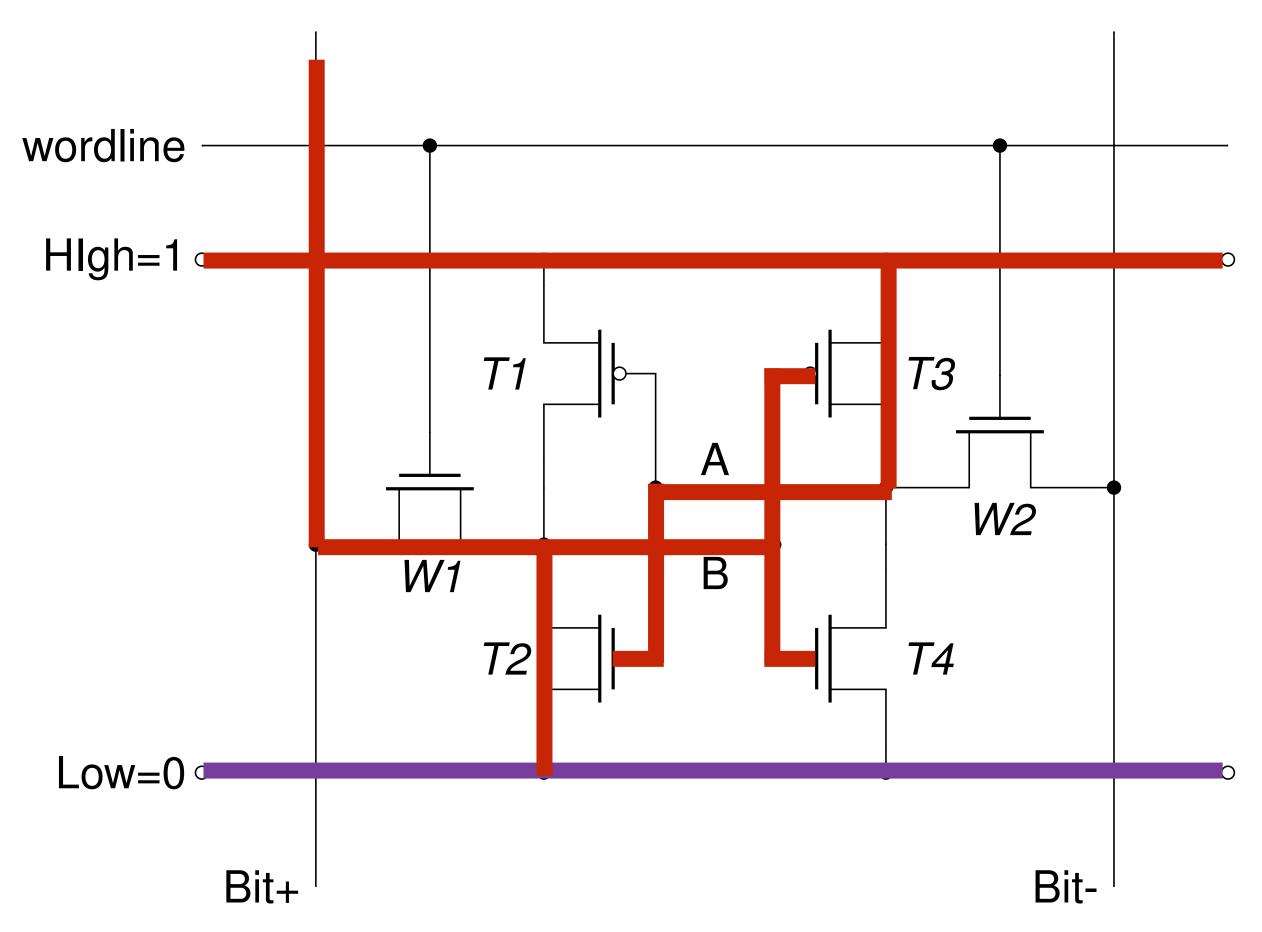
A=1 and B=0: wordline High



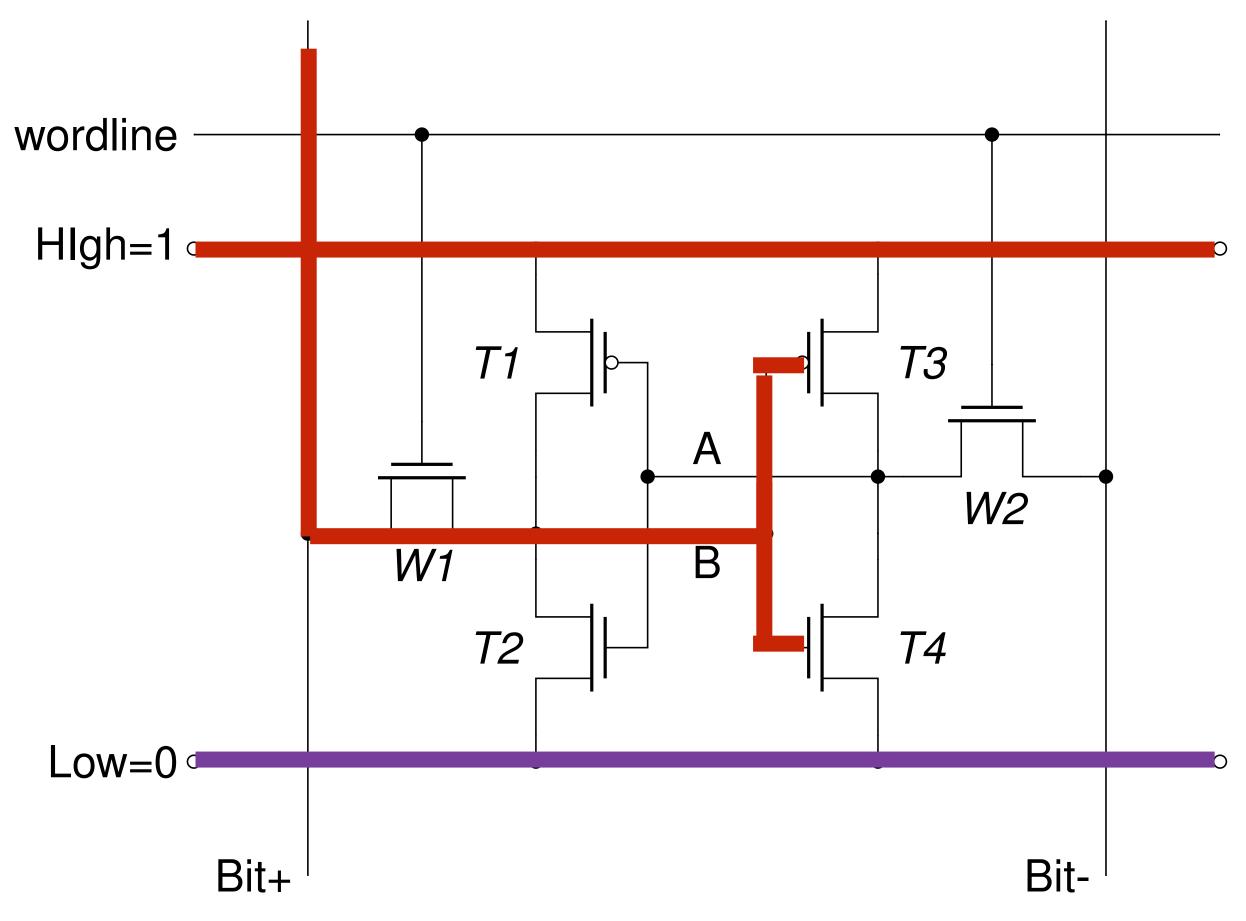
A=0 and B=1: wordline High



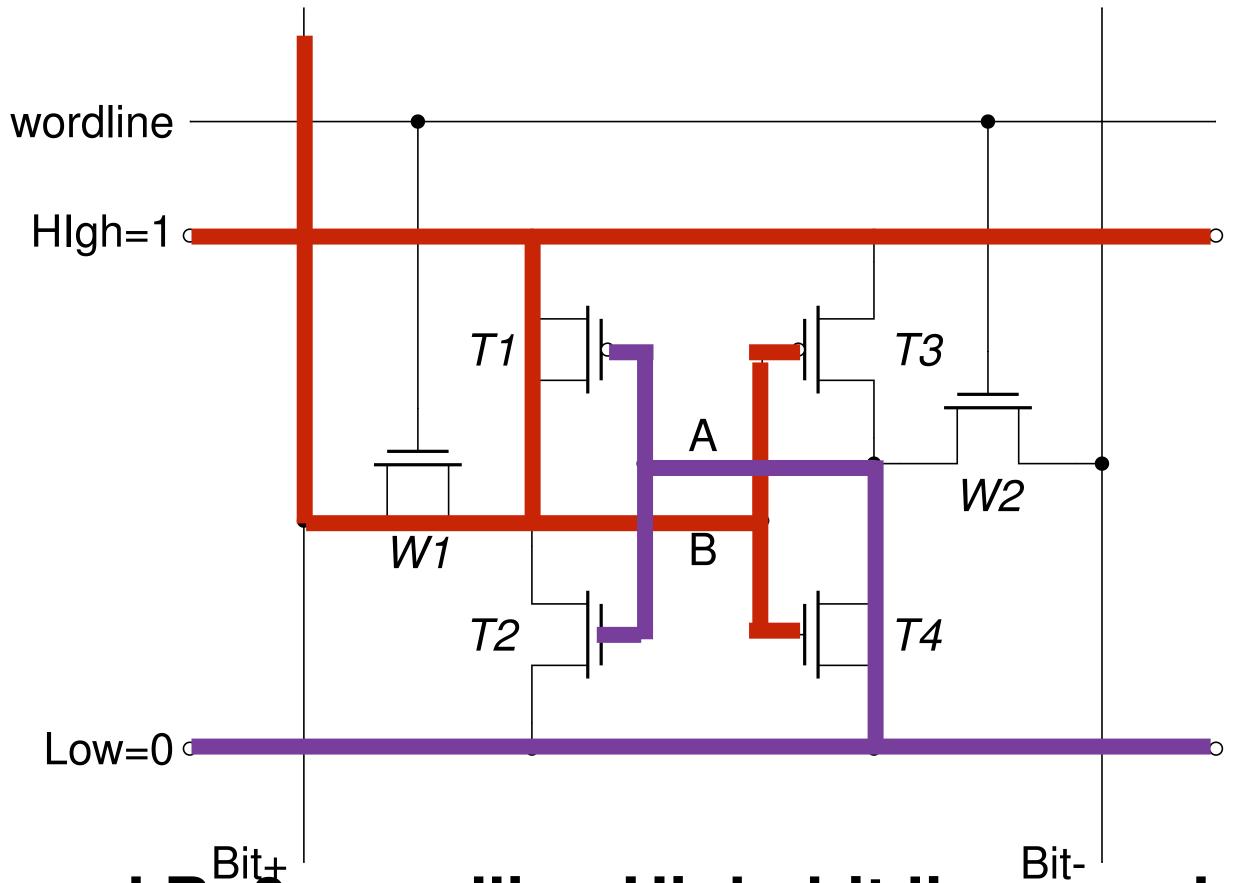
A=1 and B=0: wordline High bit lines as driver



A=1 and B=0: wordline High bit lines as driver



A=1 and B=0: wordline High bit lines as driver



A=1 and B=0: wordline High bit lines as driver Configuration flipped and stable

# Summary

