Queen Mary
University of London

Main Examination Period 2017-2018

ECS404U Computer Systems and Networks Duration: 2 hours 30 minutes

SOLUTIONS AND MARKING SCHEME

YOU ARE NOT PERMITTED TO READ THE CONTENTS OF THIS QUESTION PAPER UNTIL INSTRUCTED TO DO SO BY AN INVIGILATOR.

Instructions: This paper contains FOUR questions. **Answer ALL questions**. Cross out any answers that you do not wish to be marked.

Calculators are permitted in this examination. Please state on your answer book the name and type of machine used.

Complete all rough workings in the answer book and cross through any work that is not to be assessed.

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Exam papers must not be removed from the exam room.

Examiners: Dr A Alomainy and Prof E Robinson

Question 1

This question is about Computer Architecture

(a) Explain the function of each of these standard computer components

(i) central processing unit (CPU)

(ii) main memory

(iii) long-term memory

(iv) motherboard

[5 marks — basic]

Solution: A standard bookwork question.

(i) central processing unit (CPU): main unit that performs the actual computational operations

(ii) main memory: temporary storage of data for live processes

(iii) long-term memory: storage of data that is required to survive between processes or when the computer is turned off

(iv) motherboard: central communication network between the different components

One mark each definition if reasonably expressed, with one additional mark if well-written and grammatical.

(b) Figure 1, taken from course notes, shows the HP Proliant BL660c, a rack-mounted server. Draw a diagram of the von Neumann computer architecture and explain one way in which the Proliant conforms to the architecture, and one way in which it differs.

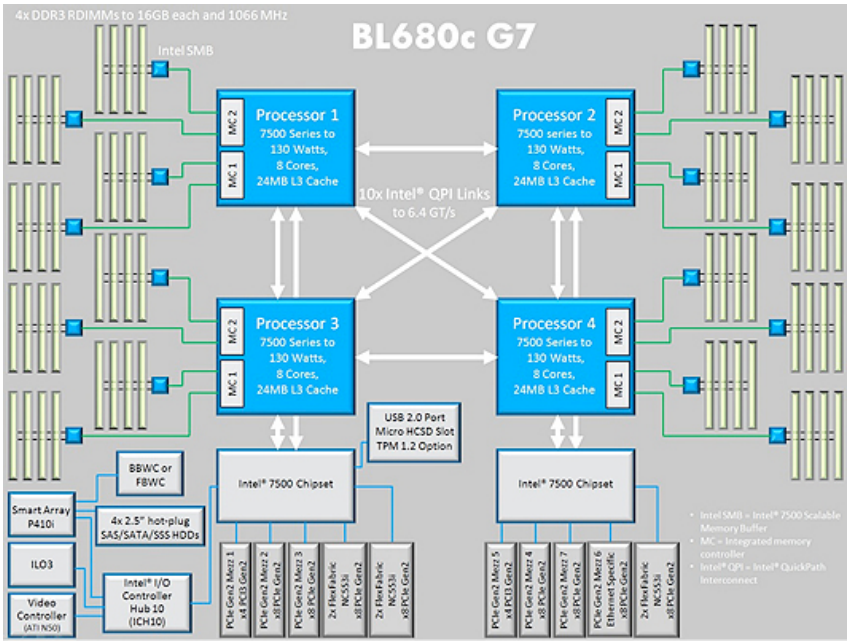
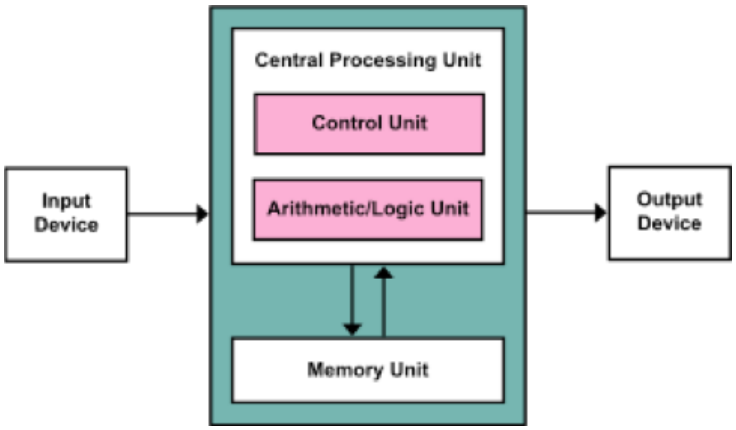


Figure 1: HP Proliant BL660c

[5 marks — basic]

Question continues on next page

Solution: Diagram as per notes should include memory, CPU, channel linking CPU and memory and some indication of IO.



Several possible answers for similarity and difference:

- Proliant also has similar components (CPU, memory, comms/IO)
- Proliant has memory communicating along single channel to CPU (each memory module links to single CPU).
- Proliant has multiple CPU's and separate memories.
- Internal comms architecture of Proliant is complex, not single channel.

2 marks for von Neumann. 2 for good diagram, 1 reasonable but significant flaws, 0 very poor or missing.
3 marks for similarity and difference. 3 if shows clear understanding of architectural differences well expressed, and makes no false statements. 2 if good but contains error. 1 if understandning unclear. 0 if nothing of merit.

(c) Explain the concept of *memory hierarchy*, give an example of a typical memory hierarchy and explain why the members of the hierarchy are in the order you have given. **[5 marks — medium]**

Solution: The memory hierarchy lists the storage mechanisms on a computer in order of proximity to the CPU Strictly this is in terms of the path data would follow, but there are other closely linked proxies for this: use of the computers comm's network, latency of response, etc.
A typical basic hierarchy might have:
cpu registers
main memory
disk memory
Students might also want to include various forms of cache.

Question continues on next page

Two marks for explanation of memory hierarchy
One mark for ordering
Two marks for example.

(d) Transistors as switches. The transistors used in VLSI have three connections: *gate*, *source* and *drain*.

(i) Explain the roles of these connections when the transistor functions as a switch.

(ii) Explain the difference between *nmos* and *pmos* transistors in terms of this functionality.

[5 marks — basic]

Solution:

(i) The gate is the switch control (the voltage at the gate determines whether the switch is open or closed). The source and drain are where the wire in and wire out are connected. The design is symmetric so there is no effective difference between them. When the switch is closed there is a connection between source and drain, and when it is open there is not.

(ii) A nmos is closed when there is a high voltage at the gate, open when there is not. A pmos is closed when there is a low voltage at the gate, open when there is not.

Three marks for explanation of switch. Two if correct but poorly expressed, one if some indication, but incorrect. Two marks for nmos v pmos. One if not completely clear, missing detail, or with difference inverted.

(e) Figure 2 shows a standard SRAM memory cell. Describe the two possible stable states it can be in (determined by the potential on A and B) when the two transistors at W1 and W2 are off so that when viewed as switches, these switches are open.

[5 marks — advanced]

Solution: T1+T2 forms an inverter with input A and output B. T3+T4 also forms an inverter with input B and output A. The only stable configurations are therefore when A and B are opposites, so both inverters are working correctly. In other words the states are when A is high and B is low, and when A is low and B is high.

5: clear structural understanding and good explanation

4: minor flaws in explanation

3: basically correct, but some serious fault

2: understanding at doubt

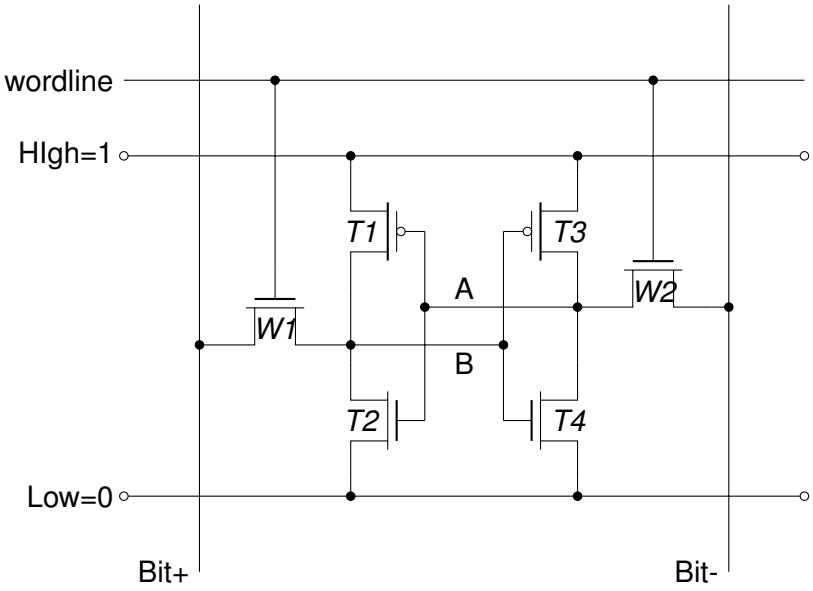


Figure 2: SRAM memory cell

1: does not demonstrate any real understanding

0: nothing of any merit produced

Question 2

This question is about forms of digital representation.

(a) This part is about the binary representation of (unsigned) numbers, and addition and multiplication in binary.

(i) The following bit sequences represent unsigned integers in binary form. Translate them to standard decimal explaining your reasoning:

- `0010 1101`
- `0001 0101`

(ii) Using the standard *binary long addition* algorithm, compute the *sum* of `0010 1101` and `0001 0101` as unsigned binary integers. Your answer should also be an unsigned binary integer.

(iii) Using the standard *binary long multiplication* algorithm, compute the *product* of `0010 1101` and `0001 0101` as unsigned binary integers. Your answer should also be an unsigned binary integer.

[8 marks — basic]

Solution:

(i) • $0010\ 1101_2 = 32 + 8 + 4 + 1 = 45_{10}$

Question continues on next page

- $0001\ 0101_2 = 16 + 4 + 1 = 21_{10}$

(ii)

```
  00101101
  00010101  +
----------
  01000010  ans
----------
  1111 1    carries
```

(iii)

```
     00101101
     00010101  *
-------------
     00101101
   0010110100
001011010000  +
-------------
  1110110001  ans
-------------
    111111    carries
```

(i) 3 marks: 2 if minor errors: 1 if major issues: 0 if nothing of value

(ii) 2 marks: 1 if algorithm clear but errors

(iii) 3 marks: 2 if minor errors: 1 if major issues: 0 if nothing of value

(b) This part is about binary representation of signed integers.

(i) Explain how 8-bit two's complement represents negative numbers, using the example of the representation of the decimal number -30.

(ii) Give one key reason why computers use two's complement to represent signed integers, rather than, as we do, a direct representation of sign and magnitude.

[5 marks — medium]

Solution:

(i) In n-bit two's complement the leading bit represents -2^{n-1}, so in 8-bit two's complement it represents -128. The remaining bits represent positive powers of 2 as in ordinary unsigned notation. So to represent -30 we will have a leading 1 representing -128, and the remaining bits have to represent $128 - 30 = 98$. Now $98 = 64 + 32 + 2$ so 98 unsigned is `110 0010` (using 7 bits) and -30 is that with a leading 1: `1110 0010`.

(ii) The key reason is that it makes for algorithmic simplicity, notably addition and multiplication use the same algorithms as for unsigned representations and hence can use the same circuitry.

(i) 3 marks: 2 if minor issues, 1 if major, 0 if nothing of value

(ii) 2 marks, 1 if basically correct but unclear.

(c) This part is about the concept of byte and the difference between Big and Little Endian

Question continues on next page

representations.

(i) Explain what is meant by a *byte*.

(ii) 32-bit two's complement is a representation of signed integers using 32 bits, but can (in principle) be implemented as either big or little endian. Explain the difference between big and little endian using the byte sequence:

01111001 11110001 11110010 11110011

You do not need to calculate exactly which numbers this represents in the two forms, but do need to explain the difference.

[5 marks — advanced]

Solution:

(i) A *byte* is 8 bits.

(ii) In both Big Endian and Little Endian the order within a byte is the same. But in Big Endian the high order bytes are stored first, while in Little Endian, they are stored last (reversing the order of the bytes as we read them). So in Big Endian this byte sequence represents the bit sequence

01111001111100011111001011110011

which is a positive number. And in Little Endian the byte sequence represents the bit sequence

11110011 11110010 11110001 01111001

which is a negative number.

(i) 1 mark, all or nothing

(ii) 4 marks. 1 for being clear order inside byte is same, 1 for being clear about abstract distinction, 1 for writing down correct explicit examples, 1 for being able to distinguish numbers.

(d) This part of the question is about hexadecimal, binary and text representation.
The following sequence is obtained as the hex dump of the contents of a short text file encoded in ASCII. For the avoidance of confusion, we are using modern ASCII where characters are 8 bits:
`4153 4349 4931 3233 3461 7363 6969`
Recall that the ASCII code for the character '0' (zero) is 48, for the character 'A' it is 65, and for the character 'a' it is 97 (these are expressed in decimal).

(i) Give the bit sequences represented by:

- The first group of four hex digits: `4153`
- The third group of four hex digits: `4931`

Question continues on next page

Explain how you reach your answers.

(ii) Given that character codes are each 8 bits, translate the second group of four hex digits into two decimal codes, each between 0 and 127.

(iii) Explaining your reasoning, what character sequence is represented by the entire sequence given above?

[7 marks — advanced]

Solution:

(i) Translate character by character, with each going to four bits:
4153_{16} = 0100 0001 0101 0011
4931_{16} = 0100 1001 0011 0001

(ii) 4349: we translate 43 and 49 separately.
$43_{16} = 4 * 16 + 3 = 64 + 3 = 67_{10}$
$49_{16} = 4 * 16 + 9 = 64 + 9 = 73_{10}$

(iii) Working similarly, decimal character codes are:

65 83 67 73 73 49 50 51 97 115 99 105 105

This is "ASCII123ascii".

(i) 2 marks total. 1 for algorithm right, 1 for accuracy.

(ii) 2 marks total, 1 or algorithm right, 1 for accuracy.

(iii) 3 marks total. 1 marks for understanding method and 2 marks for accuracy (1 if minor errors).

Question 3

This question is about Assembly Language

(a) Explain the main cause of processing delays in executing programs and functions as linked to memory and data exchange and highlight a solution commonly used in computer architectures to overcome this bottleneck issue. **[4 marks]**

Solution: One of the main bottleneck issues in processing programs on a computer is the expected delay in exchanging data and programs between the CPU and the computer main memory. One significant solution is the use of locality rep[resented by various levels of caching.

Difficulty: Basic.

2 marks for appropriate explanation about delays caused by calling function and data exchange between the CPU and main computer memory. 2 marks for mentioning the solution above.

Question continues on next page

(b) Explain what a register is, and where arithmetic operations take place in a computer. Explain what the MIPS instruction

```
li  $t0  30
```

does, where $t0 is a register, and where z is a location in the main memory and how it is different that $la . Explain also what the MIPS instruction

```
sw  $t1  x
```

does, where $t1 is a register, x is is a memory location.

[4 marks]

Solution: A register is a special piece of fast memory inside the CPU where all arithmetic operations take place. The first instruction loads an immediate value (30 in this case)onto register $t0 while $la is used to load the address of a variable. The second instruction stores the value in register $t1 into memory location x. 'sw' stands for store word and 'lw' stands for load word.

Difficulty: Medium.

1 mark for explaining register and 1 mark for mentioning arithmetic operations take place in the CPU. 1 mark each for correct explanation of the two instructions in addition to 1 mark for explaining how $la is different.

(c) Mention three methods that are used by the MIPS Assembler to get data into the program.

[3 marks]

Solution: There are basically three methods of getting data into the program: 1 Within something like an addi instruction 2 Using a data directive in the data segment 3 Using a syscall to do input

Difficulty: Basic.

1 mark for eac h method correct above.

(d) Explain what the MIPS instruction

```
div  $t1  $t0
```

does, where $t0, and $t1 are registers. Would the instruction store the outcome in one register? If not then explain your answer by describing exactly where it will be saved.

[7 marks]

Solution: The instruction divides $t1 by $t0 and puts the quotient in $LO and the remainder in $HI by using $mflo and mfhi

Question continues on next page

Difficulty: Advance.
3 marks for identifying the correct operation performed by the instruction and 2 marks for $LO register and 2 marks for $HI

(e) Now write a MIPS program that will load the numbers 40 and 80 into registers $t0 and $t1, respectively, and then divides $t1 by $t0 . Then the program should store the full division results into registers $t2 and $t3 followed by storing in memory locations w and z, respectively. **[7 marks]**

Solution:

```
li $t0 40
li $t1 80
div $t1 $t0
mflo $t2
mfhi $t3
sw $t2 w
sw $t3 z
```

Difficulty: Medium.
1 mark for each correct loading instruction. 1 mark for the 'div' instruction and 1 mark each for the $mfhi and mflo and 1 mark each for the store instructions. the word into memory z and 1 mark for the correct sequence of execution.

Question 4

This question is about Computer Networks

Figure 3 shows the Wireshark program displaying a packet it has captured (we are looking at packet No. 338 below towards the end of the top pane).

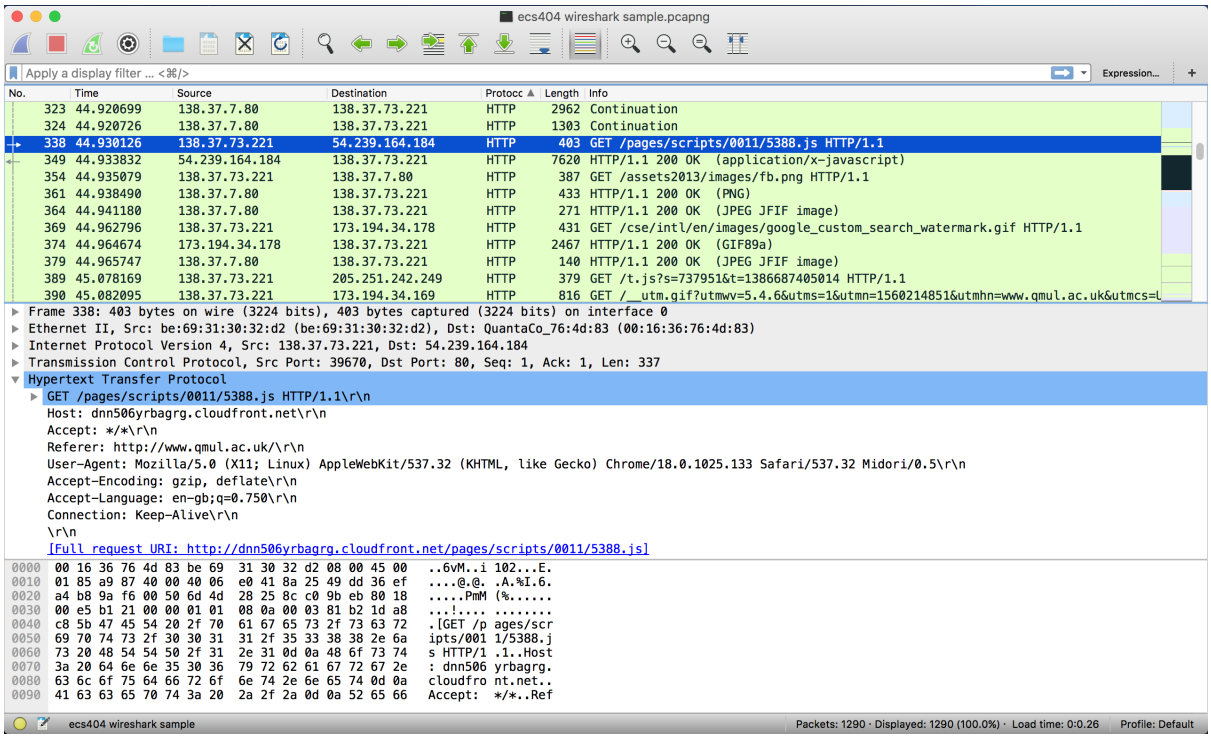


Figure 3: Wireshark display of packet 338

(a) Which protocols are being used in the following layers:

i) application

ii) transport

iii) internet

iv) link

In each case identify how you know the answer from the screenshot.

[5 marks]

Solution: Wireshark was used in the labs for this module and the students should be able to identify from the middle pane related to packet 338 that; Application: Hypertext Transfer Protocol (HTTP), Transport: Transmission Control Protocol (TCP), Internet Protocol version 4 (IPv4) and Link: Ethernet II.

Difficulty: Basic.

1 mark for each correct identified protocol (total of 4 marks) and also 1 mark for specifying that it is in the middle pane of the Wireshark window.

Question continues on next page

(b) Identify the source and destination IP addresses for this specific packet and explain what message is being sent. How is packet (338) related to packet (349)?

[6 marks]

Solution: The sender IP address is 138.37.73.221 and the destination one is 54.239.164.184. This is a HTTP request to get access to a webpage on the network cloudfront.net. Packet 349 is an acknowledgement of packet 338 request to access the webpage.

Difficulty: Advance.

1 mark for identifying the sender IP address and 1 mark for the destination one, 2 marks for the identification it is a request to access a webpage and 2 marks for correctly relating packet 349 to 338.

(c) Which 'ports' are being used (packet 338) and what is their function?

[4 marks]

Solution: The port on the destination is 80, and the one on the source is 39670. The port is used by the transport layer to identify the program sending the message on the source machine (hence the program expecting a reply), and the program on the destination machine for which the message is intended.

Difficulty: Medium.

1 mark for each port number and 2 marks for identifying it is used for transport layer communication.

(d) Packets are used in computer networking to encapsulate messages and important information for communications between different machines and ports. What are packets called for TCP (Transmission Control Protocol) and IP (Internet Protocol)? What is SMTP and what is it used for?

[4 marks]

Solution: TCP packets are called segments and IP packets are called datagrams. SMPT is Simple Mail Transfer Protocol used in mailing for sending messages and mainly used on the transmitting side.

Difficulty: Basic.

1 mark for each correct answer above. 2 marks for defining SMPT and its function.

(e) Networks work in one of two ways; circuit-based and packet-based networking. Explain each type with examples and explain whether modern networks are circuit or packet-based. **[6 marks]**

Question continues on next page

Solution: Circuit-based: you set up a persistent connection between two points on the network. Classic example: telephones. When you make a call there is a persistent connection between caller and receiver. Packet-based: you send information in individual dollops, each piece contained in a packet which tells the network where to deliver it. Classic example: the postal service Modern networks are mainly packet-based

Difficulty: Medium.

1 mark each for defining each type and 1 mark for each example. 2 marks for specifying that modern networks are network-based.

End of questions