moduleMA

//

Flow Status Successful - Sun May 7 18:25:47 2017
Quartus II 32-bit Version 13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name MA
Top-level Entity Name MA
Family Cyclone IV E
Device EP4CE30F23I7
Timing Models Final
Total logic elements 246 / 28,848 (< 1 %)
Total combinational functions 226 / 28,848 (< 1 %)
Dedicated logic registers 147 / 28,848 (< 1 %)
Total registers 147
Total pins 78 / 329 (24 %)
Total virtual pins 0
Total memory bits 32,768 / 608,256 (5 %)
Embedded Multiplier 9-bit elements 0 / 132 (0 %)
Total PLLs 0 / 4 (0 %)

FMax 77.71MHz

```
////////////////////////////////////////////////
module MA(
	input clock, reset,
	input [2:0] WBaddress,
	input [3:0] control, //3: MemRead, 2: MemWrite
	input [15:0] ALUresult,
	input [15:0] Ra,

	output reg [2:0] WBaddress_,
	output reg [1:0] control_,
	output reg [15:0] ALUresult_,
	output reg [15:0] LDresult_
	);

	wire write;
	wire [15:0] LDresult;
```

```
	//clock moving
	always @(posedge clock)
	begin
		if(reset == 1)begin
			WBaddress_ <= WBaddress;
			control_ <= control[1:0];
			ALUresult_ <= ALUresult;
			//LDresult_ <= LDresult;
		end else begin
			WBaddress_ <= 3'b000;
			control_ <= 2'b00;
			ALUresult_ <= 16'b0000_0000_0000_0000;
			//LDresult_ <= 16'b0000_0000_0000_0000;
		end
	end

	assign write = control[2] & ~control[3];

	ram2 memory(.address(ALUresult),
				.clock(clock),
				.data(Ra),
				.wren(write),
				.q(LDresult));
	always begin
		if(reset == 1)begin
			LDresult_ = LDresult;
		end else begin
			LDresult_ = 16'b0000_0000_0000_0000;
		end
	end



endmodule
```