Quantum Control Electronics

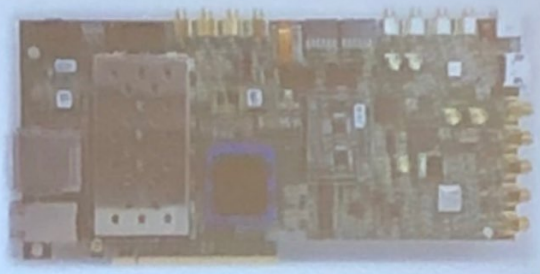
Enables programmable real-time IF waveform generation and readout signal processing

2 DAC Channels to generate control pulses and/or readout pulses

2 ADC Channels for capturing readout signals

FPGA based Micro control Sequence Processor

Programmable instruction set to sequence waveform generation from local memory with deterministic latency



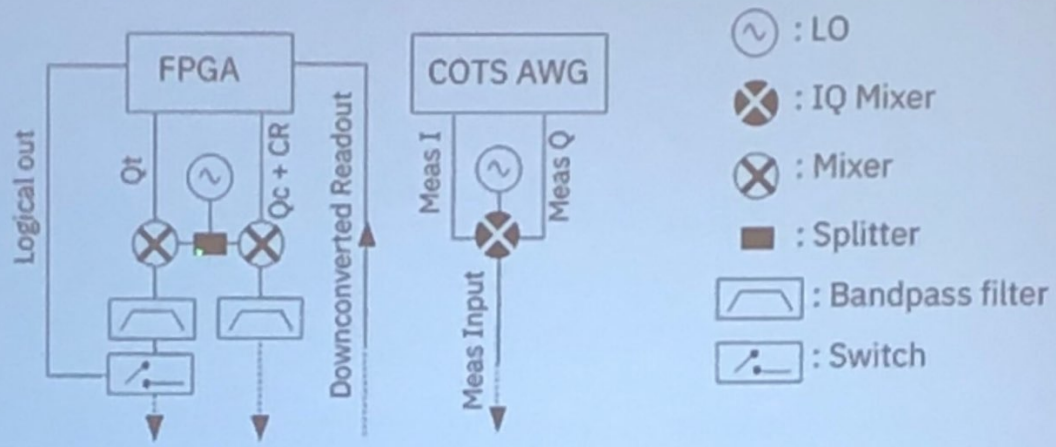
Implements branch conditions for pulse sequences

Branches are based on readout state determination (if-then-else, goto)

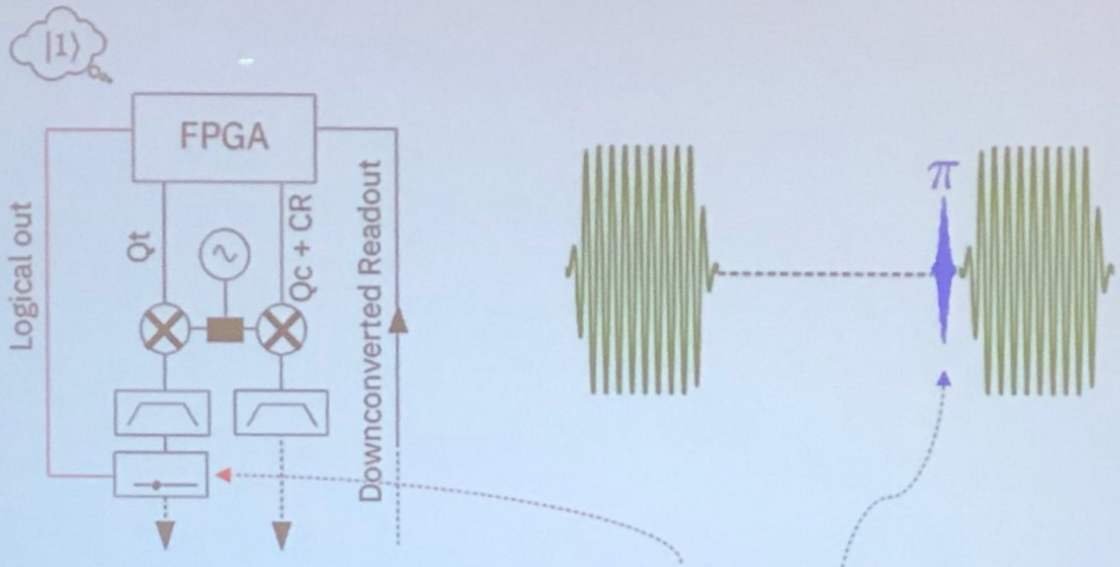
Sequences are aligned to 8 or 16 samples

Readout state determinations a shared across multiple on a local bus to enable conditions based on several qubit outcomes

Experimental setup

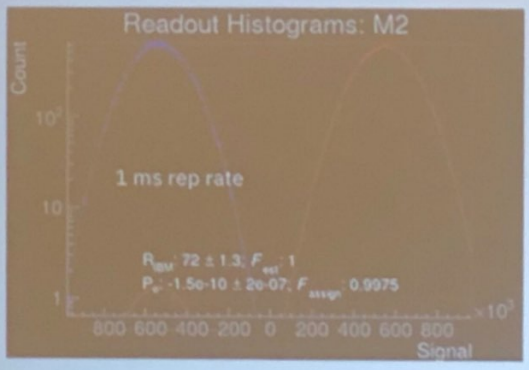


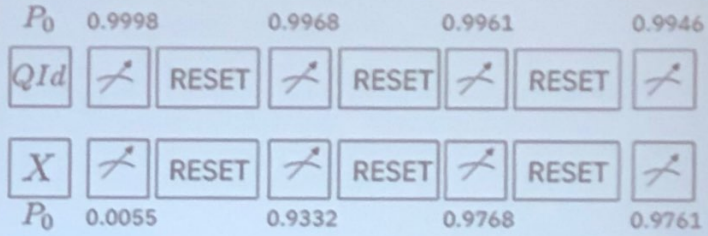
Qubit reset using FPGA logic

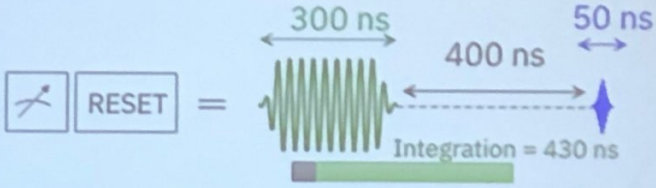


FPGA decision activates switch trigger that gates the qubit reset pulse

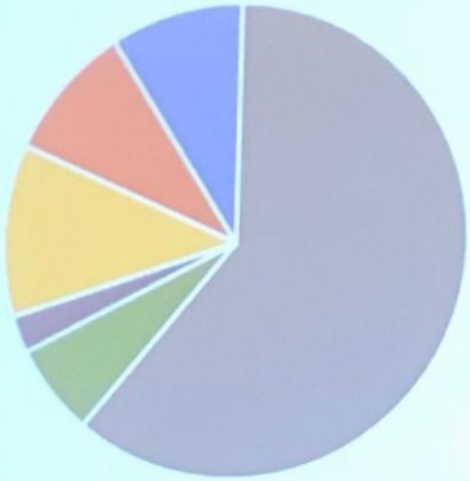
Ground state population vs number of reset operations







FPGA latency budget breakdown



- Sampling: 480
- Conditional Reset Pulse: 50
- Output Debounce: 20
- FPGA Integration Logic: 92
- ADC Chip: 72.2
- Cable Delay: 72

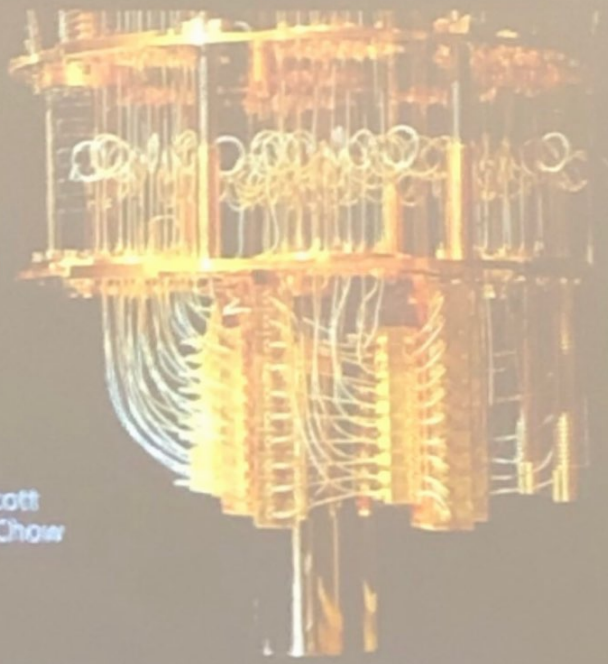
Total: 786.2ns

Device dependent (quantum):
measurement: 300 (sampling: 480)
Reset Pulse: 50
Cavity emptying: ~300ns
total: 650ns

Fixed delays (classical):
Output Debounce: 20
ADC Chip: 72.2
FPGA Integration Logic: 92
Cable Delay: 72
total: 256.2ns

Measurement cycle = 800ns

Evaluating the performance of classical electronics for quantum computing tasks in superconducting qubit systems



Antonio Córcoles, Maika Takita, Ken Inoue, Scott Lekuch, Abhinav Kandala, Jay Gambetta, Jerry Chow

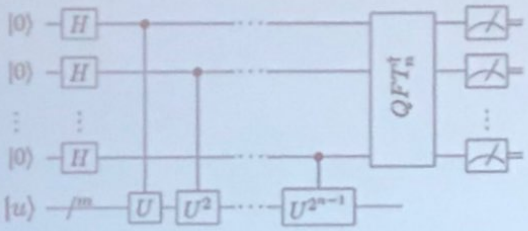
IBM T.J. Watson Research Center

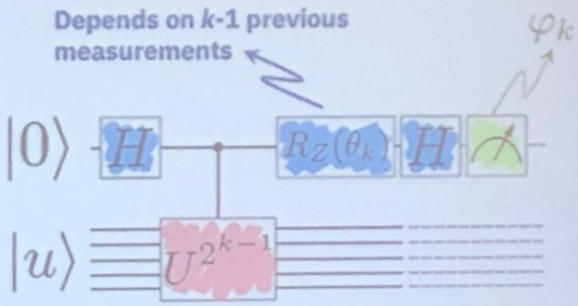
V26.2

IBM Q

Iterative Quantum Phase Estimation Algorithm

Replace the pointer qubit register by a single qubit and iteratively encode and retrieve ϕ one bit at a time





Atomic flux pulses for a superconducting quantum processor

part 1:
Real-time corrections and repeatability of flux pulses

part 2:
Performance and benefits of net-zero conditional-phase gates

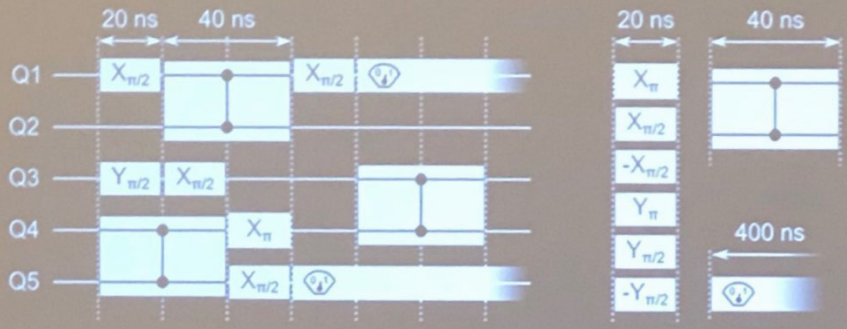
Filip K Malinowski,
M Adriaan Rol,
Livio S Ciorciaro,
Brian M Tarasinski,
Yves Salathe,
Niels Haandbaek,
Jan Šedivý,
Leonardo DiCarlo

TU Delft

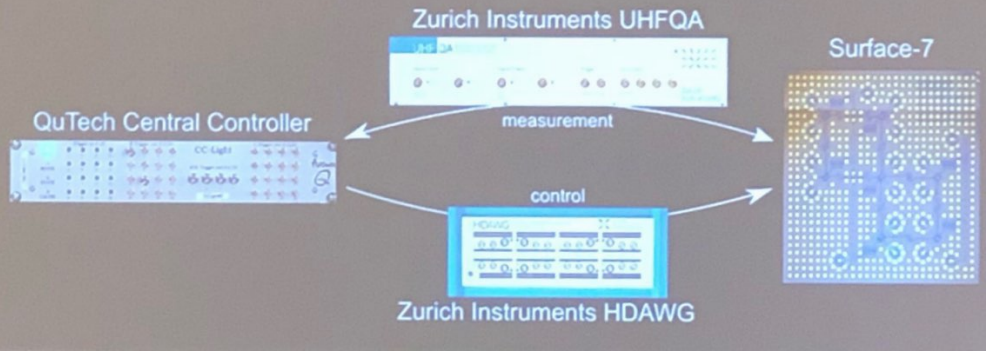
QuTech

Zurich Instruments

Quantum processor with 20 ns clock

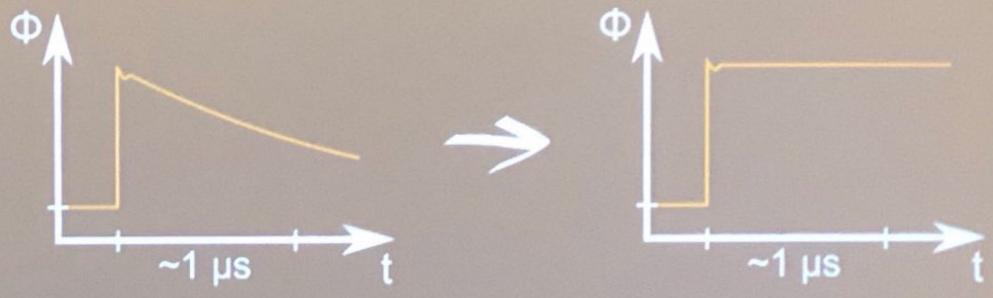


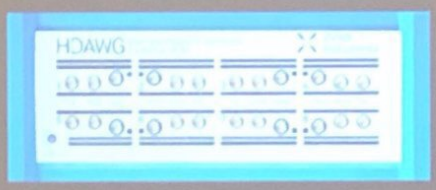
Fu, Proceedings MICRO-50, 2017
Fu, Proceedings HPCA, 2019

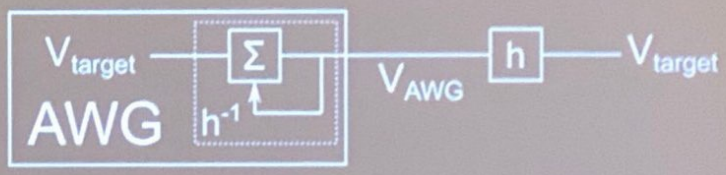


Real-time Infinite Impulse Response filter

- dedicated to long timescales (20 ns to 10 μs)
- implemented in hardware in a real-time (no precompilation)

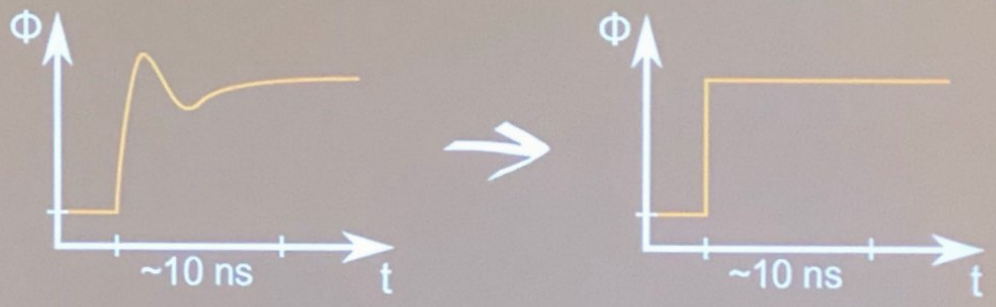






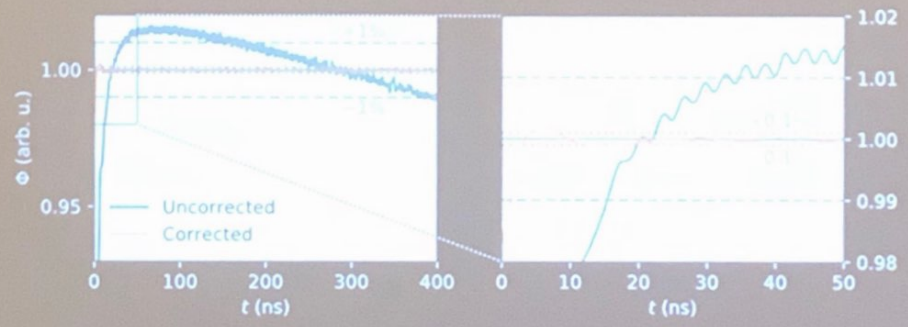
Finite Impulse Response Filter

- dedicated to short timescales (< 20 ns)
- precompiled
- waveform convolved with 10-ns-long inverter response function



Optimized step response

- 4 Infinite Impulse Response filters
- 1 Finite Impulse Response filter
- 0.1%–accurate step response



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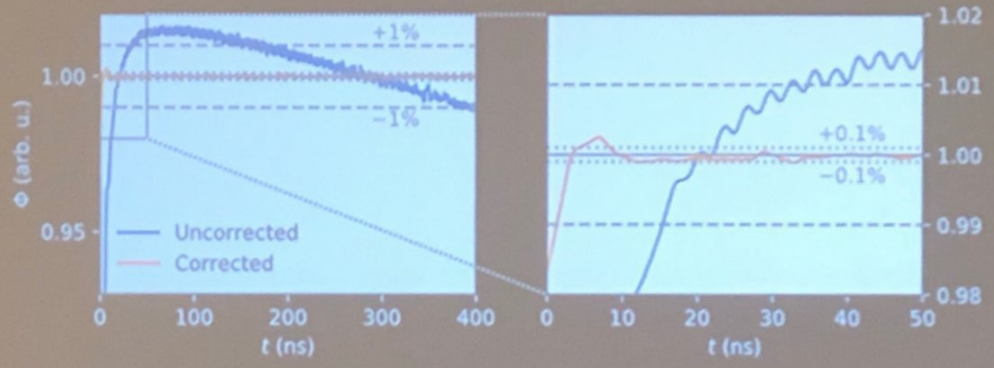
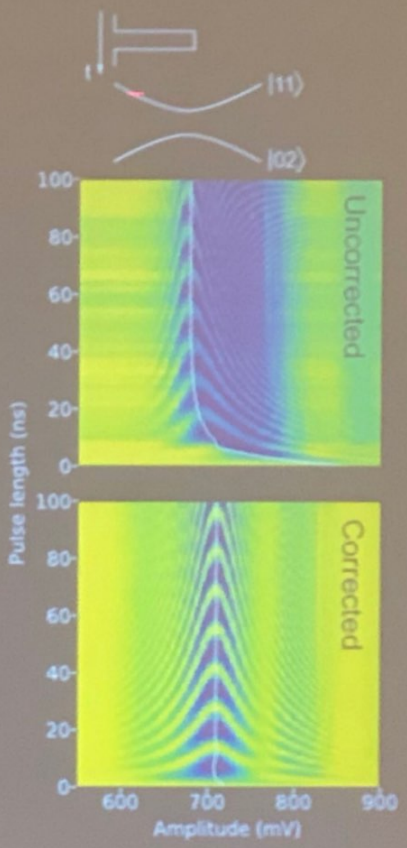
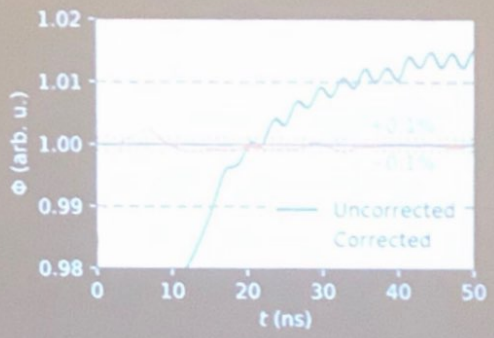




Summary

- Cryoscope uses qubit to measure flux-pulse distortions in-situ
- Long-timescale predistortion are applied in real-time, without precompilation
- With predistortions step-response accurate up to ~0.1%



Part 2:

Performance and benefits of Net-Zero conditional-phase gates

M Adriaan Rol et al.

$F = 99.1\%, L = 0.1\%$

MA Rol arXiv 1903.02492

Support:

Atomic flux pulses for a superconducting quantum processor part 2:

Performance and benefits of Net-Zero CZ gates

M. Adriaan Rol, F. Battistel, F. K. Malinowski, C. C. Bultink, B. M. Tarasinski, R. Vollmer, N. Haider, N. Muthusubramanian, A. Bruno, B. M. Terhal, L. DiCarlo

ArXiv: 1903.02492

TU Delft

QuSurf

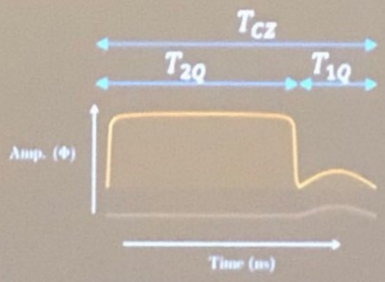
Motivation

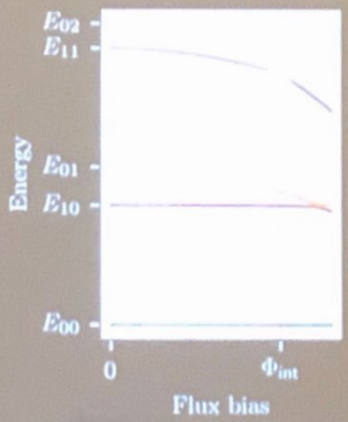
Flux-pulsed CZ gate

- Pulse into resonance with $|11\rangle \leftrightarrow |02\rangle$ avoided crossing
- $|11\rangle$ acquires conditional phase:

$$\phi_{2Q} = \varphi_{11} - \varphi_{01} - \varphi_{10}$$

$$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & e^{i\varphi_{01}} & 0 & 0 \\ 0 & 0 & e^{i\varphi_{10}} & 0 \\ 0 & 0 & 0 & e^{i\varphi_{11}} \end{pmatrix} \Rightarrow \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \end{pmatrix}$$



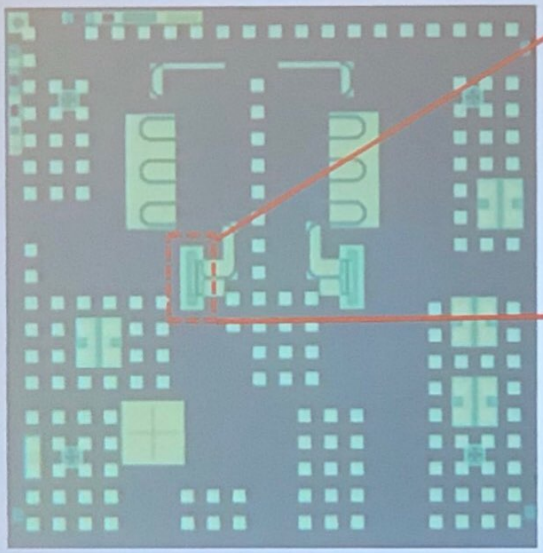


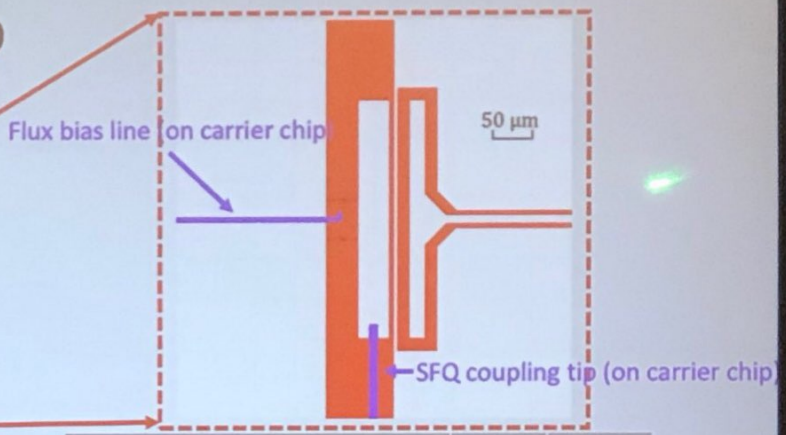
- ✓ Fast → High fidelity
- ❖ Pulse too fast → Leakage
- ❖ Distortions → History dependence
- ❖ (Low-frequency) flux noise → Dephasing

} Net-Zero

Theory: Strauch *et al.* Phys. Rev. Lett. (2003)
Experiment: DiCarlo *et al.* Nature (2009)
Fast-adiabatic pulsing theory: Martinis and Geller Phys. Rev. A (2014)

Quantum (flipped) Chip





Designed Value	left	right
Cavity frequency (GHz)	6.07	6.45
SFQ-Qubit coupling (aF)	380	250
Qubit frequency (GHz)	5	5
Qubit anharmonicity (MHz)	220	220
Qubit flux bias mutual inductance (pH)	2	2

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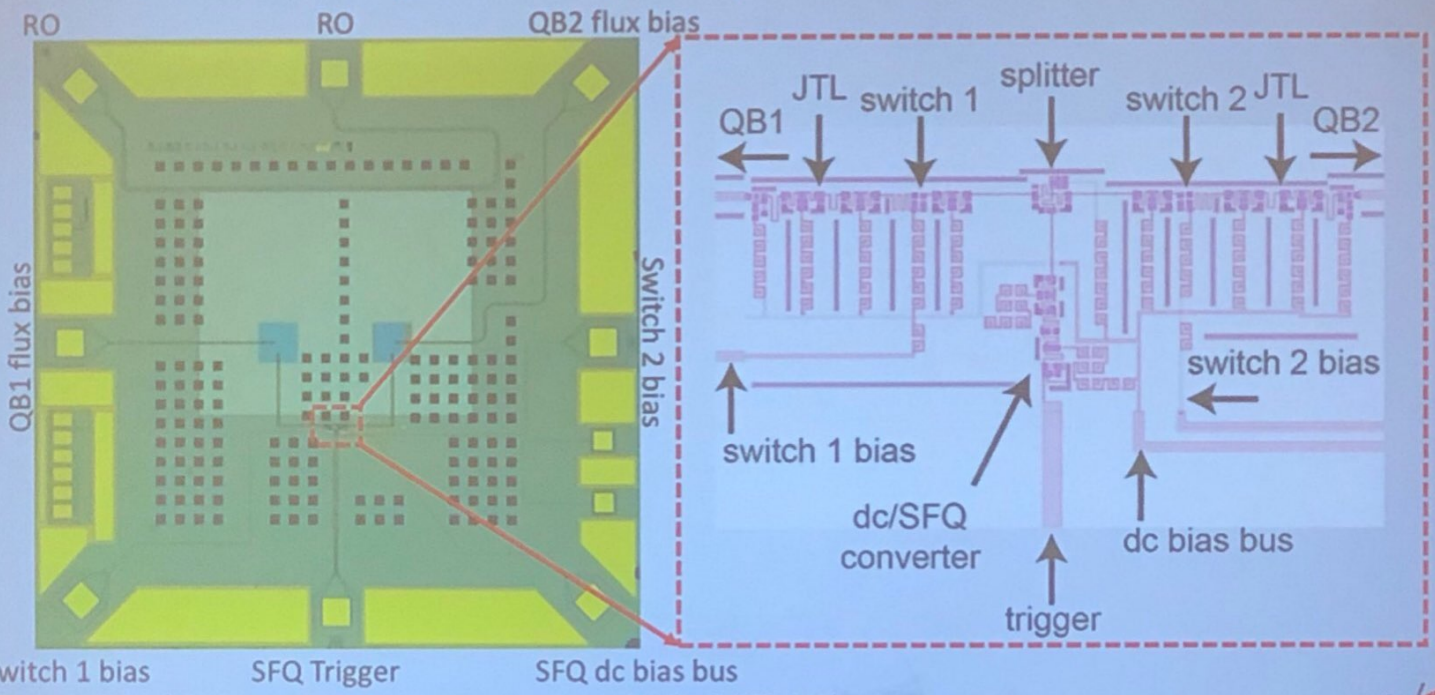
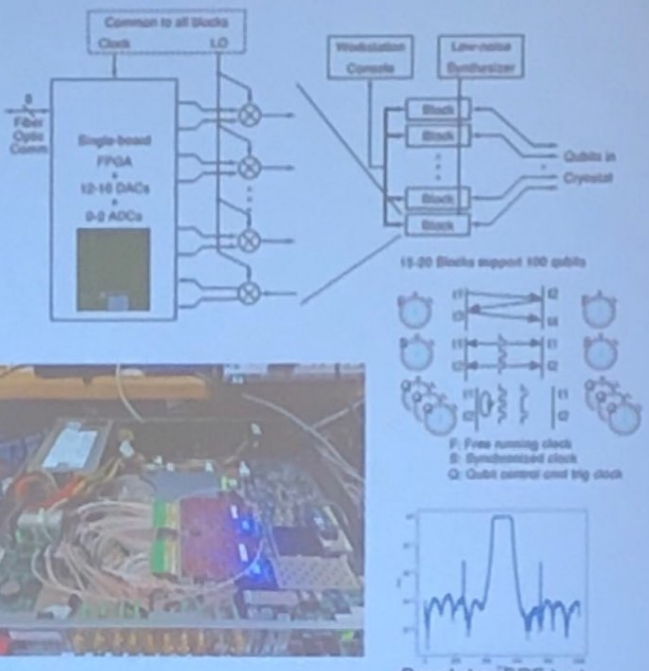
SFQ Control (Carrier) Chip



C. H. Liu - cliu447@wisc.edu

QubiC Hardware

- Single-board FPGA+DACs+ADCs board
- Start with evaluation boards
  - Xilinx VC707 evaluation board
    - Virtex 7 FPGA
    - Dual HPC FMC
    - SFP module connector
  - Abaco Systems (4DSP) FMC120
    - Quad channel 16 bit DAC @1.25GSPS
    - Quad channel 16 bit ADC @ 1GSPS
  - Digital IO pins for triggers
  - External clock @ 1GHz



Bench top BPF test

WHY ATAP ?

ACCELERATOR TECHNOLOGY & APPLIED PHYSICS DIVISION

- Typical qubit control frequency ranges between 5-7 GHz
- Challenges such as clock synchronization and removing sampling aliases and jitters are met by ATAP Division's expertise on high-frequency control

One technology to control both!

Xilinx Virtex-7 FPGA VC707 + FMC120 chassis

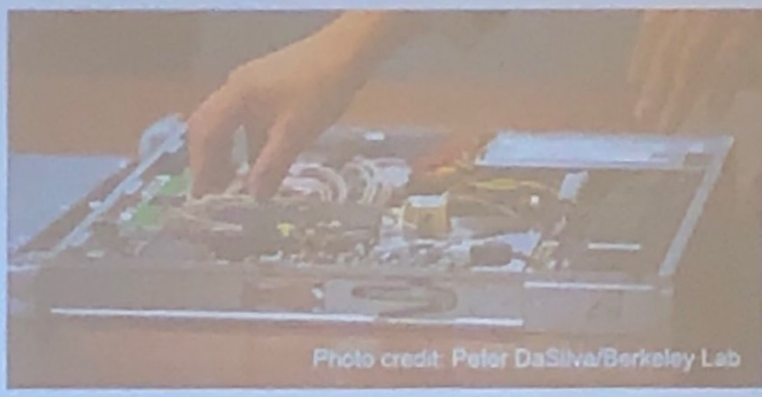
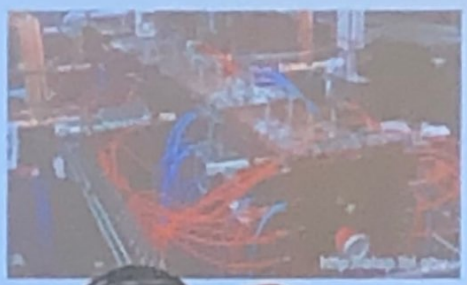
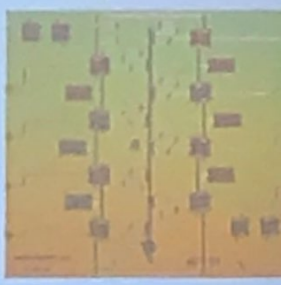


Photo credit: Peter DaSilva/Berkeley Lab





Qubit