SME 321 report

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1. Introduction

In this assignment, we'll delve into the design of four photomask layers, each associated with one of the four steps in the inverted LED chip's DBR process. We will utilize AutoCAD software to bring these photomasks to life. These four photomask layers comprise MSA, ISO, PSV, and PAD. These layers are pivotal in the chip design process, facilitating precise execution of each manufacturing step.

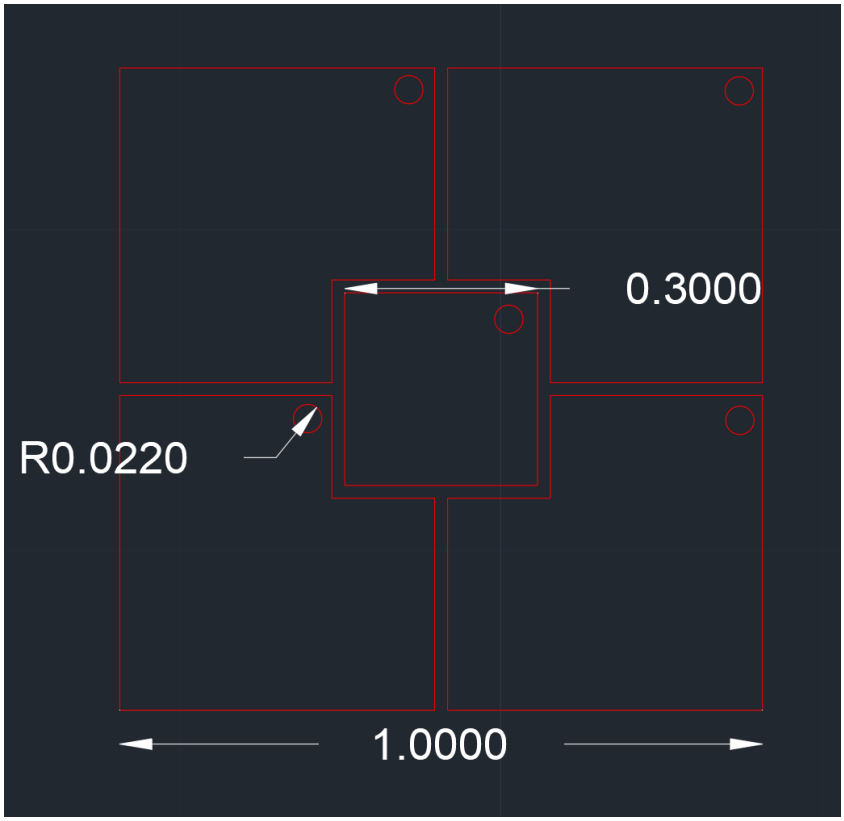
2. Details of the layout design for an individual component

(1) MSA

In the context of this first step, we will focus on 'MSA Yellow Light Defines Chip Patterns' and 'MSA Etching to Define Chip Patterns.' Specifically, for this task, we are only required to produce the outermost MSA layer structure and the internal via structures.

Details:

- To draw a 1mm x 1mm square chip on the MSA layer and divide it into five sections
- Since my ID follows the format '1211ABCD' with an even 'B,' I want to create a 0.3mm by 0.3mm square in the center and divide the surrounding area into four equal parts.
- MSA vias with a process requirement of a 22μm radius have been drawn



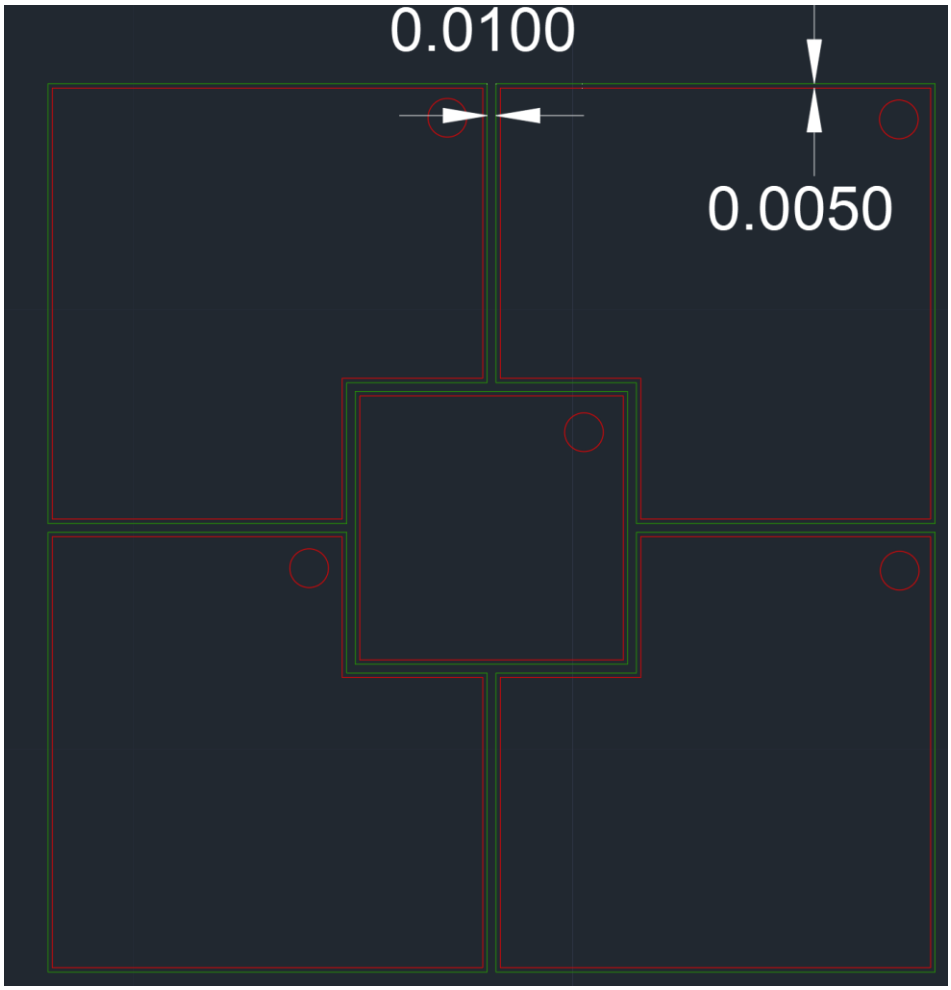
Note: In this report, all units for annotations are in millimeters (mm).

(2) ISO

The ISO regions serve the purpose of separating and isolating various areas within the chip design. For this specific task, we are only required to create the outermost ISO layer structure.

Details:

- Next, draw the ISO layer to isolate different regions.
- The process requirement for ISO-MSA is 5μm, and the process requirement for ISO-ISO is 10μm.

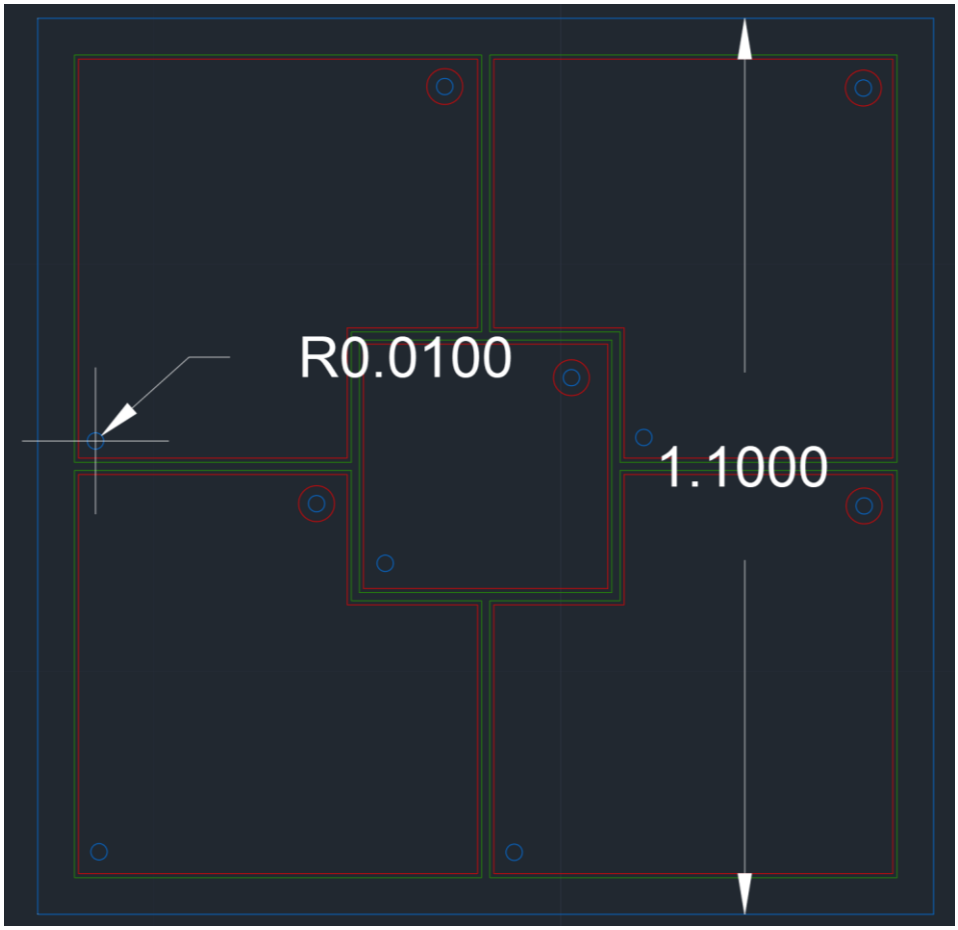


(3) PSV

In the following steps, we will continue to elaborate on the process as follows:
This task involves the creation of the PSV layer, where SiO2 is deposited to a thickness of 3600Å. This process comprises three key steps: PSV deposition, PSV photolithography, and PSV etching. Our objective is to generate the graphics for the outermost PSV layer structure and the internal via structures.
Furthermore, in a more detailed operation, we will proceed to draw the PSV layer to isolate the positive and negative terminals of the devices, leaving only the vias exposed for subsequent PAD deposition.

Details:

- The PSV process requirements entail a 10μm radius for vias
- A square with a side length of 1.1mm for the outermost perimeter.

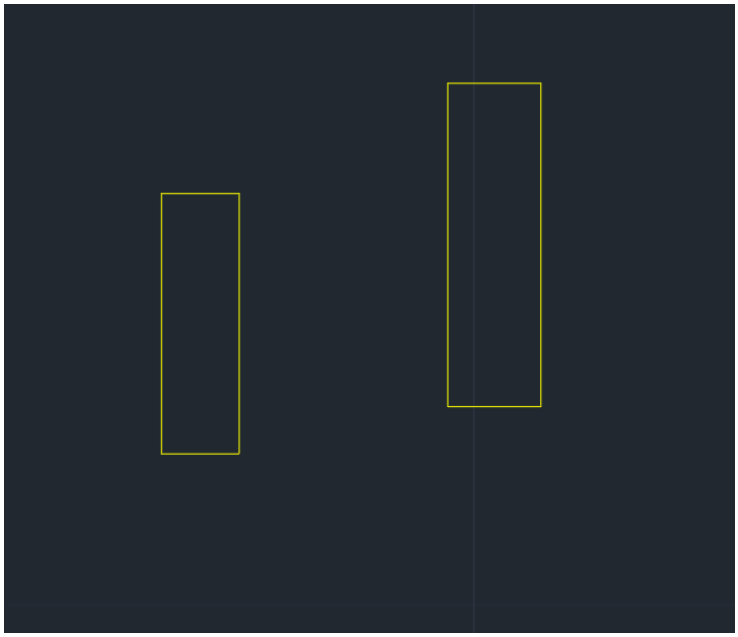


(4) PAD

Moving forward, we delve into the PAD layer processing, which involves two significant steps: PAD photolithography and PAD deposition.

Here, we emphasize that the PAD areas should exclusively cover the via regions, and the distinction between the positive and negative terminals is essential.

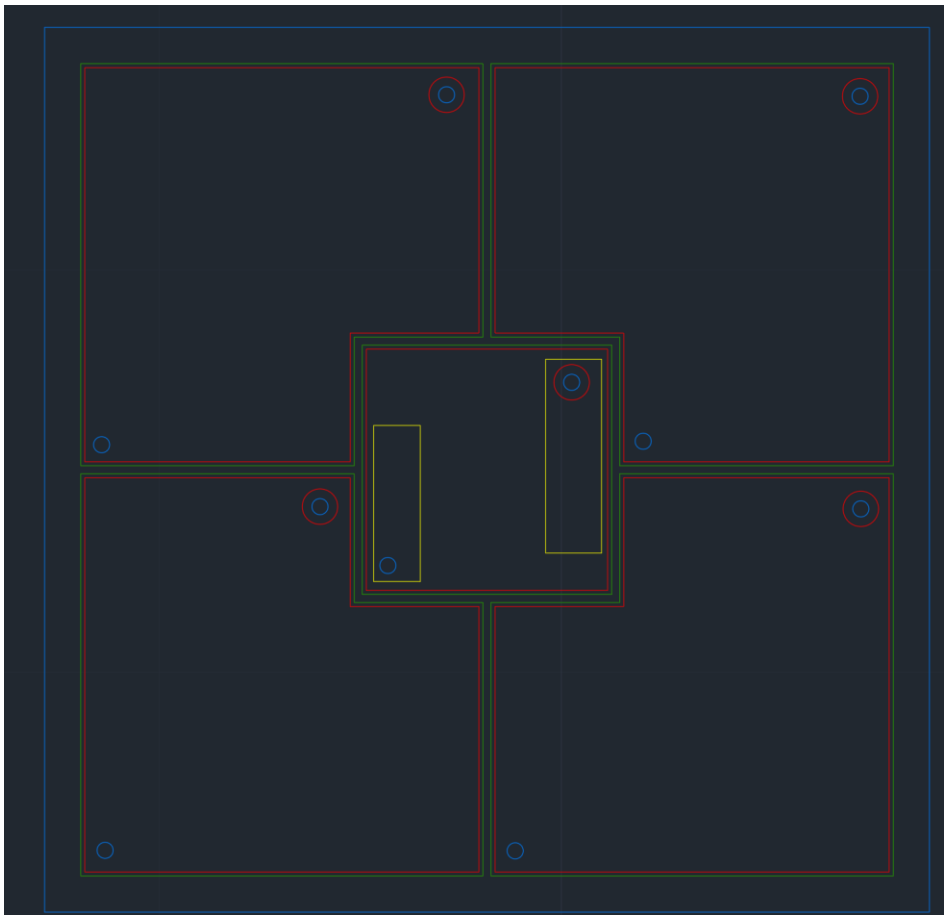
For this assignment, our goal is to create the central PAD region, facilitating interconnections between devices. The PAD layer, therefore, should exclusively cover the via areas within this central region. This configuration aligns with the assignment's scope, which primarily centers on the central PAD region and the subsequent interconnections



3. Overall layout

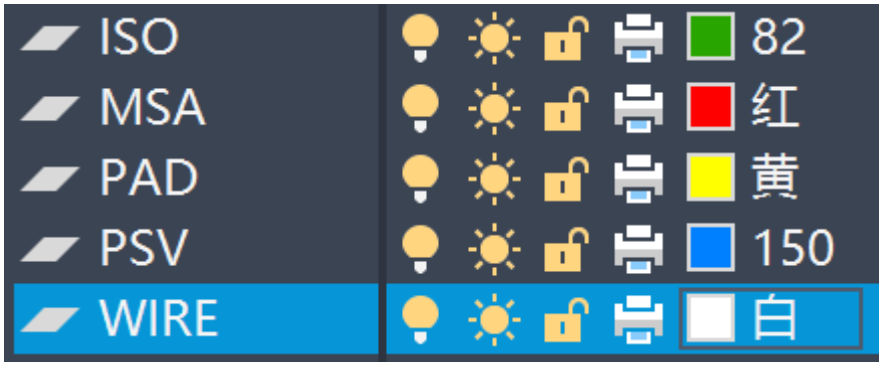
(1) Single device

Now, we will display all the layers, and an individual device is as shown in the figure.



The colors corresponding to different layers are as shown in the schematic diagram

below.



(2) The combination design of devices in series and in parallel

For the ID 12111008

ID Analysis:

From the ID, the value of CD is 08, which is 8.

Device Parameter Analysis:

Operating Voltage: 2D = 2.8V

Operating Current Range:1mA to CD/3 = 1mA to 8/3 = 2.67mA

Circuit Total Voltage & Current Analysis:

Total Voltage: Up to 8V

Total Current: Up to 4mA.

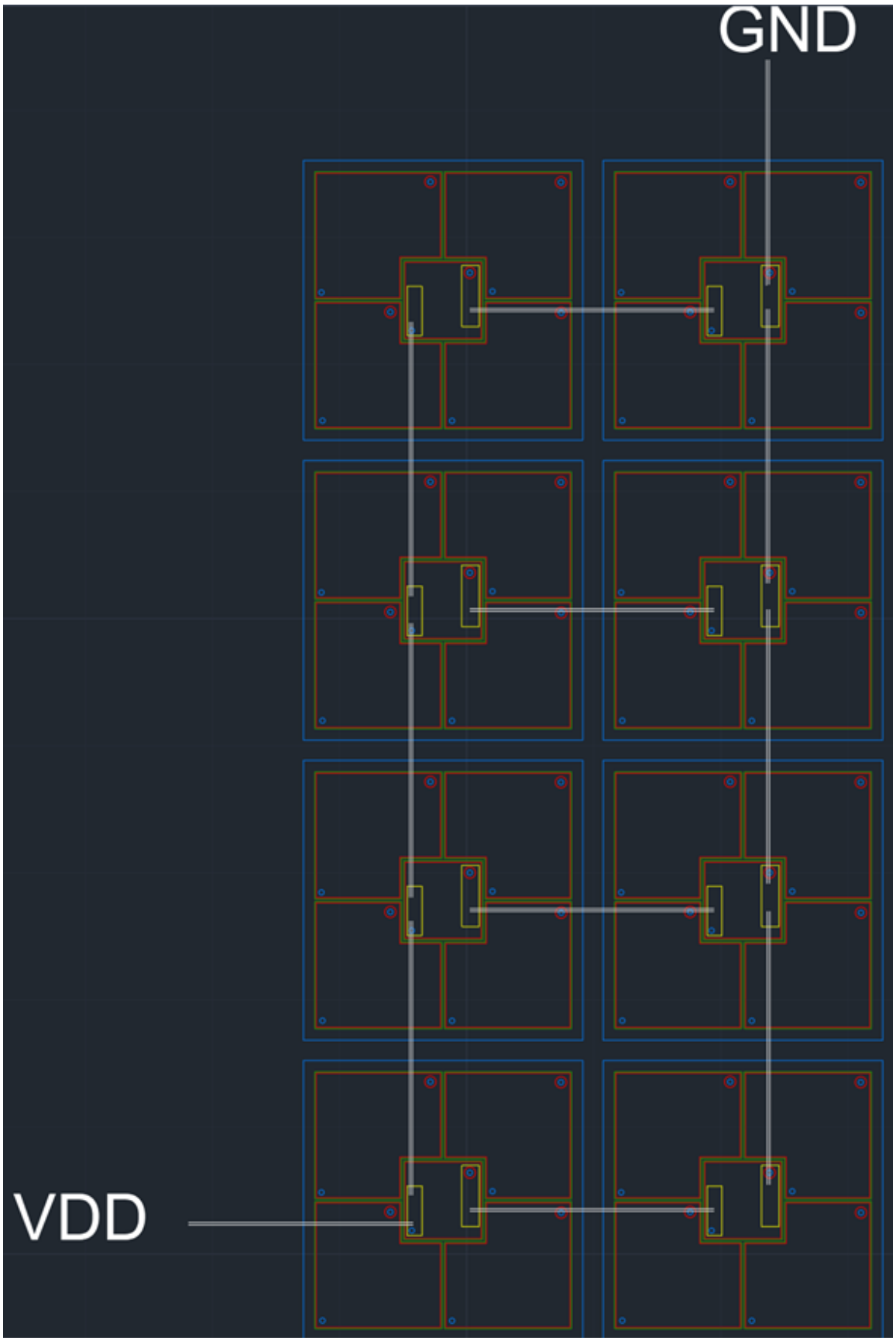
Device Configuration:

Each device operates at 2.8V and 1mA. To ensure safety, the total circuit voltage should not exceed 8V, and the total current should be within 4mA.

For the optimal configuration, I'll arrange each column with 4 devices in parallel. Then, two such columns will be placed in parallel. This ensures each device gets 2.8V, and the current for each device remains at 1mA.

Conclusion:

For the ID 12111008, the devices should be set in a 2-column by 4-row format, with all 8 devices connected in parallel, ensuring safe operation.



4. Insights and Lessons

(1) Hands-On CAD Proficiency:

I gained hands-on experience with CAD tools, allowing me to become proficient in their use and providing a natural insight into electronic design techniques.

(2) Real-World Technical Application:

I learned to interpret and apply technical specifications, emphasizing the practical aspect of attention to detail and precision in electronic design.

(3) Comprehensive Insight into Chip Layout and Manufacturing:

Through this project, I acquired a comprehensive understanding of chip layout and the manufacturing process. This encompassed different layer designs, providing insights into how they contribute to the overall functionality and efficiency of the wafer form process.