Design and Implementation of Two-Stage Amplification Circuits Based on gm/id

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***Abstract*—This paper presents the design and implementation of a two-stage operational amplifier (op-amp) using the gm/Id method in 0.18μm technology. The op-amp achieves over 60dB open-loop differential-mode gain, low power consumption, and stable operation under ±10% supply voltage variation. Simulation results validate its high performance in terms of gain, phase margin, bandwidth, and output swing, making it suitable for diverse applications.**

***Keywords*—Two-stage operational amplifier, gm/id design method, semiconductor technology, circuit design, simulation, performance validation.**

I. INTRODUCTION

Operational amplifiers (op-amps) play a critical role in analog circuits, providing high-gain amplification with a differential input and often single-ended output [1]. The op-amp designed in this project utilizes NMOS and PMOS transistors, capacitors, and resistors in 0.18μm technology, aiming to achieve high-performance specifications, including a differential-mode gain exceeding 60dB, low power consumption, and reliable operation under a ±10% supply voltage variation.

The design methodology is based on the gm/Id approach, which addresses key challenges in modern semiconductor technology, such as variations in fabrication processes and the difficulty of precisely controlling transistor parameters. This method allows for better optimization of transistor sizing and performance by leveraging the relationship between the transconductance (gm) and the drain current (Id). The project emphasizes critical design considerations, such as gain distribution, frequency compensation, and zero-pole regulation, to ensure both stability and efficiency.

The first stage of the op-amp, an Operational Transconductance Amplifier (OTA), is selected for its ability to provide high gain, while the second stage is designed to enhance voltage swing. Through detailed simulations, the design achieves key performance metrics, including a phase margin exceeding 60 degrees and a unity-gain bandwidth that meets target specifications. Under the guidance of Professor Pan and with support from teaching assistants, the project successfully meets all design requirements, demonstrating suitability for a wide range of analog applications

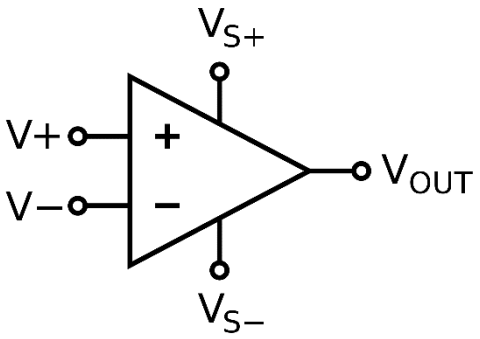

Fig. 1 Circuit diagram symbol for a representative op amp

Through this project, we've demonstrated the application of classroom knowledge to address real-world engineering challenges, producing a design that balances high performance and low power requirements. The final parameters are shown in Table I.

TABLE I. The simulation results with different VDD

parameters	*requirement*	*(1) VDD=1.8V*	*(2) VDD=1.62V*	*(3) VDD=1.98V*
A_{DM0}	more than 60dB	62.30dB	60.78dB	63.44dB
A_{CM0}	less than -20dB	-20.85dB	-21.70dB	-20.09dB
Phase margin	more than 60 deg	61.13deg	61.02deg	61.23deg
Unity gain frequency	more than 100MHz	103.14MHz	102.21MHz	103.65MHz
Up slew rate	more than 10V/us	111.95V/us	113.24 V/us	111.39 V/us
Down slew rate	more than 10V/us	51.06V/us	50.99V/us	50.70V/us
Output voltage swing	more than 800mV	over 800mV	over 800mV	over 800mV
Power	minimum	294.16 uW	261.78 uW	327.12 uW
Both use 0.18um CMOS process; V_{SS}=0V; Load=1pF; Vdc=1.1V;				

II. g_m/I_D Design Method Introduction

A. Reason for Appearance

The adoption of the g_m/I_D method in analog integrated circuit design is driven by the necessity to address certain challenges in modern semiconductor technology:

1) **Advanced Fabrication Processes:** The advanced manufacturing processes used in modern integrated circuits cannot be accurately captured by the square-law model traditionally used for MOSFET devices.
2) **Parameter Control:** Parameters provided by the foundry, such as mobility (μn) and oxide capacitance (C_{ox}), are difficult to control precisely, making traditional manual calculations and circuit analysis unreliable.

As a result, designers often resort to trial-and-error approaches, tweaking transistor dimensions until the design requirements are met by chance. This process is not only suboptimal but also lacks a standardized methodology.

The g_m/I_Dmethod was proposed to overcome these issues by combining device simulation results specific to a given process with manual calculations. This hybrid approach, aided by computer simulations, ensures accuracy in the initial stages of design and accelerates the iterative process of circuit development.

B. Significance of g_m/I_D

1) **Physical Aspect:** The cut-off frequency (f_T) of a transistor is approximately $f_T = \frac{gm}{2\pi C_{gs}}$ and since $I_D$relates to power consumption ($P = I \cdot V$), $\frac{g_m}{I_D}$ essentially reflects how to achieve the fastest response with a given current. Additionally, g_m correlates with noise, implying that $\frac{g_m}{I_D}$ is also a consideration for minimizing noise within the constraints of available current.

2) **Relationship with overdrive voltage:** According to the square-law formula, $g_m/I_D = \frac{(2I_D/V_{ov})}{I_D} = \frac{2}{V_{ov}}$. Therefore, designing with $\frac{g_m}{I_D}$ as a parameter indirectly selects the overdrive voltage (V_{ov}) of the MOSFET.

C. Selecting g_m/I_D

A larger $\frac{g_m}{I_D}$ is preferred for amplifiers, implying a smaller V_{ov} and therefore a smaller V_{ds}, which allows for a larger output swing.

A smaller $\frac{g_m}{I_D}$ is ideal for current sources, targeting high bandwidth or high f_T.

III. Two-Stage OPAMP Circuit Design

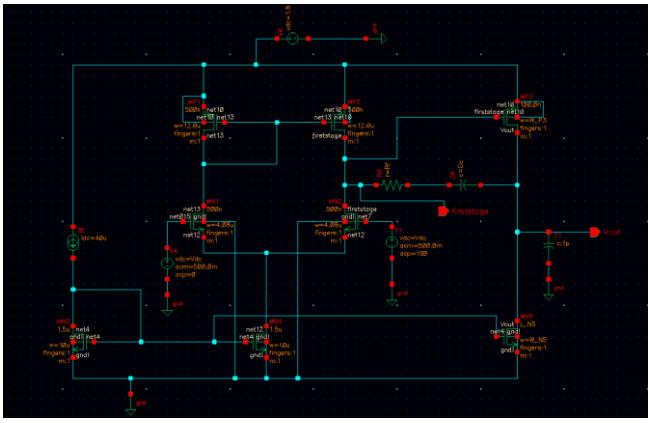

Fig. 2 Two stages circuit structure

Typical OPAMP topologies include telescopic, folded-cascode, two-stage, and gain-boosted architectures. Due to their single-stage structure, the first two topologies often face a trade-off between high-voltage gain and a substantial output swing. While gain-boosted configurations can achieve exceptionally high gain through increased output resistance (R_o) via feedback, their output swing may still fall short of meeting our requirements. Consequently, we choose a two-stage structure where the first stage provides high gain, and the second stage facilitates large swings. However, there are additional issues that need to be considered, listed below.

A. Distribution of voltage gain between the first and second-stage circuits

In the design of a two-stage amplification circuit, the primary concern is the distribution of voltage gain between the first and second-stage circuits. Initially, the inclination may be to allocate the gain equally between these two stages. However, this approach presents challenges in meeting A_{CM0} requirements. This is because only the first stage incorporates common mode rejection, while the second stage inadvertently amplifies the common mode gain. To comply with A_{CM0} specifications, it is imperative to minimize the gain in the second stage.

B. Zero-pole regulation and frequency compensation

In the design of a two-stage amplification circuit, another issue arises concerning the frequencies of the dominant pole and the first non-dominant pole. Without compensation, the separation between the dominant pole and the first non-dominant pole is insufficient to achieve a favorable phase margin. The compensation schematic is presented below. Through the addition of the Miller capacitor (C_C), the dominant pole shifts towards the origin, while the first non-dominant pole moves away from the origin, resulting in a significantly enhanced bandwidth. This phenomenon is commonly referred to as "pole splitting."

However, the inclusion of a Miller capacitor also introduces a Feedforward Circuit, thereby introducing a zero into the circuit. Typically, the presence of a zero is of little concern, but in this case, it is a right-half-plane zero, contributing additional negative phase shift and impeding the rate of magnitude decrease. Consequently, this action displaces the gain crossover further from the origin, leading to a considerable degradation in stability.

One solution to eliminate or relocate the zero involves placing a resistor in series with the compensation capacitor, thereby altering the zero frequency. By adjusting the value of resistor R_Z, the zero can be shifted into the left-half-plane, ideally compensating for the first non-dominant pole.

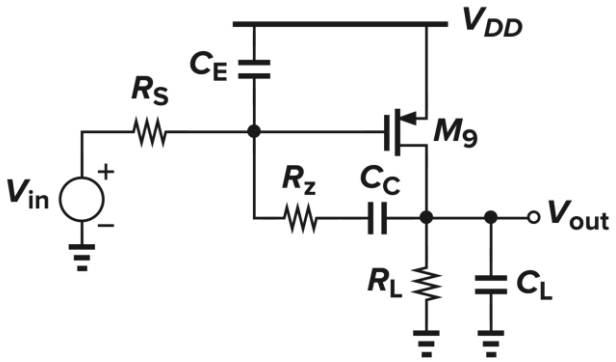

Fig. 3 Miller compensation schematic

IV. Circuit Parameter Determination Based on gm/id

The gm/id design method typically follows the outlined steps:

1) Determine gm based on GBW and phase margin, considering the impact of parasitic capacitance on GBW and phase margin predictions.

2) Predict a gm/id ratio, where the gm/id of the primary amplifying transistor ranges from 10 to 15, and the gm/id of the Current Mirror is approximately 10.

3) Determine the id based on gm and gm/id.

4) Based on A_v and self-gain vary gm/id, determine L of transistor

5) Based on id/W vary gm/id, determine W of transistor

The following are the steps we take in the calculation process using the gm/id design method.

A. Open-loop voltage gain of first stage (A_{v1}) and second stage (A_{v2})

The total low-frequency open-loop small-signal gain requirement for our op-amp is set to exceed 60dB (1000 times). Given the constraint of a common-mode gain (A_{CM0}) less than -20dB, to suppress the influence of common-mode noise at the input, we avoid excessively amplifying the common-mode noise signal by opting for a larger gain in the first stage (A_{v1}) and a smaller gain in the second stage(A_{v2}).

As the primary amplifying transistor in the second stage is PMOS, we conducted a parameter scan to analyze the intrinsic gain of PMOS transistors across various gm/id and L values. The outcomes of this investigation are depicted in Figure 3. The minimum self-gain of the PMOS is observed to be 27 with L=180nm. Consequently, the gain of the second stage falls within the range of 13.5 to 27. In the desig, we have selected $A_{v1} \geq 50$ and $A_{v2} \approx 20$.

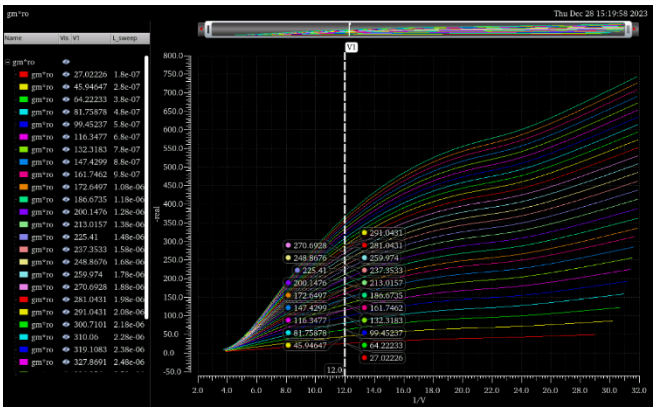

Fig. 4 PMOS self-gain under various L and gm/id with fixed VDS=0.4V

B. First Stage OTA Size

In the process of designing our two-stage operational amplifier, the sizing of transistors is a critical initial step to ensure the required amplification factors, and parameters such as g_m and I_D are met by given GBW.

1) Determining the Transconductance $(g_{m1,2})$ of the First-Stage OTA Amplifier from required (GBW)

To meet the requirement of a unity gain frequency (GBW) of 100MHz for our two-stage operational amplifier, the transconductance (g_m) of the first-stage OTA amplifier must be calculated with precision. The GBW is defined by the equation:

$$GBW = \frac{g_m}{2\pi C_{load}}$$

For the first-stage OTA, the load capacitance (C_{load}) is predominantly defined by the feedback capacitance (Cc). However, due to the impact of parasitic capacitances inherent to MOS transistors, C_{load1} is approximately 1.5 times the size of *Cc*.

Drawing from empirical knowledge, *Cc* is estimated to be about 0.2 to 0.5 times the load capacitance of the second stage (C_{load2}). In this design, we'll assume

$$Cc = 0.3C_{load2} = 0.3pF.$$

Given these assumptions and the target GBW, the required transconductance ($g_{m1,2}$) of the input NMOS transistors that provide the gain for the first-stage OTA can be determined. The equation simplifies to:

$$g_{m1,2} = GBW \cdot 2\pi C_{load1} = 100MHz \cdot 2\pi \cdot 1.5 \cdot 0.3pF = 2.83 \times 10^{-4} S$$

Therefore, the transconductance for the first stage OTA should be approximately

$$g_{m1,2} \approx 280\mu S\,.$$

This value ensures that the first-stage OTA will contribute appropriately to achieving the desired GBW for the overall amplifier

2) Calculating Current I_d and Sizing of $N1$ and $N2$ Transistors (Based on Amplification Factor (A_v) and current density $\frac{I_d}{W}$)

The sizing of the N1 and N2 transistors in the first stage of the OTA amplifier involves determining the length $(L)$from the required gain (A_v) and self-gain $(g_m \cdot r_o)$, and subsequently calculating the width W from the current per unit width (i_d/W).

Step 1: Selecting g_m/I_D for Different Purposes

For our amplifying transistors N1 and N2, we target a g_m/I_D of 14, which allows for a smaller overdrive voltage$(V_{ov})$and thus a lower (V_{ds}), enabling a larger output swing.

Step 2: Calculating the Current (i_d)

Given the g_m determined in section B and the selected g_m/I_D ratio, we can calculate the(i_d)as:

$$I_d = \frac{g_m}{(g_m/I_D)} = \frac{283\mu S}{14} \approx 20\mu A$$

Step 3: Revising g_m

With the approximate current$(i_d = 20\mu A)$, we adjust g_m accordingly:

$$g_m = i_d \cdot (g_m/I_D) = 20\mu A \cdot 14 = 280\mu S$$

Step 4: Determining $\boldsymbol{L_{N1,2}}$ from A_{v1} and Self-Gain

The intrinsic gain (self-gain) of a MOS transistor, given by $gm \cdot rout$, reflects the maximum gain available from the device. We can plot this relationship alongside $\frac{g_m}{I_D}$ to determine the appropriate length (L) of the transistors.

To achieve $A_{v1} \geq 50$, which is approximately $|A_{v1}| = g_{m1} \cdot (ro_{P1}||ro_{N1})$, we need an intrinsic gain of about 100 for a single device. By scanning different L values for transistors N1 and N2, we observe the relationship between $\frac{g_m}{I_D}$ and $gm \cdot r_o$.

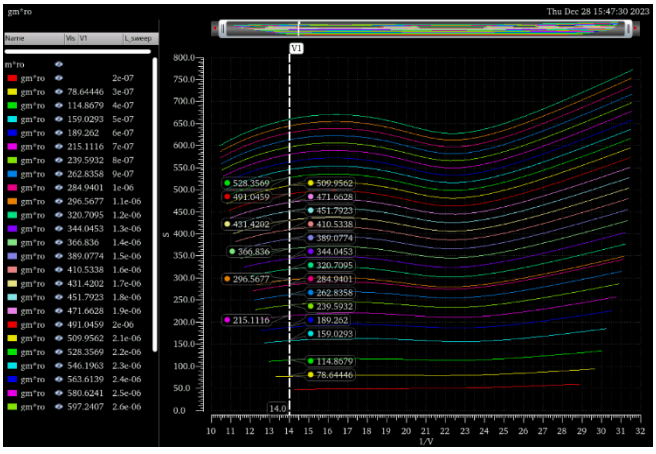

Fig. 5 NMOS self-gain under various L and gm/id with fixed VDS=0.8V

To satisfy the condition $(A_{v1} \geq 50)$, theproduct $(g_{m1} \cdot r_{o1})$ must be greater than 100. Selecting $L = 500nm$ achieves a self-gain of 159 with $V_{ds} = 0.9V$.

Step 5: Determining $\boldsymbol{W_{N1,2}}$ from current density $\frac{I_d}{W}$

After setting $L_{\{1,2\}} = 500nm$, we observe that at$\frac{g_m}{I_D} = 14$ (larger for amplifiers), the current density $(\frac{I_d}{W} =$ 4.3651) . Knowing that W and I_d are approximately proportional, we can determine the transistor widths (W) by dividing the current ($\mathrm{Id}_{\mathrm{N}_{1,2}}$) for N1 and N2 by the current density $\left(\frac{I_d}{W}\right)$:

$$\mathrm{w}_{\mathrm{N}_{1,2}} = \frac{\mathrm{Id}_{\mathrm{N}_{1,2}}}{I_\mathrm{d}/\mathrm{w}} = \frac{20\mu}{4.3651} = 4.58\mu\mathrm{m}$$

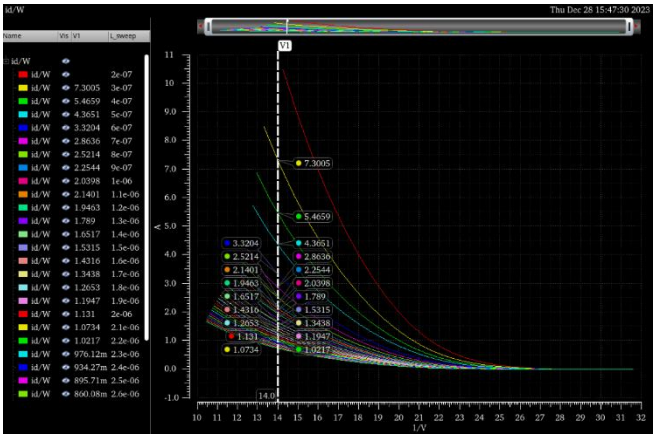

Fig. 6 NMOS id/W under various L and gm/id with fixed VDS=0.8V

This width ensures that transistors N1 and N2 will have the desired transconductance to contribute to the first-stage gain of our OTA, as per the design requirements.

3) **Sizing of OTA Load Transistors *P*1 and *P*2**

For transistors P1 and P2, which serve as the load for N1 and N2 in the OTA, the size determination follows the same foundational principle.

Step 1: Determining $\boldsymbol{L_{P1,2}}$ by Keeping $i_d \cdot r_o$ constant

With the current for N1 and N2 established and $Av2 = gm(ro_P||ro_N)$ set, we can maintain r_o constant and thus the product $i_d \cdot r_o$ constant for P1 and P2.

For N1 and N2, as shown in the figure, when $\frac{g_m}{I_D} = 14$ and $L = 500nm$, $i_d \cdot r_o = 11.3641$.

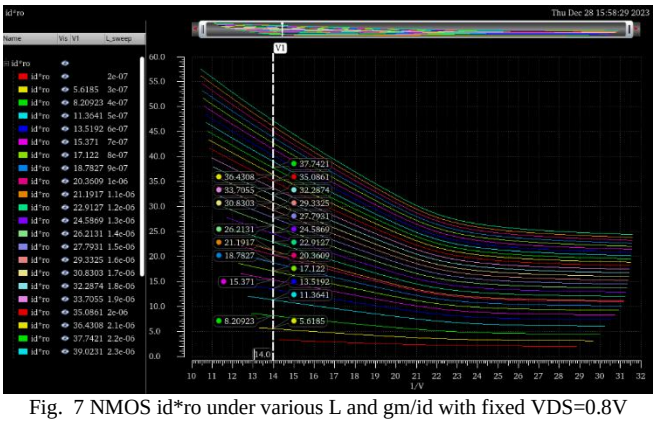

Fig. 7 NMOS id*ro under various L and gm/id with fixed VDS=0.8V

In the OTA, we keep $i_d \cdot r_o$ constant for P1 and P2 at 11.3641 $(V_{gs} = V_{ds})$. For P1 and P2, which function as current sources, a smaller ratio is preferable for higher bandwidth or f_T, and hence we choos $\frac{g_m}{I_D} = 10$.

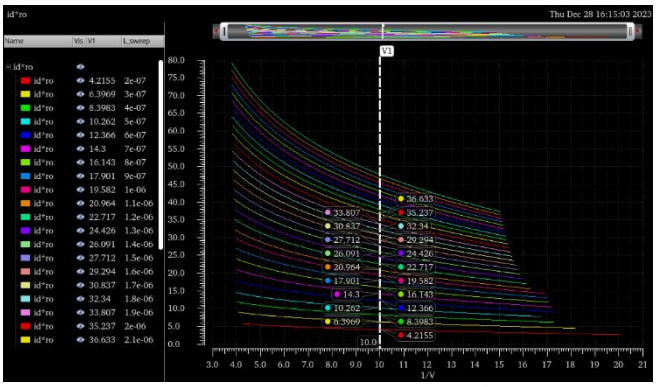

Fig. 8 PMOS id*ro under various L and gm/id with fixed VDS=0.4V

Plotting the relationship, we find that at L = 500nm, $i_d \cdot r_o$ is approximately 10.262, close to our target value.

Step 2: Determining $\boldsymbol{W_{P1,2}}$ Using Current Density $\frac{I_d}{W}$

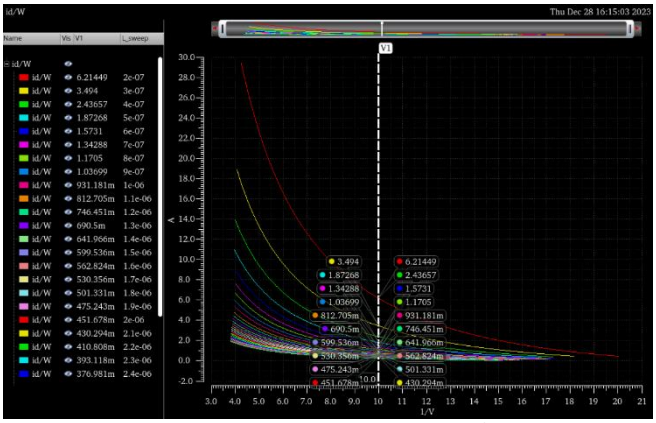

Fig. 9 PMOS id/W under various L and gm/id with fixed VDS=0.4V

From graphical analysis at L = 500nm and $\frac{g_m}{I_D} = 10$, the current density $\frac{I_d}{W}$ is found to be 1.87268. Since the current $I_d = 20\mu A$ for P1 and P2 is already set by N1 and N2, we calculate the width W for P1 and P2:

$$w_{P_{1,2}} = \frac{i_{d1,2}}{i_d/w} = \frac{20\mu}{1.87} = 10.68\mu m$$

This ensures P1 and P2 are sized appropriately to match N1 and N2 in the OTA, achieving the required gain and performance.

C. Second Stage OTA Size

Two factors influence the size of the second stage OTA. The first is ACM0, which necessitates the lowest possible gain for the second stage, as previously discussed. The second factor is the phase margin, which will be addressed later in the discussion.

1) Phase margin

To achieve the required phase margin of at least 60°, we approximate the position of the second pole. This estimation guides the determination of g_{mP3} for the P3 transistor in the second stage. Consequently, using the $\frac{g_m}{I_D}$ method, we accurately define the width of the second-stage P3 transistor to align with the current demands and phase margin requirements. Therefore, we can also decide I_{P3}.

$$\omega_{P1} \approx \frac{g_{mN1}}{1.5 \cdot C_C \cdot 2\pi}$$

$$\omega_{P2} \approx \frac{g_{mP1}}{C_L \cdot 2\pi}$$

$$\omega_{P2} > 2 \cdot \omega_{P1}$$

Because $C_C = 0.3 \cdot C_L$, then

$$\frac{g_{mP1}}{g_{mN1}} > 4$$

So

$$g_{mP1} > 1.12ms$$

If $\frac{g_m}{I_D} = 12$, then $I_d = 93.3uA$, which is not an integer multiple of the current in the first-stage amplification circuit. So, we set $I_d = 80uA$, and $\frac{g_m}{I_D} = 13$, $g_m = 1.04ms$, which is approximately fit the request.

2) Lowering Gain of Second Stage

As we mentioned before to ensure fit ACM0, self-gain should be minimum. So, the

$$L_{P3} = 180nm$$

From graphical analysis at L = 180nm and $\frac{g_m}{I_D} = 13$, the current density $\frac{I_d}{W}$ is found to be 3.61168. Since the current of $I_d = 80uA$ for P3, we calculate the width W for P3:

$$w_{P_3} = \frac{i_{d3}}{i_d/w} = \frac{80\mu}{3.61} = 22.16\mu m$$

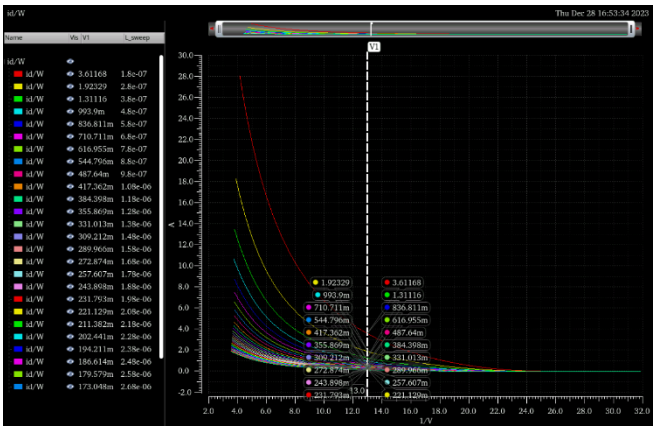

Fig. 10 PMOS id/W under various L and gm/id with fixed V_{DS}=0.4V

D. Current minor size

The size of current mirror affects A_{CM0} and current distribution. The common mode gain of common gate amplifier circuit with active current mirror load could be calculated with below circuit.

1) **Determining $L_{N3,4}$ based on A_{CM0}**

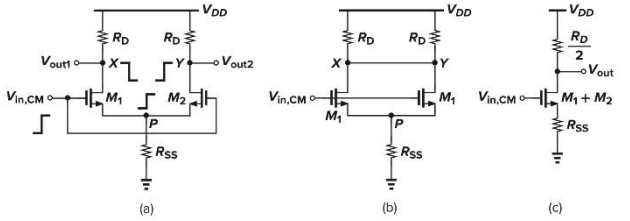

Fig. 11 (a) Differential pair sensing CM input; (b) simplified version of (a); (c) equivalent circuit of (b)

The open-loop common-mode gain of the first stage (OTA stage) is:

$$A_{CM-OTA} \approx -\frac{g_{MN_1}}{(1+2g_{MN1}R_{ss})g_{mP1}}$$

$$R_{ss} = r_{oN4}$$

Therefore, reducing A_{CM-OTA} involves increasing the output resistance of the current mirror transistors N_4, which is R_{ss}. By extending $L_{N3,4}$ to $1.5\mu m$, we enhance the resistance, which contributes to the desired gain reduction.

2) **Determining $W_{N3,4}$, W_{N5} and L_{N5} based on the current mirror proportionality**

Based on the current mirror proportionality, since $I_{dN3} = I_{dN4} = \frac{1}{2}I_{dN5} = 40\ \mu A$, We get:

$$\frac{W_{N3}}{L_{N3}} = \frac{W_{N4}}{L_{N4}}$$

$$\frac{W_{N3}}{L_{N3}} = \frac{1}{2}\frac{W_{N5}}{L_{N5}}$$

Therefore, $W_{N3,4}$ can be set to 10μm. To ensure P3 and N3 both operate in saturation region, L_{P3} and L_{N5} should not differ significantly. So, we take L_{N5} to 375nm. Then, W_{N5} should be 5μm.

However, in the simulation with L_{N5} set to 375nm, N5 does not work in saturation region, and current ratio relationship $\frac{i_{first\_stage}}{i_{second\_stage}} = 2$ is not satisfied. After experimenting with various values for L_{N5}, it was determined that setting L_{N5} to 250nm satisfies our requirements.

TABLE II. design parameter and actual parameter

MOS Size Summery						
index	***gm/id(design)***	***L(design)***	***W(design)***	***gm/id(actual)***	***L(actual)***	***W(actual)***
N1	14	500nm	4.58μm	13.58	500nm	4.08μm
N2	14	500nm	4.58μm	13.58	500nm	4.08μm
N3	uncertain	1.5μm	10μm	9.80	1.5μm	10μm
N4	uncertain	1.5μm	10μm	9.79	1.5μm	10μm
N5	uncertain	250nm	5μm	11.07	250nm	5μm
P1	10	500nm	10.69μm	10.95	500nm	12μm
P2	10	500nm	10.69μm	10.95	500nm	12μm
P3	13	180nm	22.15μm	12.64	180nm	20.18μm
Frequency Compensation						
index	***design value***			***actual value***		
C_C	0.3pF			0.325pF		
R_f	5kΩ			2.6kΩ		
Other Parameter Summery						
index	***design value***			***actual value***		
A_{v1}	≥34dB			36.81dB		
A_{v2}	≈26dB			25.72dB		
$g_{mN1,2}$	280μS			268.82μS		
g_{mP3}	1.04mS			1.07mS		
$I_{dN1,2}$	20μA			19.79μA		
I_{dP3}	80μA			84.49μA		
V_{DC}	1.2V			1.1V		
Both use 0.18um CMOS process; V_{SS}=0V; Load=1pF;						

E. R_f and C_c Based on Miller Compensation

In our design, $C_C = 0.3 \cdot C_L = 300pf$. And we give R_f an approximate value 5k.

V. Fine-Tuning to Achieve Desired Amplification and Bonus

Following the gm/id design method, we can achieve highly accurate gain predictions. However, in other areas such as GBW and phase margin, where capacitance is factored into the calculations, predictions might be significantly erroneous. This is attributed to the fact that the value of parasitic capacitance is contingent on both W and L. Consequently when computing W and L, it becomes imperative to make estimations regarding the influence of parasitic capacitance. The outcomes of the fine-tuning process are presented in TABLE II.

A. Differential-mode open loop voltage gain simulation:

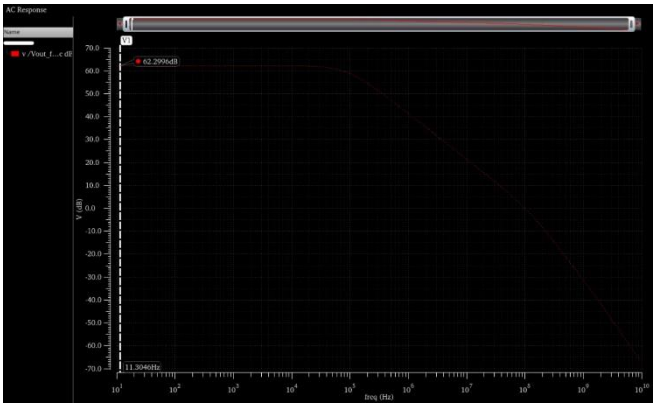

Fig. 12 Differential mode open loop voltage gain is 62.2996dB with VDD=1.80V

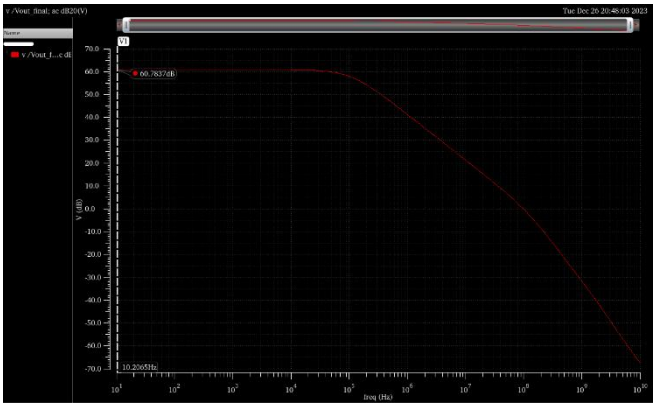

Fig. 13 Differential mode open loop voltage gain is 60.7837dB with VDD=1.62V

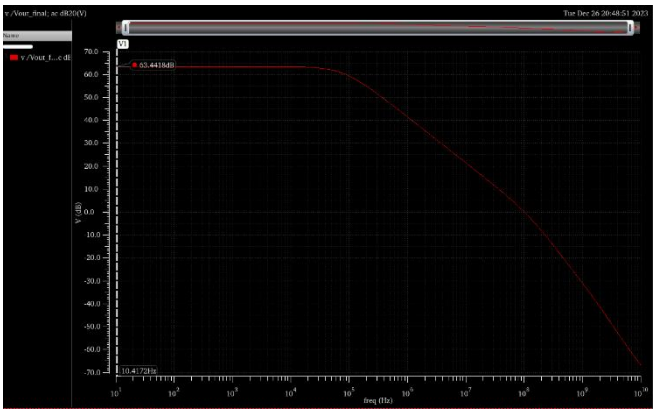

Fig. 14 Differential mode open loop voltage gain is 63.4418dB with VDD=1.98V

B. Common-mode open loop voltage gain :

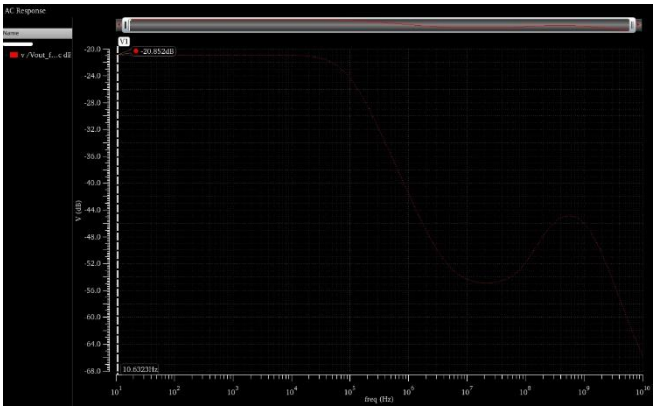

Fig. 15 Common-mode open loop voltage gain is -20.852dB with VDD=1.80V

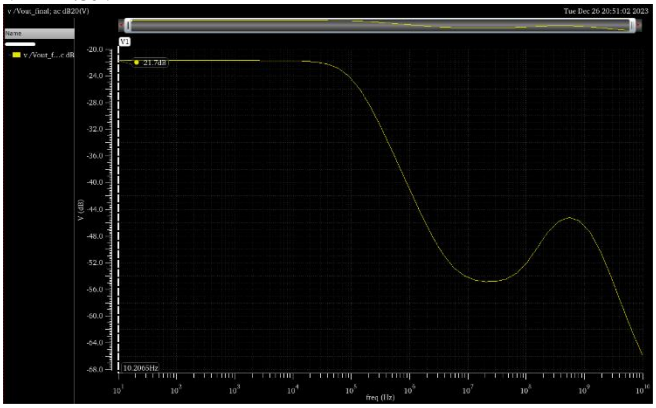

Fig. 16 Common-mode open loop voltage gain is -21.7dB with VDD=1.62V

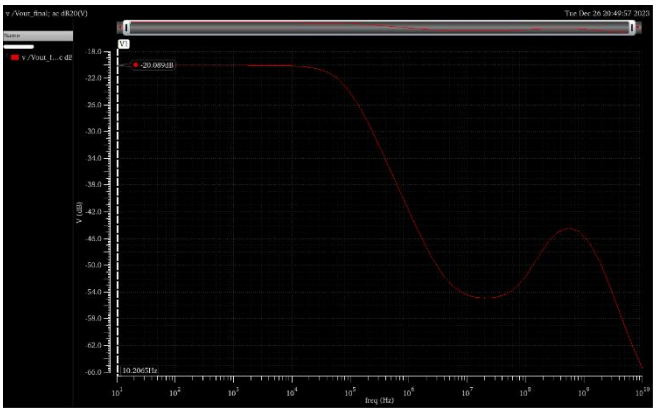

Fig. 17 Common-mode open loop voltage gain is -20.089dB with VDD=1.98V

C. Close loop phase margin

Fig. 18 Close loop phase margin is 61.126Deg with VDD=1.80V

Fig. 19 Close loop phase margin is 61.017Deg with VDD=1.62V

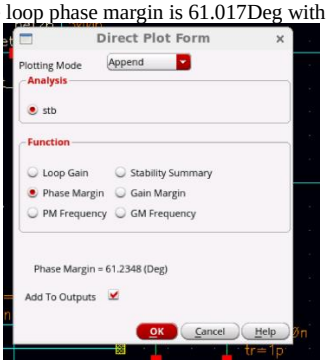

Fig. 20 Close loop phase margin is 61.2348Deg with VDD=1.98V

D. Close loop unity-gain bandwidth and 3dB fequency

Fig. 21 Close loop gain unity-gain bandwidth is 103.14 MHz and 3dB frequency is 61.14kHz with VDD=1.80V

Fig. 22 Close loop gain unity-gain bandwidth is 102.206 MHz and 3dB frequency is 74.41kHz with VDD=1.62V

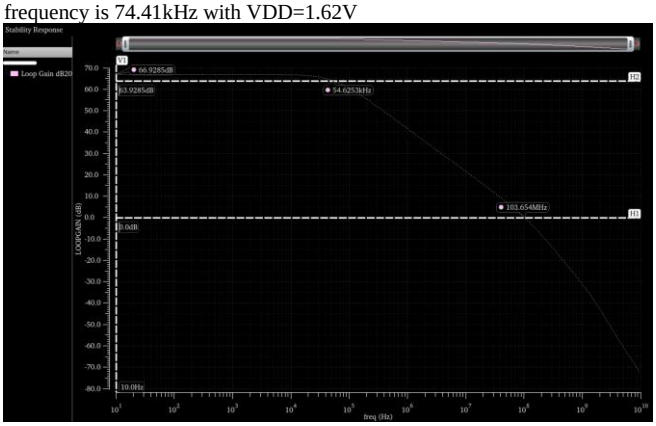

Fig. 23 Close loop gain unity-gain bandwidth is 103.65 MHz and 3dB frequency is 54.63kHz with VDD=1.98V

E. Slew rate simulation

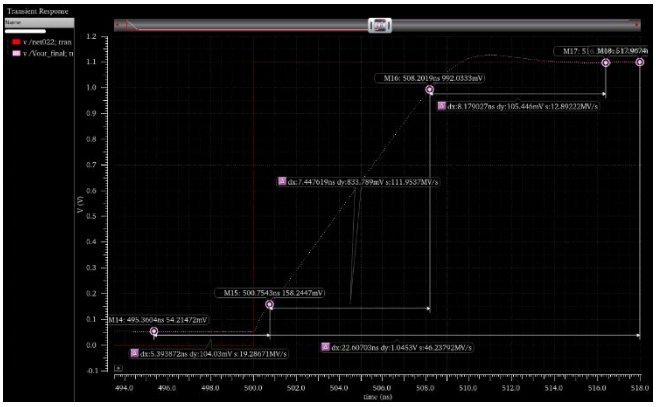

Fig. 24 up slew rate is 111.95V/us approximately with VDD=1.80V

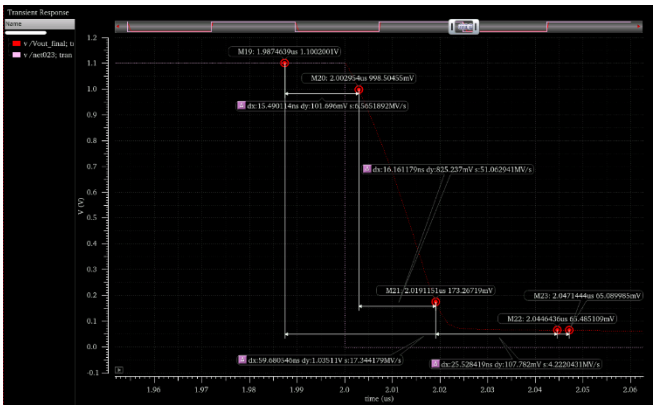

Fig. 25 down slew rate is 51.063V/us approximately with VDD=1.80V

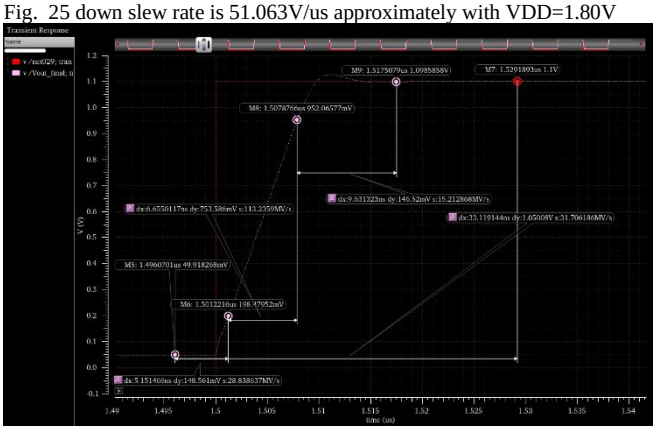

Fig. 26 up slew rate is 113.24V/us approximately with VDD=1.62V

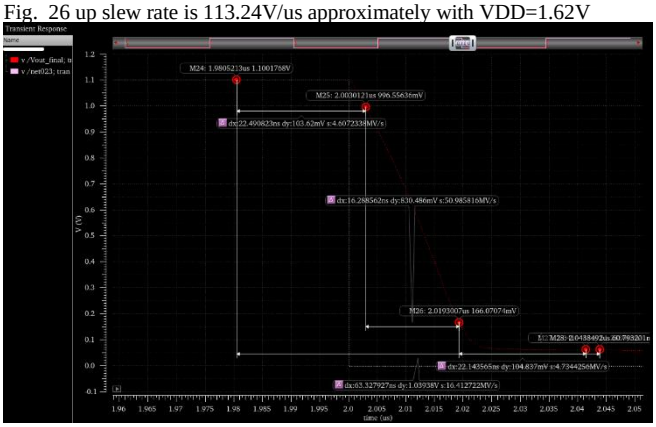

Fig. 27 down slew rate is 50.99V/us approximately with VDD=1.62V

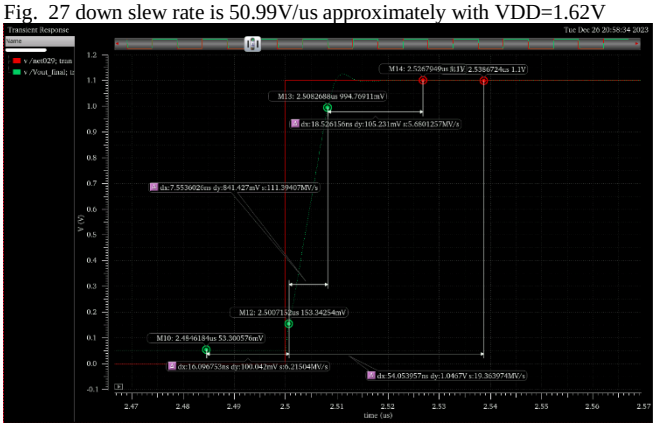

Fig. 28 up slew rate is 111.39V/us approximately with VDD=1.98V

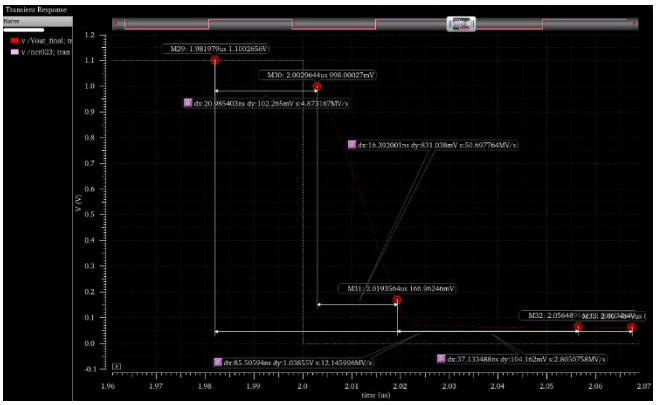

Fig. 29 down slew rate is 50.70V/us approximately with VDD=1.98V

F. Output swing test bench

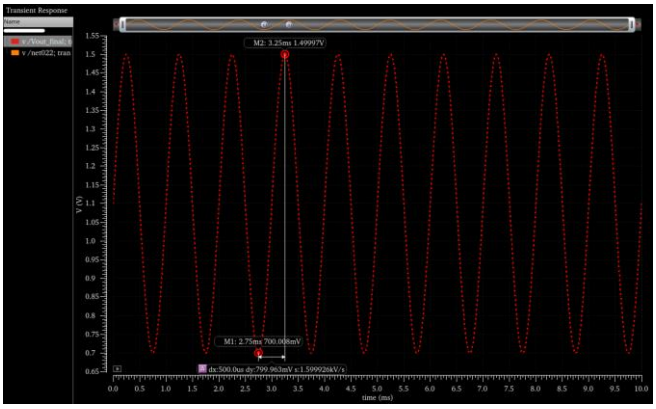

Fig. 30 swing is over 800mV with VDD=1.80V

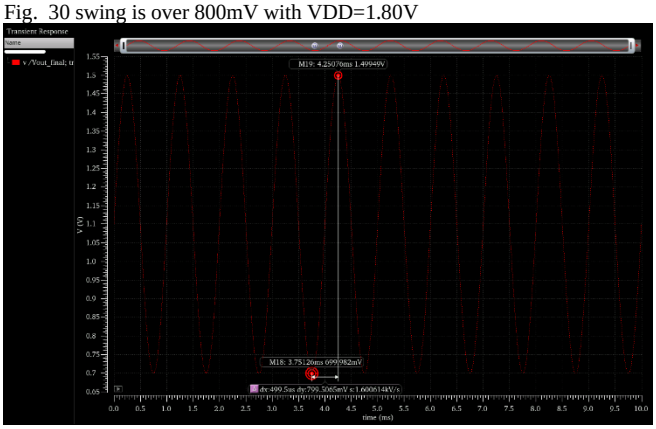

Fig. 31 swing is over 800mV with VDD=1.62V

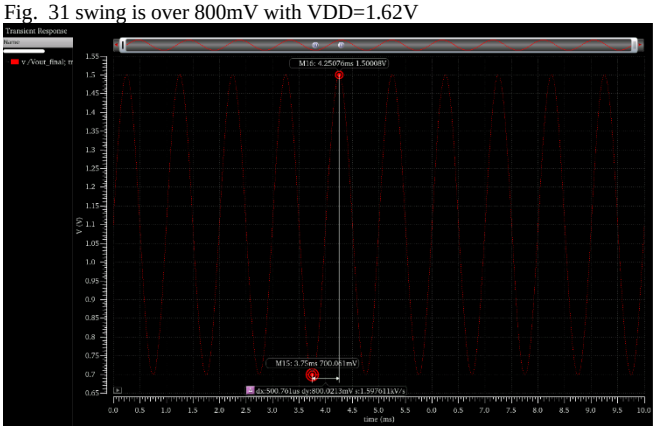

Fig. 32 swing is over 800mV with VDD=1.98V

VI. Conclusion

Through this project, we learned the general design methodology for a two-stage operational amplifier based on the advanced gm/id approach and put it into practice. We successfully met the specified criteria under the 180nm process technology, ensuring performance stability even with variations in power supply voltage.

While simulation tools offer convenient features like parameter scanning, the ability to conduct theoretical analysis and master correct design methods remains crucial for advancing beyond a spice monkey. Moreover, theoretical analyses are always based on certain ideal assumptions and may not perfectly achieve technical specifications. In such cases, fine-tuning parameters with simulation assistance becomes essential. Through this project, we engaged in practical analog circuit design, realizing the importance of complementing theoretical analysis with simulation. In future learning and endeavors, we will emphasize integrating theory and practice, striving to enhance our analog circuit design skills.