1 Example Files

1.1 Example 1

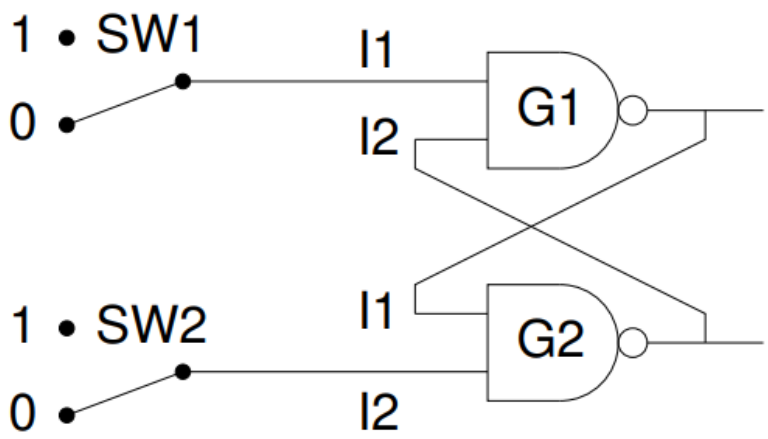

Figure 1: Example 1 - SR Latch

The following is the EBNF for this circuit:

```
[devices]
  G1, G2 = NAND;      # Defaults to 2 inputs
  SW1, SW2 = SWITCH; # Defaults to 0 i.Ie "False"

[conns]
  SW1 = G1.I1;
  SW2 = G2.I2;
  G1=G2.I1;            # Whitespace not required
  G2 = G2.I2;

# new blank lines are ignored

[monit]                 # Need a newline after a block
  G1, G2;
```

Listing 1: Code for example 1

```
[devices]G1,G2=NAND;SW1,SW2=SWITCH;[conns]SW1=G1.I1;SW2=G2.I2;G1=G2.I1;G2=G2.I2;[monit]G1,G2;
```

Listing 2: Obfuscated Code

1.2 Example 2

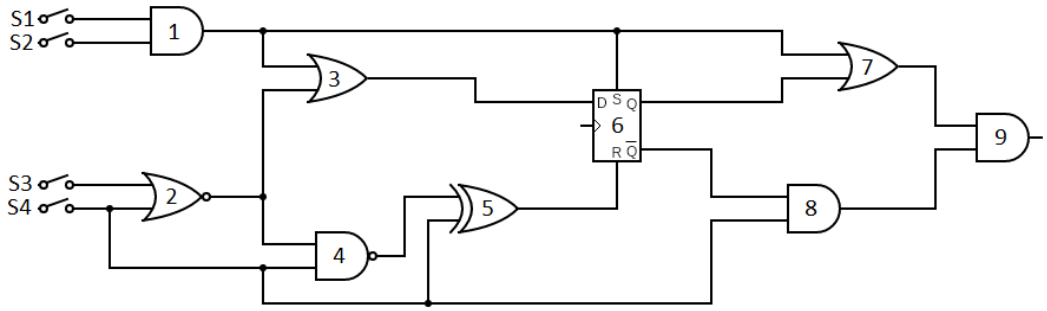

Figure 2: Example 2

The following is the EBNF for this circuit:

```
[devices]
    G1, G8, G9 = AND;          # Default 2 input AND gate
    G2 = NOR(2);               # Can specify number of inputs but defaults to 2 if not specified
    G3, G7 = OR;
    G4 = NAND;
    G5 = XOR;

    SW1, SW2 = SWITCH;         # Defaults to 0 which is "False"
    SW3, SW4 = SWITCH(0);      # Can be specified as 0 for "False" but defaults to 0 if not specified

    G6 = DTYPE;
    CLK1 = CLOCK(5);           # Clock of period 5 (Not shown in the diagram)


[conns]

    # Switch connections
    SW1 = G1.I1;
    SW2 = G1.I2;
    SW3 = G2.I1;
    SW4 = G2.I2;

    # Clock to DTYPE
    CLK1 = G6.CLK;

    G1 =  G3.I1, G6.SET, G7.I1; # Can connect output to multiple inputs, SET is "S" in the diagram
    G2 =  G3.I2, G4.I1;
    G3 =  G6.DATA;              # DATA is "D" in the diagram
    G4 =  G5.I1;
    G5 =  G6.CLEAR ;            # CLEAR is "R" in the diagram

    G6.Q = G7.I2;               # Need to specify which output of DTYPE since there are 2
    G6.QBAR: G8.I1;

    G7 = G9.I1;
    G8 = G9.I2;


[monit]
    G9, G8;
    G6.DATA;
```

Listing 3: Code for Example 2

```
[devices]G1,G8,G9=AND;G2=NOR(2);G3,G7=OR;G4=NAND;G5=XOR;SW1,SW2=SWITCH;SW3,SW4=SWITCH(0);G6=DTYPE
;CLK1=CLOCK(5);[conns]SW1=G1.I1;SW2=G1.I2;SW3=G2.I1;SW4=G2.I2;CLK1=G6.CLK;G1=G3.I1,G6.SET,G7.I1
;G2=G3.I2,G4.I1;G3=G6.DATA;G4=G5.I1;G5=G6.CLEAR;G6.Q=G7I.2;G6.QBAR:G8.I1;G7=G9.I1;G8=G9.I2;[
monit]G9,G8;G6.DATA;
```

Listing 4: Obfuscated Code for Example 2

1.3 Example 3

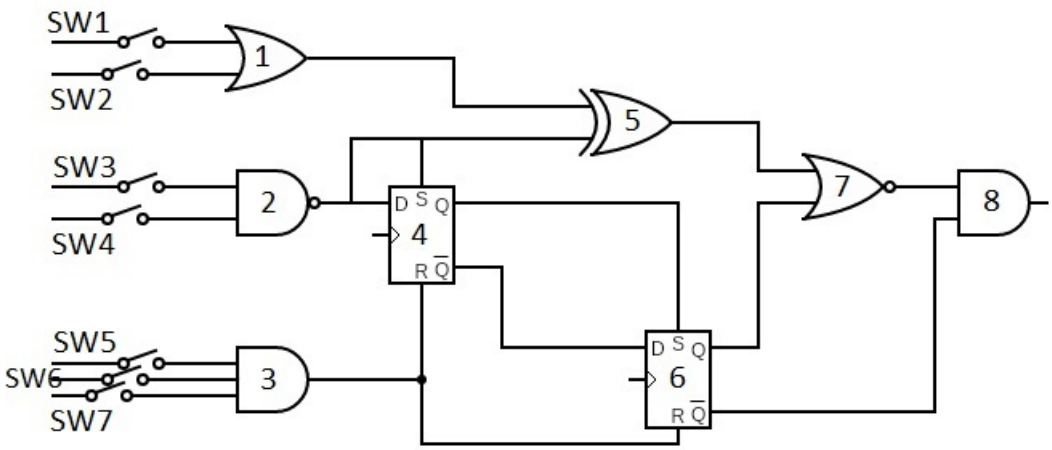

Figure 3: Example 3

The following is the EBNF for this circuit:

```
[devices]
    G1 = OR;
    G2 = NAND;
    G3 = AND(3);
    G5 = XOR;
    G7 = NOR;
    G8 = AND;

    SW1, SW2 = SWITCH;
    SW3, SW4 = SWITCH;
    SW5, SW6, SW7 = SWITCH;

    G4, G6 = DTYPE;
    CLK1 = CLOCK(10);

[conns]
    SW1 = G1.I1;
    SW2 = G1.I2;
    SW3 = G2.I1;
    SW4 = G2.I2;
    SW5 = G3.I1;
    SW6 = G3.I2;
    SW7 = G3.I3;

    CLK1 = G4.CLK;
    CLK1 = G6.CLK;

    G1 =  G5.I1;
    G2 =  G4.DATA, G4.SET, G5.I2;
    G3 =  G4.CLEAR, G6.CLEAR;
    G4.Q = G6.SET;
    G4.QBAR = G6.DATA;
    G5 =  G7.I1;
    G6.Q = G7.I2;
    G6.QBAR= G8.I2;
    G7 = G8.I1;

[monit]
    G5, G7, G8;
    G6.QBAR;
```

Listing 5: Code for Example 3

1.4 Example 4 - JK Bistable

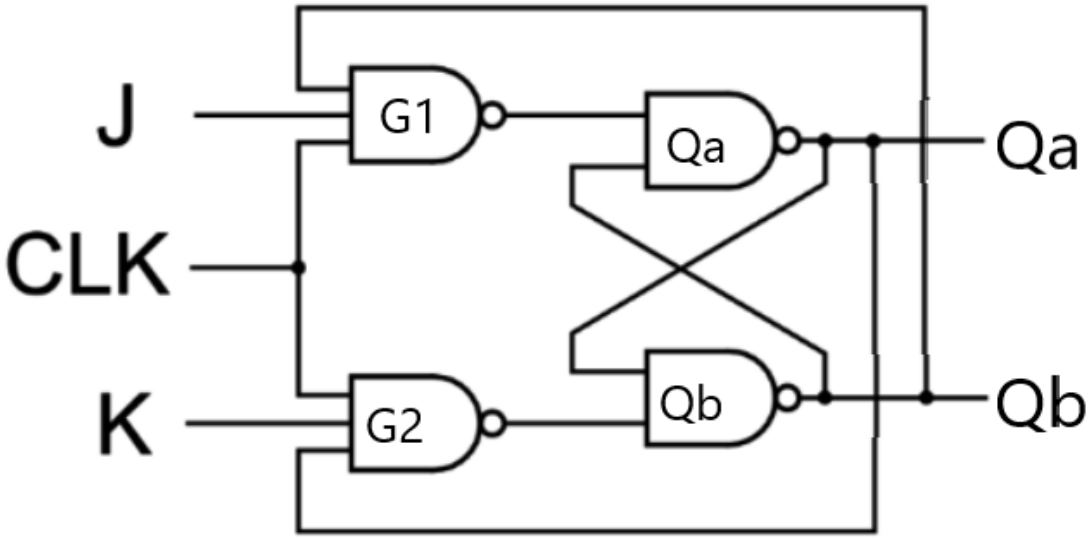

Figure 4: Example 4

The following is the EBNF for this circuit:

```
# JK BISTABLE

[devices]
Qa, Qb = NAND;
G1, G2 = NAND(3);
CLK1 = CLOCK(1);

J = SWITCH;
K = SWITCH;

[conns]

CLK1 = G1.I1, G2.I1;
J = G1.I2;
K = G2.I2;

Qa = G2.I3, Qb.I2;
Qb = G1.I3, Qa.I2;

G1 = Qa.I1;
G2 = Qb.I1;

[monit]

CLK1, Qa, Qb;
```

Listing 6: Code for Example 4

1.5 Example 5 - Counter

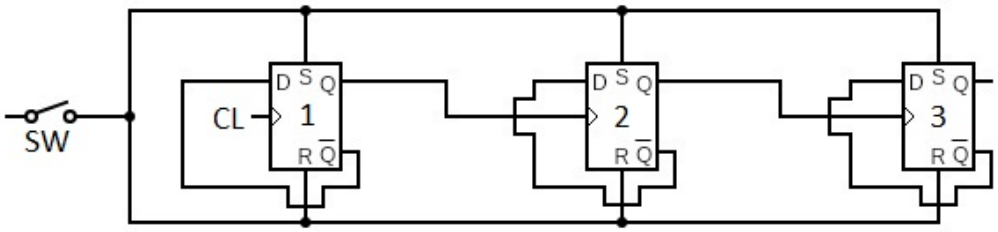

Figure 5: Example 5

The following is the EBNF for this circuit:

```
# Counter

[devices]
SW = SWITCH;
CL = CLOCK(1);
D1 = DTYPE;
D2 = DTYPE;
D3 = DTYPE;

[conns]
CL = D1.CLK;
D1.Q = D2.CLK;
D2.Q = D3.CLK;
D1.QBAR = D1.DATA;
D2.QBAR = D2.DATA;
D3.QBAR = D3.DATA;
SW = D1.CLEAR;
SW = D2.CLEAR;
SW = D3.CLEAR;
SW = D1.SET;
SW = D2.SET;
SW = D3.SET;


[monit]
CL;
D1.Q;
D2.Q;
D3.Q;
```

Listing 7: Code for Example 4