

1 Example Files

1.1 Example 1

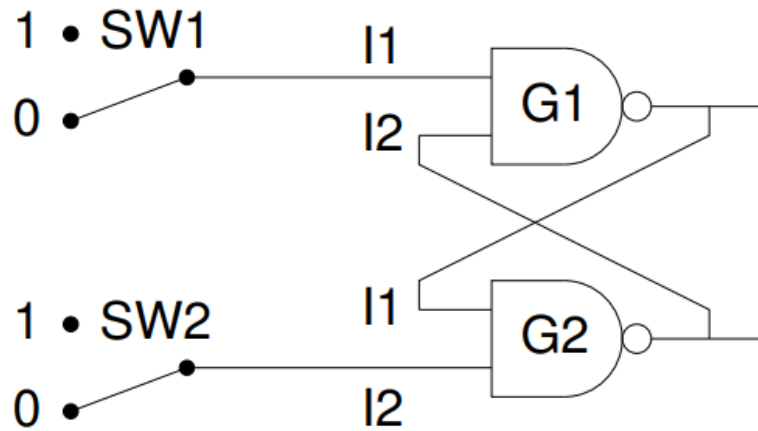


Figure 1: Example 1

The following is the EBNF for this circuit:

```
1 [devices]
2   G1, G2 = NAND;      # Defaults to 2 inputs
3   SW1, SW2 = SWITCH;  # Defaults to 0 i.Ie "False"
4
5 [conns]
6   SW1 = G1.I1;
7   SW2 = G2.I2;
8   G1=G2.I1;           # Whitespace not required
9   G2 = G2.I2;
10
11 # new blank lines are ignored
12
13 [monit]                # Need a newline after a block
14   G1, G2;
```

Listing 1: Code for example 1

```
1 [devices]G1,G2=NAND;SW1,SW2=SWITCH;[conns]SW1=G1.I1;SW2=G2.I2;G1=G2.I1;G2=G2.I2;[monit]G1,G2;
```

Listing 2: Obfuscated Code

1.2 Example 2

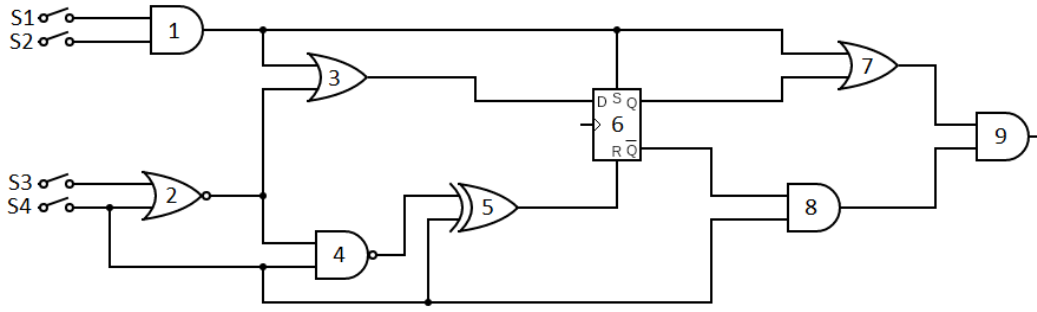


Figure 2: Example 2

The following is the EBNF for this circuit:

```

1 [devices]
2   G1, G8, G9 = AND;           # Default 2 input AND gate
3   G2 = NOR(2);                # Can specify number of inputs but defaults to 2 if not specified
4   G3, G7 = OR;
5   G4 = NAND;
6   G5 = XOR;
7
8   SW1, SW2 = SWITCH;          # Defaults to 0 which is "False"
9   SW3, SW4 = SWITCH(0);       # Can be specified as 0 for "False" but defaults to 0 if not specified
10
11  G6 = DTYPE;
12  CLK1 = CLOCK(5);             # Clock of period 5 (Not shown in the diagram)
13
14
15 [conns]
16
17  # Switch connections
18  SW1 = G1.I1;
19  SW2 = G1.I2;
20  SW3 = G2.I1;
21  SW4 = G2.I2;
22
23  # Clock to DTYPE
24  CLK1 = G6.CLK;
25
26  G1 = G3.I1, G6.SET, G7.I1;   # Can connect output to multiple inputs, SET is "S" in the diagram
27  G2 = G3.I2, G4.I1;
28  G3 = G6.DATA;                # DATA is "D" in the diagram
29  G4 = G5.I1;
30  G5 = G6.CLEAR;               # CLEAR is "R" in the diagram
31
32  G6.Q = G7.I2;                # Need to specify which output of DTYPE since there are 2
33  G6.QBAR: G8.I1;
34
35  G7 = G9.I1;
36  G8 = G9.I2;
37
38
39 [monit]
40   G9, G8;
41   G6.DATA;

```

Listing 3: Code for Example 2

```

1 [devices]G1,G8,G9=AND;G2=NOR(2);G3,G7=OR;G4=NAND;G5=XOR;SW1,SW2=SWITCH;SW3,SW4=SWITCH(0);G6=DTYPE
;CLK1=CLOCK(5);[conns]SW1=G1.I1;SW2=G1.I2;SW3=G2.I1;SW4=G2.I2;CLK1=G6.CLK;G1=G3.I1,G6.SET,G7.I1
;G2=G3.I2,G4.I1;G3=G6.DATA;G4=G5.I1;G5=G6.CLEAR;G6.Q=G7.I2;G6.QBAR:G8.I1;G7=G9.I1;G8=G9.I2;[
monit]G9,G8;G6.DATA;

```

Listing 4: Obfuscated Code for Example 2

1.3 Example 3

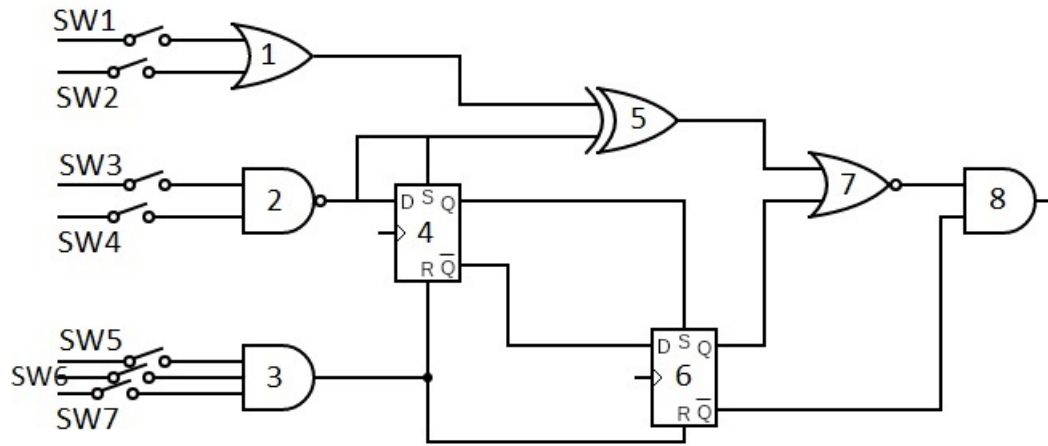


Figure 3: Example 3

The following is the EBNF for this circuit:

```

1 [devices]
2   G1 = OR;
3   G2 = NAND;
4   G3 = AND(3);
5   G5 = XOR;
6   G7 = NOR;
7   G8 = AND;
8
9   SW1, SW2 = SWITCH;
10  SW3, SW4 = SWITCH;
11  SW5, SW6, SW7 = SWITCH;
12
13  G4, G6 = DTYPE;
14  CLK1 = CLOCK(10);
15
16 [conns]
17  SW1 = G1.I1;
18  SW2 = G1.I2;
19  SW3 = G2.I1;
20  SW4 = G2.I2;
21  SW5 = G3.I1;
22  SW6 = G3.I2;
23  SW7 = G3.I3;
24
25  CLK1 = G4.CLK;
26  CLK1 = G6.CLK;
27
28  G1 = G5.I1;
29  G2 = G4.DATA, G4.SET, G5.I2;
30  G3 = G4.CLEAR, G6.CLEAR;
31  G4.Q = G6.SET;
32  G4.QBAR = G6.DATA;
33  G5 = G7.I1;
34  G6.Q = G7.I2;
35  G6.QBAR = G8.I2;
36  G7 = G8.I1;
37
38 [monit]
39  G5, G7, G8;
40  G6.QBAR;

```

Listing 5: Code for Example 3

1.4 Example 4

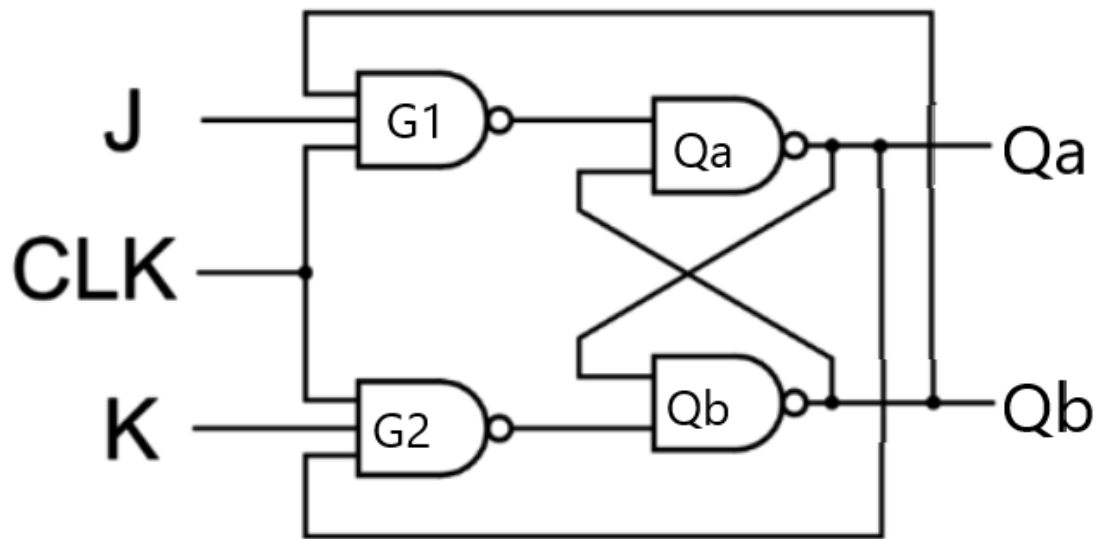


Figure 4: Example 4

The following is the EBNF for this circuit:

```
1 # JK BISTABLE
2
3 [devices]
4 Qa, Qb = NAND;
5 G1, G2 = NAND(3);
6 CLK1 = CLOCK(1);
7
8 J = SWITCH;
9 K = SWITCH;
10
11 [conns]
12
13 CLK1 = G1.I1, G2.I1;
14 J = G1.I2;
15 K = G2.I2;
16
17 Qa = G2.I3, Qb.I2;
18 Qb = G1.I3, Qa.I2;
19
20 G1 = Qa.I1;
21 G2 = Qb.I1;
22
23 [monit]
24
25 CLK1, Qa, Qb;
```

Listing 6: Code for Example 4