

1 選擇題 (2 pt each):

E

(1) Which of the following can be directly done by an application (i.e., not via a system call that asks the OS to do it) running in user mode?

- A) Disarm Interrupts
- B) Set the system timer
- C) Modify the interrupt vector
- D) Execute an I/O instruction
- E) None of the above can be done in user mode.

C

(2) ~~When a controller generates an interrupt, what happens?~~ ^{→ 107 有-一樣的}

- A) The OS checks between each instruction to see if an interrupt occurred.
- B) The OS checks to see which controller caused the interrupt.
- C) The hardware jumps to the handler through the interrupt vector.
- D) The running application calls the OS to handle the interrupt.
- E) None of the above happens after a controller generates an interrupt.

B

(3) ^{108 or 108 有-一樣的} When we allow preemption with a CPU scheduling algorithm we will often improve the average waiting time as we saw with the SRTF algorithm. But everything comes with a cost. What is the cost of allowing preemption in the scheduler?

- A) We introduce the convoy effect.
- B) We may see starvation.
- C) We will see a decrease in CPU utilization.
- D) We incur more context switches.
- E) None of the above is a cost of allowing preemption in the scheduler.

B

(4) What is the main disadvantage of Kernel Level Threads?

- A) They require an interrupt for each thread library call.
- B) A blocking system call will block the entire process.
- C) We never know what the underlying model is.
- D) They are not "thread safe".
- E) None of the above is the main disadvantage of User Level Threads.

D

(5) We illustrated the idea of the need for synchronization between processes by showing a problem with an instruction like $X=X+1$. What was the problem with this instruction?

- A) The compiler left a number in a register.
- B) The compiler produced code that was not reentrant.

- C) It was not atomic.
- D) Modern pipelined CPUs would execute things in the wrong order.
- E) None of the above explains the problem with this instruction.

- C (6) What is the meaning of the term "Unsafe State"?
- A) A process has gained control of the memory of another process.
 - B) Our memory is nearly full.
 - C) Two processes are each waiting for a resource the other process holds.
 - D) We cannot guarantee that we have enough resources to finish all running processes.
 - E) None of the above describes an "Unsafe State".

- D (7) If we are going to try to detect deadlocks, we need to decide when to do it. Which of these was NOT a suggestion as to when we might run the detection algorithm?
- A) at some time interval
 - B) when the system response is too slow
 - C) if some event wait lasts too long
 - D) when the CPU utilization is too low
 - E) All of the above were suggested times to check for deadlocks.

- A (8) 105, 108 都有
Why were multi-level page tables developed?
- A) It made lookup faster.
 - B) So they did not have to include the process identifier.
 - C) Page tables were so large that they caused external fragmentation.
 - D) So a system call was not necessarily.
 - E) None of the above

- A (9) 之前也寫過
What is the function of a log based file system?
- A) Log transactions of file system metadata updates to increase reliability.
 - B) Log all data writes for security auditing.
 - C) Log all file opens to limit access to files.
 - D) Log all data transactions to increase reliability.
 - E) None of the above

- C (10) 考過了
What is the advantage of RAID 6 over RAID 5?
- A) It is faster on a multi-block read.
 - B) It is faster on a multi-block write.

2. 記憶體空間較小

C) It can stand the loss of 2 drives at the same time.

D) It requires fewer extra drives.

E) None of the above is an advantage of RAID 6 over RAID 5.

③ 因為 0，所以不能 swap，會導致壽命降低，hard swapping 會耗電

2 (5 pt) Explain why mobile operating systems generally do not support swapping.

④ 因為 0，所以無需 swap，直接搬移就好了

3 (15 pt) Consider the following set of processes, with the length of the CPU burst given in milliseconds:

Process	Burst time	Priority
P1	9	3
P2	1	1
P3	3	3
P4	1	4
P5	5	2

The processes are assumed to have arrived in the order P1, P2, P3, P4 and P5 all at time 0.

Please draw four Gantt charts that illustrate the execution of these processes using the following scheduling algorithms: FCFS, SJF, nonpreemptive priority (a smaller priority number implies a higher priority), RR (quantum = 4).

4 (10 pt) suppose that a disk driver 5000 cylinders, numbered 0 to 4999. The drive is currently serving a request at cylinder 143, and the previous request was at cylinder 125. The queue of pending requests is

86, 1470, 800, 337, 4677, 890, 220, 32

What is the total distance (in cylinders) that the disk arm moves to satisfy all the requests for the algorithms?

a. (3pt) FCFS $143 + 57 + 1384 + 670 + 443 + 4340 + 3987 + 170 + 158$

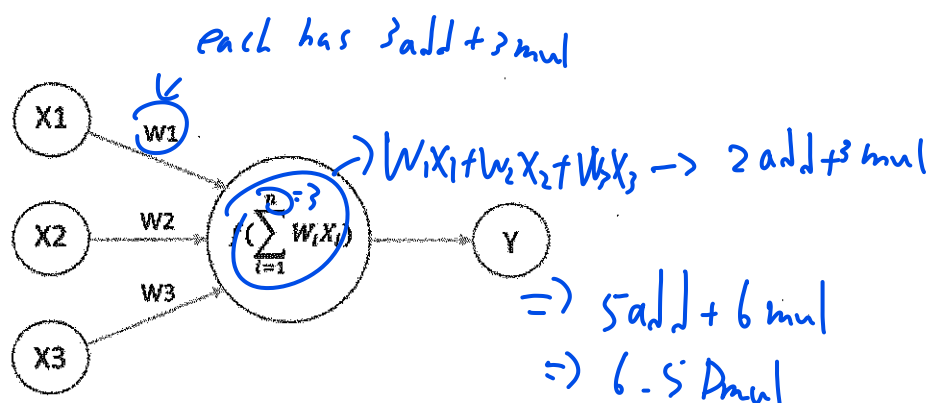
b. (3pt) SSTF $143 + 57 + 54 + 158 + 117 + 413 + 90 + 580 + 3207$

c. (4pt) C-LOOK $143 + 771 + 117 + 413 + 90 + 670 + 3207 + 4591 + 154$

5 (10 pt) In deep learning algorithms, neuron networks are applied to learn proper features to represent the input data. In the following simple neuron network, there are three inputs (X1, X2, X3) and one output (Y). The output Y can be computed

by $f(\sum_{i=1}^n W_i X_i)$, where $f(x) = \frac{1}{1+e^{-x}} \approx a + bx + cx^2$ is a non-linear sigmoid

function which modeled by a second-order polynomial function. If we assume the delay times for an adder and a multiplier are D_{ADD} and D_{MUL} , respectively. In addition, D_{ADD} is equal to $0.1 \times D_{MUL}$. Please determine the minimum delay time for this neuron network in terms of D_{MUL} . (Hint: You can perform multiplications and additions in parallel to minimize the delay time)



- 6 (5 pt) For the same neuron network shown in Problem 5, if we use a neuron processing unit (NPU) to compute the output of this neuron network, and the NPU has two adders and one multiplier. Thus, in one clock cycle, it can execute two additions and one multiplication simultaneously. Please determine the minimum clock cycles to compute the output of this neuron network when inputs are changed. *each w need only 3 mul times, and the whole part need 3 mul times*
 $\Rightarrow 6 \text{ Dmul}$
- 7 (5 pt) For the same neuron network shown in Problem 5, based on IEEE 754 standard, please calculate the memory space requirements for storing weight values (W_i) in single precision number, double precision number, and 16-bit fixed-point number format.
 $32 \times 3 = 96 \text{ bits}$ $64 \times 3 = 192 \text{ bits}$ $16 \times 3 = 48 \text{ bits}$
- 8 (5 pt) DRAM, SRAM, and flash memory are three primary memory types used in memory hierarchies. Which one has fastest access time?

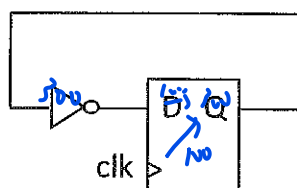
8. SRAM \rightarrow 100ns \rightarrow DRAM \rightarrow Flash

- 9 (8 pt) The following is a logic circuit, consisting of an inverter and a flip-flop.

(a) Describe the function of the circuit with its next state equation.

(b) Assume the setup time, clock-to-q delay, and hold time of the flip-flop are 100ps, 100ps, and 300ps respectively, and the inverter has 300ps delay.

What is the maximum operating frequency of the circuit?

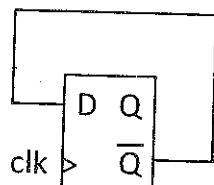


$(a) \Rightarrow Q = \neg Q$ (toggle)
 $(b) \Rightarrow 300 + 100 + 300 = 700$
 $\Rightarrow \frac{1}{700}$

- 10 (7 pt) Redo Problem 9 for the following circuit.

$$(a) \rightarrow Q = !Q$$

$$(b) 300 + 100 = 400 \rightarrow \frac{1}{400}$$



- 11 (10 pt) A page-based virtual memory system is similar to a fully-associative cache, where the basic management units are memory pages and cache blocks respectively. What is the relationship between a "page table" and a "cache tag RAM"? Describe how to check whether an item exists in the physical memory or cache?

(1) we can find the address both by page table and cachetag for the actual disk/memory

(2)
cache: valid bit
memory: dirty bit