1 選擇題 (2 pt each):

B (1) If a program terminates abnormally, a dump of memory may be examined by a ____ to determine the cause of the problem.
A) module
B) debugger
C) shell
D) control card

A (2) A boot block ____.
A) typically only knows the location and length of the rest of the bootstrap program
B) typically is sophisticated enough to load the operating system and begin its execution
C) is composed of multiple disk blocks
D) is composed of multiple disk cylinders

A (3) Which of the following statements is true?
A) Shared memory is typically faster than message passing.
B) Message passing is typically faster than shared memory.
C) Message passing is most useful for exchanging large amounts of data.
D) Shared memory is far more common in operating systems than message passing.

A (4) According to Amdahl's Law, what is the speedup gain for an application that is 60% parallel and we run it on a machine with 4 processing cores?
A) 1.82
B) .7
C) .55
D) 1.43

$\frac{1}{1-P+\frac{P}{N}} = \frac{1}{0.4+0.15} = \frac{1}{0.55} = 1.818$

B (5) Which of the following is true of multilevel queue scheduling?
A) Processes can move between queues.
B) Each queue has its own scheduling algorithm.
C) A queue cannot have absolute priority over lower-priority queues.
D) It is the most general CPU-scheduling algorithm.

C (6) _____ occurs when a higher-priority process needs to access a data structure that is currently being accessed by a lower-priority process.

A) A race condition
B) Deadlock
C) Priority inversion
D) A critical section

B (7) How many philosophers may eat simultaneously in the Dining Philosophers problem with 5 philosophers?
A) 1
B) 2
C) 3
D) 5

B (8) Suppose that there are ten resources available to three processes. At time 0, the following data is collected. The table indicates the process, the maximum number of resources needed by the process, and the number of resources currently owned by each process. Which of the following correctly characterizes this state?

Process	Maximum Needs	Currently Owned
P_0	10	4
P_1	3	1
P_2	6	4

A) It is safe.
B) It is not safe.
C) The state cannot be determined.
D) It is an impossible state.

C (9) Assume a system has a TLB hit ratio of 90%. It requires 15 nanoseconds to access the TLB, and 85 nanoseconds to access main memory. What is the effective memory access time in nanoseconds for this system?
A) 22
B) 100
C) 108.5
D) 176.5

EMAT = (0.9×15) + (0.1×85)
= 108.5ns

B (10) Suppose that the operating system uses two internal tables to keep track of open files. Process A has two files open and process B has three files open.

Two files are shared between the two processes. How many entries are in the per-process table of process A, the per-process table of process B, and the system-wide tables, respectively?

A) 5, 5, 5
B) 2, 3, 3
C) 2, 3, 5
D) 2, 3, 1

2 (5 pt) What are the two major problems associated with linked allocation of disk space routines?

3 (8 pt) The read/write speeds of SSDs (solid state drives) are much higher than those of HDDs (hard disk drives). However, an SSD can only be written to a limited amount of data before it reaches its end-of-life. A professor builds a RAID 4 system and uses 7 HDDs as data drives and an SSD as the parity drive. Please discuss the pros and cons of his design.

4 (9 pt) A professor has a solution of the reader-writer problem. The solution is based on spin-locks. Assume that the system has 100,000 locks. A reader must acquire a lock to enter the critical section, and a writer must acquire 100,000 locks to enter the critical section. Please implement his solution in C language.

5 (8 pt) Consider a CPU that supports the "TestAndSet" instruction. An engineer uses the instruction to solve the critical section problem, and his solution is shown below. A correct solution must satisfy three conditions, i.e., mutual exclusion, progress, and bounded waiting. Please prove or disprove the correctness of his solution.

```
while (TRUE) {
  while ( TestAndSet (&lock))
  ;    // do nothing

  //    critical section

  lock = FALSE;

  //       remainder section
}
```

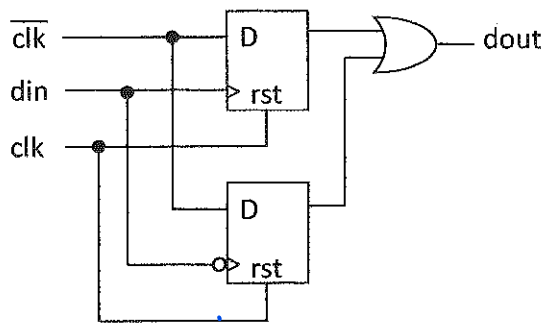
6 (5 pt) If we want to design an adder to compute the addition of two 16-bit unsigned numbers with **ONLY** 4-bit carry-look-ahead (CLA) adders and 2-to-1 multiplexers. The delay time of a 4-bit CLA adder and a 2-to-1 multiplexer are D_{CLA} and D_{MX}, respectively. In addition, D_{MX} is equal to $0.2 \times D_{CLA}$. Please determine the minimum delay time for this 16-bit adder in terms of D_{CLA}.

7 (5 pt) Based on IEEE 754 standard, the single precision numbers are stored in 32 bits with one sign bit, eight exponent bits, and 23 mantissa bits. Please show the representation of -0.6875.

8 (5 pt) Caches take advantage of temporal locality and spatial locality to improve the performance of the memory. Please briefly explain what is temporal locality and spatial locality.

9 (10 pt) The following techniques have been developed for cache optimizations: "Pipelined cache" and "multi-banked cache." Please briefly explain these techniques and how they work.

10 (8 pt) The following circuit is composed of two D-type flip-flops (DFFs) and an OR gate, where the DFFs are reset when clk=1. Describe the function of the circuit and one possible application of it.



11 (8 pt) The following is a code segment in MIPS assembly, where JAL (jump and link) jumps to the label j_target and saves its return address in R31 and JR returns to the next instruction of JAL.

```
        JAL j_target
        ...
j_target  JR R31
```

List all possible hazards when the code is executed on a classical 5-stage pipelined datapath (i.e. fetch, decode, execute, memory, and write_back). What are the minimum cycles for an interlock unit to resolve each hazard without data forwarding?

12 (9 pt) Briefly describe the basic ideas of the following terms in computer designs: (a) TLB, (b) BTB, and (c) AMAT.

9-1
The processor sends the cache address to the cache controller.
The cache controller determines which bank the address belongs to.
The cache controller sends the request to the corresponding bank.
The bank decodes the address and looks up the tag in the tag array.
If the tag match is found, the bank starts accessing the data block from the data array.
While the data block is being accessed, the cache controller can send other requests to other banks.
Once the data block is accessed, it is sent to the processor.

9-2
1.The processor sends the cache address to the cache.

2.The cache decodes the address and looks up the tag in the tag array.

3.If the tag match is found, the cache starts accessing the data block from the data array.

4.While the data block is being accessed, the cache can start processing the next request.

5.Once the data block is accessed, it is sent to the processor.