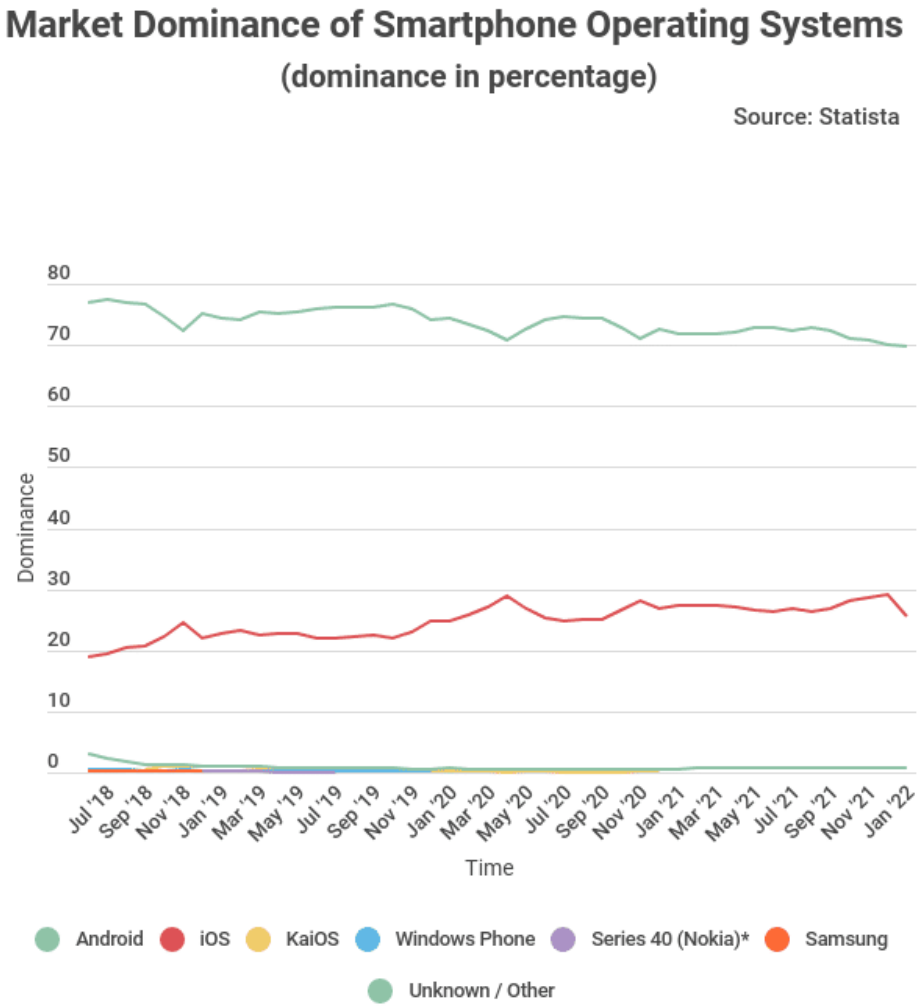
围观ART for RV的移植过程

史宁宁
PLCT实验室
shiningning@iscas.ac.cn

Android蓬勃发展



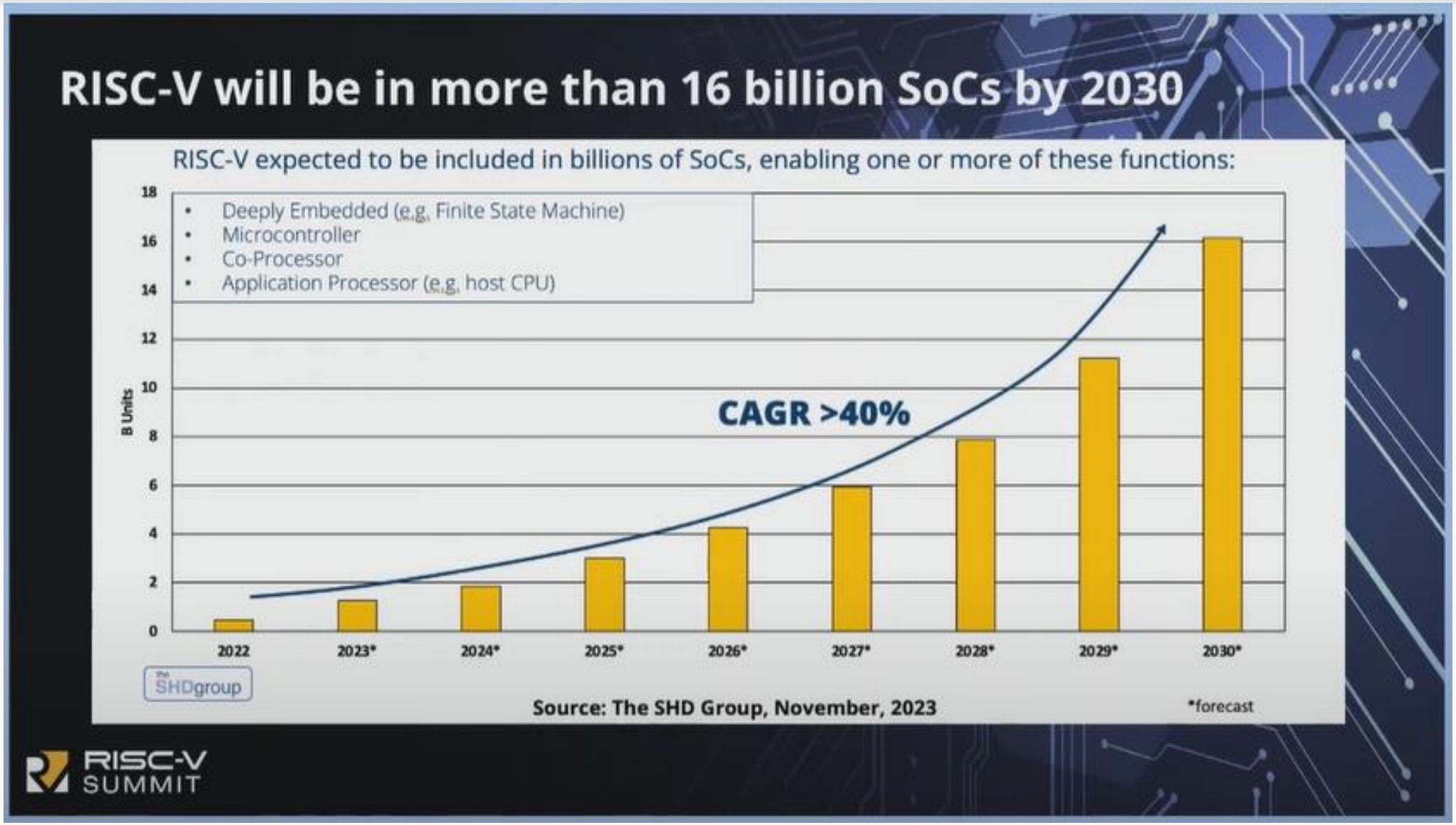
Android操作系统虽然在手机、平板电脑等领域的占比略有下降，但是相较于其他系统而言，仍然是遥遥领先。

From: https://stockapps.com/blog/android-loses-8-of-its-global-os-market-share-in-five-years/

Android Ecosystem

From: <The Android Open Source Project and RISC-V>
https://www.youtube.com/watch?v=70O_RmTWP58&list=PL85jopFZCnbPPRyjl_qMQ50DPq_iQKhFg&index=6

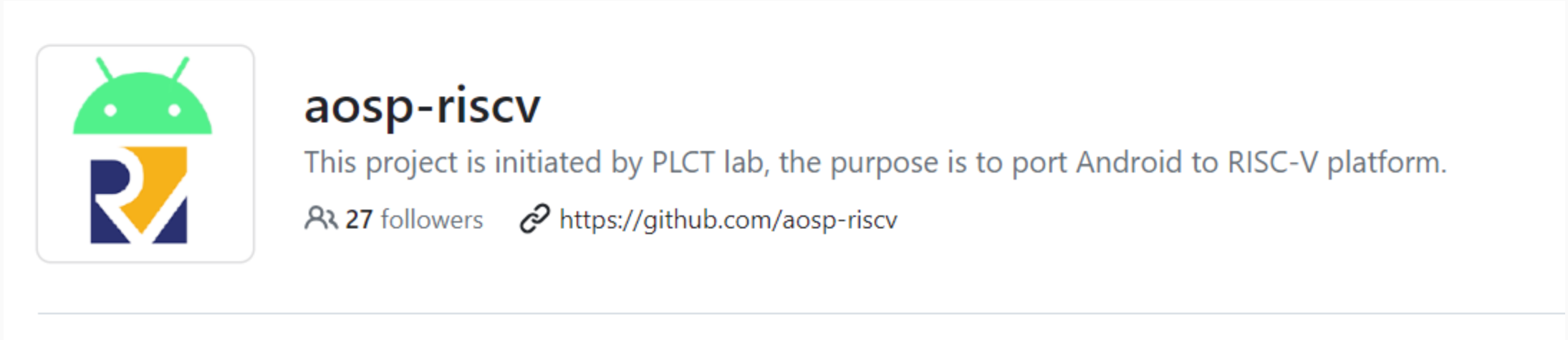
RISC-V的快速成长



From: <RISC-V is Here! Innovation and Adoption Driving the Open Compute Future>
https://www.youtube.com/watch?v=yB4rEYKhHrs&list=PL85jopFZCnbMfMRR25ENcRkhhAUGwP5C5

Android for RISC-V —— 启动

2020 年 8 月，PLCT 实验室开始尝试基于 AOSP 10 实现 RISC-V 的移植工作。 2020 年 12 月完成了 bionic 的移植并实现了一个 第一个 RISC-V 上的“Android 最小系统”(https://zhuanlan.zhihu.com/p/302870095)。建立公开的开发仓库： https://github.com/aosp-riscv。



From:汪辰《AOSP RISC-V 进展 - 向 Google 上游提交》

Android for RISC-V —— Android 10

2021 年 1 月，阿里巴巴旗下的平头哥半导体 (T-Head) 成功将 AOSP 10 移植到自己的 RISC-V 芯片上，并开源部分代码，开源仓库地址在：https://github.com/T-head-Semi/aosp-riscv 。

2021 5 月 20 日，RVI Android SIG 成立 - Han Mao (Alibaba)/Zheng Zhang (Imagination) 担任 chair/vice char。https://lists.riscv.org/g/sig-android/message/1 。PLCT 实验室积极参与。

2021 7 月 20 日，第一次 RVI Android SIG 会议，建立 RVI Android SIG 的官方主页 https://lists.riscv.org/g/sig-android，并制定了初步的开发任务列表: https://lists.riscv.org/g/sig-android/message/5 。

2021 10 月 20 日，RVI Android SIG 的官方源码仓库建立（基于 AOSP 10）：https://github.com/riscv-android-src。PLCT 实验室同时宣布加入，并贡献了第一个 PR：https://github.com/riscv-android-src/toolchain-llvm_android/pull/1 。同时开始启动向 AOSP 12 的移植工作。

From:汪辰《AOSP RISC-V 进展 - 向 Google 上游提交》

Android for RISC-V —— Android 12

Setup Android 12 on RISC-V

To download the RISC-V Android source tree to your working directory:

```
mkdir ~/riscv-android-src && cd ~/riscv-android-src
repo init -u git@github.com:riscv-android-src/manifest.git -b riscv64-android-12.0.0_dev
repo sync
cd prebuilts/rust/
git lfs pull
cd -
cd cts/
git lfs pull
cd -
rm external/angle/Android.bp
```

From: https://github.com/riscv-android-src/riscv-android/blob/main/doc/android12.md

Android for RISC-V ——Google

Google wants RISC-V to be a “tier-1” Android architecture

Google's keynote at the RISC-V Summit promises official, polished support.

RON AMADEO - 1/4/2023, 5:14 AM

From: https://arstechnica.com/gadgets/2023/01/google-announces-official-android-support-for-risc-v/

Android for RISC-V ——现状与未来

- At this time, these patches will support building and running a basic Android Open Source Project experience, but are not yet fully optimized. For example, work on a fully optimized backend for the Android Runtime (ART) is still a work in progress.

- Later this year, we expect to have the NDK ABI finalized and canary builds available on Android's public CI soon and RISC-V on x86-64 & ARM64 available for easier testing of riscv64 Android applications on a host machine. By 2024, the plan is to have emulators available publicly, with a full feature set to test applications for various device form factors!

From: https://opensource.googleblog.com/2023/10/android-and-risc-v-what-you-need-to-know.html

ART（Android Runtime）

ART:

Android Runtime

Runs Android framework and applications
Interpreter, JIT, profile based compiler

Manages application memory
Memory allocator, Garbage collector

From: Understanding Android Runtime (ART) for faster https://www.youtube.com/watch?v=1uLzSXWWfDgAndroid Developers

ART for RISC-V —— 代码提交

Android Open Source Project | CHANGES | YOUR | DOCUMENTATION | BROWSE | project:platform/art riscv64

	Subject	Owner	Reviewers	Repo	Branch	Updated	Size	Status	CR	PV	L
☆	riscv64: SPUT variants	Jaeheon Yi	Vladimír	platform/art	main	12:46 PM	L	4 missing			
☆	riscv64: Implement RISC-V Vector instructions	Roman Artem…	Santiago, Vladimír	platform/art	main	4:50 AM	XL	4 missing			
☆	riscv64: RISC-V RVV assembler tests	Roman Artem…	Santiago, Vladimír	platform/art	main	4:48 AM	XL	4 missing			
☆	riscv64: Support RISC-V RVV in disassembler	Roman Artem…	Santiago, Vladimír	platform/art	main	4:48 AM	L	4 missing			
☆	Add symbol visibility attributes for libart-runtime	Dmitrii Ishche…		platform/art	main (hide-libart-runtime-symbols)	4:18 AM	XL	3 missing			
☆	riscv64: Clean up the `SystemArrayCopy` intrinsic.	Vladimír Marko	Santiago	platform/art	main	12:00 AM	L	2 missing			
☆	riscv64: Implement SystemArrayCopy intrinsic	Aleksandr Sol…	Santiago, Vladimír	platform/art	main	Dec 12	L	Merged			
☆	riscv64: polymorphic and custom invoke	Jaeheon Yi	Vladimír	platform/art	main	Dec 12	M	Merged			
☆	riscv64: re-enable "0/1-arg" invoke fast path	Jaeheon Yi	Vladimír	platform/art	main	Dec 12	M	Merged			
☆	riscv64: Implement `Reference` intrinsics.	Vladimír Marko	Hans	platform/art	main	Dec 12	M	Merged			
☆	riscv64: Update opensbi version in buildbot-vm.sh	Vladimír Marko	Santiago	platform/art	main	Dec 11	XS	Merged			
☆	riscv64: Add RISC-V Vector register definitions	Roman Artem…	Santiago, Vladimír	platform/art	main	Dec 11	M	Merged			
☆	Draft implementation of art jni optimization.	Hang Lu	Vladimír	platform/art	main	Dec 11	L	6 missing			-1
☆	Reapply "riscv64: re-enable an invoke fast path"	Jaeheon Yi	Vladimír	platform/art	main	Dec 08	M	Merged			
☆	~~riscv64: Gather Nterp invoke logic for image writer~~	Jaeheon Yi	Vladimír	platform/art	main	Dec 07	M	Abandoned			
☆	riscv64: Implement `Integer/Long.reverse()` intrinsics.	Vladimír Marko	Santiago	platform/art	main	Dec 06	M	Merged			
☆	riscv64: Implement Unsafe.getAndAdd/-Set intrinsics.	Vladimír Marko	Santiago	platform/art	main	Dec 04	M	Merged			
☆	riscv64: Implement Unsafe CAS intrinsics.	Vladimír Marko	Santiago	platform/art	main	Dec 01	M	Merged			
☆	riscv64: Fix VarHandle GetAndUpdate intrinsic.	Vladimír Marko	Santiago	platform/art	main	Dec 01	L	Merged			
☆	riscv64: Fix VarHandle.compareAndSet intrinsics.	Vladimír Marko	Santiago	platform/art	main	Nov 30	M	Merged			
☆	riscv64: Fix reference load in VarHandle checks.	Vladimír Marko	Santiago	platform/art	main	Nov 30	XS	Merged			
☆	riscv64: Pass codegen through to GenerateReverseBytes	Samuel Holland	Santiago, Vladimír	platform/art	main	Nov 29	S	Merged			
☆	riscv64: Disable VarHandle.compareAndSet intrinsics.	Vladimír Marko	Santiago	platform/art	main	Nov 29	XS	Merged			
☆	riscv64: Implement Unsafe get/put intrinsics.	Vladimír Marko	Santiago	platform/art	main	Nov 28	L	Merged			
☆	riscv64: Implement VarHandle.GetAndUpdate intrinsics.	Vladimír Marko	Santiago	platform/art	main	Nov 24	L	Merged			

Page 1 >

From: https://android-review.googlesource.com/q/project:platform/art+riscv64

ART for RISC-V —— comments

Shining

compiler/optimizing/code_generator_riscv64.cc

#2899

Shining Patchset 1 Jun 16, 2023

The '{}' in 'case MethodLoadKind::kRuntimeCall:' maybe is not needed.

Vladimír Marko Done Patchset 1

Resolved REPLY QUOTE

```
2896    case MethodLoadKind::kRecursive:
2897      callee_method = invoke->GetLocations()->InAt(invoke->GetCurrentMethodIndex());
2898      break;
2899    case MethodLoadKind::kRuntimeCall: {
2900      GenerateInvokeStaticOrDirectRuntimeCall(invoke, temp, slow_path);
2901      return;  // No code pointer retrieval; the runtime performs the call directly.
2902    }
```

VIEW DIFF

#2917

Shining Patchset 1 Jun 16, 2023

The '{}' in 'default' maybe is not needed.

Vladimír Marko Done Patchset 1

Resolved REPLY QUOTE

```
2914        break;
2915      }
2916      FALLTHROUGH_INTENDED;
2917    default: {
2918      LoadMethod(invoke->GetMethodLoadKind(), temp, invoke);
2919      break;
2920    }
```

VIEW DIFF

From: https://android-review.googlesource.com/c/platform/art/+/2623807

ART for RISC-V —— 代码分析

知乎 | 专栏
ART RV64 代码分析

ART RV64 代码分析

分析Android Runtime RV64代码


编译船夫 · 19 篇内容

收录内容　修改介绍　…

ART RV64：Codegen提交总结(3)

二十一、 Add Finalize 本次分析所涉及的代码：2637494: RISCV: [Codegen] Add Finalize | android-review.googlesource.com... 背景介绍： 1、本次提交的内容，属于在 compiler/optimizing/code_generator_riscv64... 阅读全文

▲ 赞同 2　添加评论　分享　收藏　…

From: https://www.zhihu.com/column/c_133866135

ART for RISC-V —— 代码分析（续）

一、Define Registers for RISCV in Codegen

本次分析涉及代码： 2619265: RISCV: Define Registers for RISCV in Codegen | android-review.googlesource.com...

背景介绍：

无

提交内容分析：

1、本次提交在compiler/optimizing/code_generator.cc 添加了RV64 Codegen相关的CodeGeneratorRISCV64的相关内容，让Codegen支持RV64；

2、本次提交在compiler/optimizing/code_generator_riscv64.h中添加了几乎所有的头文件内容，并且新增了compiler/optimizing/code_generator_riscv64.cc文件；

3、本次提交在code_generator_riscv64.h和code_generator_riscv64.cc中，除了给Codegen定义寄存器，还添加了CodeGeneratorRISCV64类及其成员函数的声明和定义，但是这些成员函数基本上都没实现，留作后续继续实现；

总结延伸：

1、compiler/optimizing/code_generator_riscv64.h和compiler/optimizing/code_generator_riscv64.cc之中，并不是只有CodeGeneratorRISCV64类的声明和实现，此外还有LocationsBuilderRISCV64类和InstructionCodeGeneratorRISCV64类的声明和实现；

三、Add SetupBlockedRegisters

本次分析所涉及代码：2623801: RISCV: [Codegen] Add SetupBlockedRegisters | android-review.googlesource.com...

背景介绍：

1、本次提交的内容，属于在compiler/optimizing/code_generator_riscv64.cc之中去实现之前没有实现的具体函数；code_generator_riscv64.cc的框架是之前“ 2619265: RISCV: Define Registers for RISCV in Codegen | android-review.googlesource.com...”提交的；

提交内容分析：

1、本次提交将之前未实现（只有函数体）的compiler/optimizing/code_generator_riscv64.cc之中的CodeGeneratorRISCV64::AddLocationAsTemp()和CodeGeneratorRISCV64::SetupBlockedRegisters()两个函数进行了实现；

2、本次提交还在runtime/arch/riscv64/registers_riscv64.h中的FRegister中增加了FTMP，它是在本次提交新增的SetupBlockedRegisters()之中使用的；

总结延伸：

无

ART for RISC-V —— 课程

课程名称：一起围观ART的RISC-V实现

内容：

1、ART基础
2、ART/Android的源码构建
3、ART RV测试
4、ART RV的初始化
5、ART RV指令集/寄存器的添加
6、ART RV汇编器
7、ART RV JNI 相关内容
8、添加CodeGen的RISC-V支持
9、ART RV解释器
10、ART RV工具

Android/ART 相关资源地址

- Android源码在线查看 https://cs.android.com/
- Android源码库 https://android.googlesource.com/
- ART(Android Runtime)源码库https://android.googlesource.com/platform/art/
- Android补丁review网站 https://android-review.googlesource.com/
- 毛晗 - RISC-V 支持安卓的进展介绍https://www.bilibili.com/video/BV1RF41167nd/
- 夏立方 - Android ART for RISCV 介绍https://www.bilibili.com/video/BV1rm4y1K7mS/
- android-and-risc-v-what-you-need-to-know
- Android ART Optimization in XuanTie C920
- Challenges in Porting Android to RISC-V

Thanks!