修复内核编译错误

PLCT Lab OpenDay 2023　邢明政

前言

- 本人角色简介：

  openEuler RISC-V Kernel 维护

  - 内核适配
  - 版本升级
  - 编译、出包、测试
  - 合入新特性
  - Kernel 相关软件包的适配

内核编译错误

Toolchain: GCC 12.3.0 + Binutils 2.37

```
  CC      arch/riscv/kernel/vdso/vgettimeofday.o
  <<BUILDDIR>>/arch/riscv/include/asm/vdso/gettimeofday.h: Assembler messages:
  <<BUILDDIR>>/arch/riscv/include/asm/vdso/gettimeofday.h:79: Error: unrecognized opcode
`csrr a5,0xc01'
```

尝试在主线内核解决

```
diff --git a/arch/riscv/Kconfig b/arch/riscv/Kconfig
index 4c07b9189c86..b49cea30f6cc 100644
--- a/arch/riscv/Kconfig
+++ b/arch/riscv/Kconfig
@@ -570,11 +570,15 @@ config TOOLCHAIN_HAS_ZIHINTPAUSE
 config TOOLCHAIN_NEEDS_EXPLICIT_ZICSR_ZIFENCEI
        def_bool y
        # https://sourceware.org/git/?p=binutils-gdb.git;a=commit;h=aed44286efa8ae8717a77d94b51ac3614e2ca6dc
-       depends on AS_IS_GNU && AS_VERSION >= 23800
+       # https://gcc.gnu.org/git/?p=gcc.git;a=commit;h=98416dbb0a62579d4a7a4a76bab51b5b52fec2cd
+       depends on CC_IS_GCC && GCC_VERSION >= 120100 || \
+                  AS_IS_GNU && AS_VERSION >= 23800
        help
          Newer binutils versions default to ISA spec version 20191213 which
          moves some instructions from the I extension to the Zicsr and Zifencei
          extensions.
+         Similarly, GCC release 12.1.0 has changed the default ISA spec version to
+         20191213, so the above situation requires this option to be enabled.

 config TOOLCHAIN_NEEDS_OLD_ISA_SPEC
        def_bool y
--
```

问题根源

RISC-V GNU toolchain bumping default ISA spec to 20191213

Kito Cheng

收件人 RISC-V SW Dev (sw-dev@groups.riscv.org)、Nelson Chu、Andrew Waterman、Palmer D

Hi

It's Kito Cheng from the RISC-V GCC community, just sharing some news about the default ISA spec version that has been bumped to 20191213 on both RISC-V GCC and binutils recently, and that has one major incompatibility issue between current default ISA spec versions.

The major incompatibility issue is the csr read/write (csrr*/csrw*) instructions and fence.i instruction has separated from the `I` extension, become two standalone extensions: Zicsr and Zifencei; so you might get error messages like that: unrecognized opcode `csrr`.

How to resolve those issues?

Here is two solution to resolve:

- First one is what we recommend, adding zicsr and/or zifencei to your -march option, e.g. -march=rv64imac become -march=rv64imac_zicsr_zifencei

- The second one is a kind of workaround, using -misa-spec=2.2 to force RISC-V GCC using the older ISA spec version, however this is strongly *NOT* recommended.

- RISC-V GCC 和 Binutils 默认 ISA spec 版本升级到了 20191213，原 2.2 版本中的 I 扩展有指令被拆分出来
  - csr read/write => Zicsr
  - fence.i => Zifencei
- https://groups.google.com/a/groups.riscv.org/g/sw-dev/c/aE1ZeHHCYf4

问题根源

GCC 12.1.0

git://gcc.gnu.org / gcc.git / commit

summary | shortlog | log | commit | commitdiff | tree
(parent: 634de54) | patch

RISC-V: Change default ISA version into 20191213

author	Jia-Wei Chen <jiawei@iscas.ac.cn>	
	Tue, 18 Jan 2022 02:34:24 +0000 (10:34 +0800)	
committer	Kito Cheng <kito.cheng@sifive.com>	
	Mon, 24 Jan 2022 09:42:21 +0000 (17:42 +0800)	
commit	98416dbb0a62579d4a7a4a76bab51b5b52fec2cd	
tree	363d3b1e5b3cc003659c7102d9880725d491f866	tree
parent	634de54f9c421b7069865d0d7365ad97412f34bd	commit | diff

```
RISC-V: Change default ISA version into 20191213

Bump default ISA spec to newer version 20191213, current default ISA spec
is 2.2, but it's already out of date for a long time, sync with binutils
ISA version, convention in toolchain use.

gcc/ChangeLog:

* config.gcc: Modify default isa_spec version.
```

Binutils 2.38

git://sourceware.org / binutils-gdb.git / commit

summary | shortlog | log | commit | commitdiff | tree
(parent: 6540edd) | patch

RISC-V: Updated the default ISA spec to 20191213.

author	Nelson Chu <nelson.chu@sifive.com>	
	Thu, 30 Dec 2021 15:23:46 +0000 (23:23 +0800)	
committer	Nelson Chu <nelson.chu@sifive.com>	
	Fri, 7 Jan 2022 10:48:29 +0000 (18:48 +0800)	
commit	aed44286efa8ae8717a77d94b51ac3614e2ca6dc	
tree	8e9da28a51ecb8f5293c0db273df74ad525c41d4	tree
parent	6540edd52cc061071e1ad02c381e85de41bded1f	commit | diff

```
RISC-V: Updated the default ISA spec to 20191213.

Update the default ISA spec from 2.2 to 20191213 will change the default
version of i from 2.0 to 2.1.  Since zicsr and zifencei are separated
from i 2.1, users need to add them in the architecture string if they need
fence.i and csr instructions.  Besides, we also allow old ISA spec can
recognize zicsr and zifencei, but we won't output them since they are
already included in the i extension when i's version is less than 2.1.

bfd/
* elfxx-riscv.c (riscv_parse_add_subset): Allow old ISA spec can
```

内核编译测试

Here are the results of my tests:

gcc	binutils	patched	no patch
11.4.0	2.35	ok	ok
11.4.0	2.36	ok	ok
11.4.0	2.38	ok	ok
12.2.0	2.35	ok	error[1]
12.2.0	2.36	ok	error[2]
12.2.0	2.38	ok	ok
10.5.0	2.35	ok	ok
10.5.0	2.36	ok	ok
10.5.0	2.38	ok	error[3]
11.1.0	2.35	ok	ok
11.1.0	2.36	ok	ok
11.1.0	2.38	ok	ok
11.2.0	2.35	ok	ok
11.2.0	2.36	ok	ok
11.2.0	2.38	ok	ok

[1]
Assembler messages:
Fatal error: -march=rv32imafd_zicsr_zifencei: Invalid or unknown z ISA extension: 'zifencei'
make[2]: *** [arch/riscv/kernel/compat_vdso/Makefile:47: arch/riscv/kernel/compat_vdso/rt_sigreturn.o] Error 1

[2]
./arch/riscv/include/asm/vdso/gettimeofday.h: Assembler messages:
./arch/riscv/include/asm/vdso/gettimeofday.h:79: Error: unrecognized opcode `csrr a5,0xc01'
./arch/riscv/include/asm/vdso/gettimeofday.h:79: Error: unrecognized opcode `csrr a5,0xc01'
./arch/riscv/include/asm/vdso/gettimeofday.h:79: Error: unrecognized opcode `csrr a5,0xc01'
./arch/riscv/include/asm/vdso/gettimeofday.h:79: Error: unrecognized opcode `csrr a5,0xc01'
make[2]: *** [scripts/Makefile.build:243: arch/riscv/kernel/vdso/vgettimeofday.o] Error 1

[3]
cc1: error: '-march=rv64imac_zicsr_zifencei': unsupported ISA subset 'z'
cc1: error: ABI requires '-march=rv64'
make[2]: *** [scripts/Makefile.build:243: scripts/mod/empty.o] Error 1
make[2]: *** Waiting for unfinished jobs....
cc1: error: '-march=rv64imac_zicsr_zifencei': unsupported ISA subset 'z'
cc1: error: ABI requires '-march=rv64'

新的问题

- **Binutils 2.36** 开始支持 Zifencei ，并对 I 扩展拆分
- GCC 11.1.0 开始支持了 **-march** 指定新扩展

新的问题

- **Binutils 2.36** 开始支持 Zifencei ，并对 I 扩展拆分
- GCC 11.1.0 开始支持了 **-march** 指定新扩展
- GCC bugfix backport: **12.1.0 , 11.3.0**

问题根源

git://sourceware.org / binutils-gdb.git / commit

summary | shortlog | log | commit | commitdiff | tree
(parent: d5a71b1) | patch

RISC-V: Add i-ext as the implicit extension when e-ext is set.

```
author     Nelson Chu <nelson.chu@sifive.com>
           Mon, 12 Apr 2021 08:58:47 +0000 (16:58 +0800)
committer  Nelson Chu <nelson.chu@sifive.com>
           Mon, 12 Apr 2021 09:51:07 +0000 (17:51 +0800)
commit     f0bae2552db1dd4f1995608fbf6648fcee4e9e0c
tree       a0a6692a3a876f275e796099ea5291349716e1ed        tree
parent     d5a71b1131778cf2a023855966831eb2457d50d6        commit | diff
```

```
RISC-V: Add i-ext as the implicit extension when e-ext is set.

The linker does not care the default versions of the extensions, since
it does not have the default ISA spec setting.  Therefore, linker won't
insert the implicit extensions for the input objects.  But we used to
insert the i-ext as the explicit extension, even if the e-ext is set.
This causes linker to report "cannot find default versions of the ISA
extension `i'" errors when linking the input objects with e-ext.
```

- Backport: GCC 12.1.0, 11.3.0
- GCC 11.1.0, 11.2.0 依然存在这个问题

Patch Link

- https://lore.kernel.org/linux-riscv/20230809165648.21071-1-xingmingzheng@iscas.ac.cn/
- https://lore.kernel.org/linux-riscv/20230824190852.45470-1-xingmingzheng@iscas.ac.cn/

回到当前

- 筹备 openEuler RISC-V **2403** 版本
- Kernel **6.6 LTS**
- 新特性合入
  - oE-RV Livepatch
  - 硬件厂商 kernel 合并

感谢聆听