National Taiwan Normal University
Department of Computer Science and Information Engineering
CSU0029, Final exam
2, Jun, 2022

This is a open-book exam. You have 110 minutes. Before the exam time ends, submit one multiple-page PDF file which contains your answers to the course website. Make your answers as concise as possible. Sentence fragments are ok. We will maximally record 100 points instead of 116 points that are shown in whole exam paper.

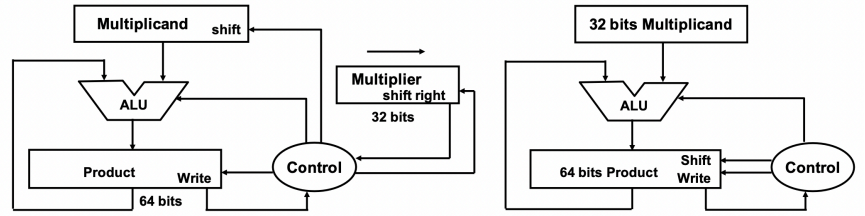
Note: We will take off points if a correct answer also includes incorrect or irrelevant information. In the other words, do not put in everything you know in hopes of saying the correct buzzword.

NTNU Honor Code

In accordance with both the letter and the spirit of the Honor Code, I will not cheat on this exam nor will I assist someone else cheating.

1. (10 points) A cache with data size 1Mbytes contains 32K blocks and is eight-way set associative. The byte address `0x11D9A4F1` is accessed and is a hit in this cache. Assume that the corresponding tag value is "T", what is "T mod 5"?

2. (10 points) A 32bit multiplication can be designed as a sequential version (A) in the below figure. The same multiplication function can be achieved by a reduced hardware version (B). In particular, since when a shift is usually faster than addition, a Booth's algorithm is to find a string of 1's in multiplier and to replace the sequential additions with an initial subtract from Multiplicand when we see a first 1 and then later add Multiplicand for the test bit after the last 1. Determine whether each of the following statements is true (T) or false (F)?



(A) Sequential version of multiplication (B) Reduced version with Booth's multiplication

(a) The Multiplicand of version (A) has to be a 64-bit register.

(b) The product register of version (B) has to perform a logical shift right.

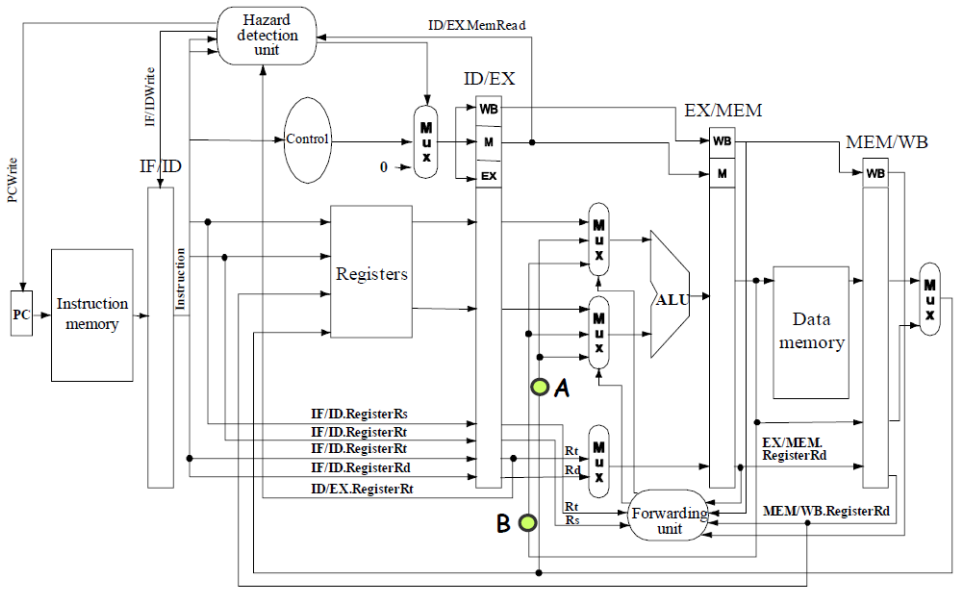
(c) The product register of version (B) has to be initialized with the Multiplier.

(d) The ALU of version (B) has to be a 64-bit adder (can also perform subtract).

(e) For a multiplier value 0x00FF0F00, a Booth multiplication will perform only 2 adds, 2 subtracts, and 32 shifts

(a)	(b)	(c)	(d)	(e)

3. (10 points) Given the pipelined MIPS CPU below where assume both forwarding and stall mechanisms have been designed, which of following statements are correct?



(a) Assume the path labeled A has been cut, the following code snippet will fail.

```
add $s2, $s0, $s1
add $s3, $s0, $s2
```

(b) Assume the path labeled A has been cut, the following code snippet will fail.

```
add $t1, $t1, $s2
add $t1, $t0, $t2
add $s2, $s1, $t1
```

(c) Assume the path labeled B has been cut, the following code snippet will fail.

```
add $t1, $t1, $s2
add $t1, $t0, $t2
add $s2, $s1, $t1
```

(d) Assume the path labeled A has been cut, the following code snippet will fail

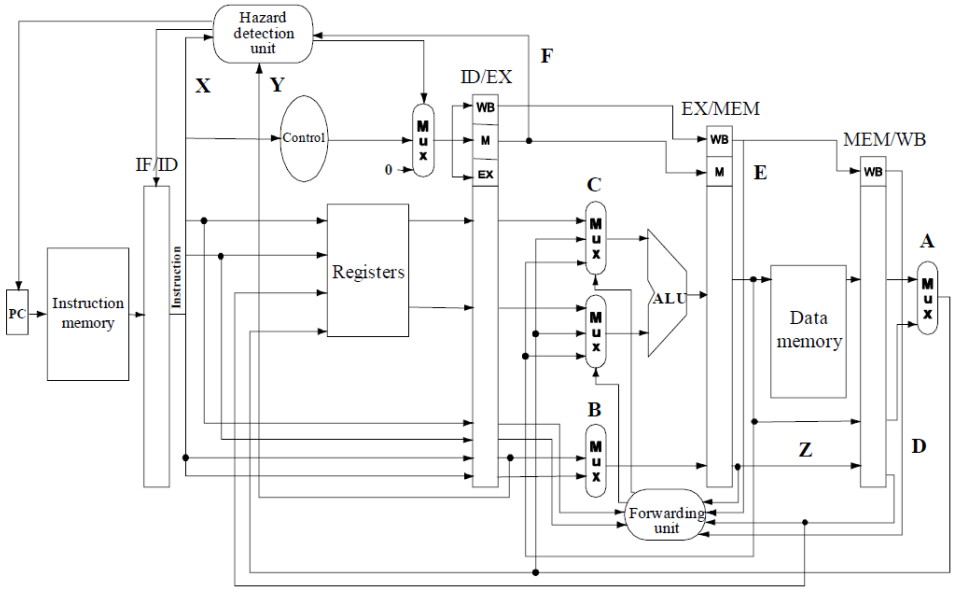
```
lw $s0, 4($t1)
add $s2, $s0, $s1
```

(e) Assume the path labeled B has been cut, the following code snippet will fail.

```
lw $s0, 4($t1)
add $s2, $s0, $s1
```

4. The following figure shows the pipelined datapath with control signals. For the instruction sequence below, please answer the following questions.

```
add $1, $2, $3
and $1, $1, $4
lw $5, 4($1)
sub $7, $5, $6
or $8, $5, $7
```



(a) (6 points) Please give the control signals of multiplexors A, B, C and control lines D, E, F for clock cycle 5. Note that the answer for each signal should be one of the follows: 0, 1, 00, 01, 10, or 11.

	A	B	C	D	E	F
Control Signal						

(b) (3 points) For clock cycle 5, what are sent through lines X, Y, and Z? Please write down the corresponding register numbers ($1, $2 ... $8).

	X	Y	Z
Register Number			

(c) (3 points) How many cycles does it take to finish the execution of this instruction sequence?

5. (10 points) The following descriptions are about RISC and CISC processors. Determine whether each of the following statements is true (T) or false (F)?

   (a) The instruction format complexity of CISC is more than that of RISC.

   (b) The clock cycle time of instructions in CISC is more than that in RISC.

   (c) The clock cycle per instruction in CISC is more than that in RISC.

   (d) The performance of CISC is more than that of RISC.

   (e) The power consumption of CISC is more than that of RISC.

   (f) RISC has become obsolete now.

   (g) MIPS computer systems belong to RISC architecture.

   (h) RISC has a larger register set comprised of most general purpose registers, as compared to CISC computer.

   (i) CISC can operate directly arithmetic instructions in memory data.

   (j) CISC has uniform instruction format.

(a)	(b)	(c)	(d)	(e)
(f)	(g)	(h)	(i)	(j)

6. The following two C and MIPS assembly programs perform the same task.

```
Clear1(int array[], int size) {
 int i;
 for (i = 0: i < size; i += 1)
    array[i] = 0;
}
```

```
clear2(int *array, int size) {
 int *p:
 for(p=&array[0];p<&array[size];
     p = p + 1)
     *p = 0;
}
```

```
        move $t0, ARY1
loop1:  sll  $t1, $t0,2
        add  $t2, $a0,$t1

        sw   $zero, 0($t2)
        addi $t0, $t0, ARY2
        slt  $t3, $t0, ARY3

        bne  $t3, $zero, loop1
```

```
        move $t0,PTR1
        sll  $t1,$a1,2
        add  $t2,$a0,$t1

loop2:  sw   $zero, 0($t0)
        addi $t0, $t0, PTR2
        slt  $t3, $t0, PTR3

        bne  $t3, $zero, loop2
```

(a) (3 points) The ARY1 and PTR1 should be:

(a) ARY1 = $zero; PTR1 = $a0
(b) ARY1 = $a0; PTR1 = $zero
(c) ARY1 = $a0; PTR1 = $a0
(d) ARY1 = $zero; PTR1 = $zero

(b) (3 points) The ARY2 and PTR2 should be:

(a) ARY2 = 1; PTR2 = 1
(b) ARY2 = 4; PTR2 = 4
(c) ARY2 = 1; PTR2 = 4
(d) ARY2 = 4; PTR2 = 4

(c) (3 points) The ARY3 and PTR3 should be:

(a) ARY3 = $t2; PTR3 = $a1
(b) ARY3 = $a1; PTR3 = $a1
(c) ARY3 = $t2; PTR3 = $t2
(d) ARY3 = $a1; PTR3 = $t2

7. (10 points) For a pipelined implementation, assume that $\frac{1}{4}$ of the load Instructions are immediately followed by an instruction that uses the result, half of the branches are miss-predicted with 1 clock cycle delay, and jumps always cause 1 clock cycle of delay. If the instruction mix is 24% loads, 20% stores, 30% ALU instructions, 20% branches, and 6% jumps. The average CPI is "K". What is "Round($K \times 234$) mod 5"?

8. (10 points) Use 32-bit IEEE 754 single precision to encode "-1234.6875_{10}". If K is the number of "1" in this 32-bit value, then what is "K mod 5"?

9. Calculate the performance of a processor taking into account stalls due to data cache and instruction cache misses. The data cache has a 92% hit rate and a 2-cycle hit latency. Assume that latency to memory and the cache miss penalty together is 100 cycles. The instruction cache has a hit rate of 90% with a miss penalty of 50 cycles. Assume the load never stalls a dependent instruction and assume the processor must wait for stores to finish when they miss the cache. Finally, assume that instruction cache misses and data cache misses never occur at the same time.
   (a) (5 points) Calculate the average memory access latency for the data cache.
   (b) (5 points) Assume the base CPI using a perfect memory system is 1. Calculate the additional CPI of the pipeline due to the Instruction cache stalls.
   (c) (5 points) Same as (b), but calculate the additional CPI due to the data cache stalls.
   (d) (5 points) Assume 30% of instructions are loads and stores. Calculate the overall CPI for the machine.

10. Assume 4KB pages, a 4-entry two-way set associative TLB and true LRU replacement. Given the virtual address references, and the initial TLB and page table states provided below. If pages must be brought in from disk, increase the next largest page number. i.e., When the page table is accessed, if that particular page is on disk, the page number would be 13 since the largest page number in the page table at the beginning is 12. Which of following statements is (are) true?

Virtual address references: 4669, 2227, 13916, 34587, 48870, 12608

TLB

Set	valid	tag	Physical page number
0	0	11	12
0	1	3	6
1	1	7	4
1	0	4	9

Page Table

valid	Physical page number or in disk
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

(a) (3 points) For the given address references, list the corresponding virtual page numbers.

(a) 0, 0, 0, 2, 2, 0
(b) 1, 0, 3, 0, 3, 3
(c) 1, 0, 3, 8, 11, 3
(d) 0, 0, 1, 4, 5, 1
(e) 1, 0, 1, 0, 1, 1

(b) (3 points) For the given address references, the corresponding indexes to the TLB are

(a) 0, 0, 0, 2, 2, 0
(b) 1, 0, 3, 0, 3, 3
(c) 1, 0, 3, 8, 11, 3
(d) 0, 0, 1, 4, 5, 1
(e) 1, 0, 1, 0, 1, 1

(c) (3 points) For the given address references, the corresponding tags to the TLB are

(a) 0, 0, 0, 2, 2, 0
(b) 1, 0, 3, 0, 3, 3
(c) 1, 0, 3, 8, 11, 3

(d) 0, 0, 1, 4, 5, 1

(e) 1, 0, 1, 0, 1, 1

(d) (3 points) For the given reference, accesses to TLB are

(a) miss, miss, miss, miss, miss, miss

(b) miss, hit, miss, miss, miss, miss

(c) miss, miss, hit, hit, hit, hit

(d) miss, miss, miss, miss, miss, hit

(e) miss, hit, hit, miss, hit, hit

(e) (3 points) For the given reference, how many page faults in total?

(a) None

(b) 1

(c) 2

(d) 3

(e) 4