CS 354 - Machine Organization & Programming Tuesday, October 29th, 2019

Midterm Exam 2 (~18%): Thursday, November 7th, 7:15 - 9:15 pm

Project p4A (~2%): DUE at 10 pm on Tuesday, November 5th

Project p4B (~4%): Assigned later this week

Homework hw4 (1.5%): DUE at 10 pm on Thursday, October 31st

Last Time

Set Associative Cache
Replacement Policies
Fully Associative Cache
Writing to Caches
Cache Performance Metrics
Cache Parameters and Performance

Today

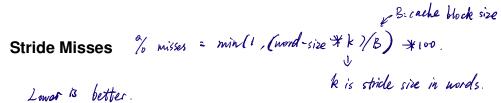
Impact of Stride Memory Mountain C, Assembly, & Machine Code Low-level View of Data Registers Instructions - MOV, PUSH, POP

Next Time

More Instructions and Operands

Read: B&O 3.5, 3.6

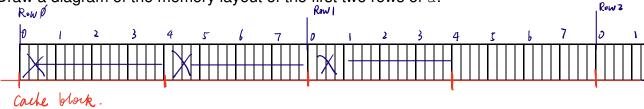
Impact of Stride



Example:

```
int initArray(int a[][8], int rows) {
  for (int i = 0; i < rows; i++)
    for(int j = 0; j < 8; j++)
        a[i][j] = i * j;
}</pre>
```

→ Draw a diagram of the memory layout of the first two rows of a:



Assume: a is aligned with cache blocks and is too big to fit entirely into the cache words are 4 bytes, block size is 16 bytes direct-mapped cache is initially empty, write allocate used

→ Indicate the order elements are accessed in the table below and mark H for hit or M for miss:

a[i][j]	j = 0	1	2	3	4	5	6	7
i = 0	IM	24	3H	4H.	M_T	61-1	74	84
1	9 M	10 H	ПН	124.			•	

→ Now exchange the i and j loops mark the table again:

a[i][j]	j = 0	1	2	3	4	5	6	7
i = 0	IM							
1	2 <i>M</i>							
	3M							

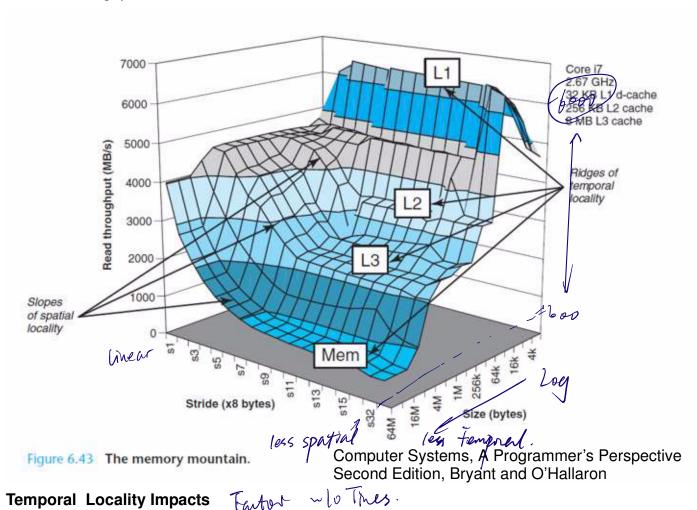
Memory Mountain

Independent Variables

stride - 1 to 16 double words step size used to scan through array size - 2K to 64 MB arraysize

Dependent Variable

read throughput - 0 to 7000 MB/s



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Spatial Locality Impacts

* Memory access speed is not characterized by a single value

14's a landsape that combe explorted through the use of

spetial and temporal leventy

C, Assembly, & Machine Code

C Function	Assembly (AT&T)	Machine (hex)
<pre>int accum = 0; int sum(int x, int y) { int t = x + y; accum += t; return t; }</pre>	<pre>sum: pushl %ebp movl %esp, %ebp movl 12(%ebp), %eax addl 8(%ebp), %eax addl %eax, accum popl %ebp</pre>	55 89 e5 8b 45 0C 03 45 08 01 05 ?? ?? ?? ?? 5D
 → What aspects of the mac 	thet enable is be more that enable is be more that each with symitax and and run on different platform hine does C hide from us? e details - marking in	ns
· is very machine de	i representation of machi	ndition codes
→ Why Learn Assembly?	rege construets, - logical -variance - composideretand stack, c	rames, and data types. The data such as arrays and stacks.
Machine Code (MC) * is elementary of	inefficiencies and vule piler optimizations. U instrus and death in modings that a particular an IA-32 instructions? Under	Rabilities 1
1-15	/	

Low-Level View of Data

C's View

- · variables are declared to be sperific types
- · types can be composed compositives built from arrays and structs.

Machine's View

memony is like an array of bytes indexed by addresses where each elevent

- * Memory contains bits that do not disting with instructions from different data types or pointer addresses.
 - → How does a machine know what it's getting from memory?
 - 1. by how were is accessed: instruction Fetchirg. V.S. operand bading.
 - 2. by the instruction itself: operation (what type) and what size)

Assembly Data Formats

	С	IA-32	Assembly Suffix	Size in bytes	
	char	byte	В	1	
	short	word	W	2	
	int	double word	l	4	l: Long
	long int	double word	l	4	0
APDR.	char*	double word	l	4	
	float	single precision	S	4	
	double	double prec	ℓ	8	
	long double	extended prec	t	10	

* In IA-32 a word is actually 2 bytes.

Registers

- · are the factest memory directly accessed by ALV
- can store 1,2, and 4 bytes of data.
 or 4 bytes for addresses

prenamed locations that store up to 32 bits.

8 bit, higher

'		8 bit, mg	8 Bit
	0.4	n=8-15 hits	
bit	31 	16 15 8	/ / 0 ——————————————————————————————————
%eax	Accommonator	%ax < > %ah	%al ← → Bits
%ecx	count	%cx %ch	%cl
%edx	data	%dx %dh	%dl >
%ebx	base	%bx %bh	%b1
%esi	source index.	%si	
%edi	destination index	%di-	
%esp	Stack pointer	%sp	
%ebp	buse pointer	%bp	
L _			
32 bit		16 bits register	4 5 ·
bit 1	9-42	12x 0-1	

Program Counter PC seip extended instruction pointer Stores address of next instruction.

Condition Code Registers

I bit registers that store status.

of most veneral ALV operations.

Instructions - MOV, PUSH, POP

What? These are instructions to copy data from source s to destination of.

Why? enables into to be moved around in mem and registers.

How?

instruction class MOV S, D MOV b MOV b MOV W MOV l	operation $P \leftarrow S$	description copies & To D
MOVS S, D MOVS b w MOVS b l MOVS W l	D < signestanded (s)	copies s sign extended to d.
MOVZS, D MOVZ b v b l w l	D < reroextended (s).	lopies s zero extended to d.
pushl S	R[%esp] < R[%esp]-4 MI R[%esp]] <s< td=""><td>push 8 onto stack.</td></s<>	push 8 onto stack.
popl D	D < MIR[% esp]] R[%esp] <-R[%esp]+4	pop from stack to D

Practice with Data Formats

→ What data format suffix should replace the _ given the registers used?