

Computer Architecture

과제 #2: Architecture Simulation

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2차 과제 목적

■ Architecture Simulation을 사용한 Application 성능 평가

■ Architecture Level에서 Application 특성 분석

■ Application 특성을 고려한 Architecture 성능 최적화

2차 과제 내용

■ Architecture Simulation을 통한 Application 특성 및 성능 분석

- Architecture Simulator에서 Benchmark Application 수행
- Architecture Level Performance Measurement를 활용한
 Application 특성 분석

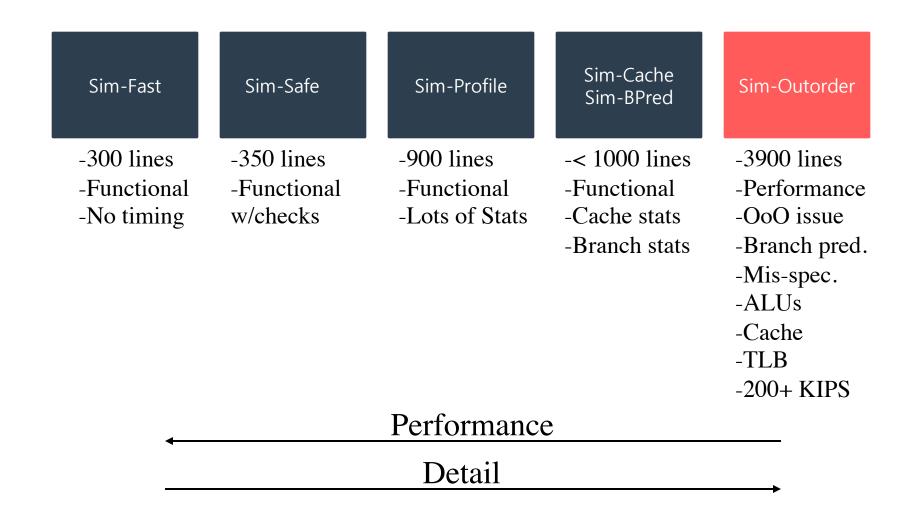
■ Application 특성을 고려한 Architecture 성능 최적화

- Architecture Simulator의 중요 Configuration 분석
- Application 특성에 맞게 Architecture Simulator의 Configuration 조정 후 성 능 향상 측정

Simulator

- Architecture Simulator는 무엇인가?
 - Computing Device의 Behavior를 Reproduce (재생산?) 하는 Tool
- Simulator를 왜 사용할까?
 - 더욱 빠르고 유연한 Software Development Cycle
 - 쉽게 Design Space Exploration을 가능하게 함
 - HW를 직접 구하지 않아도, 작성한 SW가 해당 HW에서 잘 돌아갈 수 있을지 알 수 있음
 - System 구성에 용이함
- 이번 과제에서는 SimpleScalar를 사용함
 - Academia 및 Industry에서 널리 사용되어 왔음

SimpleScalar



Download VirtualBox

➤ https://virtualbox.org/wiki/Downloads



VirtualBox

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Documentation

End-user docs

Technical docs

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Download VirtualBox

Here, you will find links to VirtualBox binaries and its source code.

VirtualBox binaries

By downloading, you agree to the terms and conditions of the respective license.

If you're looking for the VirtualBox 5.1.30 packages, see VirtualBox 5.1 builds. Consider upgrading.

- VirtualDox 5.2.0 platform packages. The binaries are released under the terms of the GPL version 2.
 - → Windows hosts
- Click!
- Linux distributions
- ⇒Solaris hosts

Update Nov 3 2017: The Guest Additions image with the 5.2.0 release had problems with a number of Linu

- VirtualBox 5.2.0 Oracle VM VirtualBox Extension Pack → All supported platforms
 Support for USB 2.0 and USB 3.0 devices, VirtualBox RDP, disk encryption, NVMe and PXE boot for Intel card
 The Extension Pack binaries are released under the VirtualBox Personal Use and Evaluation License (PUEL).
 Please install the extension pack with the same version as your installed version of VirtualBox:
- VirtualBox 5.2.0 Software Developer Kit (SDK)
 ⇒All platforms

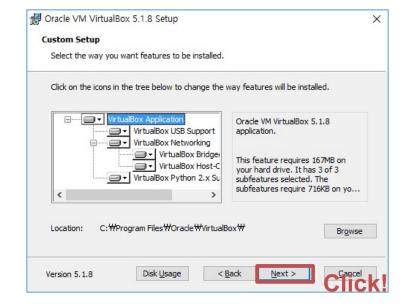
See the changelog for what has changed.

You might want to compare the SHA256 checksums or the MD5 checksums to verify the integrity of downloaded pa

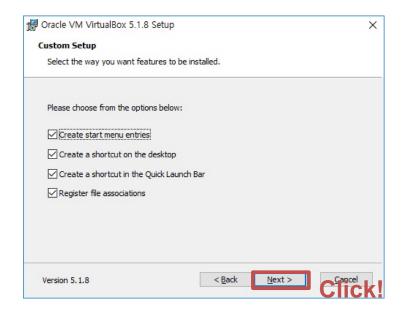
Note: After upgrading VirtualBox it is recommended to upgrade the guest additions as well.

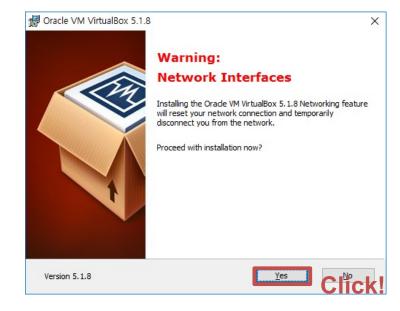
♦ Install VirtualBox



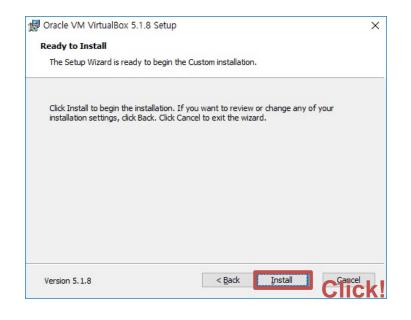


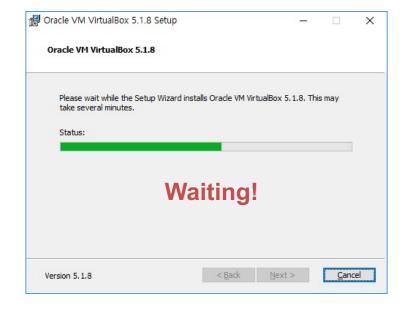
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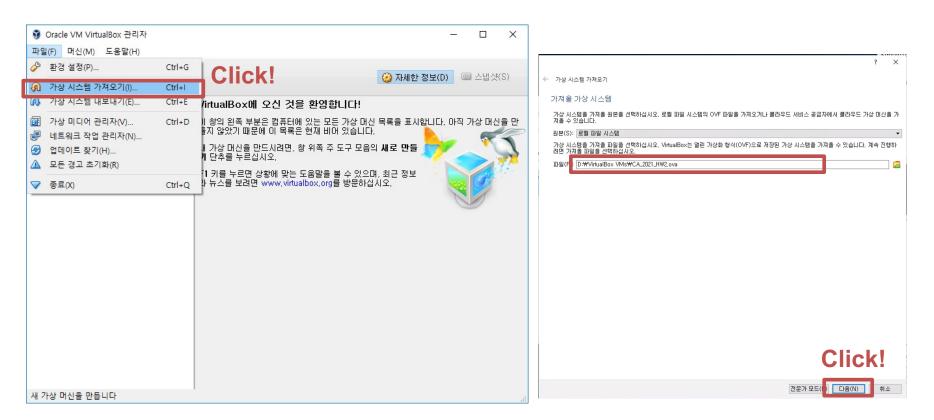


♦ Install VirtualBox

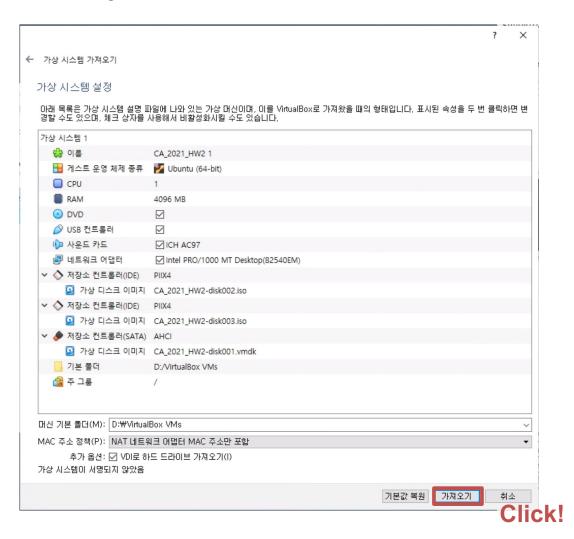




- **♦** Import Virtual System
 - ➤ 스마트 캠퍼스에서 ova 파일 다운로드



♦ Import Virtual System



♦ Import Virtual System



♦ Execute SimpleScalar



- Execute a Terminal
- **Enter the Directory of** SimpleScalar

'cd simplesim-3.0/'

- **Execute Benchmarks using** SimpleScalar
 - GCC

./sim-outorder benchmarks/cc1.alpha -O benchmarks/1stmt.i

ANAGRAM

./sim-outorder benchmarks/anagram.alpha benchmarks/words < benchmarks/anagram.in > benchmarks/OUT

COMPRESS95

./sim-outorder benchmarks/compress95.alpha < benchmarks/compress95.in > benchmarks/OUT

GO

./sim-outorder benchmarks/go.alpha 50 9 benchmarks/2stone9.in > benchmarks/OUT

Execute SimpleScalar

```
sim: ** starting performance simulation **
warning: partially supported sigprocmask() call...
sim: ** simulation statistics **
sim num insn
                                 5019 # total number of instructions committed
sim_num_refs
                                 1907 # total number of loads and stores committed
sim_num_loads
                                 927 # total number of loads committed
sim_num_stores
sim_num_branches
                            980.0000 # total number of stores committed
                                  909 # total number of branches committed
sim_elapsed_time
                                   1 # total simulation time in seconds
                           5019.0000 # simulation speed (in insts/sec)
sim inst rate
                                 6034 # total number of instructions executed
sim total insn
                                 2161 # total number of loads and stores executed
sim_total_refs
sim_total_loads
                                 1091 # total number of loads executed
sim total stores
                           1070.0000 # total number of stores executed
sim total branches
                                 1072 # total number of branches executed
sim cycle
                               13303 # total simulation time in cycles
sim_IPC
                              0.3773 # instructions per cycle
sim_CPI
                              2.6505 # cycles per instruction
                              0.4536 # total instructions (mis-spec + committed) per cycle
sim_exec_BW
sim_IPB
                              5.5215 # instruction per branch
IFQ_count
IFQ_fcount
                               11056 # cumulative IFQ occupancy
                                2360 # cumulative IFQ full count
ifq_occupancy
                              0.8311 # avg IFQ occupancy (insn's)
                              0.4536 # avg IFQ dispatch rate (insn/cycle)
ifq rate
                              1.8323 # avg IFO occupant latency (cycle's)
ifq latency
ifq_full
                              0.1774 # fraction of time (cycle's) IFQ was full
RUU_count
                               44856 # cumulative RUU occupancy
RUU fcount
                                1039 # cumulative RUU full count
                              3.3719 # avg RUU occupancy (insn's)
ruu occupancy
                              0.4536 # avg RUU dispatch rate (insn/cycle)
ruu_rate
                              7.4339 # avg RUU occupant latency (cycle's)
ruu_latency
                               0.0781 # fraction of time (cycle's) RUU was full
ruu_full
LSQ_count
                                16523 # cumulative LSQ occupancy
                                  353 # cumulative LSQ full count
LSQ_fcount
                              1.2421 # avg LSQ occupancy (insn's)
0.4536 # avg LSQ dispatch rate (insn/cycle)
2.7383 # avg LSQ occupant latency (cycle's)
0.0265 # fraction of time (cycle's) LSQ was full
lsq occupancy
lsq rate
lsq_latency
lsq_full
sim slip
                               62260 # total number of slip cycles
avg_sim_slip
                              12.4049 # the average slip between issue and retirement
                                 1115 # total number of bpred lookups
bpred bimod.lookups
bpred_bimod.updates
                                  909 # total number of updates
bpred_bimod.addr_hits
                                  503 # total number of address-predicted hits
bpred_bimod.dir_hits
                                  730 # total number of direction-predicted hits (includes addr-hits)
bpred_bimod.misses
                                  179 # total number of misses
bpred bimod.jr hits
                                  108 # total number of address-predicted hits for JR's
bpred_bimod.jr_seen
                                  182 # total number of JR's seen
bpred_bimod.jr_non_ras_hits.PP
                                            16 # total number of address-predicted hits for non-RAS JR's
                                            38 # total number of non-RAS JR's seen
bpred_bimod.jr_non_ras_seen.PP
```

Simulation Statistics

- Total number of instructions
- Total number of loads and stores
- Total number of branches
- Total simulation time in cycles
- Instruction per cycle
- Cycles per instruction

◆ Configurations of Simulation

```
ca2021@ca2021-VirtualBox:~/simplesim-3.0$ ./sim-outorder -h
sim-outorder: SimpleScalar/Alpha Tool Set version 3.0 of August, 2003.
Copyright (c) 1994-2003 by Todd M. Austin, Ph.D. and SimpleScalar, LLC.
All Rights Reserved. This version of SimpleScalar is licensed for academic
non-commercial use. No portion of this work may be used by any commercial
entity, or for any commercial purpose, without the prior written permission
of SimpleScalar, LLC (info@simplescalar.com).
Usage: ./sim-outorder {-options} executable {arguments}
sim-outorder: This simulator implements a very detailed out-of-order issue
superscalar processor with a two-level memory system and speculative
execution support. This simulator is a performance simulator, tracking the
latency of all pipeline operations.
 -option
                 <args>
                                      <default> # description
-config
                 <string>
                                         <null> # load configuration from a file
-dumpconfig
                 <string>
                                          <null> # dump configuration to a file
                 <true|false>
                                           true # print help message
                 <true|false>
                                           false # verbose operation
                 <true|false>
                                           false # enable debug message
                 <true|false>
                                           false # start in Dlite debugger
-seed
                 <int>
                                              1 # random number generator seed (0 for timer seed
                 <true|false>
                                          false # initialize and terminate immediately
-chkpt
                 <string>
                                          <null> # restore EIO trace execution from <fname>
-redir:sim
                 <string>
                                          <null> # redirect simulator output to file (non-interac
tive only)
-redir:prog
                 <string>
                                         <null> # redirect simulated program output to file
-nice
                 <int>
                                              0 # simulator scheduling priority
-max:inst
                                              0 # maximum number of inst's to execute
-fastfwd
                 <int>
                                              0 # number of insts skipped before timing starts
-ptrace
                 <string list...> #
                                         <null> # generate pipetrace, i.e., <fname|stdout|stderr
> <range>
-fetch:ifqsize
                <int>
                                              4 # instruction fetch queue size (in insts)
-fetch:mplat
                                              3 # extra branch mis-prediction latency
-fetch:speed
                                              1 # speed of front-end of machine relative to exec
ution core
-bpred
                                           bimod # branch predictor type {nottaken|taken|perfect|
                 <string>
bimod|2lev|comb}
-bpred:bimod
                                  # 2048 # bimodal predictor config ()
-bpred:2lev
                 <int list...>
                                  # 1 1024 8 0 # 2-level predictor config (<l1size> <l2size> <his
t size> <xor>)
-bpred:comb
                                  # 1024 # combining predictor config (<meta_table_size>)
                 <int>
-bpred:ras
                                               8 # return address stack size (0 for no return sta
                 <int>
ck)
-bpred:btb
                 <int list...>
                                  # 512 4 # BTB config (<num sets> <associativity>)
                                            <null> # speculative predictors update in {ID|WB} (de
-bpred:spec_update <string>
fault non-spec)
-decode:width
                 <int>
                                  #
                                              4 # instruction decode B/W (insts/cycle)
-issue:width
                 <int>
                                  #
                                              4 # instruction issue B/W (insts/cycle)
-issue:inorder
                <true|false>
                                           false # run pipeline with in-order issue
-issue:wrongpath <true|false>
                                           true # issue instructions down wrong execution paths
```

- Type ./sim-outorder -h
- Important Configurations
 - fetch:ifqsize
 - bpred
 - decode:width
 - issue:width
 - cache:dl1
 - cache:dl2
 - cache:il1
 - cache:il2
 - res:ialu
 - res:imult
 - res:memport
 - res:fpalu
 - res:fpmult

주의: cache:dl1lat, cache:dl2lat, 등 Latency 값을 직접 변경해서는 안됨

과제 채점 Focus

- 과제 Report의 비중: 100%
 - Report에 반드시 포함되어야 하는 내용
 - 학과, 학번, 이름, 제출 일자
 - 각 Benchmark Application에 대해
 - 기본 Configuration에서 측정한 성능 기술 (2점)
 - 각 Application이 어떤 특성을 갖고 있는지 분석한 내용 서술 (2점)
 - SimpleScalar Simulator Configuration 분석한 내용 서술 (2점)
 - 각 Benchmark Application에 대해
 - Configuration 변경하고, 측정한 성능 기술 (2점)
 - 왜 Configuration을 그렇게 변경했는지 기술 (4점)
 - Configuration 변경 전과 변경 후 성능 Graph로 비교 (3점)
- 성능 향상 수치 (4개 Application의 평균)의 상위 10명은 추가 점 수 부여 (1점)

과제 채점 Focus

- 제출 기한
 - 6월 11일 (금) 11:59 PM
- 제출 방법
 - 스마트 캠퍼스를 통해 파일들 제출
 - 제출할 파일 목록
 - 보고서
 - 파일 제출 방법
 - "ca2_학번.zip"으로 압축하여 제출 (다른 형식도 무관)