

ECD Lab-04 JFET Common Source Amplifier Simulation

In this labwork we were tasked with designing and simulating a JFET circuit in a SPICE software using the given circuit in the assignment. For this lab we were not asked to assemble this circuit in the lab. Our aim is to calculate the required values and simulate our circuit.

Question 1

In the first part we need to find appropriate values for resistors.

Note: Gain is given as 2 in the assignment but n type JFET normally have negative gain so I am going to take this as -2.

First of all we should find the small signal equivalent circuit:

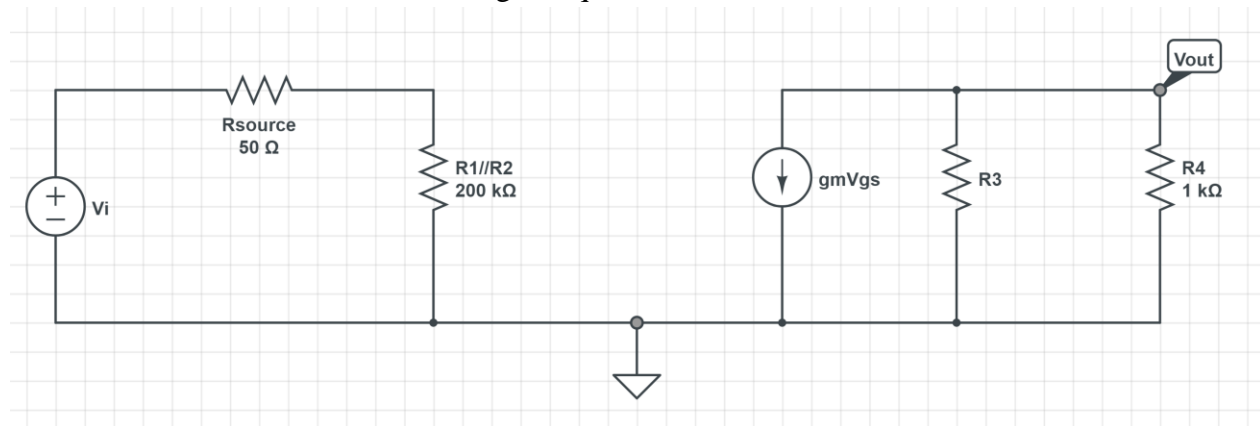


Figure 1(Equivalent circuit - Capacitors are shorted)

We know that the output resistance is 1 kΩ, Kill the sources and Connect Vx to the output:

Kill the independent sources and connect V_x to find the output resistance

$$I_x = g_m V_{gs} + \frac{V_x}{R_0} \quad V_{gs} = 0$$

$$I_x = \frac{V_x}{R_0}$$

$$R_0 = \frac{V_x}{I_x} = R_x = 1k$$

$R_0 = 1k$

output R_x given as 1k

Gain and I_{DSS} is given, by using these we can find g_m , i_d and V_{gs} :

$$A_v = \frac{V_o}{V_i} = -2 \rightarrow \text{given} \quad V_i = V_{gs}$$

$$V_o = -g_m V_{gs} (R_L \parallel R_D) \rightarrow 0.5V$$

$$\frac{V_o}{V_i} = -2 = -g_m (0.5) \rightarrow \boxed{g_m = 4}$$

Book Equation (4-62) $\rightarrow g_m = \frac{2I_{DSS}}{|V_p|} \left(1 - \frac{V_{gs}}{V_p}\right) = 4$ $I_{DSS} = 16mA$ $-g_m = 4$

$$\boxed{V_{gs} = -1.87V}$$

Book Equation (4-54) $i_D = I_{DSS} \left(1 - \frac{V_{gs}}{V_p}\right)^2 \rightarrow \boxed{i_D \approx 7mA}$

Finally we can find resistor values. We know $R_{in} = 200k\Omega$. Lets say R_1 is $1000k\Omega$.

$$V_g = V_{DD} \frac{R_2}{R_1 + R_2} = \frac{1}{R_1} R_{in} V_{DD}$$

$$V_g = \frac{20(200)}{R_1} \quad V_s = 7R_s$$

$$V_s = i_D R_s = 7R_s$$

Let's say $R_1 = 1000k$
 $R_{in} = 200k \rightarrow R_2 \text{ becomes } 250k$

$$V_g = \frac{20(200)}{1000} \quad V_s = 7R_s \rightarrow V_{gs} = -1.87V$$

R_s is around $0.4k - 1k$

I will pick $560\Omega \rightarrow \boxed{R_s = 560\Omega}$

$$\boxed{R_1 = 1000k}$$

$$\boxed{R_2 = 250k}$$

Finally we found that $R_1 = 1000k\Omega$ and $R_2 = 250k\Omega$ and $R_s = 560\Omega$.

Question 2

In this question I have implemented the given circuit design in LTspice software by using the values that I have found in the previous section:

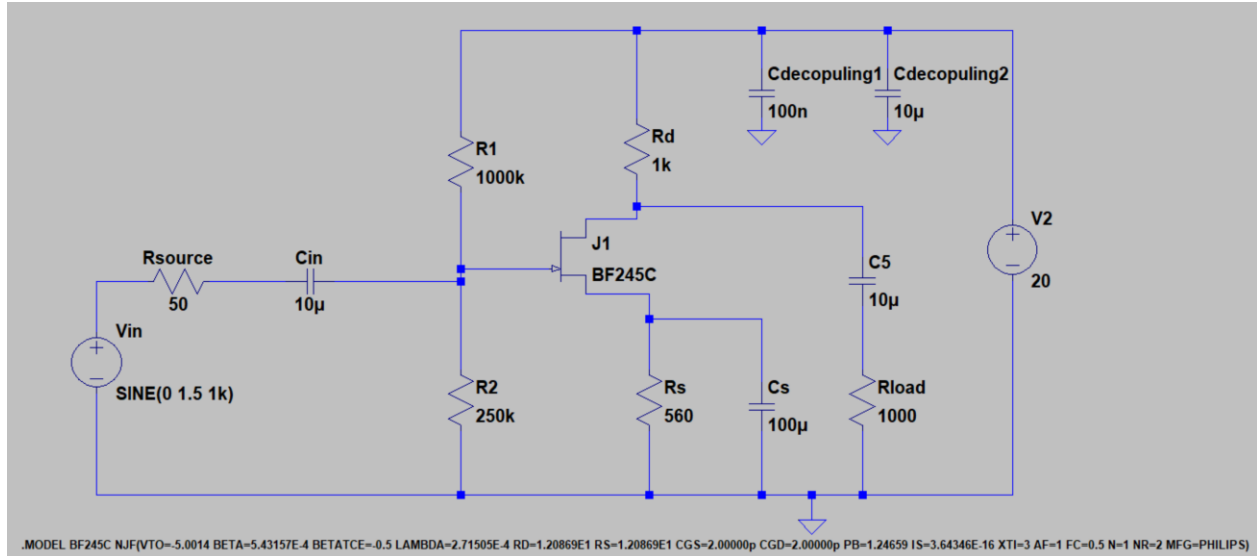


Figure 2 (JFET figure was not available in the software, I added it with a directive)

BF245C was not present in the LTspice because of that I have found the values from internet and put them in using directive command.

Note: Input is 0.25V peak-to-peak for these:

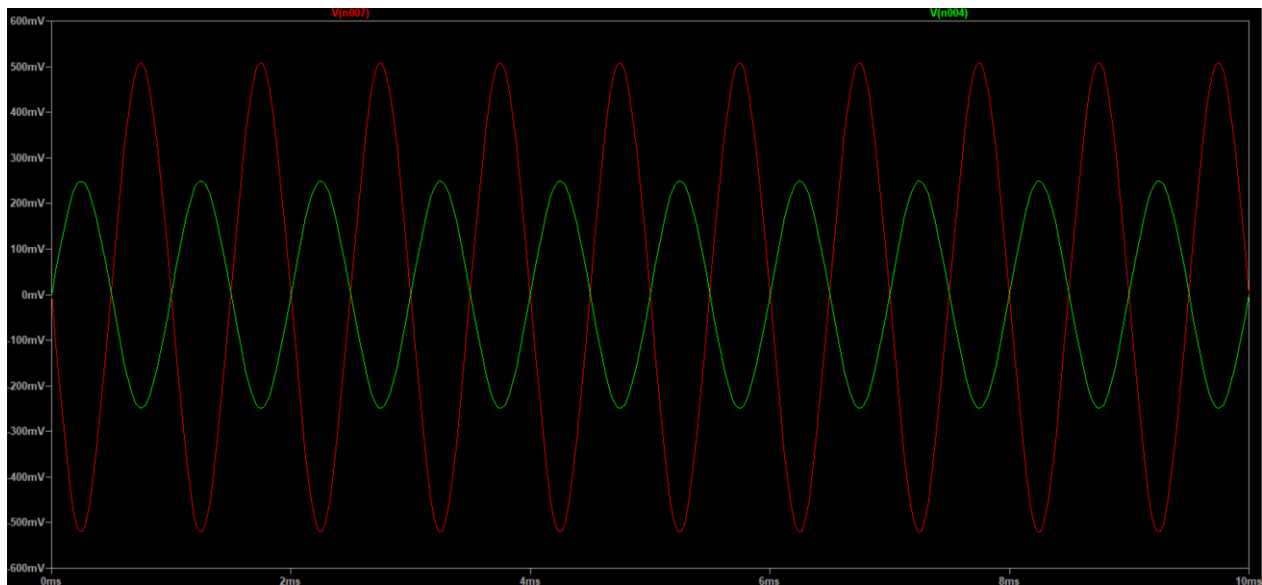


Figure 3 (Input ($V(n004)$ - green) and Output ($V(n007)$ - Red))

We can clearly see from the plots that the output signal is -2 times of the input signal as expected.

For this part I have set the input to 10V (high value) to find output voltage swing:

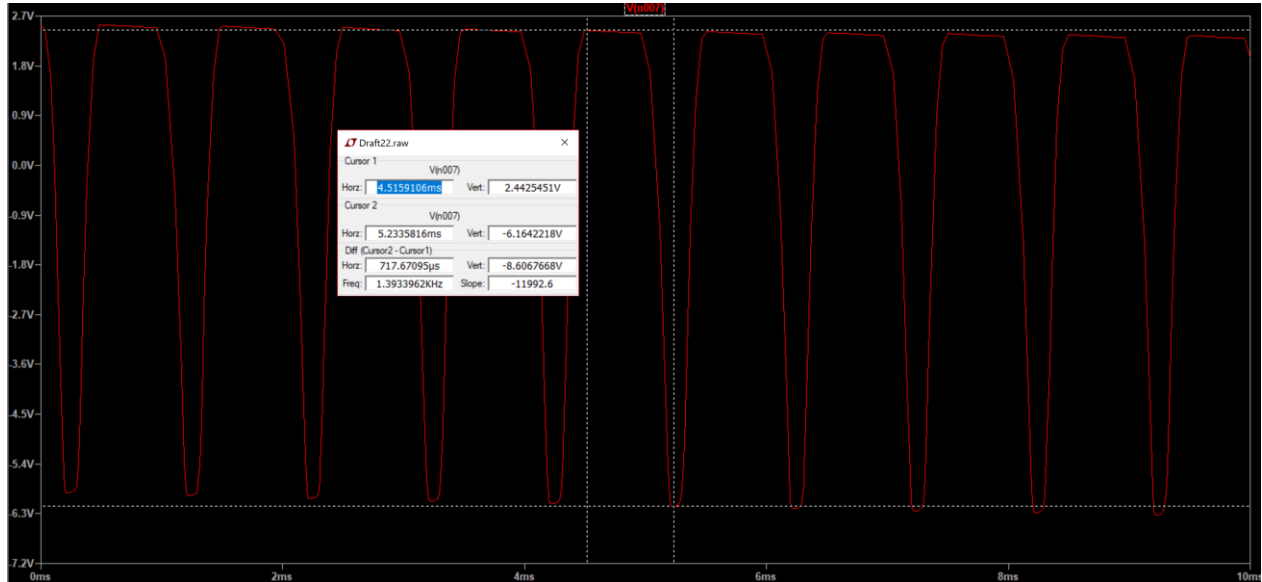


Figure 4 (output voltage swing)

Output is around 2.44V and -6.16V so the Swing is 8.6V.

For the last part I have used the FFT utility of the Software:

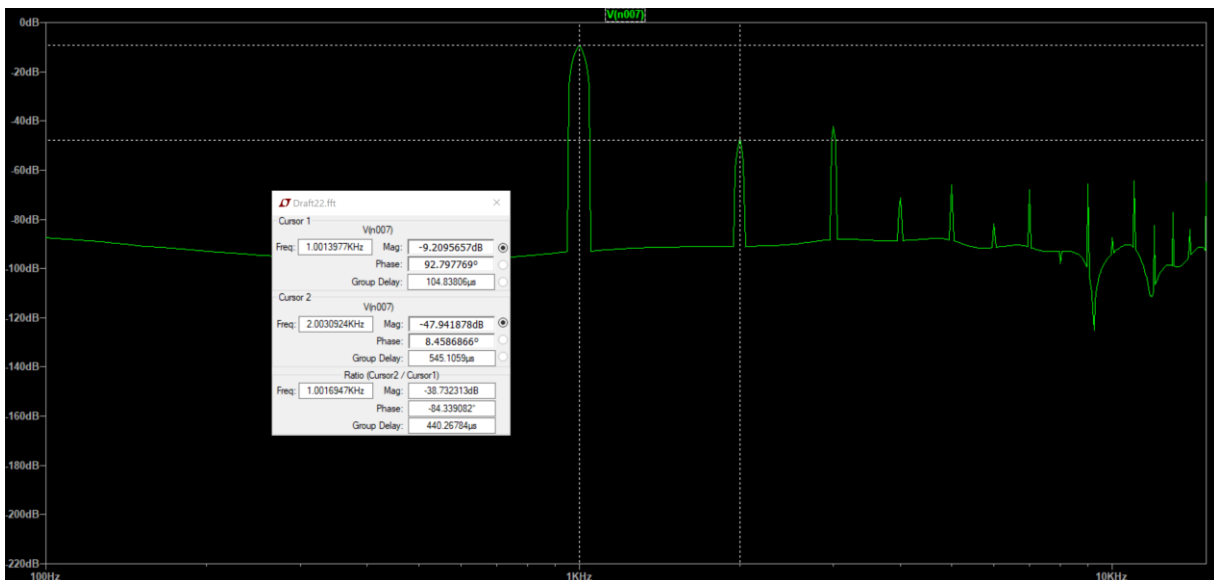


Figure 5 (Input is 0.25V)

First harmonic is 1kHz and ac peak level for which the highest harmonic has less than 1% amplitude compared to the fundamental occurs at 2kHz. 40 DB less, 1% distortion.

3 times the input voltage:



Figure 6(0.75V input)

5 times the input voltage:

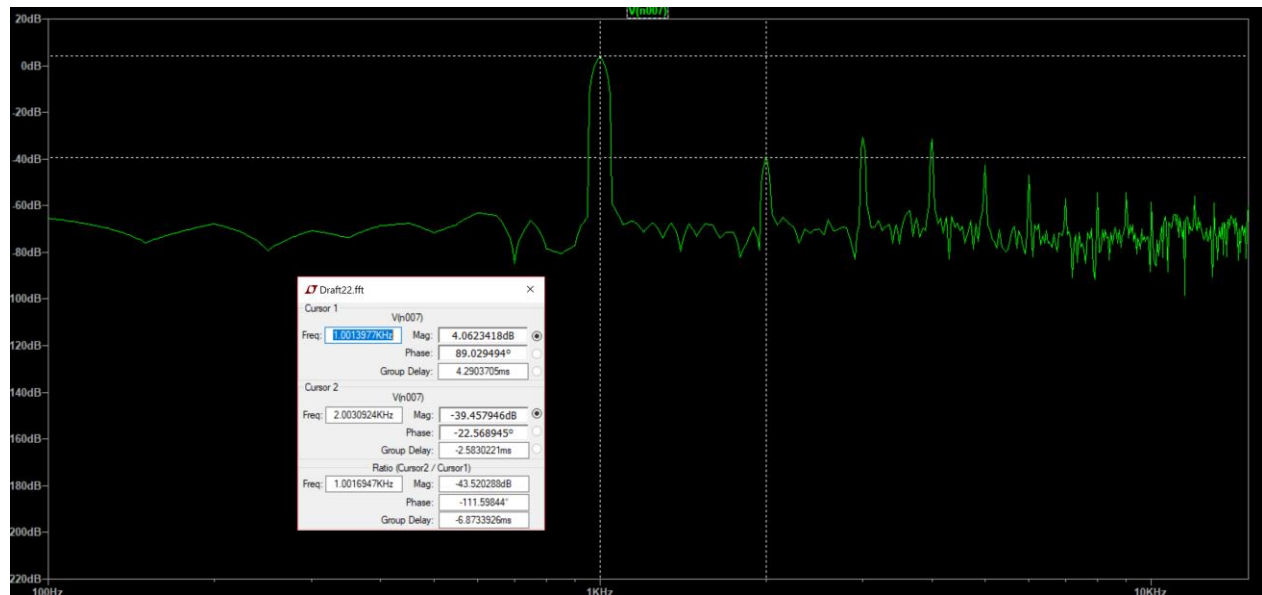


Figure 7 (Input is 1.25V)

Conclusion

Small signal analysis does not include the unwanted harmonics. In small signal input case this analysis is valid since the effect of the unwanted harmonics is minimal. However as we increased the input voltage small signal analysis start to become incorrect since the unwanted harmonics have more effects in high voltages. Which basically means that the small signal analysis becomes invalid when the signal is not actually small.