Yusuf Ziya Dilek
ID: 21501462
EE 313 Lab-02

Part A

First of all, I have implemented the given design in LTSpice software in this manner:

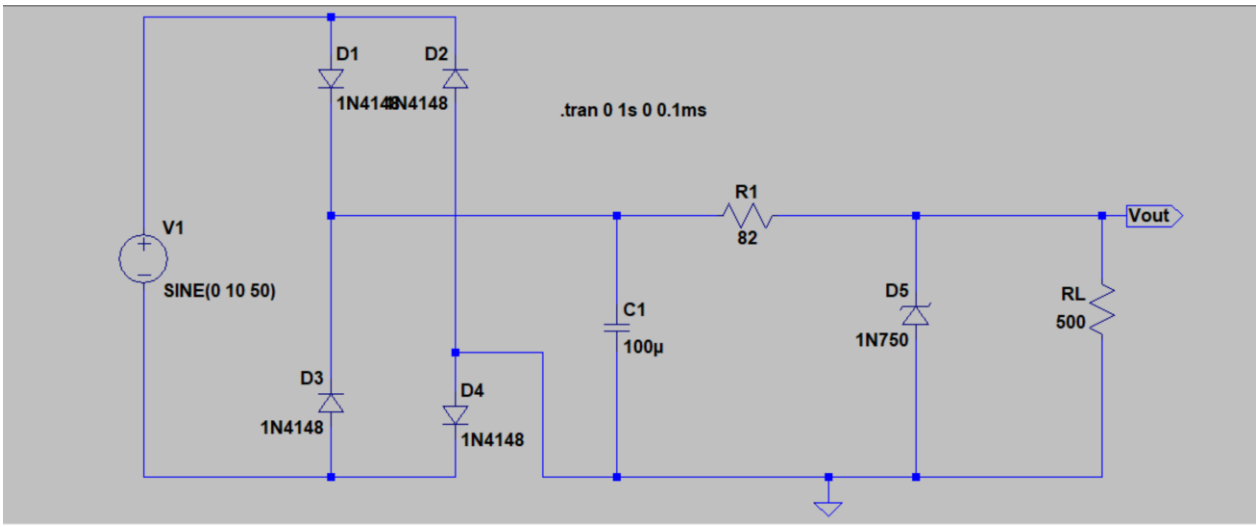

Figure 1 (LTSpice implementation)

However in the assignment the circuit was incomplete. We were asked to find a suitable value for R2 such that the ripple in the output is acceptable. Calculations turned out to be like this:

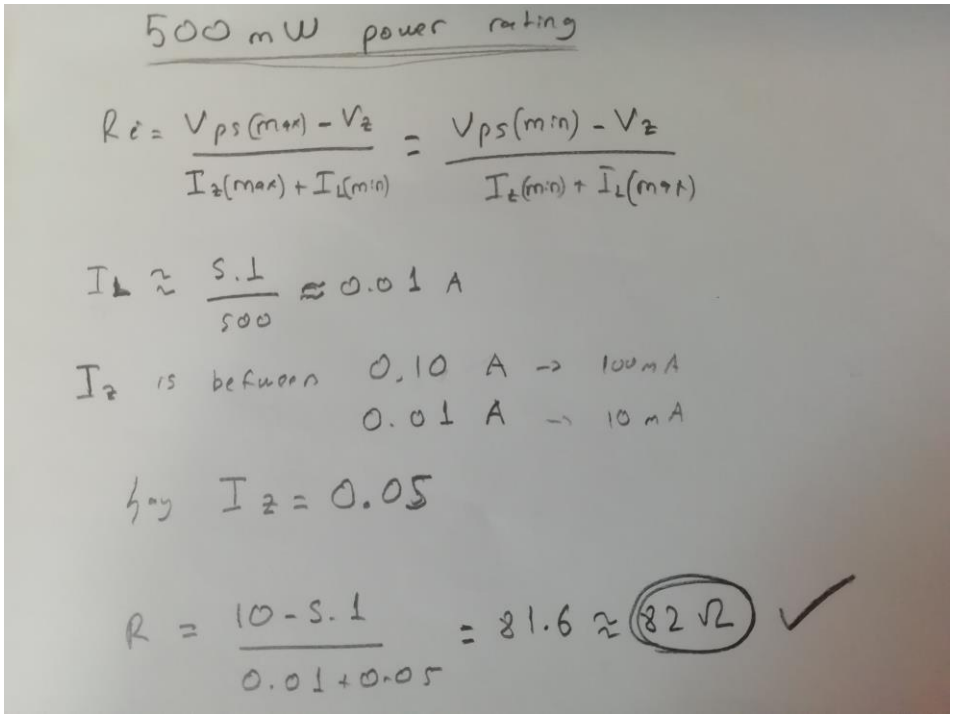

Figure 2 (Calculations for R2)

Then I have proceed to software simulation part I order to test my design before the lab implementation part. The output waveform was like this:

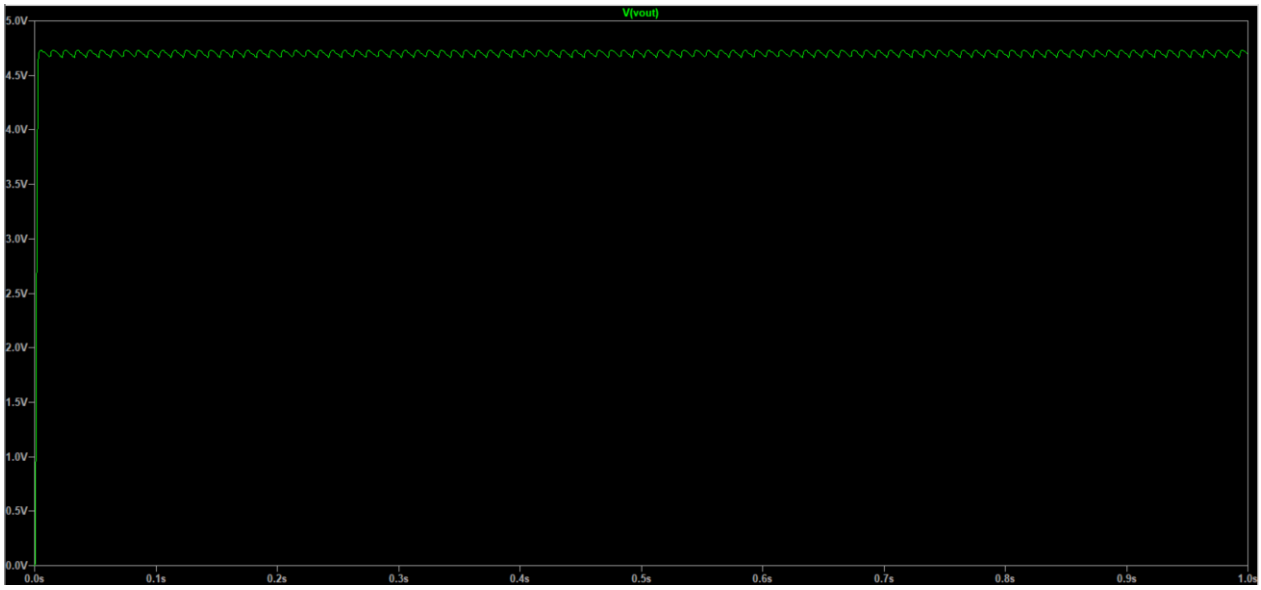

Figure 3 (Software simulation result)

As expected output waveform is a constant value with some ripple on it in the steady state. In this simulation zener is 4.7v but in lab I have used a 5.1V zener so the expected output voltage will be around 5.1V in the experiment though I am expecting to see a similar waveform in the labwork.

After completing designing and simulating my circuit I have implemented it in the lab:

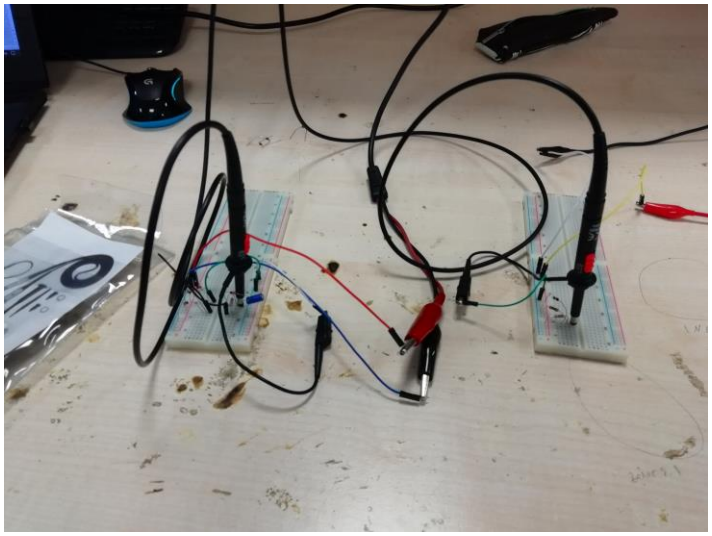

Figure 4 (Left breadboard is for Part A, Right is for Part B and C)

At the output I have seen this waveform:

Figure 5 (Output waveform of the circuit in the part A)

The output signal is around 5V with a ripple of around 480mV. This waveform looks very similar to the simulation results.

Note: Output voltage is supposed to be constant 5.1V but the zener we use in real life is not ideal so there is some r_z inside of it which causes this ripple.

Part B

In this section, as we instructed in the assignment I have eliminated the bridge rectifier and the capacitor from the circuit and we left with this:

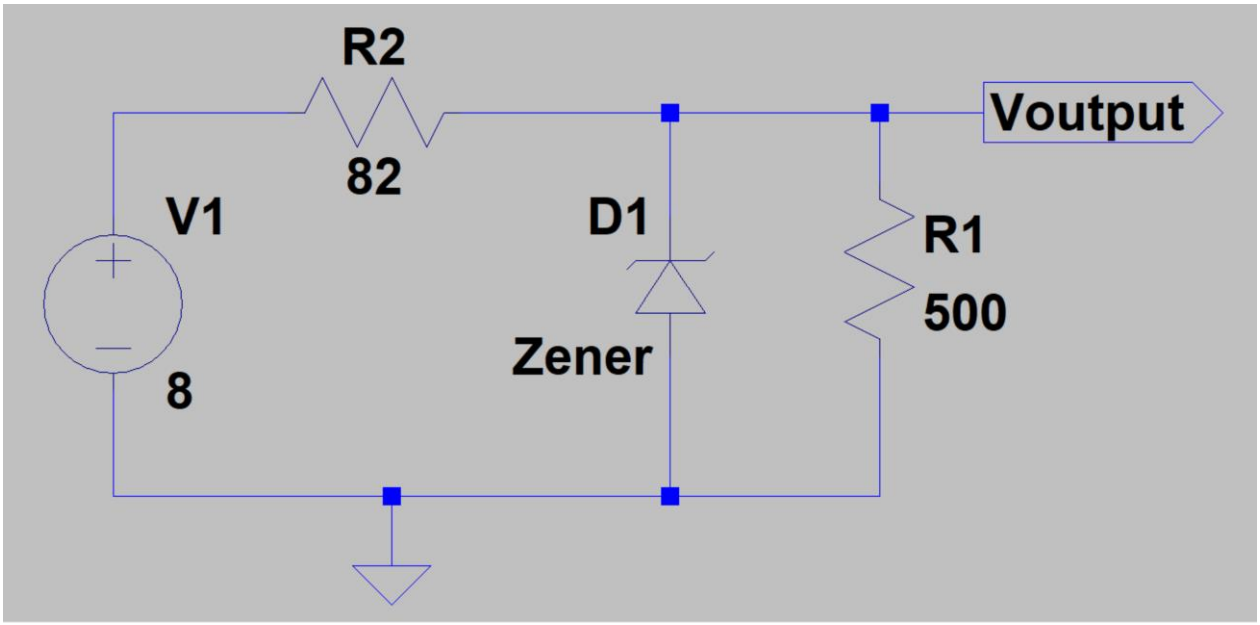

Figure 6 (Circuit Design for Part B and C, input will be varied)

Lab implementation looked like this:

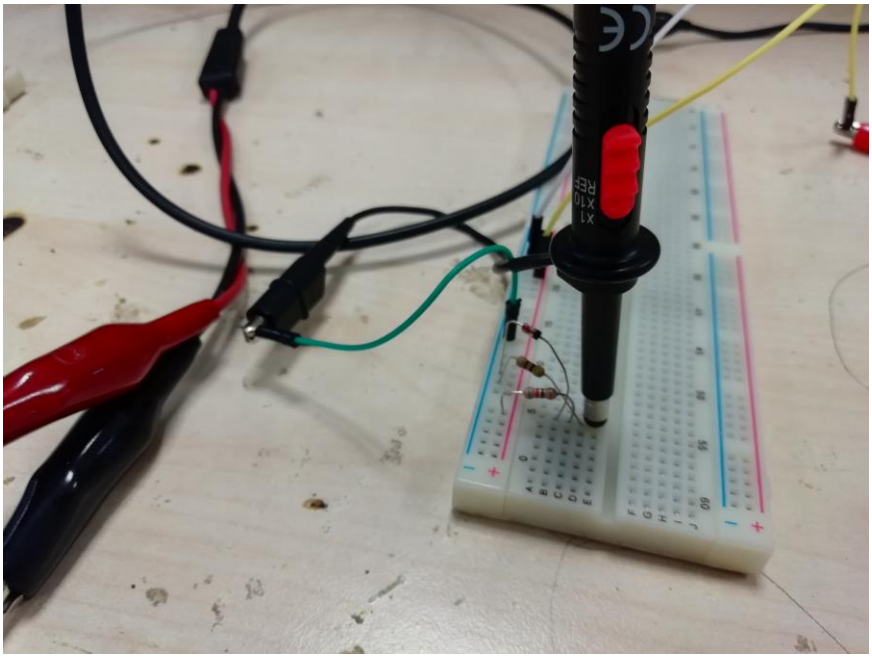

Figure 7 (Lab implementation)

For this part I have set the voltage supply to 7V and 9V to see source regulation. These were the results:

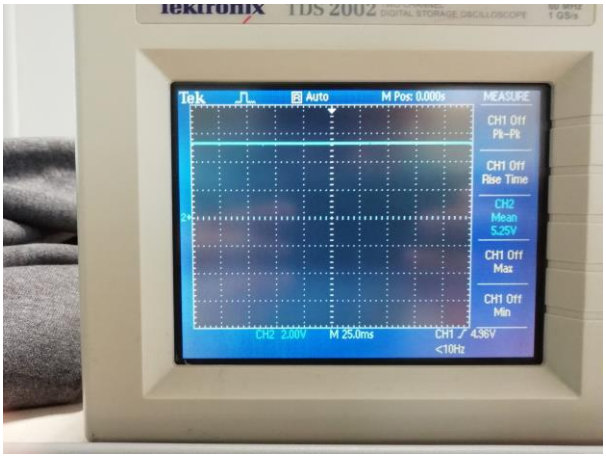

Figure 8 (7V input)

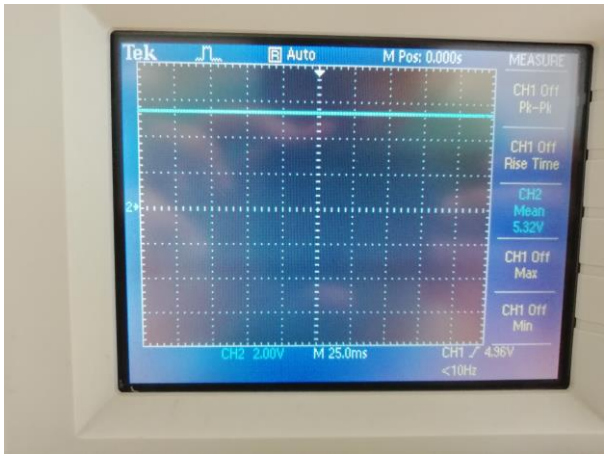

Figure 9 (9V input)

As we can see when source is 7V the output is 5.25V, and when it is 9V the output is 5.32 volt. So the Source regulation becomes:

$$\Delta V_{ps} = 2\ Volts\ and\ \Delta V_{Source} = 0.07\ Volts$$

$$Source\ regulation = \frac{0.07}{2} \times 100 = 3.5\%$$

Part C

In this part I have used the same circuit in the part B but the difference is the input is fixed 8V and RL is varied.

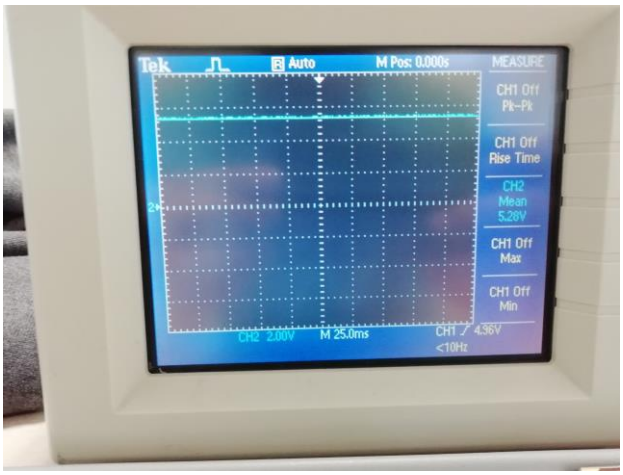

Figure 10 (RL is 500 ohms)

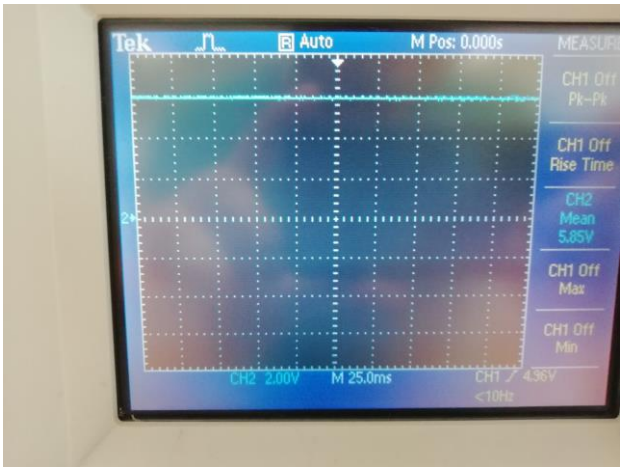

Figure 11 (RL = No load)

As we can see when RL is 500 Ohms the output is 5.28V, and when there is no-load the output is 5.85 volt. So the Load regulation becomes:

$$V_{load} = 5.28\, Volts\ and\ V_{no\ load} = 5.85\, Volts$$

$$Source\ regulation = \frac{5.85 - 5.28}{5.28} \times 100 = 10.7\%$$

Conclusion

In this lab we have tried to implement a voltage regulator circuit with 5.1V zener. The circuit structure is given we only needed to find suitable resistor value and observe the output signals. For part A, we have used all componets (bridge, capacitor, zener,resitors). Theoretically the output voltage supposed to be constant 5.1V but it was not the case in our circuit because the zener we use is expectedly not ideal which causes some ripple in the output signal. For part B we have varied the input signal between 7V and 9V. The output should remain same for ideal zener but again our zener is not ideal so the change in the input voltage caused some miniscule change in the output signal. This fluctuation known as source regulation. For part C, we fixed the input voltage at 8V but changed the load resistor between 500 Ohms and infinity. Which resulted in some fluctuations in the output signal also known as the load regulation. The results were naturally were little bit different from the ideal case since we are using no-ideal diode but they are pretty close to the expected results with minor differences.