## Schematic: Arch Mix

| SHEET | SHEET NAME |
|---|---|
| 01 | Title / Revision History |
| 02 | Block Diagram |
| 03 | Main Power |
| 04 | MCU Power |
| 05 | MCU PinOut |
| 06 | SDRAM / Flash / SD Card |
| 07 | Boot CFG / LCD / LED / BUT |
| 08 | USB / EXP Headers |
| | |
| | |
| | |

## Revision History

| DATE | REVISION | DESCRIPTION |
|---|---|---|
| 2018/11/20 | Arch Mix_v1.0_SCH_181120 | Initial Release |
| | | |
| | | |

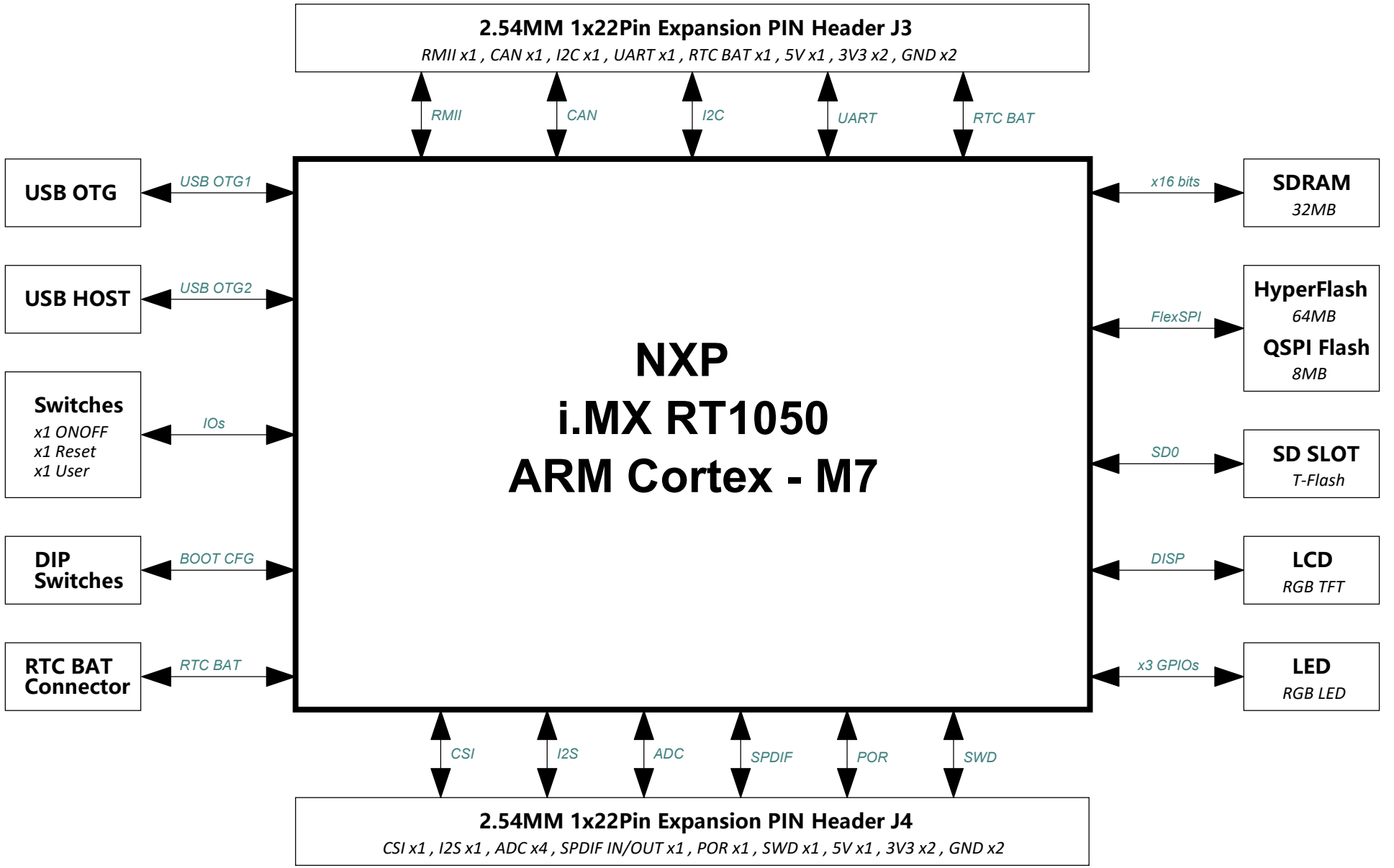
seeed The IoT Hardware Enabler

https://www.seeedstudio.com

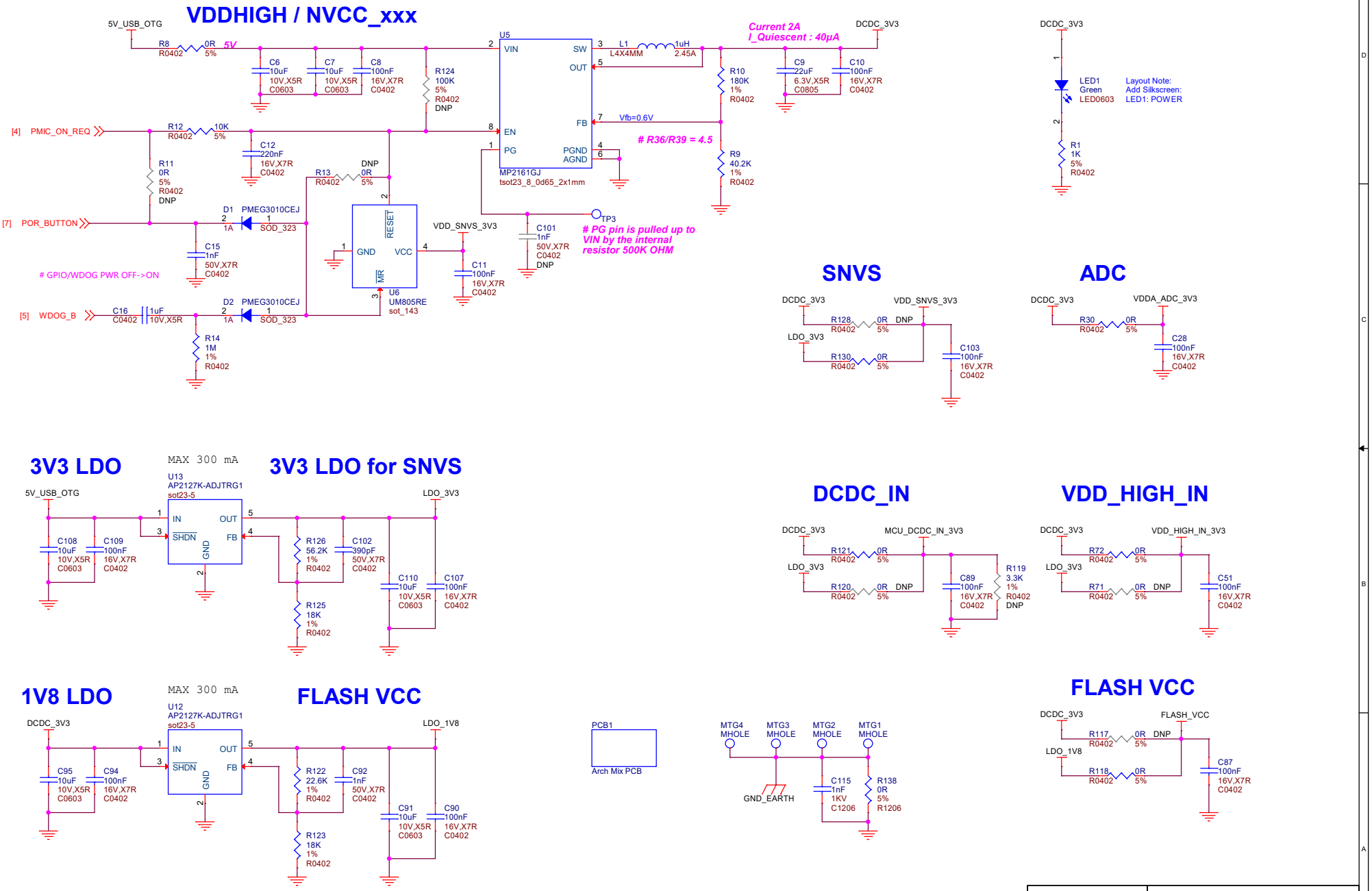
Title: Arch Mix

| Size: A3 | Document Number: 01 Title / Revision History | Rev: v1.0 |
|---|---|---|
| Draw By: XinJQ | Date: Tuesday, November 20, 2018 | Sheet: 1 of 8 |

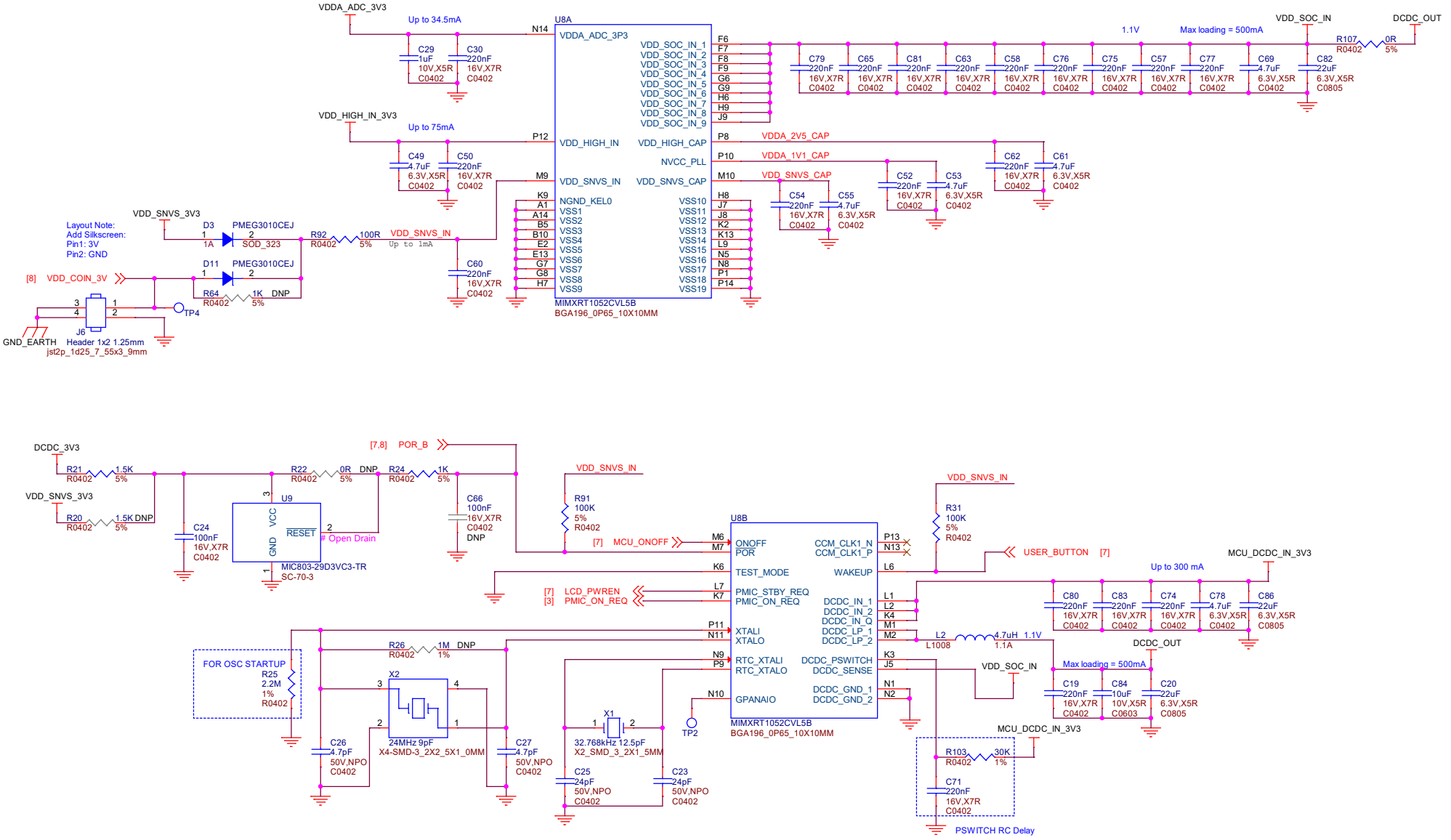
# ##### Arch Mix Blcok Diagram #####



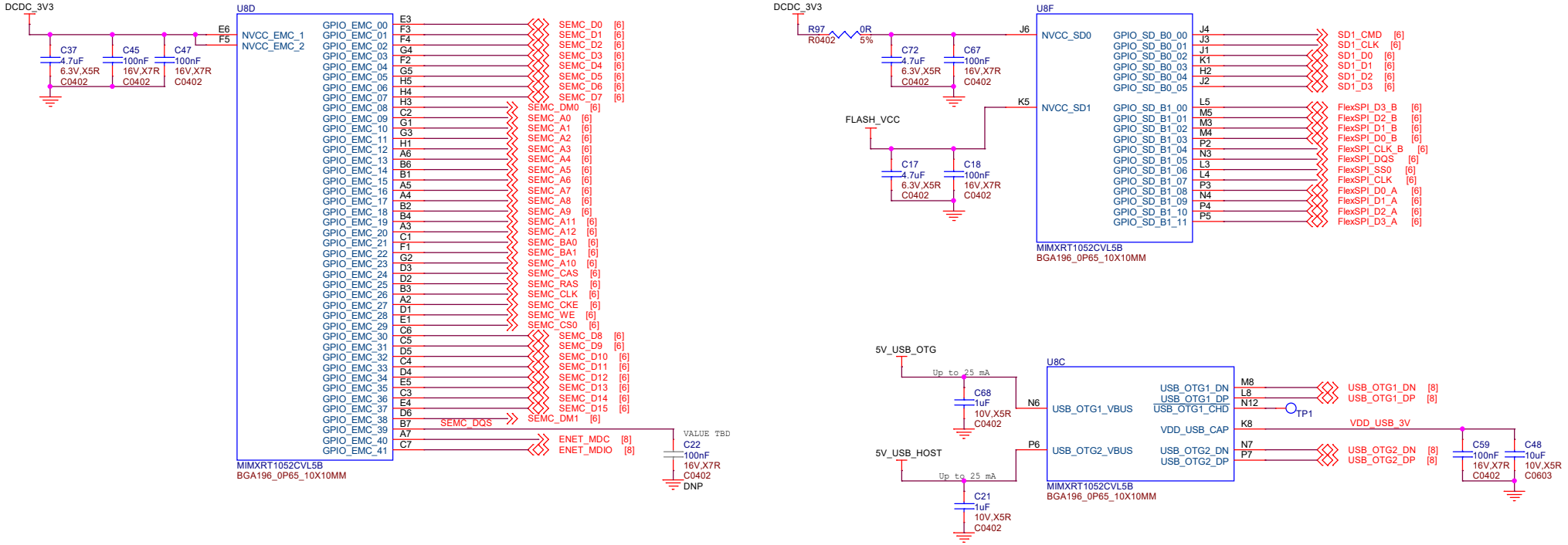

| | | |
|---|---|---|
| seeed The IoT Hardware Enabler | https://www.seeedstudio.com | |
| | Title: Arch Mix | |
| Size: A3 | Document Number: 02 Block Diagram | Rev: v1.0 |
| Draw By: XinJQ | Date: Monday, November 19, 2018 | Sheet: 2 of 8 |



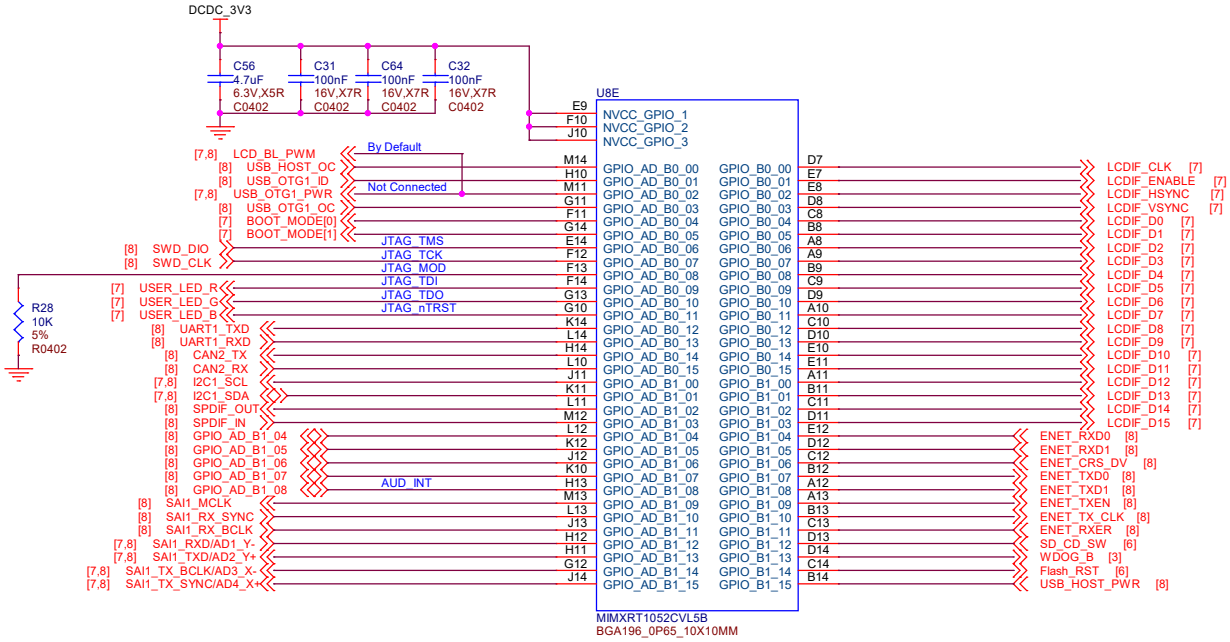

| | | |
|---|---|---|
| seeed The IoT Hardware Enabler | https://www.seeedstudio.com | |
| | Title: Arch Mix | |
| Size: A3 | Document Number: 03 Main Power | Rev: v1.0 |
| Draw By: XinJQ | Date: Monday, November 19, 2018 | Sheet: 3 of 8 |



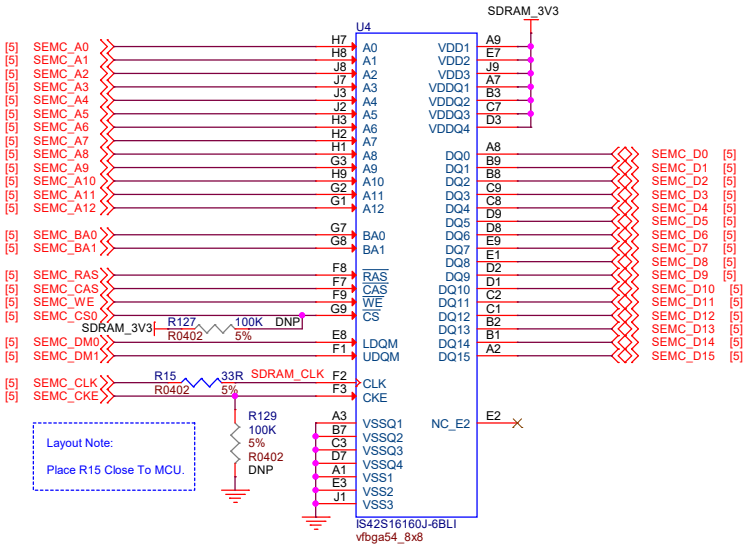

| | | |
|---|---|---|
| seeed The IoT Hardware Enabler | https://www.seeedstudio.com | |
| | Title: Arch Mix | |
| Size: A3 | Document Number: 04 MCU Power | Rev: v1.0 |
| Draw By: XinJQ | Date: Monday, November 19, 2018 | Sheet: 4 of 8 |



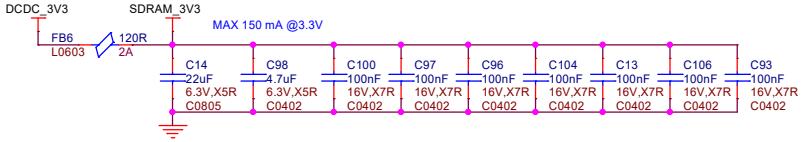

# MCU PINOUT

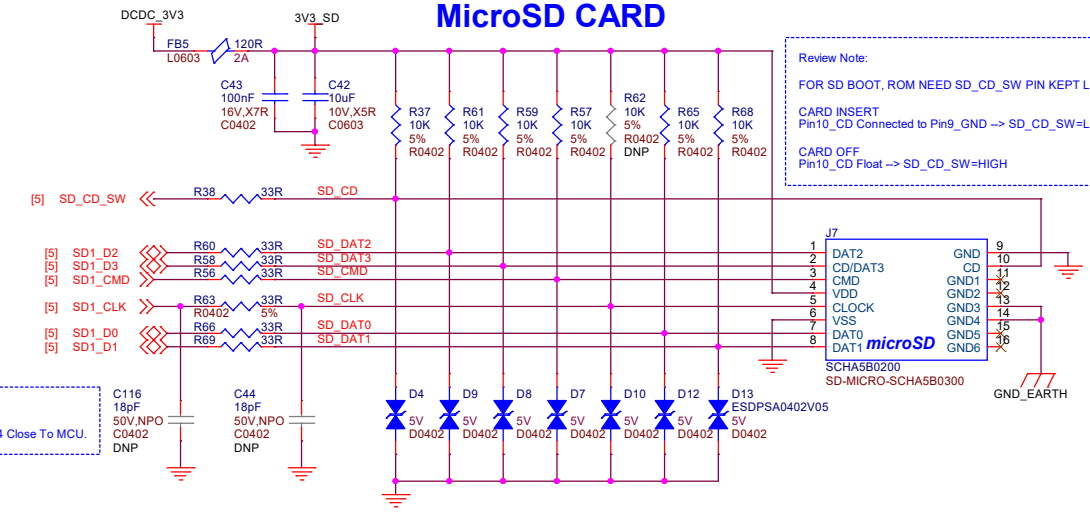



| | | |
|---|---|---|
| seeed The IoT Hardware Enabler | https://www.seeedstudio.com | |
| Title: Arch Mix | | |
| Size: A3 | Document Number: 05 MCU PinOut | Rev: v1.0 |
| Draw By: XinJQ | Date: Monday, November 19, 2018 | Sheet: 5 of 8 |




## SDRAM 32MB




## MicroSD CARD

Layout Note:

The SDRAM interface (running at up to 166 MHz):

1. The SDRAM routing must be separated into three groups: data, address, and control.
2. Route all signals at the same length within 100 Mils.
3. The controlled impedance for the single-ended traces must be 50 Ω.

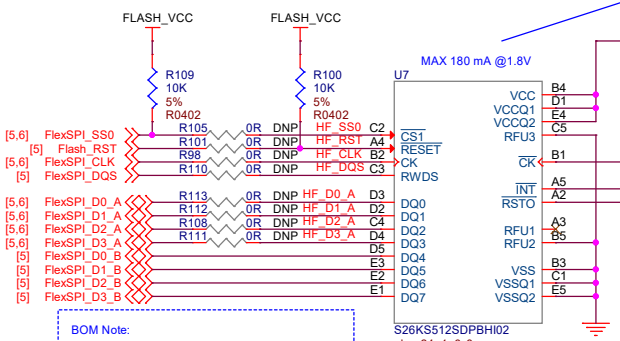
The SD module interfaces (running at up to 50 MHz):

1. Follow similar SDRAM rules for data, address, and control as for the SD interfaces.

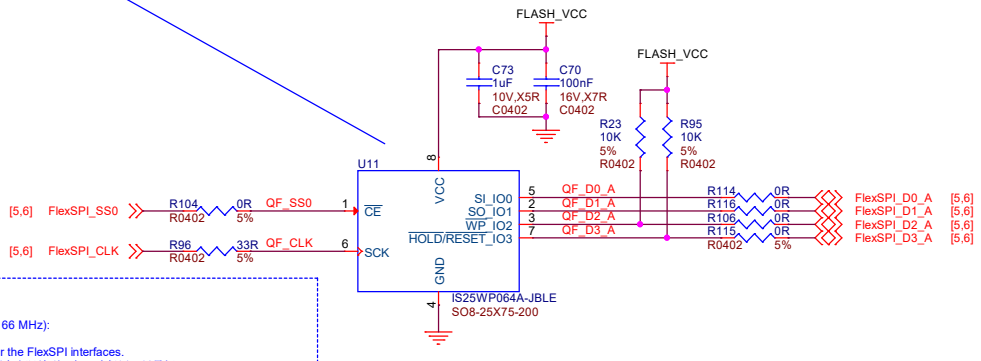
**Option 1: USE HyperFlash (DNP U11 and series R)**

**Option 2: USE QSPI FLASH (DNP U7 and series R)**

## 1V8 HyperFlash 64MB




## 1V8 QSPI Flash 8MB




Layout Note:

The FlexSPI interface (HyperFlash, QSPI Flash, running at up to 166 MHz):

1. Follow similar SDRAM rules for data, address, and control as for the FlexSPI interfaces.
2. 有分叉的信号，走"T"型拓扑结构，即分叉电阻按"T"型放置，且两个电阻放到一起，确保尾巴尽量短。
3. 需放到一起的电阻包括：R105 and R104, R98 and R96, R113 and R114, R112 and R116, R108 and R106, R111 and R115.
4. 以下信号组，需要控制等长：

FlexSPI_SS0 + HF_SS0 ,
FlexSPI_CLK + HF_CLK,
FlexSPI_D0_A + HF_D0_A,
FlexSPI_D1_A + HF_D1_A,
FlexSPI_D2_A + HF_D2_A,
FlexSPI_D3_A + HF_D3_A,
FlexSPI_DQS + HF_DQS,
FlexSPI_CLK_B,
FlexSPI_D0_B,
FlexSPI_D1_B,
FlexSPI_D2_B,
FlexSPI_D3_B

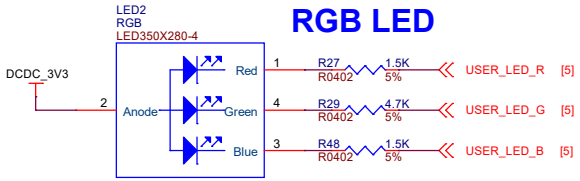
FlexSPI_SS0 + QF_SS0 ,
FlexSPI_CLK + QF_CLK,
FlexSPI_D0_A + QF_D0_A,
FlexSPI_D1_A + QF_D1_A,
FlexSPI_D2_A + QF_D2_A,
FlexSPI_D3_A + QF_D3_A.

| | | |
|---|---|---|
| seeed The IoT Hardware Enabler | https://www.seeedstudio.com | |
| | Title: Arch Mix | |
| Size: A3 | Document Number: 06 SDRAM / Flash / SD Card | Rev: v1.0 |
| Draw By: XinJQ | Date: Monday, November 19, 2018 | Sheet: 6 of 8 |

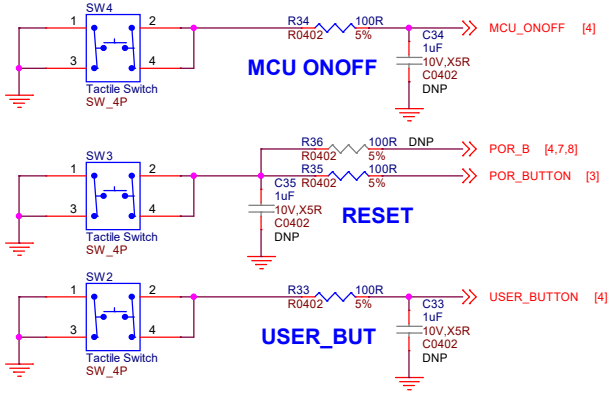
# FUSE MAP

| | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **TYPE** | **BOOT_CFG[11]** | **BOOT_CFG[10]** | **BOOT_CFG[9]** | **BOOT_CFG[8]** | **BOOT_CFG[7]** | **BOOT_CFG[6]** | **BOOT_CFG[5]** | **BOOT_CFG[4]** | **BOOT_CFG[3]** | **BOOT_CFG[2]** | **BOOT_CFG[1]** | **BOOT_CFG[0]** |
| **FlexSPI1 (Serial NOR)** | *Infinit-Loop:<br>(Debug USE only)<br>0 - Disable<br>1- Enable* | *FLASH_TYPE<br>000-Device supports 3B read by default<br>001-Device supports 4B read by default<br>010-HyperFlash 1V8<br>011-HyperFlash 3V3<br>100-MXIC Octal DDR* | | | *0* | *0* | *0* | *0* | *HOLD TIME:<br>00 - 500us<br>01 - 1ms<br>10 - 3ms<br>11 - 10ms* | | *EncryptedXIP<br>0 - Disabled<br>1- Enabled* | *Reserved* |
| **SD** | *Infinit-Loop:<br>(Debug USE only)<br>0 - Disable<br>1- Enable* | *Reserved* | *Bus Width:<br>0 - 1-bit<br>1 - 4-bit* | *SD1 VOLTAGE SELECTION:<br>0 - 3.3V<br>1 - 1.8V* | *0* | *1* | *SD/SDXC Speed:<br>00 - Normal/SDR12<br>01 - High/SDR25<br>10 - SDR50<br>11 - SDR104* | | *SD Power Cycle Enable:<br>'0' - No power cycle<br>'1' - Enabled via USDHC_RST pad* | *SD Loopback Clock Source Sel: (for SDR50 and SDR104 only)<br>'0' - through SD<br>'1' - direct* | *Port Select:<br>0 - eSDHC1<br>1 - eSDHC2* | *Fast Boot:<br>0 - Regular<br>1 - Fast Boot* |

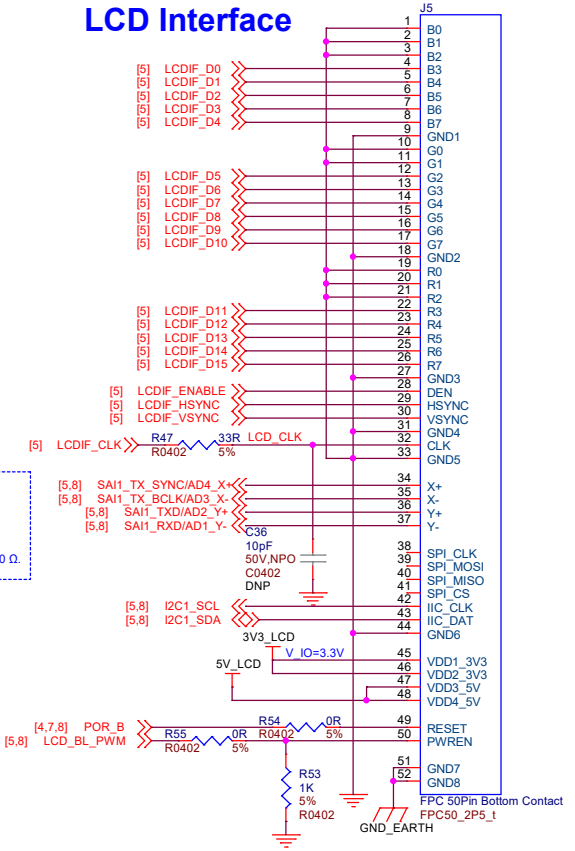
## RGB LED




## Button



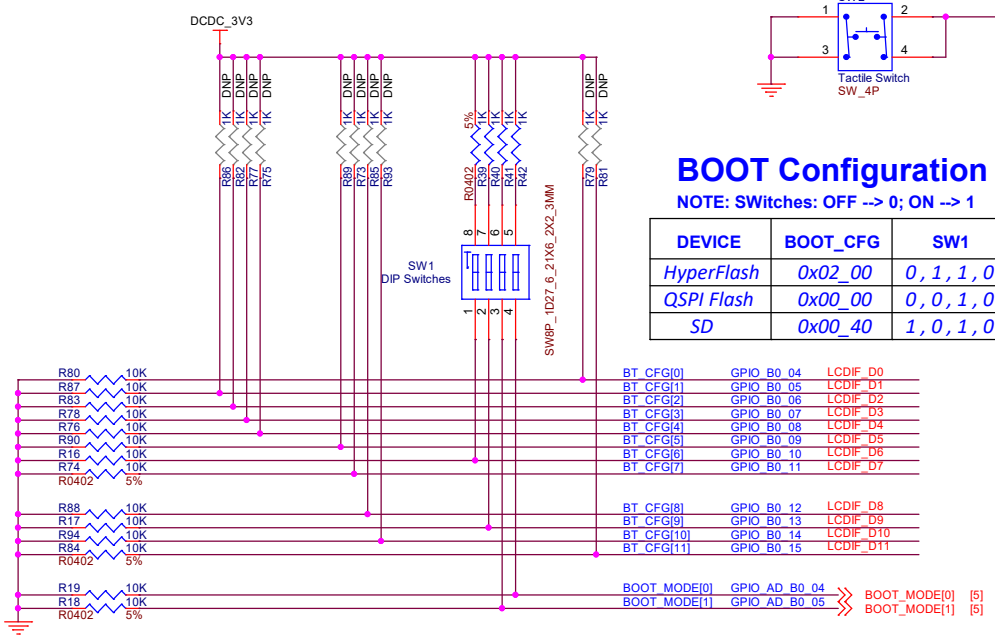

## LCD Interface




## BOOT Configuration

**NOTE: SWitches: OFF --> 0; ON --> 1**

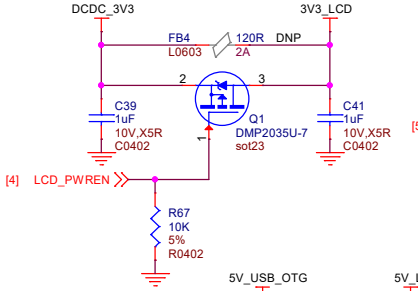
| DEVICE | BOOT_CFG | SW1 |
|---|---|---|
| *HyperFlash* | *0x02_00* | *0,1,1,0* |
| *QSPI Flash* | *0x00_00* | *0,0,1,0* |
| *SD* | *0x00_40* | *1,0,1,0* |

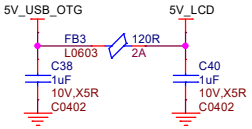



Layout Note:

The LCD interface (running at up to 75 MHz):

1. Route all signals at the same length within 100 Mils.
2. The controlled impedance for the single-ended traces must be 50 Ω.

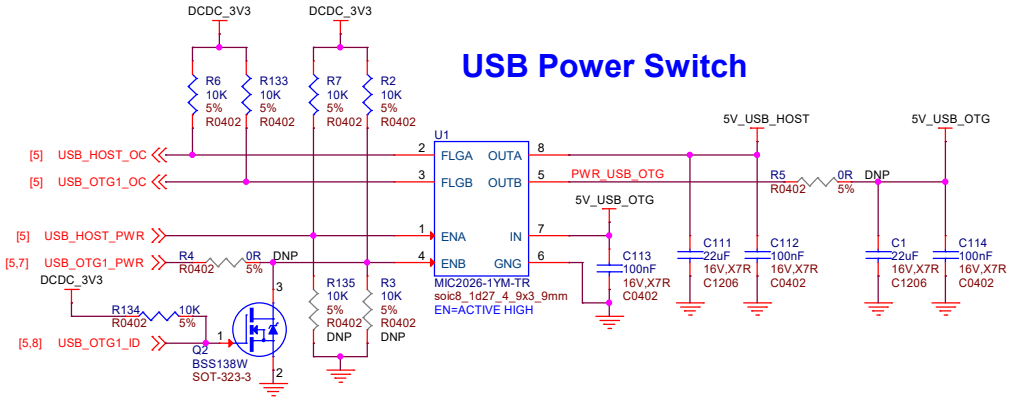


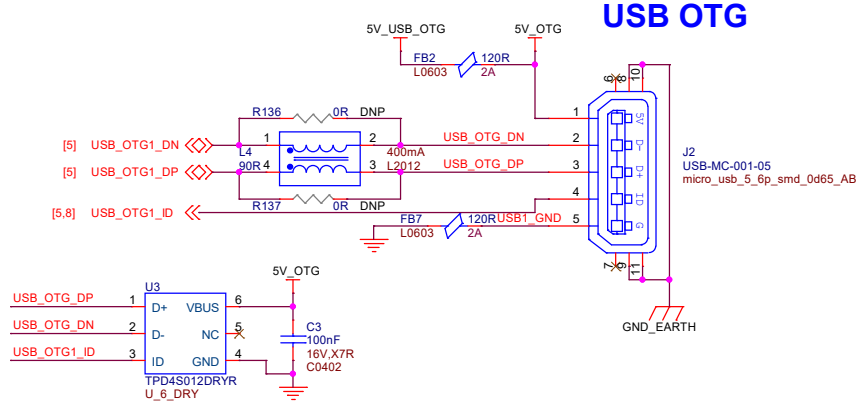




seeed The IoT Hardware Enabler

https://www.seeedstudio.com

| | | |
|---|---|---|
| Title: Arch Mix | | |
| Size: A3 | Document Number: 07 Boot CFG / LCD / LED / BUT | Rev: v1.0 |
| Draw By: XinJQ | Date: Monday, November 19, 2018 | Sheet: 7 of 8 |




## Debug Interface

### UART

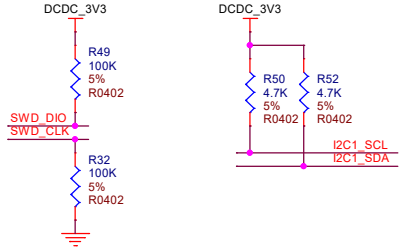
Layout Note:

Add Silkscreen:
J3: UART
Pin22: 3V3
Pin21: GND
Pin20: TXD
Pin19: RXD

### SWD

Layout Note:

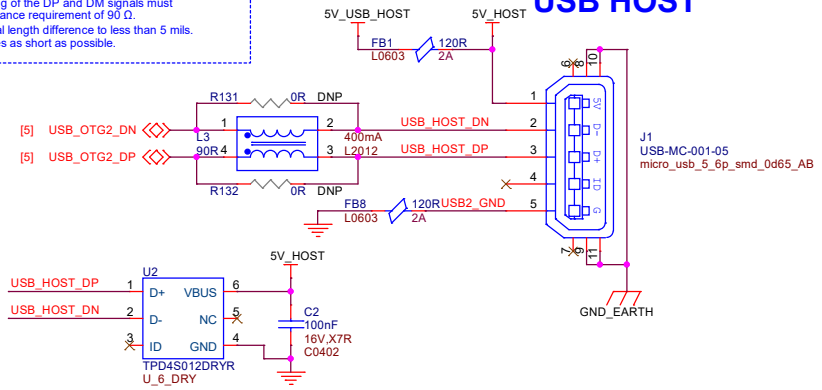
Add Silkscreen:
J4: SWD
Pin22: 3V3
Pin21: GND
Pin20: SWDIO
Pin19: SWDCLK
Pin18: RESET

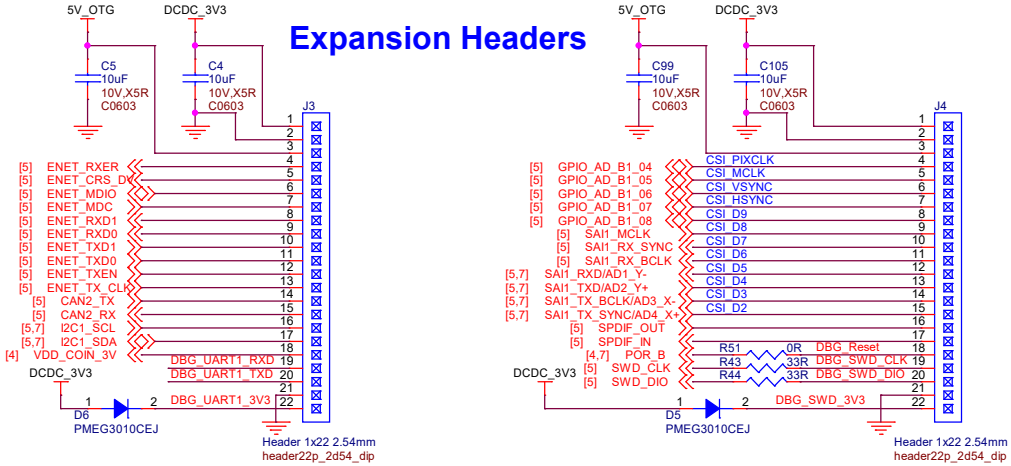


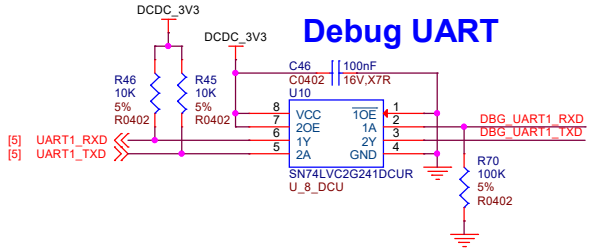

Layout Note:

The USB interface (USB 2.0):

1. Route the high-speed clocks and the DP and DM differential pair firstly.
2. Route the DP and DM signals on the top (or bottom) layer of the board.
3. The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90 Ω.
4. Match the overall differential length difference to less than 5 mils.
5. Keep the DP and DM traces as short as possible.




Layout Note:

The ENET(RMII) signals must be length-matched by TX and RX groups:

That is, the TX group should be matched within 300 Mil (7.62 mm), and the RX group should be matched within 300 Mil (7.62 mm). Total length should not exceed 1750 Mil (44.5 mm).

There is no requirement to match the TX and RX groups because their clocks are not related.

Layout Note:

The CSI interface (running at up to 80 MHz):

1. Route all signals at the same length within 100 Mils.
2. The controlled impedance for the single-ended traces must be 50 Ω.

| | | |
|---|---|---|
| seeed The IoT Hardware Enabler | https://www.seeedstudio.com | |
| Title: Arch Mix | | |
| Size: A3 | Document Number: 08 USB / EXP Headers | Rev: v1.0 |
| Draw By: XinJQ | Date: Monday, November 19, 2018 | Sheet: 8 of 8 |