GROUP 7 - NTPIANS

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Specifications and Features

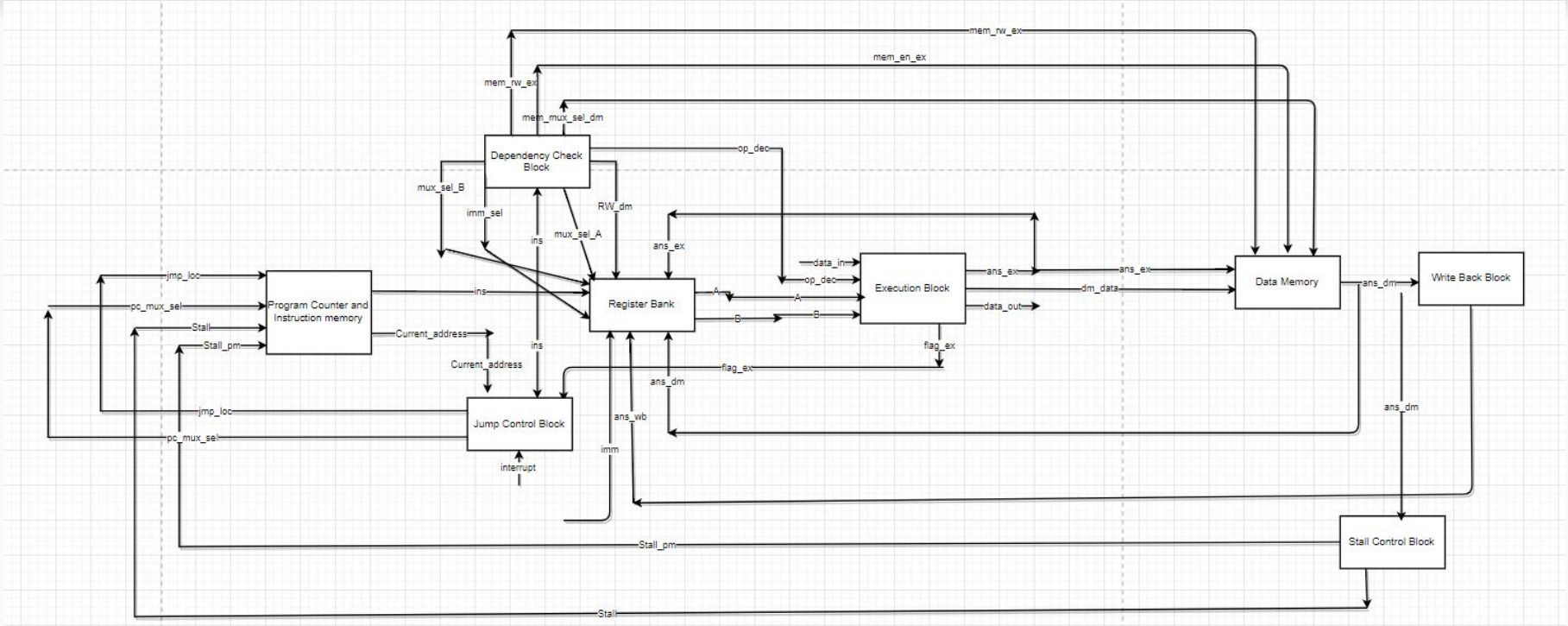
- 8-bit Processor.
- Instruction Size 24-bit.
- 28 Distinct Instructions.
- Fixed Instruction Size (24 bits).
- RISC based architecture.
- 5 Staged pipelined processor.
- Maximum Clock Frequency 579.374 MHz.
- 32 Registers.
- Ideal CPI = 1.
- Five types of Instruction format (R, I, J, M and I/O type).

Specifications and Features

- Harvard type architecture as there are separate storage blocks and signal pathways are provided for data memory and program memory.
- Two types of addressing modes register direct mode and register immediate addressing mode.
- Simpler Architecture.
- CPI = 1.33333333.
- Program Memory 768 bytes.
- Data Memory 256 bytes.
- 21 pins (data_in 8, data_out 8, clk, reset, Vcc, Ground and interrupt each)

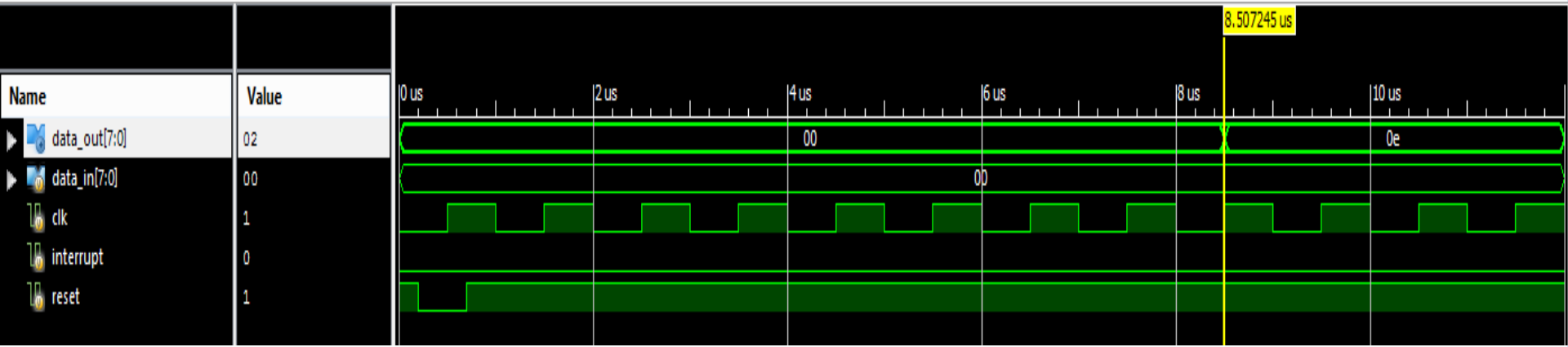
All the modules contain clk and reset as inputs

Block Diagram



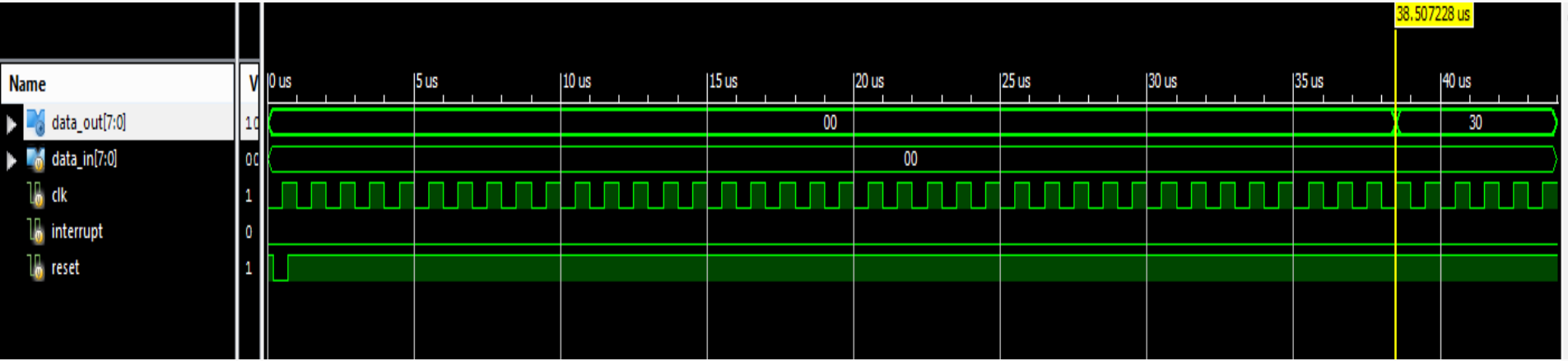
Simulation Results

Addition



Simulation Results

Multiplication



Comparison of our design with 8085

OUR PROCESSOR	INTEL 8085
RISC 8-bit Address bus.	Semi CISC 16-bit Address bus.
8-bit CPU.	8-bit CPU.
Max Clock frequency 579.374 MHz.	Clock frequency 3 - 6 MHz.
5 staged pipelined processor.	Single stage non-pipelined processor.
21 pins.	40 pins.
32 Registers.	6 Registers (B, C, D, E, H, L) and 1 Accumulator .

Comparison of our design with 8085

External Memory cannot be added.	External memory can be added.
Harvard based architecture.	Von Neumann based architecture.
Fixed Instruction size(24 bits).	Varying Instruction size(8-24 bits).
28 distinct Instructions.	74 distinct instructions.
Program memory is 768 bytes and Data Memory is of 256 bytes.	Program memory and Data Memory combined is of 65536 bytes.
No Accumulator.	Contains Accumulator.
Only one Interrupt.	Five hardware Interrupts.
No Stack Pointer.	Stack Pointer.

Challenges Faced

- Some new concepts like IP core generator, Program memory have to be consciously implemented.
- The warnings that were generated and debugging them was tough but interesting task.
- Latches were generated while synthesizing the code. We had to convert them to flip-flops.
- Design of assembly code was tricky.

Feedback

- Our design does not support Branch Prediction. Design changes can be made to make our design support Branch Prediction.
- Cache memory can be introduced to the architecture and RAM size can be increased.
- Different types addressing modes should be implemented.

Thank You