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INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous) Dundigal, Hyderabad – 500 043

LABORATORY WORK SHEET

Date:	19	08	2022
	24.4	12.04	Contraction

Roll No: \$1951A6754 Name: P-JYOTHI PRASANNA

Exp No: 10 Experiment Name: ENERGY BAND GAP OF SEMICONDUCTOR

DAY TO DAY EVALUATION:

		Algorithm	Source Code	Program Execution			
	Preparation	Performance in the Lab	Calculations and Graphs	Results and Error Analysis	Viva	Total	
Max. Marks	4	4	4	4	4	4 20	
Obtained	4	4	4	4	4	20	

Signature of the I/C

START WRITING FROM HERE:

AIM: To determine the unorgy band gap of a given semiconductor using a diode in revouse bias.

APPARATUS:

P-N diode

Power supply

Vollmeter_

Microammeter

Thermometer

FORMULA:

Energy land gap of semiconductor

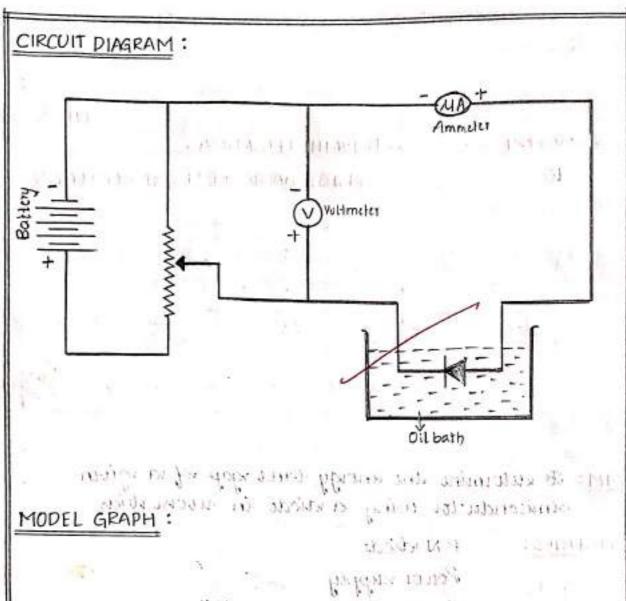
Eg = @lepe x2 x 1.38 x10-23 Joule

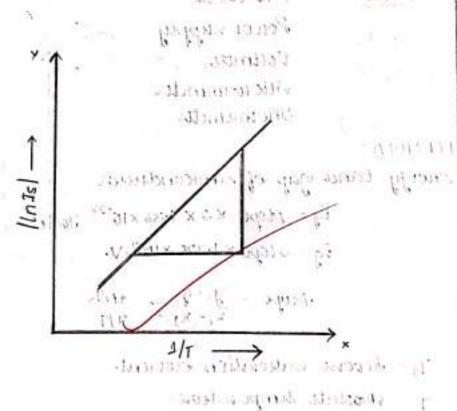
Eg = Stope x 1.725 x 10 4eV.

810px = 31-41 this

Is = Reverse isationation current-

T = Abotlute stemporature.





OBSERVATION TABLE:

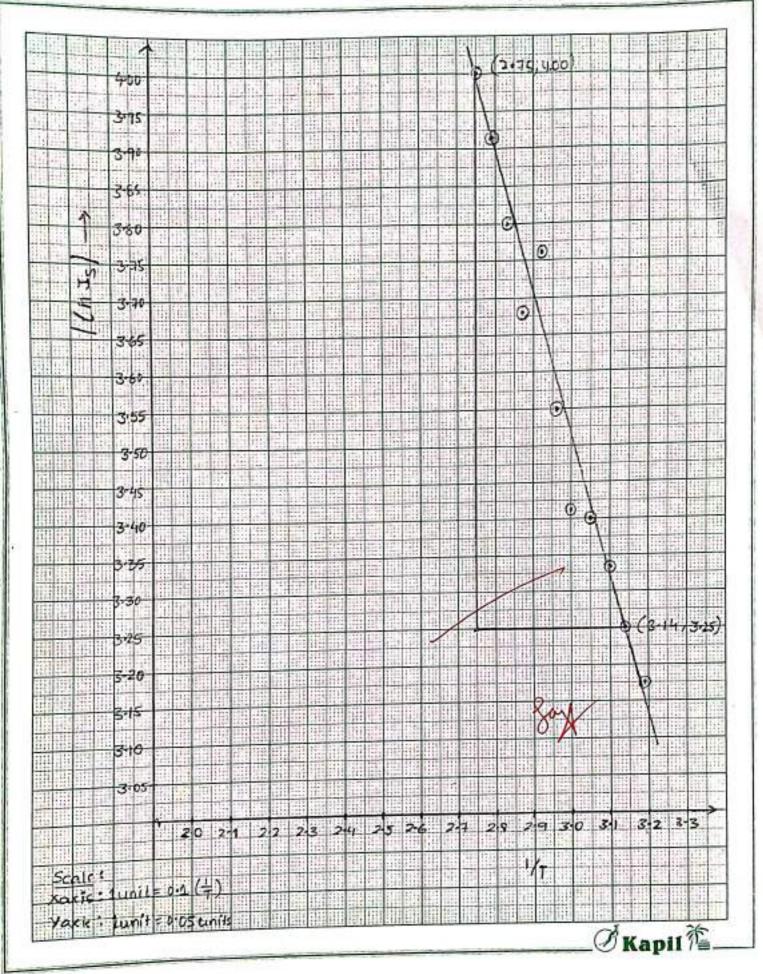
	REVERSE BIAS	1/7	RATURE	TEMPE
	CURRENT (Js)	(xid-3)	" TY	t°c \
13.314.00	na 1990 a.v. n ≥ 1 55 n 30	2.75	363 144	90
3:91 71	50 (1)	2.79	358	85
100 13.80 P	rot 3:44 mail	1411 2183 110	ः उड्डा	6.,800
3.68	11 11 11. 11. 11. 11. 11. 11. 11.	2.67.	. 348	45
1511-1 3 546 2 331	43 -5(10)	2.92	343	70
3.55	101 to 35 10 10 10	- 52.96	338	65
	* 109 3.5 0000	13.00		SIN 60 (11)
3.40	30, 1, 3.	3.05	328	55
3-33	28	3.10	323	50
3:25	111126 put	3.14	318	45
San 3117 350	13 14 24 1 1 3	113.19 Min	Janualia . }	40.100

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The renergy band gap of a given semiconductor is

Eq = (H:92) x 2 x (1.38 x 10.23) J

1Eg/=3.312X10eV



VIVA VOCE:

1. Define enougy gap?

The relifference of unergy between the bottom of the reconduction band and the top of the valence bond of the electrons in a crystalline solid.

- 2. How pn junction is formed?
 The pn junction is created by the method of doping.
 The p-vside; positive side of the semiconductor has an excess of sholes and the n-side; negative side has an excess of electrons.
- 3. What we intrinsic and extrinsic semiconductor?
 Intrinsic semiconductor are volity reliant on demperature while extrinsic semiconductor are raffected by temp.

 and the number of rontaminants present.
- 4. Discuss forward and reverse biasing of diode.

 Forward biasing occurs when the voltage across to diode permits the naturals flow of sewment where as neverse biasing denotes a woltage across the diode in the opposite divedion:
- 5- Explain depletion layer in pn jurction.

 Depletion layer is a region in p-n junction diode where no mobile charge carries are present. Depletion layer acts like a barrier that opposes the flow of electrons from n-side and holes from p-side.

Say