		T					T															
DACE	ADDRESS 0x50200000	OFFSET	NAME PION	Bits	VALUE	notes PIO1 address: 0x50300000	SET 0X0000	PIO1 address: 0x50300000														
BASE	UX50200000			11-8				PIO1 address: Ux50300000														
CTDI	50200000	0000	CLKDIV RESTART SM_RESRART SM_ENABLE	7:4	0x00000001	PIO control register. SM_ENABLE, SM_RESTART and CLKDIV_RESTART is rest to 0x0.  '' denotes the reserved value where we cannot find the detail values.		PIO control register														
CIRL	50200000	UXUUU	TXEMPTY	27:24	UXUUUUUU1			PIO control register														
			TXEMPTY TXFULL RXEMPTY	27:24 19:16 11:8		FIFO status register. The first four bits of RXFULL and TXFULL are 0 after the rest with																
FSTAT	50200004	0x00000004		3:0	0x0f000f01	the following four bits of them being reserved one. Additionally, the first four bits of RXEMPTY and TXEMPTY are 1 with the rest of bits being reserved one.	0x0f000f01	FIFO status register = pio fifo joi	oin .													
			TXSTALL TXOVER RXUNDER	27:24 19:16 11:8 3:0		· ·																
			TXOVER RXUNDER	19:16		FIFO debug register. The first four bits to be RXSTALL, RXUNDER and TXOVER and TXSTALL are all 0 after resetting, the rest of bitsare being reserved ones.																
FDEBUG	50200008	0x00000008	RXSTALL	3:0	0x00000000	TXSTALL are all 0 after resetting, the rest of bitsare being reserved ones.	0x01000e00	FIFO debug register														
			RX3	31:28 27:24 23:20 19:16 15:12																		
			RX2	23:20																		
			TX2 RX1	19:16 15:12																		
			TX1	11:8																		
FLEVEL	5020000c	0x0000000c	TX0	3:0	0x00000000	FIFO levels All of bits of this register is resetted to 0 after the offsetting, no reserved bits for	0x00000000	FIFO levels														
						Direct write access to the TX FIFO for this state machine. Each write pushes one word to the FIFO. Attempting to write to a full																
						Write pushes one word to the FIFO. Attempting to write to a full FIFO has no effect on the FIFO state or contents, and sets the sticky FDEBUG_TXOVER error flag for this FIFO. All of bits of this register is rested to 0																
						sticky FDEBUG_TXOVER error flag for this FIFO. All of bits of this register is rested to 0 after the offsetting and there is no reserved bits in the register, additionally, there are no																
TXF0	50200010		TXF0	31:0	0x00000000	message being printed out.	0x00000000	Direct write access to the TX FIF4														
TXF1		0x00000014		31:0	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the	e 0x00000000	Direct write access to the TX FIFE	O for this state mad	ine. Eachwrite pr	ushes one word to	o the FIFO. Attemp	ting to write to a fi	ulFIFO has no effect or	the FIFO state or conte	ents, and sets thestic	ky FDEBUG_TXC	OVER error flag fo	r this FIFO.			
TXF2 TXF3	50200018 5020001c	0x00000018 0x0000001c	TXF3	31:0	0x00000000 0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the Direct write access to the TX FIFO for this state machine.	e 0x00000000	Direct write access to the TX FIFE	O for this state mad	ine. Eachwrite pi	ushes one word to	o the FIFO. Attemp	iting to write to a fi	JIFIFO has no effect or	the FIFO state or conte	ents, and sets thestic	ky FDEBUG_TXC	OVER error flag to	r this FIFO.			
IXF3	5020001C	UXUUUUUU1C	IXF3	31:0	UXUUUUUUU	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to tr Direct read access to the RX FIFO for this state machine. Each	ie uxuuuuuuu	Direct write access to the TX FIF4	O for this state maci	ine. Eachwrite pi	usnes one word to	b the FIFU. Attemp	iting to write to a ri	JIIFIFO has no effect or	the FIFO state or conte	ents, and sets thestic	XY FDEBUG_IXC	JVER error riag to	If this FIFO.			
						read pops one word from the FIFO. Attempting to read from an																
						IFDEBUG RXUNDER error flag for this FIFO. The data returned to																
RXF0	50200020	0x00000020	RXEO	31-0	0x963f69b2	the system on a read from an empty FIFO is undefined. The rule for setting the value is basically the same as TXFn	0x14fea89d	Direct read access to the RX FIF	O for this state mad	ina Earbraad n	one one word from	n the EIEO Attenno	ting to read from :	anamohy EIEO has no a	ffect on the EIEO state	and eate the etickuEl	DEBLIG BYLINDS	ED arror flag for th	sie EIEO. The data	a returned to the evets	am on a read from	an amphy EIEO is undefined
RXF1		0x00000024	RXF1	31:0	0x245a3d99	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the	e 0x0db36757	Direct read access to the RX FIF	O for this state mach	ine. Eachread or	ops one word from	n the FIFO. Attemp	ting to read from a	nempty FIFO has no e	ffect on the FIFO state.	and sets the stickvFl	DEBUG RXUNDE	R error flag for th	nis FIFO. The data	returned to the syste	em on a read from	an empty FIFO is undefined
RXF2			RXF2	31:0	0xadf83d99	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the	e 0xb3060127	Direct read access to the RX FIF	O for this state mack	ine. Eachread po	ops one word from	n the FIFO. Attemp	ting to read from a	nempty FIFO has no e	ffect on the FIFO state,	and sets the stickyFl	DEBUG RXUNDE	R error flag for th	nis FIFO. The data	returned to the syste	em on a read from	an empty FIFO is undefined
RXF3	5020002c	0x0000002c	RXF3	31:0	0xa8fc7caf	Direct read access to the RX FIFO for this state machine. Each read pops one word from the	e oxb8250d8e	Direct read access to the RX FIF	O for this state mac	ine. Eachread po	ops one word from	n the FIFO. Attemp	ting to read from a	anempty FIFO has no e	ffect on the FIFO state,	and sets the stickyFl	DEBUG_RXUNDE	R error flag for th	nis FIFO. The data	returned tothe syste	em on a read from	an empty FIFO is undefined
INSTR MEMO	50200030	0x00000030	Write-only access to instruction memory	k 15:0	0x00000000	Write-only access to instruction memory location 0. The first half of this registe is resetted to 0 with the second half being the reserved ones.	0x00000000	Write-only access to instruction n	memory location ∩													
INSTR_MEMn	50200030+4n	0x48+4n	Write-only access to instruction memory	15:0	0x00000000	Write-only access to instruction memory location n		Write-only access to instruction n	memory location n													
INSTR_MEM31	502000c4	0x000000c4	Write-only access to instruction memory	15:0	0x00000000	Write-only access to instruction memory location 31	0x00000000	Write-only access to instruction m	memory location 31													
			INT	31:16		Clock divisor register for state machine n. Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 258). The frist 8 bits are reserved ones with the FRAC is reseted to 0. The																
SM0_CLKDIV	50200c8	0x000000c8	FRAV	31:16 15:8	0x000fa000	CLKDIV_FRAC / 256). The trist 8 bits are reserved ones with the FRAC is reseted to 0. The last 4 bits of the INT is reseted to vaue 1.	0x000fa000	Clock divisor register for state ma	achine n. Frequency	= clock freq / (CL	.KDIV_INT + CLK	(DIV_FRAC / 256)										
			EXEC_STALLED SIDE_EN	31																		
			SIDE_PINDIR	29																		
			SIDE_PINDIR JMP_PIN OUT_EN_SEL INITIALE_OUT_EN OUT_STICKY WRAP_TOP	29 28:24 23:19																		
			INLINE_OUT_EN	18																		
			WRAP TOP	17 16:12 11:7																		
			STATUS SEL	11:7		Execution/hebavioural settings for state machine n. The 6 to 6 bits are reserved ones and																
SM0_EXECCTRL	502000cc	0x0cc		3:0	0x00017a00	Execution/behavioural settings for state machine n. The 5 to 6 bits are reserved ones and the 12 to 16 bits are offset to 0x1f, the rest of the bits are being reseted to 0.	0x00013800	Execution/behavioural settings fo	or state machine n													
			FJOIN RX FJION TX PULL THRESH PUSH THRESH OUT SHIFTDIR IN SHIFTDIR AUTOPULL AUTOPULL AUTOPULL	31																		
			PULL_THRESH	29:25 24:20																		
			PUSH_THRESH OUT_SHIFTDIR	24:20																		
			IN_SHIFTDIR	18		Control behaviour of the input/output shift registers for state																
SM0 SHIFTCRTL			AUTOPULL																			
IOMU_SHIFTCRTL	502000d0	0x0d0	AUTOPUSH	16	0x40060000	machine (). The first half of the reciptor' hits are the reserved once with the 18, 10 hits rese	0x40060000	Control behaviour of the input/out	tput shift registers fo	r statemachine 0												
	502000d0	0x0d0	AUTOFOSH	16	0x40060000	machine (). The first half of the reciptor' hits are the reserved once with the 18, 10 hits rese				r statemachine 0												
SM0_ADDR		0x0d0 0x0d4 0x0d8	AUTOPUSH  Current instruction address of state mac	16 th 4:0	0x40060000 0x00000014 0x00006221	machine 0. The first half of the register bits are the reserved ones with the 18, 19 bits rese Current instruction address of state machine 0. The first four bits are resetd to 0 with the rest bits of it are reserved.	0x00000010	Current instruction address of sta	ate machine 0		rogram counterW	frite to execute an in	instruction immedia	ately (including jumps)	and then resume execution	ion						
	502000d0 502000d4 502000d8	0x0d0 0x0d4 0x0d8	Current instruction address of state mac	15:0	0x40060000 0x00000014 0x00006221	machine (). The first half of the reciptor' hits are the reserved once with the 18, 10 hits rese	0x00000010	Current instruction address of sta	ate machine 0		rogram counterW	frite to execute an in	instruction immedia	ately (including jumps)a	and then resume execution	ion.						
SM0_ADDR			Current instruction address of state mac	15:0		machine 0. The first half of the register bits are the reserved ones with the 18, 19 bits rese Current instruction address of state machine 0. The first four bits are resetd to 0 with the rest bits of it are reserved.	0x00000010	Current instruction address of sta	ate machine 0		rogram counterW	frite to execute an in	instruction immedi	ately (including jumps)a	and then resume executi	ion.						
SM0_ADDR			Current instruction address of state mac	15:0		machine 0. The first half of the register bits are the reserved ones with the 18, 19 bits rese Current instruction address of state machine 0. The first four bits are resetd to 0 with the rest bits of it are reserved.	0x00000010	Current instruction address of sta	ate machine 0		rogram counterW	frite to execute an is	nstruction immedi	ately (including jumps)a	and then resume execution	ion.						
SMO_ADDR SMO_INSTR	502000d8		Current instruction address of state mac	15:0		machine. O The first half of the register bits aire the reserved ones with the 18,19 bits rese Current instruction aboves of statem enachine. On the first four bits are reserved to with the reat bits of it are reserved.  Read to see the instruction currently addressed by state machine(i's program counterWrite	0x00000010 t 0x00006221	Current instruction address of sta Read to see the instruction current	ate machine 0		rogram counterW	frile to execute an is	instruction immedia	ately (including jumps)s	and then resume execution	ion.						
SMO_ADDR SMO_INSTR			Current instruction address of state mac  SIDESET_COUNT SET_COUNT OUT_COUNT IN BASE SIDESET_BASE SET_BASE SET_BASE OUT_BASE	15:0 31:29 28:26 25:20 19:15 14:10 9:5 4:0	0x00006221	machine O. The first half of the register bits aire the reserved once with the 18,10 bits rese Current instruction states of states machine. On the rist for bits are received to with the read to see the instruction currently addressed by state machine's program counterWrite Radio see the instruction currently addressed by state machine's program counterWrite State machine on control O. Since only the 26 to 28 bits are offset to 0x51/011	0x00000010	Current instruction address of sta Read to see the instruction current	ate machine 0 ently addressed by st	ate machine0's pr	rogram counterW	frite to execute an is	instruction immedi	ately (including jumps)a	and then resume executi	ion.						
SMO_ADDR SMO_INSTR	502000d8		Current instruction address of state mac SIDESET_COUNT SET_COUNT OUT_COUNT SIDESET_BASE SIDESET_BASE OUT_BASE INT FRAW INT	15:0	0x00006221	machine. O The first half of the register bits aire the reserved ones with the 18,19 bits rese Current instruction aboves of statem enachine. On the first four bits are reserved to with the reat bits of it are reserved.  Read to see the instruction currently addressed by state machine(i's program counterWrite	0x00000010 t 0x00006221	Current instruction address of sta Read to see the instruction current	ate machine 0 ently addressed by st	ate machine0's pr	rogram counterW	frite to execute an is	instruction immedi	ately (including jumps)s	and then resume executi	ion.						
SM0_ADDR SM0_INSTR	502000d8		CUTENT INSTRUCTION Address of state mac SIDESET. COUNT SET COUNT OUT_COUNT IN BASE SIDESES. BASE OUT_BASE. IN TERMS.	15:0 31:29 28:26 25:20 19:15 14:10 9:5 4:0	0x00006221 0x20003000	machine O. The first half of the register bits aire the reserved once with the 18,10 bits rese Current instruction states of states machine. On the rist for bits are received to with the read to see the instruction currently addressed by state machine's program counterWrite Radio see the instruction currently addressed by state machine's program counterWrite State machine on control O. Since only the 26 to 28 bits are offset to 0x51/011	0x00000010 tx 0x00006221 0x20003000	Current instruction address of sta Read to see the instruction current	ate machine 0 ently addressed by st	ate machine0's pr	rogram counterW	frite to execute an in	instruction immedi	ately (including jumps)a	and then resume executi	ion.						
SM0_ADDR SM0_INSTR	502000d8		CUTENT INSTRUCTION Address of state mac SIDESET. COUNT SET COUNT OUT_COUNT IN BASE SIDESES. BASE OUT_BASE. IN TERMS.	15:0 31:29 28:26 25:20 19:15 14:10 9:5 4:0 31:16 15:8 31	0x00006221 0x20003000	machine O. The first half of the register bits aire the reserved once with the 18,10 bits rese Current instruction states of states machine. On the rist for bits are received to with the read to see the instruction currently addressed by state machine's program counterWrite Radio see the instruction currently addressed by state machine's program counterWrite State machine on control O. Since only the 26 to 28 bits are offset to 0x51/011	0x00000010 tx 0x00006221 0x20003000	Current instruction address of sta Read to see the instruction current	ate machine 0 ently addressed by st	ate machine0's pr	rogram counterW	frite to execute an i	instruction immedi	ately (including jumps)a	and then resume execution	ion.						
SM0_ADDR SM0_INSTR	502000d8		CUTENT INSTRUCTION Address of state mac SIDESET. COUNT SET COUNT OUT_COUNT IN BASE SIDESES. BASE OUT_BASE. IN TERMS.	15:0 31:29 28:26 25:20 19:15 14:10 9:5 4:0 31:16 15:8 31	0x00006221 0x20003000	machine O. The first half of the register bits aire the reserved once with the 18,10 bits rese Current instruction states of states machine. On the rist for bits are received to with the read to see the instruction currently addressed by state machine's program counterWrite Radio see the instruction currently addressed by state machine's program counterWrite State machine on control O. Since only the 26 to 28 bits are offset to 0x51/011	0x00000010 tx 0x00006221 0x20003000	Current instruction address of sta Read to see the instruction current	ate machine 0 ently addressed by st	ate machine0's pr	rogram counterW	frite to execute an in	instruction immedi	ately (including jumps)a	and then resume executi	ion.						
SM0_ADDR SM0_INSTR	502000d8		CUTENT INSTRUCTION Address of state mac SIDESET. COUNT SET COUNT OUT_COUNT IN BASE SIDESES. BASE OUT_BASE. IN TERMS.	15:0 31:29 28:26 28:26 19:15 14:10 9:5 4:0 31:16 15:8 31 30 29 28:24 23:19	0x00006221 0x20003000	machine O. The first half of the register bits aire the reserved once with the 18,10 bits rese Current instruction states of states machine. On the rist for bits are received to with the read to see the instruction currently addressed by state machine's program counterWrite Radio see the instruction currently addressed by state machine's program counterWrite State machine on control O. Since only the 26 to 28 bits are offset to 0x51/011	0x00000010 tx 0x00006221 0x20003000	Current instruction address of sta Read to see the instruction current	ate machine 0 ently addressed by st	ate machine0's pr	rogram counterW	frite to execute an in	instruction immedi	ately (including jumps)a	then resume execution	ion.						
SM0_ADDR SM0_INSTR	502000d8		Current instruction address of state mac SIDESET_COUNT OUT_COUNT NOT DOWN TO STATE TAKE NOT DOWN TO STATE TAKE OUT_BASE	15:0 31:29 28:26 28:26 28:20 19:15 14:10 9:5 4:0 15:8 31 30 29 28:24 23:19 18 17 16:12	0x00006221 0x20003000	machine O. The first half of the register bits aire the reserved once with the 18,10 bits rese Current instruction states of states machine. On the rist for bits are received to with the read to see the instruction currently addressed by state machine's program counterWrite Radio see the instruction currently addressed by state machine's program counterWrite State machine on control O. Since only the 26 to 28 bits are offset to 0x51/011	0x00000010 tx 0x00006221 0x20003000	Current instruction address of sta Read to see the instruction current	ate machine 0 ently addressed by st	ate machine0's pr	rogram counterW	frite to execute an in	instruction immedi	ately (including Jumps)s	ind then resume execution	ion.						
SM0_ADDR SM0_INSTR SM0_PINCTRL SM1_CLKDIV	502000ds 502000dc 50200e0	0x0d8 0x0dc 0x0e0	Current instruction address of state mac SIDESET_COUNT OUT_COUNT NOT DOWN TO STATE TAKE NOT DOWN TO STATE TAKE OUT_BASE	15:0 31:29 28:26 25:20 19:15 14:10 9:5 4:0 31:16 15:8 31	0.000005221 0.220033000 0.00010000	machine C. The first half of the register bits air et ne reserved ones with the 18, 19 bits rese Current instruction shares of states machine. On the rist for bits are reserved to the thin Characteristic control of the control of	0x0000010 tx 0x00006221 0x20003000 0x20003000	Current instruction address of sta Resaft to see their instruction current State machine gin control Clock divisor register for states ma Transparring or clock fleet (CLASIA)	ate machine 0 milly addressed by st achine 1 V_INT + CLKDIV_FF	ate machine0's pr	rogram counterW	frite to execute an in	instruction immedia	ately (including jumps)a	and then resume execution	ion.						
SM0_ADDR SM0_INSTR	502000ds 502000dc 50200e0		Current instruction address of state mac SIDESET_COUNT OUT_COUNT No N	15:0 31:29 28:26 28:26 28:20 19:15 14:10 9:5 4:0 15:8 31 30 29 28:24 23:19 18 17 16:12	0x00006221 0x20003000	machine O. The first half of the register bits aire the reserved once with the 18,10 bits rese Current instruction states of states machine. On the rist for bits are received to with the read to see the instruction currently addressed by state machine's program counterWrite Radio see the instruction currently addressed by state machine's program counterWrite State machine on control O. Since only the 26 to 28 bits are offset to 0x51011	0x00000010 tx 0x00006221 0x20003000	Current instruction address of sta Read to see the instruction current	ate machine 0 milly addressed by st achine 1 V_INT + CLKDIV_FF	ate machine0's pr	rogram counte/W	frite to execute an i	instruction immedi	ately (including jumps)s	ind then resume execution	ion.						
SM0_ADDR SM0_INSTR SM0_PINCTRL SM1_CLKDIV	502000ds 502000dc 50200e0	0x0d8 0x0dc 0x0e0	Current instruction address of state mac SIDESET_COUNT OUT_COUNT No N	15:0 31:26 28:26 28:26 28:26 28:26 28:20 19:15 14:10 9:5 4:0 15:8 31 30 29 29 28:24 23:19 18 17 16:12 11:7 4 3:0	0.000005221 0.220033000 0.00010000	machine C. The first half of the register bits air et ne reserved ones with the 18, 19 bits rese Current instruction shares of states machine. On the rist for bits are reserved to the thin Characteristic control of the control of	0x0000010 tx 0x00006221 0x20003000 0x20003000	Current instruction address of sta Resaft to see their instruction current State machine gin control Clock divisor register for states ma Transparring or clock fleet (CLASIA)	ate machine 0 milly addressed by st achine 1 V_INT + CLKDIV_FF	ate machine0's pr	rogram counterW	frite to execute an in	instruction immedia	ately (including jumps)a	nd then resume executs	ion.						
SM0_ADDR SM0_INSTR SM0_PINCTRL SM1_CLKDIV	502000ds 502000dc 50200e0	0x0d8 0x0dc 0x0e0	Current instruction address of state mac SIDESET_COUNT OUT_COUNT No N	15:0 31:26 28:26 28:26 28:26 28:26 28:20 19:15 14:10 9:5 4:0 15:8 31 30 29 29 28:24 23:19 18 17 16:12 11:7 4 3:0	0.000005221 0.220033000 0.00010000	machine C. The first half of the register bits air et ne reserved ones with the 18, 19 bits rese Current instruction shares of states machine. On the rist for bits are reserved to the thin Characteristic control of the control of	0x0000010 tx 0x00006221 0x20003000 0x20003000	Current instruction address of sta Resaft to see their instruction current State machine gin control Clock divisor register for states ma Transparring or clock fleet (CLASIA)	ate machine 0 milly addressed by st achine 1 V_INT + CLKDIV_FF	ate machine0's pr	rogram counterW	ritle to execute an i	instruction immedi	ately (including jumps)a	and then resume execution	ion.						
SM0_ADDR SM0_INSTR SM0_PINCTRL SM1_CLKDIV	502000ds 502000dc 50200e0	0x0d8 0x0dc 0x0e0	Current instruction address of state mac SIDESET_COUNT OUT_COUNT No N	15:0 31:29 28:26 28:26 28:20 19:15 14:10 9:5 4:0 15:8 31 30 29 28:24 23:19 18 17 16:12	0.000005221 0.220033000 0.00010000	machine C. The first half of the register bits air et ne reserved ones with the 18, 19 bits rese Current instruction shares of states machine. On the rist for bits are reserved to the thin Characteristic control of the control of	0x0000010 tx 0x00006221 0x20003000 0x20003000	Current instruction address of sta Resaft to see their instruction current State machine gin control Clock divisor register for states ma Transparring or clock fleet (CLASIA)	ate machine 0 milly addressed by st achine 1 V_INT + CLKDIV_FF	ate machine0's pr	rogram counterW	frite to execute an is	instruction immedi	aately (including jumps)a	and then resume execution	on.						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_CLKDIV	50200048 502000dc 50200e0 50200e4	0x0d8 0x0dc 0x0e0	Current instruction address of state mac  SIDESET_COUNT SET_COUNT SET_COUNT NOT SET_CO	15:0 31:26 28:26 28:26 28:26 28:26 28:20 19:15 14:10 9:5 4:0 15:8 31 30 29 29 28:24 23:19 18 17 16:12 11:7 4 3:0	0x00006521 0x20003000 0x00010000	machine C. The first half of the register bits aire the reserved ones with the 18, 19 bits rese Current instruction. On the first for this received to the high control of the control of the reserved.  Rad to see the instruction currently addressed by state machine's program counterWrite.  State machine pin control O. Since only the 26 to 28 bits are offset to 0x55(101)  Clock divisor register for state machine 1  Frequency = clock freq? (CLKDIV_BT + CLKDIV_FRAC / 286)  Execution/behavioural settings for state machine 1	0x0000010 to 0x00008221 0x20003000 0x00010000 0x0001f000	Current instruction address of state Read to see the instruction current State machine pin control Clock dwisor register for state ma- Frequency – clock freq / (CL/KSh.  Execution behavioural settings for	ate machine 0  atemathre 0  atemathre 0  atemathre 1  achine 1  y_INT + CLKDIV_FF	ate machine0's pr		frite to execute an ia	instruction immedi	ately (including jumps)a	and then resume execution	ion.						
SM0_ADDR SM0_INSTR  SM0_INSTR  SM1_CLKDIV  SM1_CLKDIV  SM1_EXECCTRL	50200048  5020004  50200e4	0x048 0x046 0x0e0 0x0e4 0x0e4	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT No.	15:0 31:29 28:28 28:28 28:28 28:28 19:15 14:10 18:40 31:18	0±00006921  0±00000000  0±00010000  0±00010000	machine C. The first half of the register bits air et ne reserved ones with the 18, 19 bits rese Current instruction based of state machine. On the rist for bits needs to 0 with the Comment of the comment of the co	0x0000010 0x00000021 0x20003000 0x00010000 0x00016000 0x000060000	Current instruction address of state Resaft to see the instruction current State matchine pin control Clock division register for other ma Frequency is clock free / (CLKDN  Execution-behavioural settings for	ate machine 0 mity addressed by st addressed b	ate machine0's pr		frite to execute an is	instruction immedi	ately (including jumps)a	ind then resume executi	on.						
SM0_ADDR SM0_INSTR SM0_INSTR SM0_INSTR SM0_PINCTRL SM1_CLKDIV SM1_EXECCTRL SM1_SM6FTCTRL SM1_ADDR	50200048 502000dc 50200e0 50200e4	0x0d8 0x0dc 0x0e0	Current instruction address of state mac  SIDESET_COUNT SET_COUNT SET_COUNT NOT SET_CO	15:0 31:29 28:28 28:28 28:28 28:28 19:15 14:10 18:40 31:18	0x00000000 0x00010000 0x00010000 0x00010000 0x00010000	machine C. The first half of the register bits aire the reserved ones with the 18, 19 bits rese Current instruction. On the first for this received to with the 18 bits reserved.  Rad to see the instruction currently addressed by state machine's program counterWrite.  State machine pin control O. Since only the 26 to 28 bits are offset to 0x55(101)  Clock divisor register for state machine 1  Frequency = chock freq / (CLKDIV_INT + CLKDIV_FRAC / 286)  Execution/behavioural settings for state machine 1  Control behaviour of the inputiouply shift registers for state machine 1  Control behaviour of the inputiouply shift registers for state machine 1  Current instruction address of state machine 1	0x0000010 0x00000000 0x00010000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of stall Read for see their instruction current State machine pin control Clock divisor register for state ma Frequency's clock free? (CLRDIN Execution/behavioural settings to Control behaviour of the inpution.	ate machine 0 mity addressed by st addressed by st actions 1 v_mt + CLKDIV_Fs or state machine 1 steps shift registers for ste machine 1	ate machine's p			instruction immedia	ately (including jumps)	and then resume execution	on.						
SM0_ADDR SM0_INSTR  SM0_INSTR  SM1_CLKDIV  SM1_CLKDIV  SM1_EXECCTRL	50200048  5020004  50200e4	0x048 0x046 0x0e0 0x0e4 0x0e4	Current instruction address of state mac  SIGESET_COUNT OUT_COUNT HIS BURGET HASE OUT_GASE OU	15:0 31:29 28:28 28:28 28:28 28:28 19:16 19:16 19:16 19:16 19:18 30 30 20:29:28 20:29:29 11:17 11:7 30 30 30 30 30 30 30 31 31 31 31 30 30 30 30 30 30 30 31 31 31 30 30 30 30 30 30 30 30 30 31 31 31 30 30 30 30 30 30 30 30 30 30 30 30 30	0±00006921  0±00000000  0±00010000  0±00010000	machine C. The first half of the register bits air et ne reserved ones with the 18, 19 bits rese Current instruction based of state machine. On the rist for bits needs to 0 with the Comment of the comment of the co	0x0000010 0x00000021 0x20003000 0x00010000 0x00016000 0x000060000	Current instruction address of state Resaft to see the instruction current State matchine pin control Clock division register for other ma Frequency is clock free / (CLKDN  Execution-behavioural settings for	ate machine 0 mity addressed by st addressed by st actions 1 v_mt + CLKDIV_Fs or state machine 1 steps shift registers for ste machine 1	ate machine's p			instruction immedia	ately (including jumps)a	and then resume execution	on.						
SM0_ADDR SM0_INSTR SM0_INSTR SM0_INSTR SM0_PINCTRL SM1_CLKDIV SM1_EXECCTRL SM1_SM6FTCTRL SM1_ADDR	50200048 5020004c 50200e0	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac.  SIDESET_COUNT SET_COUNT SET_COUNT No. DATE of the count of the cou	15:0 31:29 28:28 28:28 28:28 28:28 19:16 19:16 19:16 19:16 19:18 30 30 20:29:28 20:29:29 11:17 11:7 30 30 30 30 30 30 30 31 31 31 31 30 30 30 30 30 30 30 31 31 31 30 30 30 30 30 30 30 30 30 31 31 31 30 30 30 30 30 30 30 30 30 30 30 30 30	0x00000000 0x00010000 0x00010000 0x00010000 0x00010000	machine C. The first half of the register bits air et ne reserved ones with the 18, 19 bits rese Current instruction acrossed of state machine. On the rist for bits are reset to 0 with the Country of the control of the reset	0x0000010 0x00000000 0x00010000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of stall Read for see their instruction current State machine pin control Clock divisor register for state ma Frequency's clock free? (CLRDIN Execution/behavioural settings to Control behaviour of the inpution.	ate machine 0 mity addressed by st addressed by st actions 1 v_mt + CLKDIV_Fs or state machine 1 steps shift registers for ste machine 1	ate machine's p			instruction immedia	ately (including jumps)a	ind then resume executed	on.						
SM0_ADDR SM0_INSTR SM0_INSTR SM0_INSTR SM0_PINCTRL SM1_CLKDIV SM1_EXECCTRL SM1_SM6FTCTRL SM1_ADDR	50200048 5020004c 50200e0	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT No.	15:0 31:29 28:28 28:28 28:28 28:28 19:16 19:16 19:16 19:16 19:18 30 30 20:29:28 20:29:29 11:17 11:7 30 30 30 30 30 30 30 31 31 31 31 30 30 30 30 30 30 30 31 31 31 30 30 30 30 30 30 30 30 30 31 31 31 30 30 30 30 30 30 30 30 30 30 30 30 30	0x00000000 0x00010000 0x00010000 0x00010000 0x00010000	machine C. The first half of the register bits air et ne reserved ones with the 18, 19 bits rese Current instruction acrossed of state machine. On the rist for bits are reset to 0 with the Country of the control of the reset	0x0000010 0x00000000 0x00010000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of stall Read for see their instruction current State machine pin control Clock divisor register for state ma Frequency's clock free? (CLRDIN Execution/behavioural settings to Control behaviour of the inpution.	ate machine 0 mity addressed by st addressed by st actions 1 v_mt + CLKDIV_Fs or state machine 1 steps shift registers for ste machine 1	ate machine's p			instruction immedia	ately (including jumps)a	and then resume execution	ion.						
SM0_ADDR SM0_INSTR SM0_INSTR SM0_INSTR SM0_PINCTRL SM1_CLKDIV SM1_EXECCTRL SM1_SM6FTCTRL SM1_ADDR	50200048 5020004c 50200e0	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Curret instruction address of state mac  SIDESET_COUNT OUT_COUNT No. TO STATE TO STATE TO STATE NO. TO STATE TO STATE NO.	1500 3129 2826 2826 2826 2826 2826 2826 2826 28	0x00000000 0x00010000 0x00010000 0x00010000 0x00010000	machine C. The first half of the register bits air et ne reserved ones with the 18, 19 bits rese Current instruction acrossed of state machine. On the rist for bits are reset to 0 with the Country of the control of the reset	0x0000010 0x00000000 0x00010000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of stall Read for see their instruction current State machine pin control Clock divisor register for state ma Frequency's clock free? (CLRDIN Execution/behavioural settings to Control behaviour of the inpution.	ate machine 0 mity addressed by st addressed by st actions 1 v_mt + CLKDIV_Fs or state machine 1 steps shift registers for ste machine 1	ate machine's p			instruction immedia	ately (including jumps)e	ind then resume executed	on.						
SMO_ADDR SMO_INSTR  SMO_PINCTRL SM1_CLKDIV  SM1_EXECCTRL SM1_SHIFTCTRL SM1_ADDR SM1_INSTR	50200048 5020004c 5020004 5020004 5020004 5020006 5020006 5020006	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT OUT_COUNT NOT	15:0 31:29 28:28 28:28 28:28 28:28 19:15 14:10 18:40 31:18	0.20003000 0.20003000 0.00010000 0.00010000 0.00001000 0.00000000 0.00000000	machine C. The first half of the register bits air ethe reserved ones with the 18, 19 bits rese Courter stansiction shades of states machine. On the relation bits an exceeded to with the Courter stansiction states of the state of the sta	0x0000010 0x00000000 0x00010000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of stall Read to see the instruction current State machine pin control Clock divisor register for state ma Frequency in clock free / (CLKDN, Control technologies) of the impution Current instruction address of state Control technologies of the impution Current instruction address of state Need to see the instruction in Need to see t	ate machine 0 mity addressed by st addressed by st actions 1 v_mt + CLKDIV_Fs or state machine 1 steps shift registers for ste machine 1	ate machine's p			instruction immedia	ately (including jumps)a	and then resume execution	ion.						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL SM1_SHIFTCTRL SM1_ADDR SM1_INSTR	50200048 5020004c 50200e0	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Curret instruction address of state mac  SIDESET_COUNT OUT_COUNT No. TO STATE TO STATE TO STATE NO. TO STATE TO STATE NO.	15:0 31:29 20:20 2	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C. The first half of the register bits air ethe reserved ones with the 18, 19 bits rese (correct instruction abused of sitter machine.) The first four bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite Read to see the instruction currently addressed by state machine's program counterWrite State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101) Clock divisor register for state machine 1 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256) Execution/behavioural settings for state machine 1 Control behaviour of the inputiously shift registers for state machine 1 Current instruction address of state machine 1 State machine pin control	0x00000010 to 0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of state Read to see the instruction current State machine pin control Clock divisor register for state may Prequency in clock free / (CLXCI).  Execution/behavioural settings for Control behaviour of the impulsor Current instruction address of state Read to see the instruction current White to resecuting an instruction in	ate machine 0  softensed by st  actine 1  softensed by st  softensed by st	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			instruction immedi	ately (including jumps)e	ind then resume executed	ion.						
SMO_ADDR SMO_INSTR  SMO_PINCTRL SM1_CLKDIV  SM1_EXECCTRL SM1_SHIFTCTRL SM1_ADDR SM1_INSTR	50200048 5020004c 5020004 5020004 5020004 5020006 5020006 5020006	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT	1500 3129 2826 2826 2826 2826 2826 2826 2826 28	0.20003000 0.20003000 0.00010000 0.00010000 0.00001000 0.00000000 0.00000000	machine C. The first half of the register bits air ethe reserved ones with the 18, 19 bits rese Courter stansiction shades of states machine. On the relation bits an exceeded to with the Courter stansiction states of the state of the sta	0x00000010 to(0x00000010 to(0x00000000000000000000000000000000000	Current instruction address of state Resal to see the instruction current State matchine pin control Cook divisor register for other ma Frequency w clock fires / (CLKON  Execution-behavioural settings for Control behavioural settings for Control techniques of the imputious Current instruction address of state White for executing an instruction current White for executing an instruction in State matchine pin control Cook divisors register for state ma	ate machine 0  softensed by st  actine 1  softensed by st  softensed by st	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			instruction immedi	ately (including jumps)a	md then resume execution	ion.						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL SM1_SHIFTCTRL SM1_ADDR SM1_INSTR	50200048  5020004  5020004  5020008  5020006  5020006  5020006  5020010	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT	15:0 31:29 20:20 2	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C. The first half of the register bits air ethe reserved ones with the 18, 19 bits rese (correct instruction abused of sitter machine.) The first four bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite Read to see the instruction currently addressed by state machine's program counterWrite State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101) Clock divisor register for state machine 1 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256) Execution/behavioural settings for state machine 1 Control behaviour of the inputiously shift registers for state machine 1 Current instruction address of state machine 1 State machine pin control	0x00000010 to 0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of state Read to see the instruction current State machine pin control Clock divisor register for state may Prequency in clock free / (CLXCI).  Execution/behavioural settings for Control behaviour of the impulsor Current instruction address of state Read to see the instruction current White to resecuting an instruction in	ate machine 0  softensed by st  actine 1  softensed by st  softensed by st	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			matruction immedi	ately (including Jumps)	and then resume executed the second s	ion.						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL SM1_SHIFTCTRL SM1_ADDR SM1_INSTR	50200048  5020004  5020004  5020008  5020006  5020006  5020006  5020010	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT	15:0 31:29 20:20 2	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C. The first half of the register bits air ethe reserved ones with the 18, 19 bits rese (correct instruction abused of sitter machine.) The first four bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite Read to see the instruction currently addressed by state machine's program counterWrite State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101) Clock divisor register for state machine 1 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256) Execution/behavioural settings for state machine 1 Control behaviour of the inputiously shift registers for state machine 1 Current instruction address of state machine 1 State machine pin control	0x00000010 to 0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of state Read to see the instruction current State machine pin control Clock divisor register for state may Prequency in clock free / (CLXCI).  Execution/behavioural settings for Control behaviour of the impulsor Current instruction address of state Read to see the instruction current White to resecuting an instruction in	ate machine 0  softensed by st  actine 1  softensed by st  softensed by st	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			instruction immedi	ately (including jumps)a	md then resume execution	ion.						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL SM1_SHIFTCTRL SM1_ADDR SM1_INSTR	50200048  5020004  5020004  5020008  5020006  5020006  5020006  5020010	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT SUPPLIES S	15:0 31:29 20:20 2	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C. The first half of the register bits air ethe reserved ones with the 18, 19 bits rese (correct instruction abused of sitter machine.) The first four bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite Read to see the instruction currently addressed by state machine's program counterWrite State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101) Clock divisor register for state machine 1 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256) Execution/behavioural settings for state machine 1 Control behaviour of the inputiously shift registers for state machine 1 Current instruction address of state machine 1 State machine pin control	0x00000010 to 0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of state Read to see the instruction current State machine pin control Clock divisor register for state may Prequency in clock free / (CLXCI).  Execution/behavioural settings for Control behaviour of the impulsor Current instruction address of state Read to see the instruction current White to resecuting an instruction in	ate machine 0  softensed by st  actine 1  softensed by st  softensed by st	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			restruction immedi	ately (including jumps)a	and then resume execution	on.						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL SM1_SHIFTCTRL SM1_ADDR SM1_INSTR	50200048  5020004  5020004  5020008  5020006  5020006  5020006  5020010	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	COUNT AND COUNT SUPPLY OF THE COUNT SUPPLY	1500 31226 28260 19161 1	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C. The first half of the register bits air ethe reserved ones with the 18, 19 bits rese (correct instruction abused of sitter machine.) The first four bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite Read to see the instruction currently addressed by state machine's program counterWrite State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101) Clock divisor register for state machine 1 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256) Execution/behavioural settings for state machine 1 Control behaviour of the inputiously shift registers for state machine 1 Current instruction address of state machine 1 State machine pin control	0x00000010 to 0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of state Read to see the instruction current State machine pin control Clock divisor register for state may Prequency in clock free / (CLXCI).  Execution/behavioural settings for Control behaviour of the impulsor Current instruction address of state Read to see the instruction current White to resecuting an instruction in	ate machine 0  softensed by st  actine 1  softensed by st  softensed by st	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			instruction immedi	ately (including jumps)a	and then resume execution	ion.						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL SM1_SHIFTCTRL SM1_ADDR SM1_INSTR	50200048  5020004  5020004  5020008  5020006  5020006  5020006  5020010	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT IN BUSINESS NOT STATE ASSESS  SET_BASE  OUT_ENSTERMENT AMP_PIN OUT_ENSTERMENT SERVER SET_FAME SEE_COUNT SET_FAME SET_FAME SEE_COUNT SE	1500 31226 28260 19161 1	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C. The first half of the register bits air ethe reserved ones with the 18, 19 bits rese (correct instruction abused of sitter machine.) The first four bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite Read to see the instruction currently addressed by state machine's program counterWrite State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101) Clock divisor register for state machine 1 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256) Execution/behavioural settings for state machine 1 Control behaviour of the inputiously shift registers for state machine 1 Current instruction address of state machine 1 State machine pin control	0x00000010 to 0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of state Read to see the instruction current State machine pin control Clock divisor register for state may Prequency in clock free / (CLXCI).  Execution/behavioural settings for Control behaviour of the impulsor Current instruction address of state Read to see the instruction current Write to resecuting an instruction in	ate machine 0  softensed by st  actine 1  softensed by st  softensed by st	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			restruction immedi	ately (including jumps)a	and then resume execution	on.						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL  SM1_SM1FTCTRL SM1_RSTR  SM1_PINCTRL  SM2_CLKDIV	5020048  5020046  502004  502004  5020068  5020068  5020068  5020064	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT OUT_COUNT No. SIDESET_COUNT OUT_COUNT No. SIDESET_COUNT OUT_COUNT NO. SIDESET_SASE OUT_SASE OUT_SASE OUT_SASE OUT_SASE NO. SIDESET_SASE OUT_SASE NO. SIDESET_COUNT SIDES	15:0 31:29 20:20 2	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C . The first half of the register bits air et he reserved ones with the 18, 19 bits rese Current instruction actives of state machine. On the rist for bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite.  State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101)  Clock divisor register for state machine 1  Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)  Execution/behavioural settings for state machine 1  Current instruction address of state machine 1  State machine pin control  State machine pin control  State machine pin control  Clock divisor register for state machine 2  Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00000010 0x00000000 0x00000000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000	Current instruction address of stall Read for see their instruction current State machine pin control Clock divisor register for state mar Frequency in clock free / (CLKDI). Execution behaviour of the impulsion Control behaviour of the impulsion Current instruction address of stall Read to see the instruction current Writes for security an instruction in State machine pin control Clock divisor register for state mar Frequency in clock free / (CLKDI).	ate machine 0 bit of mitty addressed by st add	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			instruction immedi	ately (including jumps)a	and then resume execution	ion.						
SM0_ADDR SM0_INSTR  SM0_INSTR  SM0_INSTR  SM1_CAXDIV  SM1_EXECCTIR.  SM1_EXECCTIR.  SM1_EXECCTIR.  SM1_EXECCTIR.  SM1_EXECCTIR.  SM1_EXECCTIR.  SM1_EXECCTIR.  SM1_EXECCTIR.  SM1_EXECCTIR.  SM2_CAXDIV	50200048  5020004  5020004  5020008  5020006  5020006  5020006  5020010	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT	1500 31226 28260 19161 1	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C. The first half of the register bits air ethe reserved ones with the 18, 19 bits rese (correct instruction abused of sitter machine.) The first four bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite Read to see the instruction currently addressed by state machine's program counterWrite State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101) Clock divisor register for state machine 1 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256) Execution/behavioural settings for state machine 1 Control behaviour of the inputiously shift registers for state machine 1 Current instruction address of state machine 1 State machine pin control	0x00000010 to 0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	Current instruction address of state Read to see the instruction current State machine pin control Clock divisor register for state may Prequency in clock free / (CLXCI).  Execution/behavioural settings for Control behaviour of the impulsor Current instruction address of state Read to see the instruction current Write to resecuting an instruction in	ate machine 0 bit of mitty addressed by st add	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			restruction immedi	ately (including jumps)a	and then resume execution	on.						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL  SM1_SM1FTCTRL SM1_RSTR  SM1_PINCTRL  SM2_CLKDIV	5020048  5020046  502004  502004  5020068  5020068  5020068  5020064	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT	1500 31262 28260 19161 1	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C . The first half of the register bits air et he reserved ones with the 18, 19 bits rese Current instruction actives of state machine. On the rist for bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite.  State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101)  Clock divisor register for state machine 1  Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)  Execution/behavioural settings for state machine 1  Current instruction address of state machine 1  State machine pin control  State machine pin control  State machine pin control  Clock divisor register for state machine 2  Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00000010 0x00000000 0x00000000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000	Current instruction address of stall Read for see their instruction current State machine pin control Clock divisor register for state mar Frequency in clock free / (CLKDI). Execution behaviour of the impulsion Control behaviour of the impulsion Current instruction address of stall Read to see the instruction current Writes for security an instruction in State machine pin control Clock divisor register for state mar Frequency in clock free / (CLKDI).	ate machine 0 bit of mitty addressed by st add	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			instruction immedi	ately (including jumps)a	and then resume executed the second sec	ion.						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL  SM1_SM1FTCTRL SM1_RSTR  SM1_PINCTRL  SM2_CLKDIV	5020048  5020046  502004  502004  5020068  5020068  5020068  5020064	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT	1500 31226 28260 19161 1	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C . The first half of the register bits air et he reserved ones with the 18, 19 bits rese Current instruction actives of state machine. On the rist for bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite.  State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101)  Clock divisor register for state machine 1  Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)  Execution/behavioural settings for state machine 1  Current instruction address of state machine 1  State machine pin control  State machine pin control  State machine pin control  Clock divisor register for state machine 2  Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00000010 0x00000000 0x00000000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000	Current instruction address of stall Read for see their instruction current State machine pin control Clock divisor register for state mar Frequency in clock free / (CLKDI). Execution behaviour of the impulsion Control behaviour of the impulsion Current instruction address of stall Read to see the instruction current Writes for security an instruction in State machine pin control Clock divisor register for state mar Frequency in clock free / (CLKDI).	ate machine 0 bit of mitty addressed by st add	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			instruction immedi	ately (including jumps)a	and then resume execution	in the second se						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL  SM1_SM1FTCTRL SM1_RSTR  SM1_PINCTRL  SM2_CLKDIV	5020048  5020046  502004  502004  5020068  5020068  5020068  5020064	0x048 0x046 0x0e0 0x0e4 0x0e4 0x0e8 0x0ec	Current instruction address of state mac  SIDESET_COUNT OUT_COUNT	1500 31292 20200 11915 1	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C . The first half of the register bits air et he reserved ones with the 18, 19 bits rese Current instruction actives of state machine. On the rist for bits are reserved to the with the Read to see the instruction currently addressed by state machine's program counterWrite.  State machine pin control O. Since only the 26 to 28 bits are offset to 0x5(101)  Clock divisor register for state machine 1  Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)  Execution/behavioural settings for state machine 1  Current instruction address of state machine 1  State machine pin control  State machine pin control  State machine pin control  Clock divisor register for state machine 2  Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00000010 0x00000000 0x00000000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000 0x0001000	Current instruction address of stall Read for see their instruction current State machine pin control Clock divisor register for state mar Frequency in clock free / (CLKDI). Execution behaviour of the impulsion Control behaviour of the impulsion Current instruction address of stall Read to see the instruction current Writes for security an instruction in State machine pin control Clock divisor register for state mar Frequency in clock free / (CLKDI).	ate machine 0 bit of mitty addressed by st add	ate machine0's put  (AC / 256)  r state machine 1's pate to put  pumps) and then			instruction immedi	ately (including jumps) a	and then resume executed the second se	ion.						
SM0_ADDR SM0_NSTR  SM0_PINCTPL SM1_CLKDIV  SM1_EXECCTRL  SM1_SNETCTRL SM1_NSTR  SM1_PINCTRL  SM2_CLKDIV  SM2_EXECCTRL	5020048  5020040  502004  502004  5020060  5020068  5020064  5020064  5020064  5020064	0x0e6 0x0e0 0x0e4 0x0e8 0x0e0 0x0e0 0x0e8 0x0e0 0x0f0 0x0f4	Current instruction address of state mac  SIGESET COUNT OUT COUNT	1500 31292 20200 11915 1	0.20003000  0.20003000  0.00010000  0.00010000  0.000010000  0.00000000	machine C. The first half of the register bits are the reserved ones with the 18, 19 bits rese Cornett instruction ables of state machine. On the rist for bits are reset to 0 with the 18 bits reset of the control of	0x00000010 0x00000221 0x00000000 0x00010000 0x00010000 0x00010000 0x00010000 0x00010000	Current instruction address of stall Read for see their instruction current State machine pin control Clock divisor register for state ma Frequency in clock free? (CLKDIN Control behavioural settings for Control behavioural settings for Control behavioural settings for Control behavioural settings for Control behaviour of the happidous Control behaviour of the happidous Contro	ate machine 0  intly addressed by st  achine 1  v_INT + CLKDIV_FF  containe 1  v_INT + CLKDIV_FF  intly addressed by st  intly addressed by st  containe 2  v_INT + CLKDIV_FF  achine 2  v_INT + CLKDIV_FF  achine 2  v_INT + CLKDIV_FF  containe 3  containe cont	ate machine0's p  r state machine 1 ste machine 1 s p  jumps) and then	) XIOgram counter resume executio		instruction immedi	ately (including jumps)a	and then resume execution	in the second se						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL SM1_ADDR SM1_NSTR  SM1_PINCTRL SM2_CLKDIV  SM2_EXECCTRL	5020048  5020046  502004  502006  502006  502006  502006  502006  502006  502006	0x046 0x046 0x046 0x046 0x066 0x066 0x066 0x066 0x066 0x066 0x066 0x066	Current instruction address of state mac  SIDESET_COUNT  SIDESET_COUNT OUT_COUNT IN BUSINESS  NOT SANSE  OUT_BASE  OUT_BASE  IN I	1500 31202 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 2	0x00006021 0x20003000 0x30010000 0x30010000 0x30010000 0x30000000 0x30000000 0x300000000 0x300000000	machine C. The first half of the register bits are the reserved ones with the 18, 19 bits rese Current instruction acreed of older that half of the received of which the control of the control of the received of the three of the control of the received of the three of the control of the received of the control of the received of the control of the c	0x00000010 0x00000221 0x00000221 0x00000020 0x00010000 0x00010000 0x00010000 0x00010000 0x00010000 0x00010000	Current instruction address of stall Read for see their instruction current State machine pin control Clock divisor register for state may Proquency in clock free / (CLKD). Execution/behavioural settings for Control behaviour of the impulsion Current instruction address of stall Read to see the instruction current White to rescute an instruction in Trequency in clock free / (CLKD). State machine pin control Clock divisor register for state properties of the pin control Clock divisor register for state properties of clock free / (CLKD). Execution/behavioural settings for Execution/behavioural settings for Control behaviour of the impulsion.	ate machine 0 intly addressed by st  toput  toput  shift registers for  the machine 1 intly addressed by st	ate machine0's p  r state machine 1 ste machine 1 s p  jumps) and then	) XIOgram counter resume executio		instruction immedi	ately (including jumps) a	and then resume executed	ion.						
SM0_ADDR SM0_NSTR  SM0_PINCTRL SM1_CLXDV  SM1_EXECCTRL SM1_ADDR SM1_PINCTRL SM2_CLXDV  SM2_EXECCTRL  SM2_EXECCTRL SM2_EXECCTRL SM2_EXECCTRL	5020048  5020046  502004  5020068  5020068  5020068  5020068  5020068  5020066  5020066	0x046 0x0e8 0x0e8 0x0e8 0x0e8 0x0e8 0x0f0 0x0f4 0x0f6	Current instruction address of state mac  SIGESET COUNT OUT COUNT	1500 31202 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 2	0x00000000 0x00010000 0x00010000 0x00010000 0x00000000	machine C. The first half of the register bits aire the reserved ones with the 18, 19 bits rese Current instruction ablessed sidster machine. On the rist for bits are reset to 0 with the 18 per control of the research of t	0-00000010 0-00000221 0-00000000 0-000010000 0-000010000 0-000010000 0-00000000	Current instruction address of stall Read for see their instruction address of stall Read for see their instruction current and the seed of the seed o	alter machine 0  achine 1  v_NT + CLKDIV_FE  achine 1  v_NT + CLKDIV_FE  achine 2  v_NT + CLKDIV_FE  achine 3  v_NT + CLKDIV_FE  achine 4  achin	ate machine0's p  r state machine 1 ste machine 1 is pampe) and then  LAC / 256)	nogram counter resume execution		instruction immedi	ately (including jumps)a	md then resume execution	in the second se						
SM0_ADDR SM0_INSTR  SM0_PINCTRL SM1_CLKDIV  SM1_EXECCTRL SM1_ADDR SM1_NSTR  SM1_PINCTRL SM2_CLKDIV  SM2_EXECCTRL	5020048  5020046  502004  502006  502006  502006  502006  502006  502006  502006	0x046 0x046 0x044 0x046 0x066 0x066 0x066 0x066 0x066 0x066 0x066 0x066	Current instruction address of state mac  SIDESET_COUNT  SIDESET_COUNT OUT_COUNT IN BUSINESS  NOT SANSE  OUT_BASE  OUT_BASE  IN I	1500 31202 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 10216 20200 2	0x00006021 0x20003000 0x30010000 0x30010000 0x30010000 0x30000000 0x30000000 0x300000000 0x300000000	machine C. The first half of the register bits are the reserved ones with the 18, 19 bits rese Current instruction acreed of older that half of the received of which the control of the control of the received of the three of the control of the received of the three of the control of the received of the control of the received of the control of the c	0-00000010 0-00000221 0-00000000 0-000010000 0-000010000 0-000010000 0-00000000	Current instruction address of stall Read for see their instruction address of stall Read for see their instruction current and the seed of the seed o	alter machine 0  achine 1  v_NT + CLKDIV_FE  achine 1  v_NT + CLKDIV_FE  achine 2  v_NT + CLKDIV_FE  achine 3  v_NT + CLKDIV_FE  achine 4  achin	ate machine0's p  r state machine 1 ste machine 1 is pampe) and then  LAC / 256)	nogram counter resume execution		instruction immedi	ately (including Jumps) is	and then resume executed	ion.						

				SIDESET_COUNT SET_COUNT OUT_COUNT	31:29				
				SET COUNT	28:26		1	l	
				OUT COUNT	25:20		1	l	
- 1				IN DACE	19:15		1	l	
- 1				IN BASE SIDESET BASE	14:10		1	l	
- 1				SIDESET_BASE	14:10		1	l	
- 1				SET_BASE	9:5		1	l	
SM2	PINCTRL	502010c	0x10c	OUT BASE	4:0	0x14000000	State machine pin control	0x14000000	State machine pin control
-				INT	31-16		Clock divisor register for state machine 3		
				FRAV		0x00010000	Clock divisor register for state machine 3		Clock divisor register for state machine 3 Frequency = clock fleet, (CLKDIV, INT - CLKDIV, FRAC / 256)
SM3	CLKDIV	5020110			15:8	0x00010000	Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00010000	Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)
				EXEC STALLED	31				
- 1				SIDE EN	30		1	l	
- 1				SIDE PINDIR	20		1	l	
- 1				JMP PIN	20		1	l	
- 1			1	JMP_PIN	28:24	I		I	
- 1				OUT_EN_SEL	23:19		1	l	
- 1				INLINE OUT EN	18		1	l	
- 1				OUT STICKY	17		1	l	
- 1				WRAP TOP	16:12		1	l .	
- 1				WPAP BOTTOM	11-7		I .	l	
- 1				CTATUE CEI	1,		I .	l	
			0x114	OUT EN SEL  INLINE OUT EN  OUT STICKY  WRAP TOP  WRAP BOTTOM  STATUS_SEL  STATUS_N	l* .	0x0001f000	L		
SM3	EXECCTRL	5020114	0x114	STATUS_N	3:0	0x00011000	Execution/behavioural settings for state machine 3	0x0001f000	Execution/behavioural settings for state machine 3
- 1				FJOIN_RX FJION_TX	31		I .	l	
- 1				E HON TY	30		1	l .	
- 1				PULL THRESH	29:25		1	l .	
- 1				PUSH THRESH	24:20		1	l .	
- 1				PUSH_IHRESH	24:20		I .	l	
- 1				OUT_SHIFTDIR IN SHIFTDIR	19		I .	l	
- 1				IN SHIFTDIR	18		I .	l	
- 1				AUTOPULL AUTOPUSH	17		I .	l	
SM3	SHIFTCTRL	5020118	0x118	AUTOPUSH	16	0x000c0000	Control behaviour of the input/output shift registers for state machine 3	0x000c0000	Control behaviour of the input/output shift registers for state machine 3
0110	ADDR	502011c	0x11c	Current instruction address of state mach	4.0	0×00000000	Current instruction address of state machine 3	0x00000000	Current instruction address of state machine 3
SM3	ADDR	502011C	UX11C	Current instruction address of state mach	4:0			UXUUUUUUUU	
- 1			1		I	I	Read to see the instruction currently addressed by state machine 3's program counter	I	Read to see the instruction currently addressed by state machine 3's program counter
SM3	INSTR	5020120	0x120		15:0	0x0000fcfe	Write to execute an instruction immediately (including jumps) and then resume execution.	0x00007df3	Write to execute an instruction immediately (including jumps) and then resume execution.
1000							, including jumps) and their results execution.		The state of the s
			1	SIDESET_COUNT	31:29	I		I	
			1	SET_COUNT	28:26 25:20	I		I	
			1	OUT_COUNT	25:20	I		I	
				IN BASE	19:15		I .	l	
- 1				SIDESET_COUNT SET_COUNT OUT_COUNT IN BASE SIDESET_BASE	14:10		I .	l	
			1	SET BASE	0.5	I		I	
leun	PINCTRL	E020124	0x124	OUT BASE	4.0	0x14000000	State machine pin control	0-14000000	State machine pin control
SM3	_ FIIVO ( KL	0020124	UX 124	OUI_BAGE	4.0	0X 14000000	plate macinie pin control	UX 14000000	osate madrine pin control