	ADDRESS	OFFSET	NAME	Bits	VALUE	notes	SET 0X0000FF	PS
BASE	0x50200000		PIO0			PIO1 address: 0x50300000		PIO1 address: 0x50300000
			CLKDIV_RESTART	11:8				
			SM_RESRART	7:4		PIO control register. SM_ENABLE, SM_RESTART and CLKDIV_RESTART is rest to 0x0.		
CTRL	50200000	0x000	SM_ENABLE	3:0	0x00000001	'-' denotes the reserved value where we cannot find the detail values.		PIO control register
			TXEMPTY	27:24				
			TXFULL	19:16		FIFO status register. The first four bits of RXFULL and TXFULL are 0 after the rest with		
			RXEMPTY	11:8		the following four bits of them being reserved one. Additionally, the first four bits of		
FSTAT	50200004	0x00000004	RXFULL	3:0	0x0f000f01	RXEMPTY and TXEMPTY are 1 with the rest of bits being reserved one.	0x0f000f01	FIFO status register = pio_fifo_join
			TXSTALL	27:24				
			TXOVER	19:16				
			RXUNDER	11:8		FIFO debug register. The first four bits to be RXSTALL, RXUNDER and TXOVER and		
FDEBUG	50200008	0x00000008	RXSTALL	3:0	0x00000000	TXSTALL are all 0 after resetting, the rest of bitsare being reserved ones.	0x01000e00	FIFO debug register
			RX3	31:28				
			TX3	27:24				
			RX2	23:20				
			TX2	19:16				
			RX1	15:12				
			TX1	11:8				
			RX0	7:4				
FLEVEL	5020000c	0x0000000c	TX0	3:0	0x00000000	FIFO levels All of bits of this register is resetted to 0 after the offsetting, no reserved bits for t	0x00000000	FIFO levels
						Direct write access to the TX FIFO for this state machine. Each		
						write pushes one word to the FIFO. Attempting to write to a full		
						FIFO has no effect on the FIFO state or contents, and sets the		
						sticky FDEBUG_TXOVER error flag for this FIFO. All of bits of this register is rested to 0		
						after the offsetting and there is no reserved bits in the register, additionally, there are no		
TXF0	50200010	0x00000010	TXF0	31:0	0x00000000	message being printed out.	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the FIFO. Attempting to write to a fullFIFO has no effect on the FIFO state or contents, and sets thesticky FDEBUG_TXOVER error flag for this FIFO.
TXF1	50200014	0x00000014	TXF1	31:0	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the FIFO. Attempting to write to a fullFIFO has no effect on the FIFO state or contents, and sets thesticky FDEBUG_TXOVER error flag for this FIFO.
TXF2	50200018	0x00000018	TXF2	31:0	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the FIFO. Attempting to write to a fullFIFO has no effect on the FIFO state or contents, and sets thesticky FDEBUG_TXOVER error flag for this FIFO.
TXF3	5020001c	0x0000001c	TXF3	31:0	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the	0x00000000	Direct write access to the TX FIFO for this state machine. Eachwrite pushes one word to the FIFO. Attempting to write to a fullFIFO has no effect on the FIFO state or contents, and sets thesticky FDEBUG_TXOVER error flag for this FIFO.
						Direct read access to the RX FIFO for this state machine. Each		
						read pops one word from the FIFO. Attempting to read from an		
						empty FIFO has no effect on the FIFO state, and sets the sticky		
						FDEBUG_RXUNDER error flag for this FIFO. The data returned to		
						the system on a read from an empty FIFO is undefined. The rule for setting the value is		
RXF0	50200020	0x00000020	RXF0	31:0	0x963f69b2	basically the same as TXFn	0x14fea89d	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the FIFO. Attempting to read from anempty FIFO has no effect on the FIFO state, and sets the stickyFDEBUG_RXUNDER error flag for this FIFO. The data returned tothe system on a read from an empty FIFO is undefined.
RXF1	50200024	0x00000024	RXF1	31:0	0x245a3d99	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the	0x0db36757	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the FIFO. Attempting to read from anempty FIFO has no effect on the FIFO state, and sets the stickyFDEBUG_RXUNDER error flag for this FIFO. The data returned tothe system on a read from an empty FIFO is undefined.
RXF2	50200028	0x00000028	RXF2	31:0	0xadf83d99	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the	0xb3060127	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the FIFO. Attempting to read from anempty FIFO has no effect on the FIFO state, and sets the stickyFDEBUG_RXUNDER error flag for this FIFO. The data returned tothe system on a read from an empty FIFO is undefined.
RXF3	5020002c	0x0000002c	RXF3	31:0	0xa8fc7caf	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the	0xb8250d8e	Direct read access to the RX FIFO for this state machine. Eachread pops one word from the FIFO. Attempting to read from anempty FIFO has no effect on the FIFO state, and sets the stickyFDEBUG_RXUNDER error flag for this FIFO. The data returned tothe system on a read from an empty FIFO is undefined.
						Write-only access to instruction memory location 0. The first half of this regisie is resetted		
INSTR_MEM0	50200030	0x00000030	Write-only access to instruction memory lo	15:0	0x00000000	to 0 with the second half being the reserved ones.	0x00000000	Write-only access to instruction memory location 0
INSTR_MEMn	50200030+4n	0x48+4n	Write-only access to instruction memory lo	15:0	0x00000000	Write-only access to instruction memory location n	0x00000000	Write-only access to instruction memory location n
INSTR_MEM31	502000c4	0x000000c4	Write-only access to instruction memory lo	15:0	0x00000000	Write-only access to instruction memory location 31	0x00000000	Write-only access to instruction memory location 31
						Clock divisor register for state machine n. Frequency = clock freq / (CLKDIV_INT +		
			INT	31:16		CLKDIV_FRAC / 256). The first 8 bits are reserved ones with the FRAC is reseted to 0. The		
SM0_CLKDIV	50200c8	0x000000c8	FRAV	15:8	0x00fa0000	last 4 bits of the INT is reseted to vaue 1.	0x00fa0000	Clock divisor register for state machine n. Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)
			EXEC_STALLED	31				
			SIDE_EN	30				
			SIDE_PINDIR	29				
			JMP_PIN	28:24				
			OUT_EN_SEL	23:19				
			INLINE_OUT_EN	18				
			OUT_STICKY	17				
			WRAP_TOP	16:12				
			WRAP_BOTTOM	11:7				
			STATUS_SEL	4		Execution/behavioural settings for state machine n. The 5 to 6 bits are reserved ones and		
SM0_EXECCTRL	502000cc	0x0cc	STATUS_N	3:0	0x00017a00	the 12 to 16 bits are offset to 0x1f, the rest of the bits are being reseted to 0.	0x00013800	Execution/behavioural settings for state machine n
			FJOIN_RX	31				
			FJION_TX	30				
			PULL_THRESH	29:25				
			PUSH_THRESH	24:20				
			OUT_SHIFTDIR	19				
			IN_SHIFTDIR	18				
			AUTOPULL	17		Control behaviour of the input/output shift registers for state		
SM0_SHIFTCRTL	502000d0	0x0d0	AUTOPUSH	16	0x40060000	machine 0. The first half of the register' bits are the reserved ones with the 18, 19 bits reset t	0x40060000	Control behaviour of the input/output shift registers for statemachine 0
						Current instruction address of state machine 0. The first four bits are resetd to 0 with the		
SM0_ADDR	502000d4	0x0d4	Current instruction address of state mach	4:0	0x00000014	rest bits of it are reserved.	0x00000010	Current instruction address of state machine 0
SM0_INSTR	502000d8	0x0d8		15:0	0x00006221	Read to see the instruction currently addressed by state machine0's program counterWrite t	0x00006221	Read to see the instruction currently addressed by state machine0's program counterWrite to execute an instruction immediately (including jumps)and then resume execution.
			SIDESET_COUNT	31:29				
			SET_COUNT	28:26				
			OUT_COUNT	25:20				
			IN_BASE	19:15				
			SIDESET_BASE	14:10				
			SET_BASE	9:5				
SM0_PINCTRL	502000dc	0x0dc	OUT_BASE	4:0	0x20003000	State machine pin control 0. Since only the 26 to 28 bits are offset to 0x5(101)	0x20003000	State machine pin control
			INT	31:16		Clock divisor register for state machine 1		Clock divisor register for state machine 1
SM1_CLKDIV	50200e0	0x0e0	FRAV	15:8	0x00010000	Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00010000	Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)
			EXEC_STALLED	31				
			SIDE_EN	30				
			SIDE_PINDIR	29				
			JMP_PIN	28:24				
			OUT_EN_SEL	23:19				
			INLINE_OUT_EN	18				
			OUT_STICKY	17				
			WRAP_TOP	16:12				
			WRAP_BOTTOM	11:7				
			STATUS_SEL	4				
SM1_EXECCTRL	50200e4	0x0e4	STATUS_N	3:0	0x0001f000	Execution/behavioural settings for state machine 1	0x0001f000	Execution/behavioural settings for state machine 1
			FJOIN_RX	31				
			FJION_TX	30				
			PULL_THRESH	29:25				
			PUSH_THRESH	24:20				
			OUT_SHIFTDIR	19				
			IN_SHIFTDIR	18				
			AUTOPULL	17				
SM1_SHIFTCTRL	50200e8	0x0e8	AUTOPUSH	16	0x000c000	Control behaviour of the input/output shift registers for state machine 1	0x000c0000	Control behaviour of the input/output shift registers for state machine 1
SM1_ADDR	50200ec	0x0ec	Current instruction address of state mach	4:0	0x0000000	Current instruction address of state machine 1	0x0000000	Current instruction address of state machine 1
						Read to see the instruction currently addressed by state machine 1's program counter		Read to see the instruction currently addressed by state machine 1's program counter
SM1_INSTR	50200f0	0x0f0		15:0	0x0000fcfe	Write to execute an instruction immediately (including jumps) and then resume execution.	0x00007df3	Write to execute an instruction immediately (including jumps) and then resume execution.
			SIDESET_COUNT	31:29				
			SET_COUNT	28:26				
			OUT_COUNT	25:20				
			IN_BASE	19:15				
			SIDESET_BASE	14:10				
			SET_BASE	9:5				
SM1_PINCTRL	50200f4	0x0f4	OUT_BASE	4:0	0x00000000	State machine pin control	0x00000000	State machine pin control
			INT	31:16		Clock divisor register for state machine 2		Clock divisor register for state machine 2
SM2_CLKDIV	50200f8	0x0f8	FRAV	15:8	0x00010000	Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00010000	Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)
			EXEC_STALLED	31				
			SIDE_EN	30				
			SIDE_PINDIR	29				
			JMP_PIN	28:24				
			OUT_EN_SEL	23:19				
			INLINE_OUT_EN	18				
			OUT_STICKY	17				
			WRAP_TOP	16:12				
			WRAP_BOTTOM	11:7				
			STATUS_SEL	4				
SM2_EXECCTRL	50200fc	0x0fc	STATUS_N	3:0	0x0001f000	Execution/behavioural settings for state machine 2	0x0001f000	Execution/behavioural settings for state machine 2
			FJOIN_RX	31				
			FJION_TX	30				
			PULL_THRESH	29:25				
			PUSH_THRESH	24:20				
			OUT_SHIFTDIR	19				
			IN_SHIFTDIR	18				
			AUTOPULL	17				
SM2_SHIFTCTRL	5020100	0x100	AUTOPUSH	16	0x000c0000	Control behaviour of the input/output shift registers for state machine 2	0x000c0000	Control behaviour of the input/output shift registers for state machine 2
SM2_ADDR	5020104	0x104	Current instruction address of state mach	4:0	0x00000000	Current instruction address of state machine 2	0x00000000	Current instruction address of state machine 2
						Read to see the instruction currently addressed by state machine 2's program counter		Read to see the instruction currently addressed by state machine 2's program counter
SM2_INSTR	5020108	0x108		15:0	0x0000fcfe	Write to execute an instruction immediately (including jumps) and then resume execution.	0x00007df3	Write to execute an instruction immediately (including jumps) and then resume execution.

			SIDESET_COUNT SET_COUNT OUT_COUNT IN_BASE SIDESET_BASE SET_BASE	31:29 28:26 25:20 19:15 14:10 9:5				
SM2_PINCTRL	502010c	0x10c	OUT_BASE	4:0	0x14000000	State machine pin control	0x14000000	State machine pin control
SM3_CLKDIV	5020110	0x110	INT FRAV	31:16 15:8	0x00010000	Clock divisor register for state machine 3 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)	0x00010000	Clock divisor register for state machine 3 Frequency = clock freq / (CLKDIV_INT + CLKDIV_FRAC / 256)
SM3_EXECCTRL	5020114	0x114	EXEC_STALLED SIDE_EN SIDE_PINDIR JMP_PIN OUT_EN_SEL INLINE_OUT_EN OUT_STICKY WRAP_TOP WRAP_BOTTOM STATUS_SEL STATUS_N	31 30 29 28:24 23:19 18 17 16:12 11:7 4 3:0	0x0001f000	Execution/behavioural settings for state machine 3	0x0001f000	Execution/behavioural settings for state machine 3
SM3_SHIFTCTRL	5020118	0x118	FJOIN_RX FJOIN_TX PULL_THRESH PUSH_THRESH OUT_SHIFTDIR IN_SHIFTDIR AUTOPULL AUTOPUSH	31 30 29:25 24:20 19 18 17 16	0x000c0000	Control behaviour of the input/output shift registers for state machine 3	0x000c0000	Control behaviour of the input/output shift registers for state machine 3
SM3_ADDR	502011c	0x11c	Current instruction address of state mach	4:0	0x00000000	Current instruction address of state machine 3	0x00000000	Current instruction address of state machine 3
SM3_INSTR	5020120	0x120		15:0	0x0000fcfe	Read to see the instruction currently addressed by state machine 3's program counter Write to execute an instruction immediately (including jumps) and then resume execution.	0x00007df3	Read to see the instruction currently addressed by state machine 3's program counter Write to execute an instruction immediately (including jumps) and then resume execution.
			SIDESET_COUNT SET_COUNT OUT_COUNT IN_BASE SIDESET_BASE SET_BASE	31:29 28:26 25:20 19:15 14:10 9:5				
SM3_PINCTRL	5020124	0x124	OUT_BASE	4:0	0x14000000	State machine pin control	0x14000000	State machine pin control