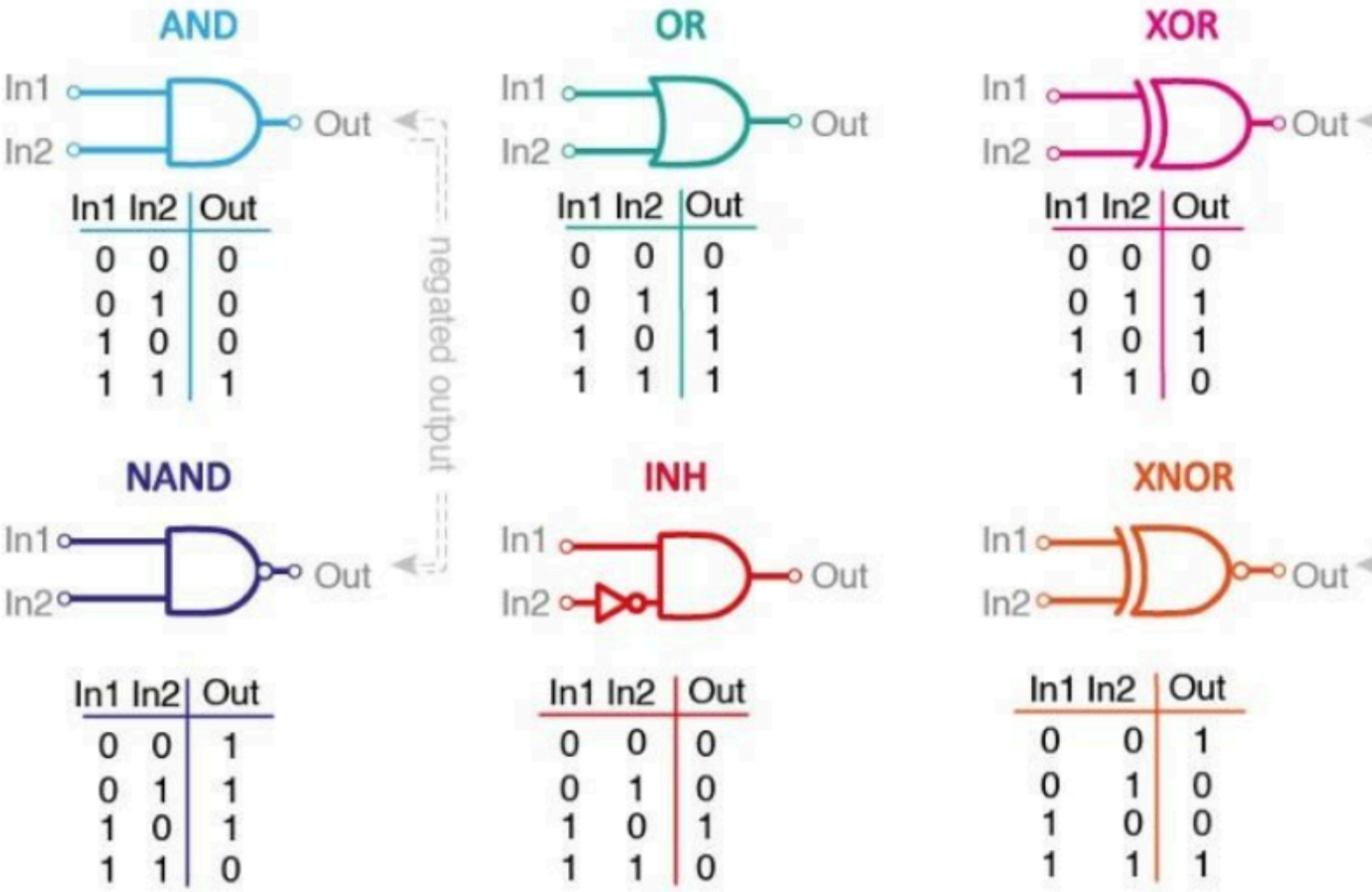
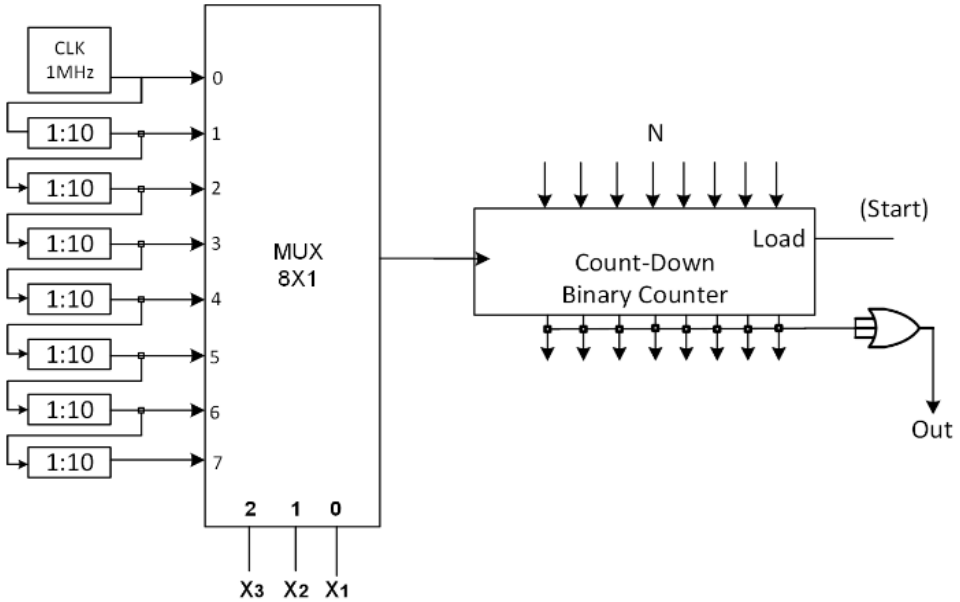
Highlight = Correct, Highlight = Wrong, Highlight = Maybe 7



Consider the following programmer timer, If the time period of the timer at the output of the circuit is 2.5sec what should be N and X3X2X1?

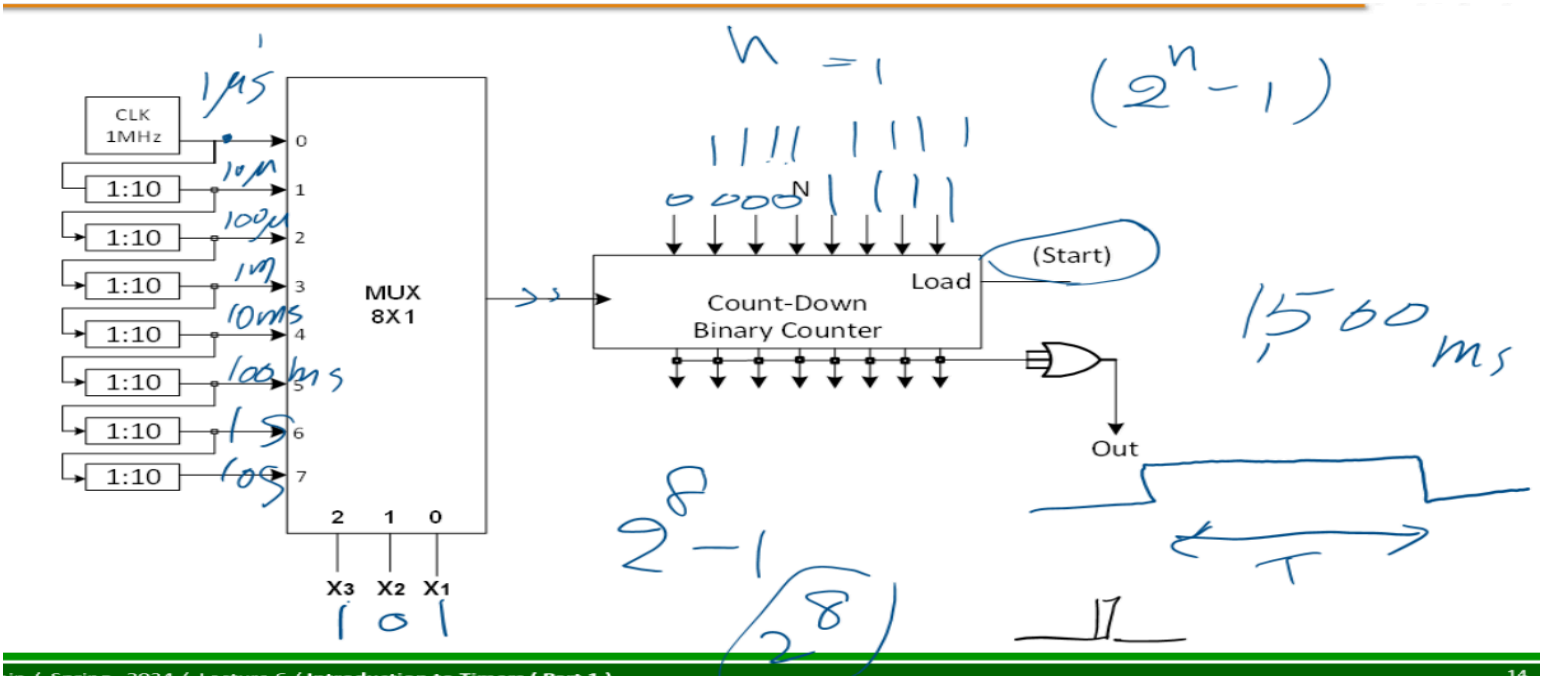
(1:10 blocks are frequency divider)



A. N=250 & X3X2X1=011

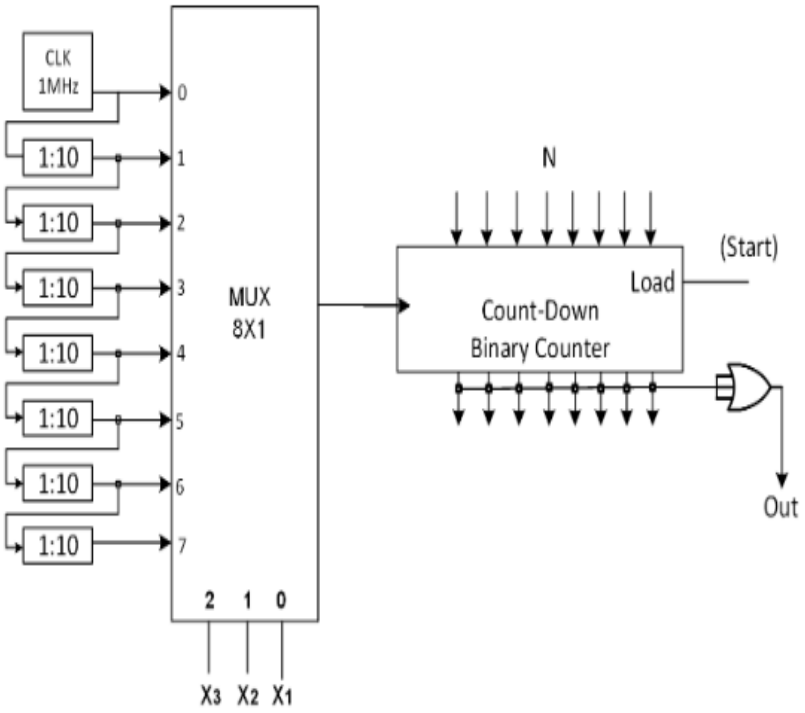
B. N=25 & X3X2X1=111
C. N=250 & X3X2X1=101 (Wrong)
D. N=250 & X3X2X1=100
E. None of them

Answer:
A.N=250 & X3X2X1=011. This would give 250 * 1ms = 0.25s
B. N=25 & X3X2X1=111 This would give 25 * 10s = 250s
C. N=250 & X3X2X1=101 This would give 250 * 0.1= 25s
D. N=250 & X3X2X1=100 This would give 250 * 10ms= 2.5s (this is correct option)



Consider following programmer timer, If the time period of the timer at the output is 5miutes what should be N and X3X2X1 values?

(1:10 blocks are frequency divider)

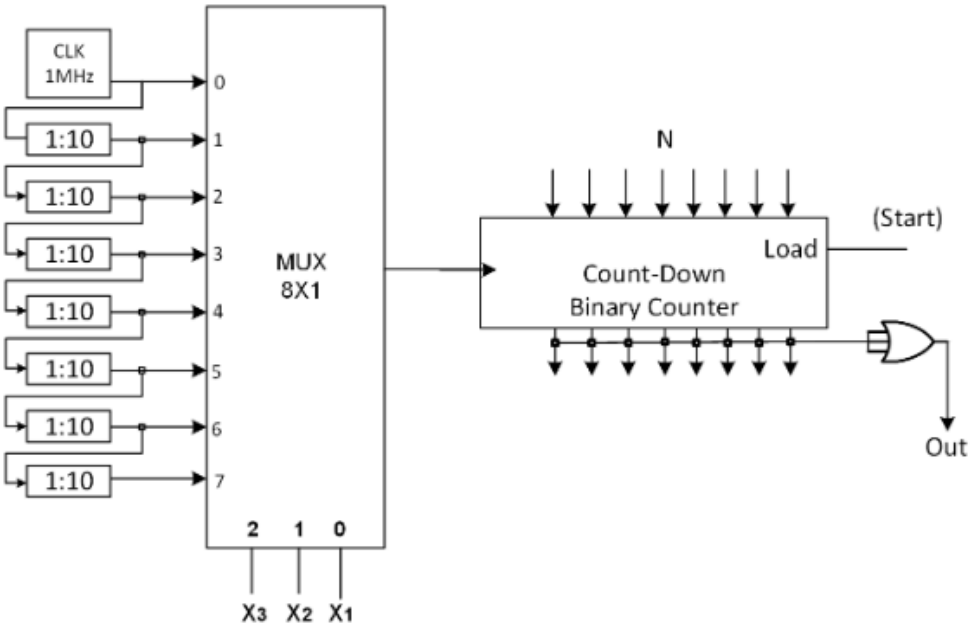


A. N=30 & X3X2X1=111
B. N=300 & X3X2X1=110
C. N=30 & X3X2X1=101 (wrong)
D. N=00011111 & X3X2X1=101
E. None of them

Answer:
5 mins = 300 sec
A.N=30 & X3X2X1=111. This would give 30 * 10s = 300s (5 minutes)
B. N=300 & X3X2X1=110 This would give 300 * 1s = 300s (5 minutes)
C. N=30 & X3X2X1=101 This would give 30 * 100ms = 3s (not 5 minutes)
D. N=00011111 & X3X2X1=101N = 31 in decimal, so this would give 31 * 100ms = 3.1s (not 5 minutes)
Given that the programmable divider typically uses smaller values for N, option A is more likely to be the intended correct answer.

Consider the following programmer timer, what is the time period of the timer at the output if N=300 & X3X2X1=111?

(1:10 blocks are frequency divider)



A. 30sec
B. 3sec
C. 300sec (Wrong)
D. 30msec
E. It is not possible to make it

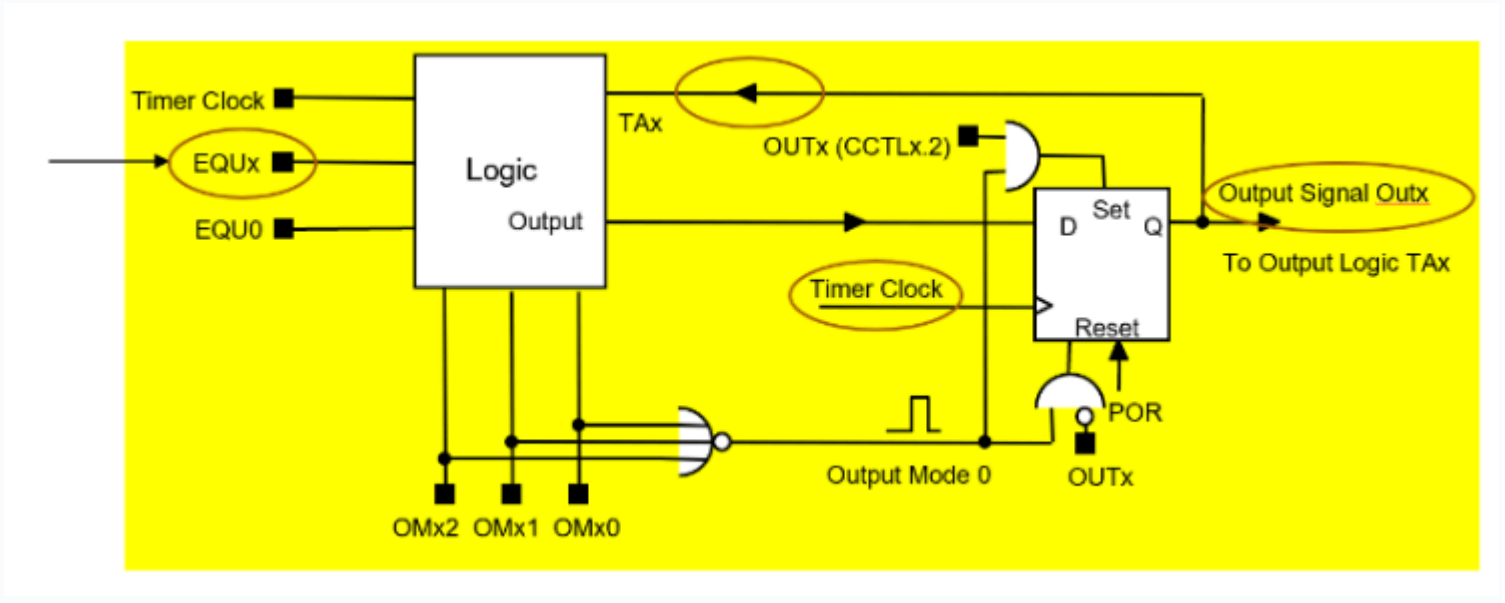
Answer:
N=300 & X3X2X1=111. This would give 300 * 10s = 3000s

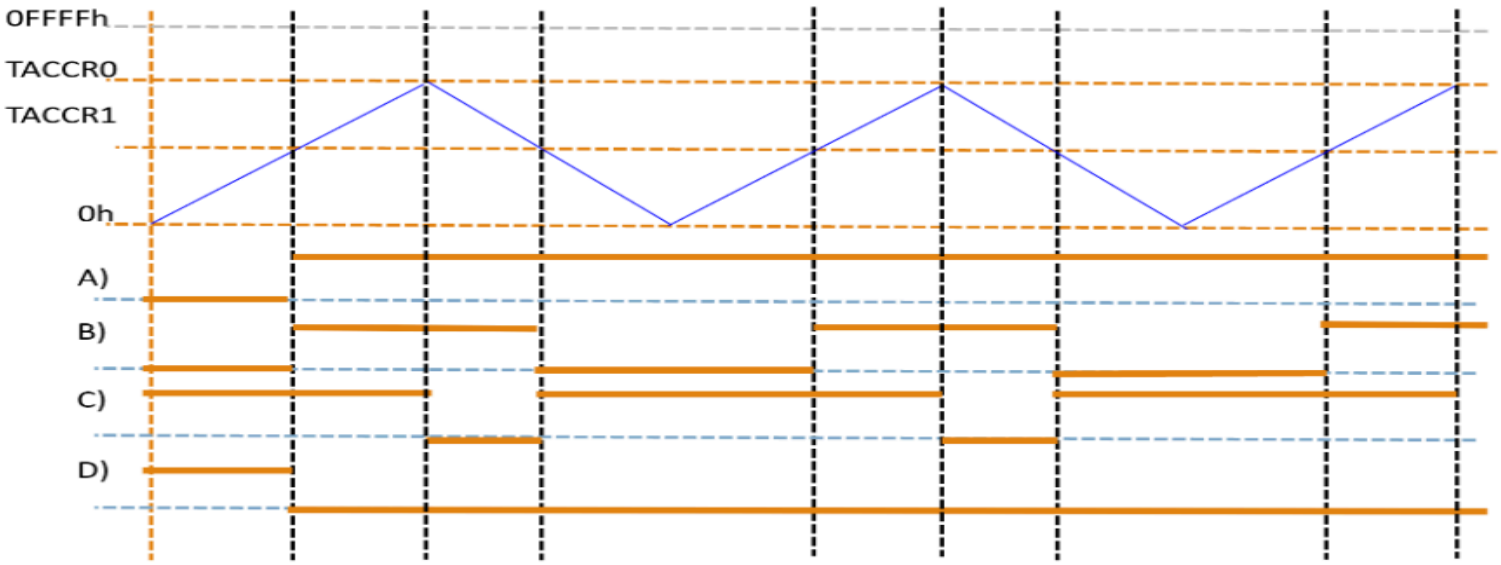
Consider the following programmer timer, what is the time period of the timer at the output if N=200 & X3X2X1=110?
(1:10 blocks are frequency divider)

A. 20sec
B. 2sec (Wrong)
C. 200sec
D. 20msec
E. 200us

Answer:
N=200 & X3X2X1=110. This would give 200 * 1s = 200s

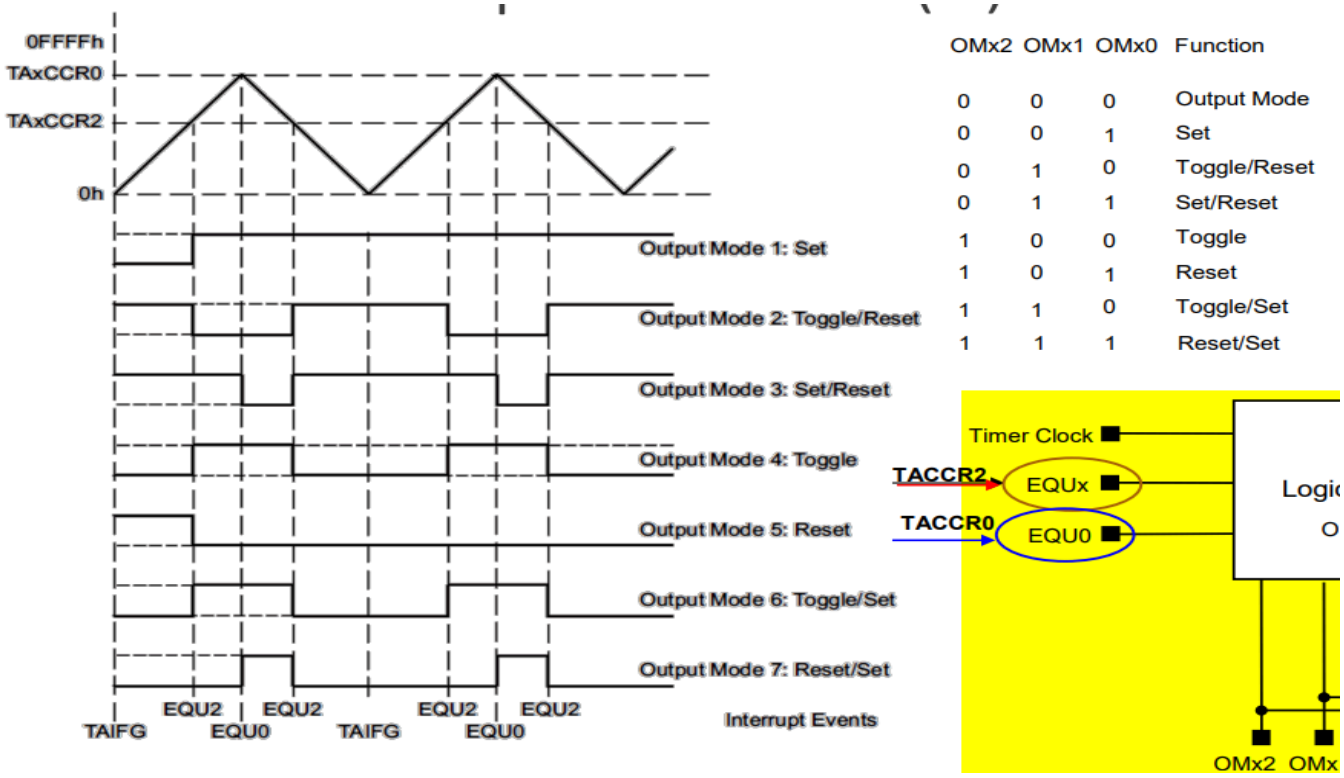
In Timer-A-MSP430x1xx, with up/down mode (MCx=11)
Which of the following waveforms, is the result of (OMx2 OMx1 OMx0 =110)?





A.Line A
B.Line B
C.Line C (Wrong)
D.Line D
E.None of them

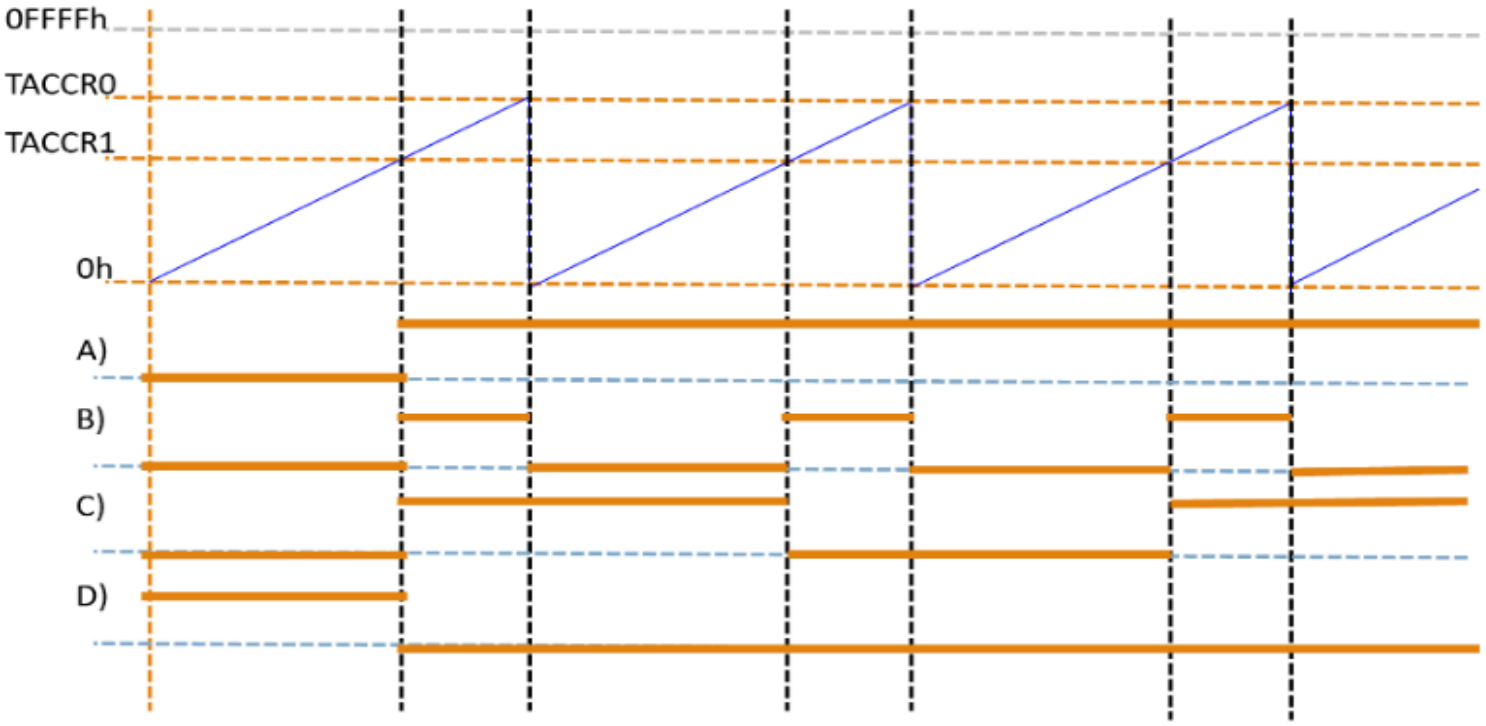
Answer:
UP/DOWN Mode (MCx=11)



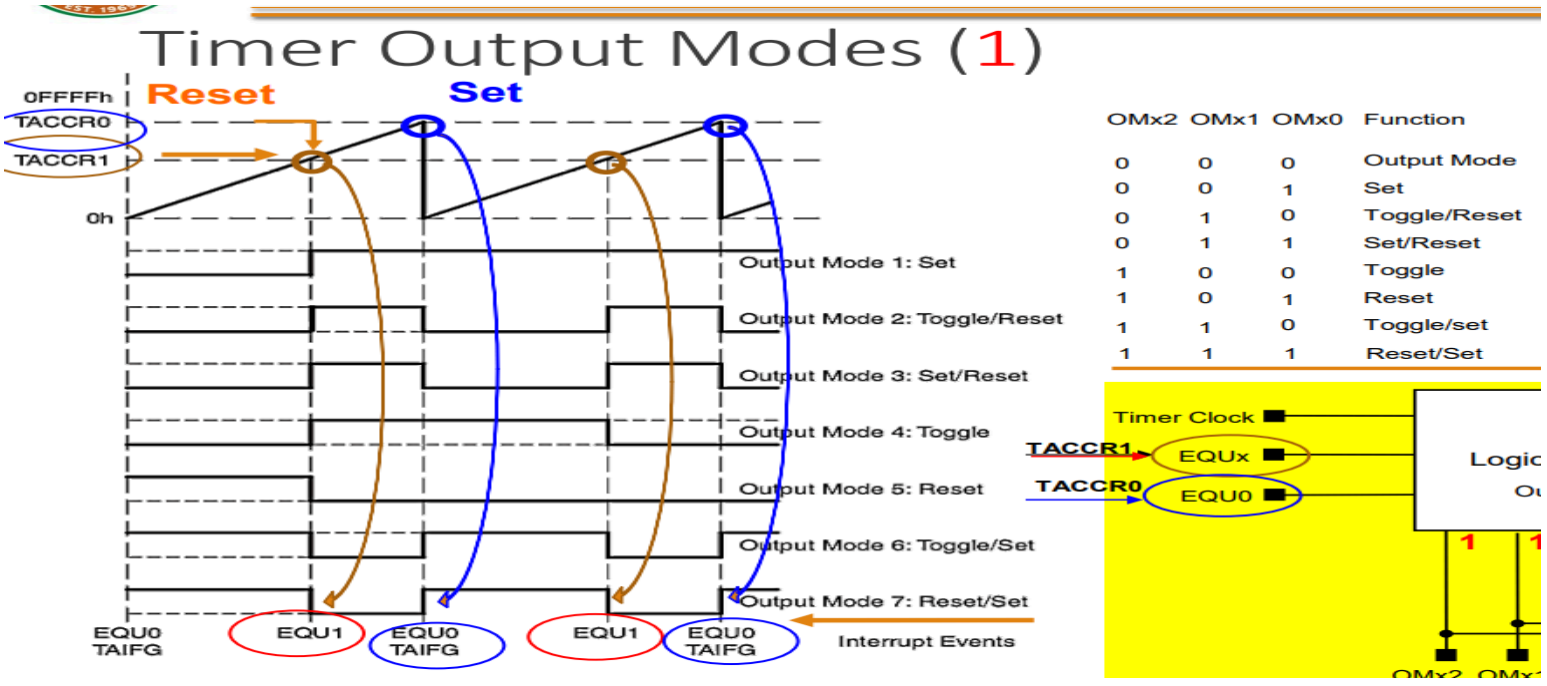
In Timer-A-MSP430x1xx, with up mode (MCx=01)

If the timer output mode is selected as (OMx2 OMx1 OMx0 =011) specify the output waveform.

A. **line A**
B. **Line B**
C. **Line C**
D. **Line D**
E. **None of them**

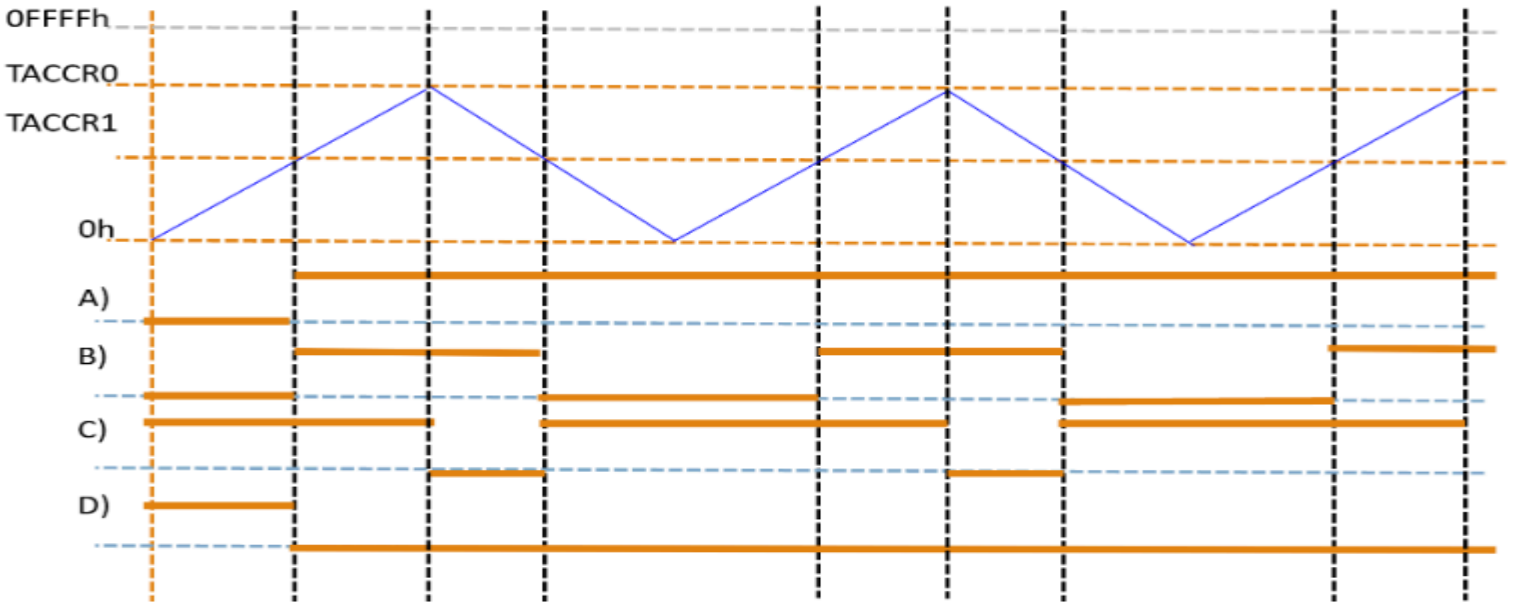


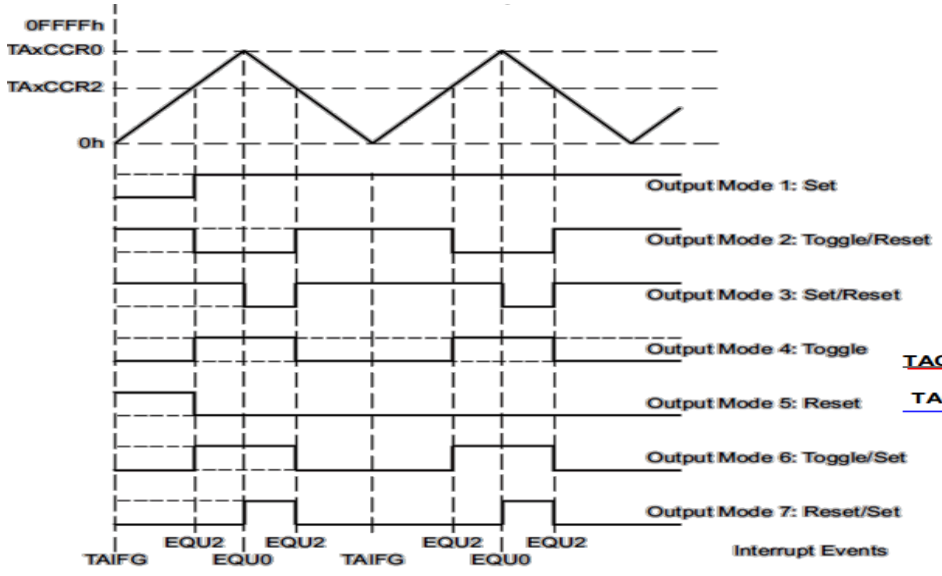
\



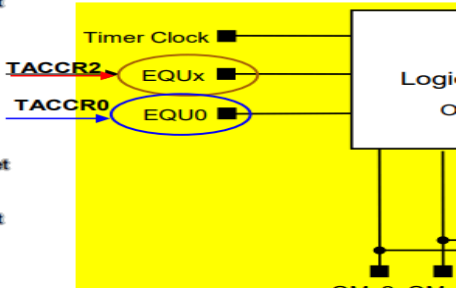
In Timer-A-MSP430x1xx, with up/down mode (MCx=11)Which of the following waveforms, is the result of the Toggle mode (OMx2 OMx1 OMx0 =100)?

A. line A
B. Line B
C. Line C (Wrong)
D. Line D
E. None of them



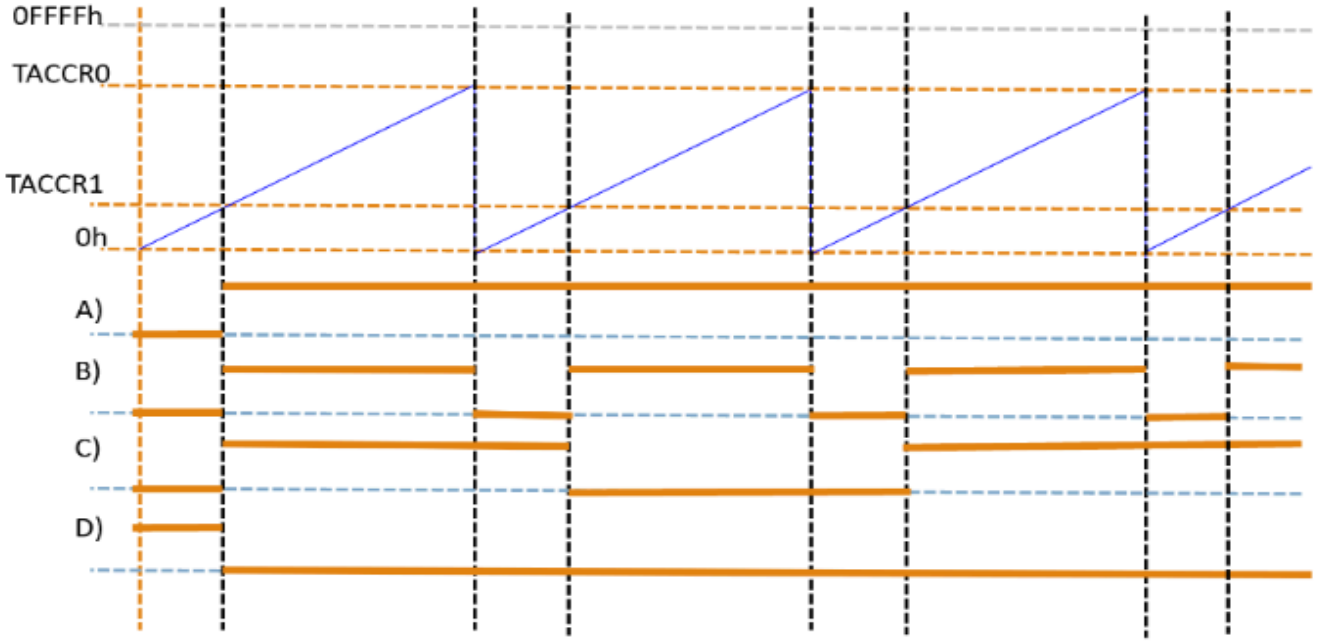


OMx2	OMx1	OMx0	Function
0	0	0	Output Mode
0	0	1	Set
0	1	0	Toggle/Reset
0	1	1	Set/Reset
1	0	0	Toggle
1	0	1	Reset
1	1	0	Toggle/Set
1	1	1	Reset/Set



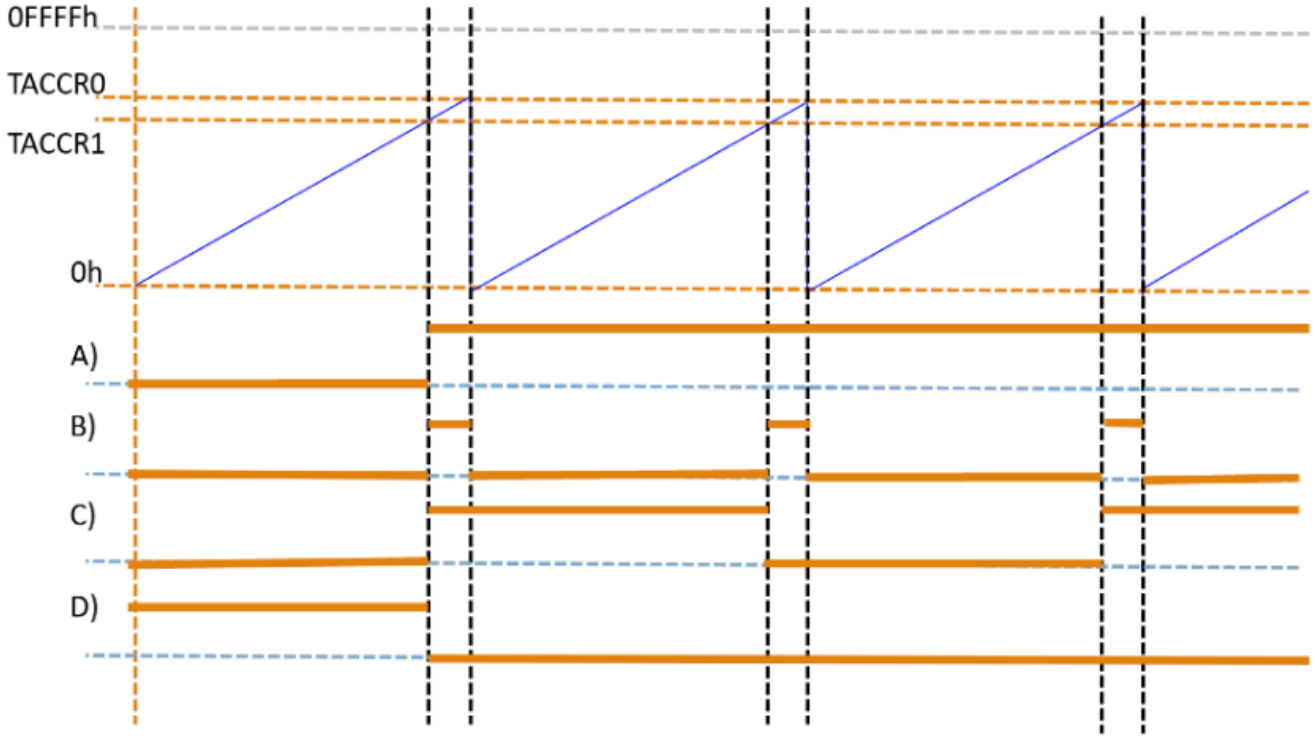
In Timer-A-MSP430x1xx, with up mode (MCx=01)If the timer output mode is selected as (OMx2 OMx1 OMx0 =111) specify the output waveform.

A. Line A
B. Line B
C. Line C
D. Line D
E. None of them

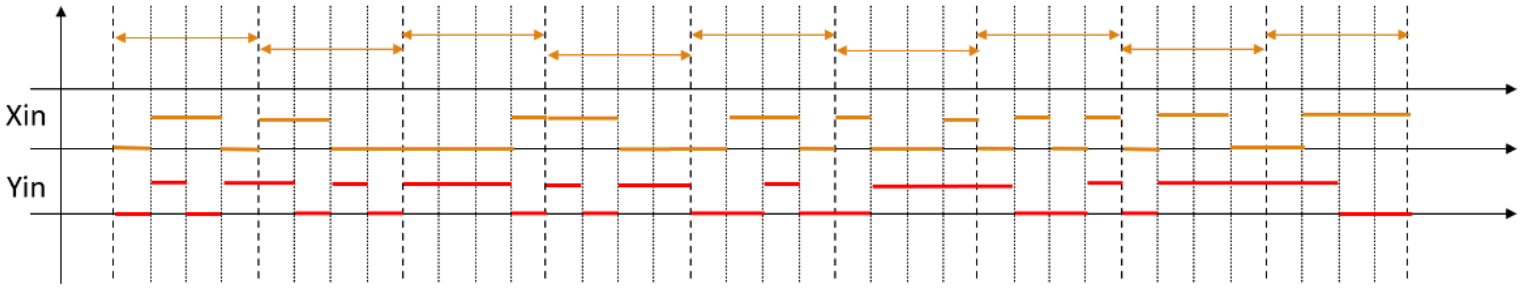


In Timer-A-MSP430x1xx, with up mode (MCx=01)If the timer output mode is selected as (OMx2 OMx1 OMx0 =100) specify the output waveform.

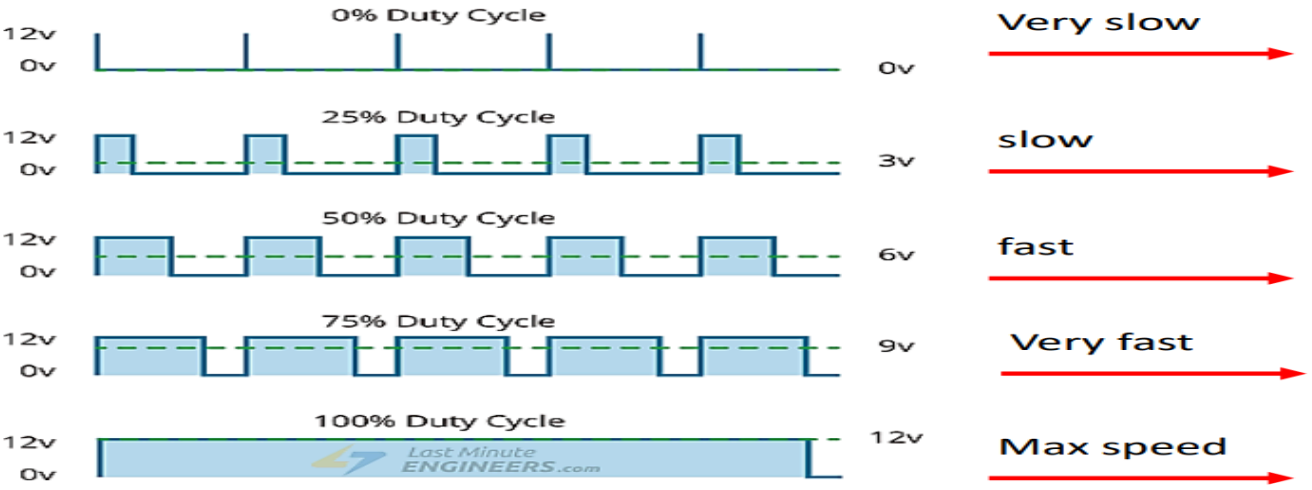
A. Line A
B. Line B
C. Line C
D. Line D
E. Line E



The following graph is showing Xin and Yin as two different sequences of binary inputs with 4 bits as a word. Each of them could be a binary input for a DC motor control for controlling its speed, the graph contains 9 words (each word is 4-bits). If PWM is used with D/A conversion for driving a DC motor, which of them makes more speed for the motor?



A. Yin is driving motor faster
B. Xin is driving motor faster
C. Both cause drive the motor with the same speed (wrong)
D. It is not possible to figure it out by this graph, more information is needed
E. PWM is not a good method for converting digital to analog



In Timer-A-MSP430x1xx, What would be CLK frequency of the 16bit Timer counter if TBSSEL=01 and IDx=10?

A. It is not clear
B. 32768 Hz
C. 4096 Hz
D. 8192 Hz
E. None of them

Answer:
TBSSEL = 01: This typically means that the timer is sourced from the internal **ACLK** (Auxiliary Clock), which is derived from the crystal oscillator (typically 32.768 kHz for low-power applications).

IDx = 10: This indicates the division factor of the timer clock. The binary `10` represents a division by **4**.

1. **TBSSEL = 00**: `TBSSEL__TACLK`
   - **Timer_A clock (TACLK)** is the external clock source, which can come from an external oscillator or another timer output.
2. **TBSSEL = 01**: `TBSSEL__ACLK`
   - **Auxiliary Clock (ACLK)**, which is typically sourced from a 32.768 kHz crystal, making it ideal for low-power, time-based applications. It's often used in real-time clock setups or when accurate timing is needed over longer intervals.
3. **TBSSEL = 10**: `TBSSEL__SMCLK`
   - **Sub-main Clock (SMCLK)** is a higher-speed clock than ACLK, typically running at a few MHz and sourced from the system's main clock. It's commonly used in timing operations where higher precision or shorter intervals are required.
4. **TBSSEL = 11**: `TBSSEL__INCLK`
   - **Internal Clock (INCLK)** is another clock input, though it's less commonly used compared to ACLK and SMCLK.

The `IDx` field typically uses two bits to determine the division factor:

- `00` : Divide by 1
- `01` : Divide by 2
- `10` : Divide by 4
- `11` : Divide by 8

- The effective clock frequency for the Timer counter can be calculated as follows:

$$\text{Timer Clock Frequency} = \frac{\text{ACLK Frequency}}{\text{Divider}}$$

- Substituting the values:

$$\text{Timer Clock Frequency} = \frac{32,768 \text{ Hz}}{4} = 8,192 \text{ Hz}$$

Conclusion

The clock frequency of the 16-bit Timer counter with $TBSSEL = 01$ and $IDx = 10$ is:

$$\text{CLK frequency} = 8,192 \text{ Hz}$$

In Timer-A-MSP430x1xx,What would be the value of TB0CCR0 for measuring 0.8sc with ACLK which is 32.768kHz and Idx=00?

A. 13107
B. 16034
C. 50000
D. 26214
E. None of them

Answer:
IDx = 00: No division, so the input clock frequency to the timer is 32.768 kHz.

To find out how many counts are needed to measure 0.8 seconds, use the following formula:

$$\text{Timer Counts} = \text{Timer Frequency} \times \text{Time}$$

Substituting the values:

$$\text{Timer Counts} = 32,768\,\text{Hz} \times 0.8\,\text{s}$$

$$\text{Timer Counts} = 32,768 \times 0.8 = 26,214.4$$

Since TB0CCR0 must be an integer value, we round it to the nearest whole number:

$$\text{Timer Counts} \approx 26,214$$

In Timer-A-MSP430x1xx,What would be the maximum time period measurement in Continues mode with ACLK which is 32.768kHz and Idx=00.

A. 65535
B. 36536
C. 50000
D. 26214
E. None of them (wrong)

Answer:
Timer-A is in Continuous mode
ACLK (Auxiliary Clock) is used, which is 32.768 kHz
IDx = 00, which means no input divider is used (divide by 1)
The maximum time period would be the time it takes to count from 0 to 65535 with the given clock:
Time period = (Maximum count + 1) / Clock frequency= 65536 / 32768 Hz= 2 seconds

---

In Timer-A-MSP430x1xx,
What would be CLK frequency of the 16bit Timer counter if TBSSEL=01 and IDx=11?

A. It is not clear
B. 32768 Hz
C. 4096 Hz
D. 8192 Hz
E. None of them

Answer:
IDx = 11 sets the input clock divider to 8
Time Clock Frequency = 32768/8 = 4096 Hz

In Timer-A-MSP430x1xx, which of the following items is not correct?

A. ACLK(Auxiliary Clock) is around 32KHz as low-frequency clock for the peripheral modules like real-time clk
B. SMCLK(Sub-Main Clock) is a high-frequency clock and it is used for peripheral modules like Timers,
C. MCLK(Main Clock) is used as a clock source for the CPU
D. A, B & C are incorrect(Wrong)
E. A, B & C are correct

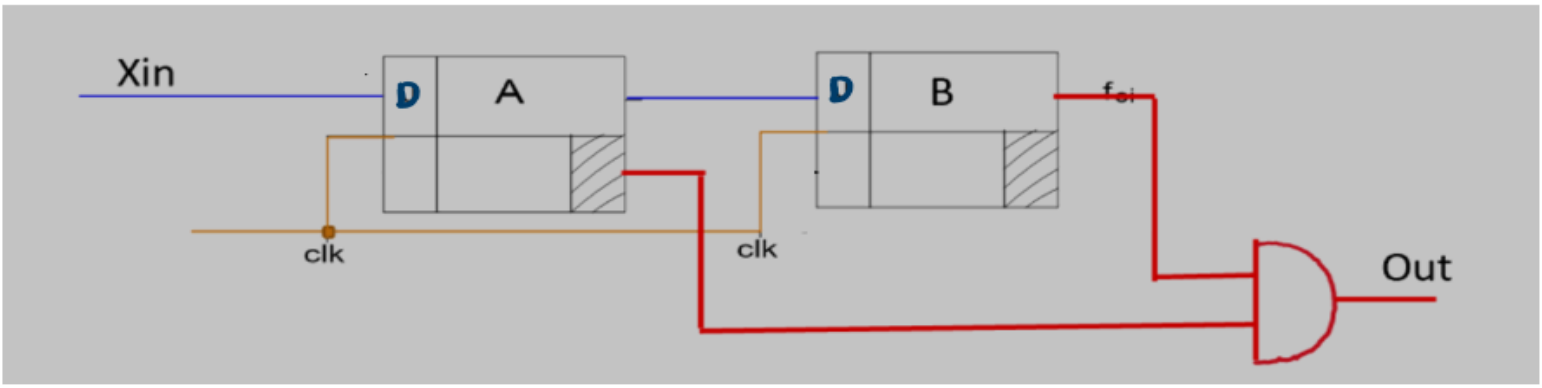
Consider Timer-A-MSP430x1xx, in the Timer Capture Compare Block, what is the duty of two bits “Capture mode” (CCMx1 & CCMx0) ?

A. Selection of mode for capture or compare (Wrong)
B. Connection to VCC and GND
C. The active edge control of input signal or make it disable

D. Selection of the CLK input
E. None of them

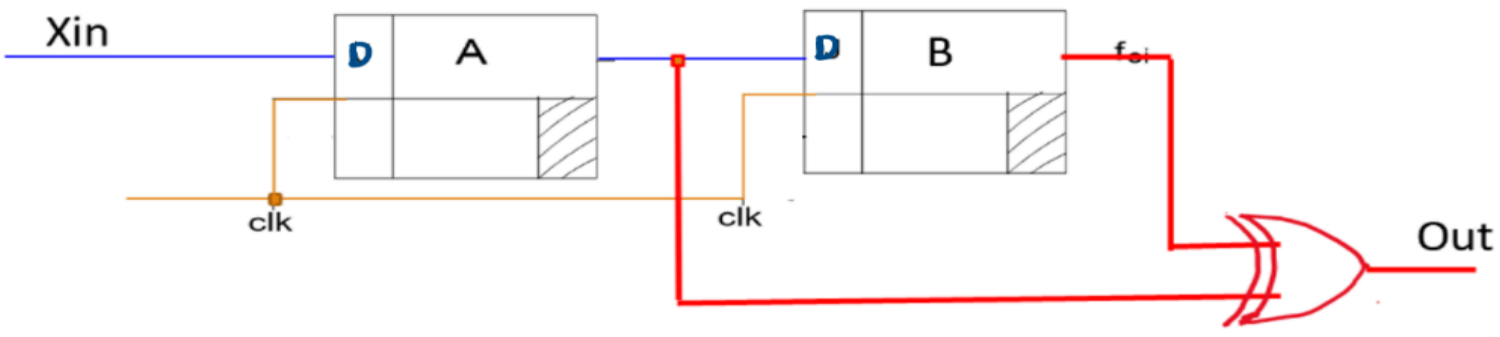
Answer:
In the Timer_A Capture/Compare Block, the CM (Capture Mode) bits are used to select the edge of the input signal that triggers a capture event. The CM bits control whether the capture occurs on the rising edge, falling edge, both edges, or if the capture is disabled. When the capture occurs on the selected edge of the input signal, the timer value is copied into the TAxCCRn register, and the interrupt flag (CCIFG) is set. This functionality is crucial for applications that need to record time events, which can be used for speed computations or time measurements.

Consider the following circuit, what is the operation of the output?



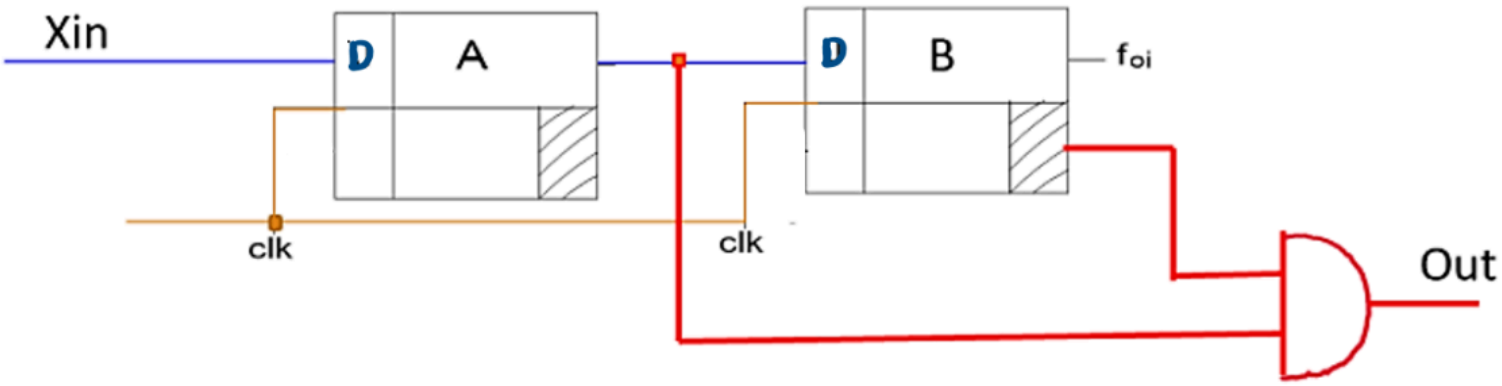
A. High to Low edge detector
B. Low to High edge detector
C. High to Low and Low to High edge detector
D. 1:4 frequency divider
E. None of them

Consider the following circuit, what is the operation of the output?



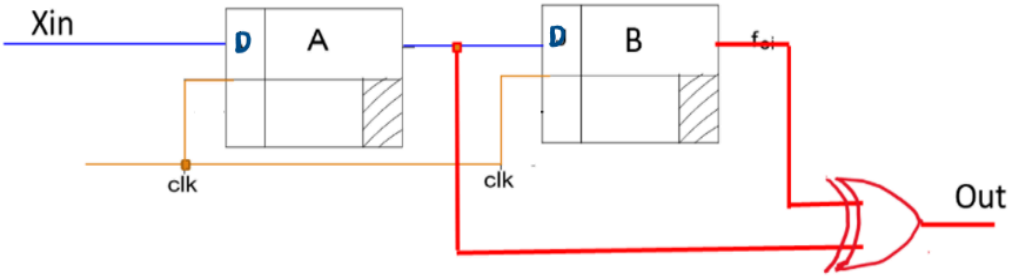
A. High to Low edge detector
B. Low to High edge detector
C. Both High to Low and Low to High edge detector
D. 1:4 frequency divider
E. None of them

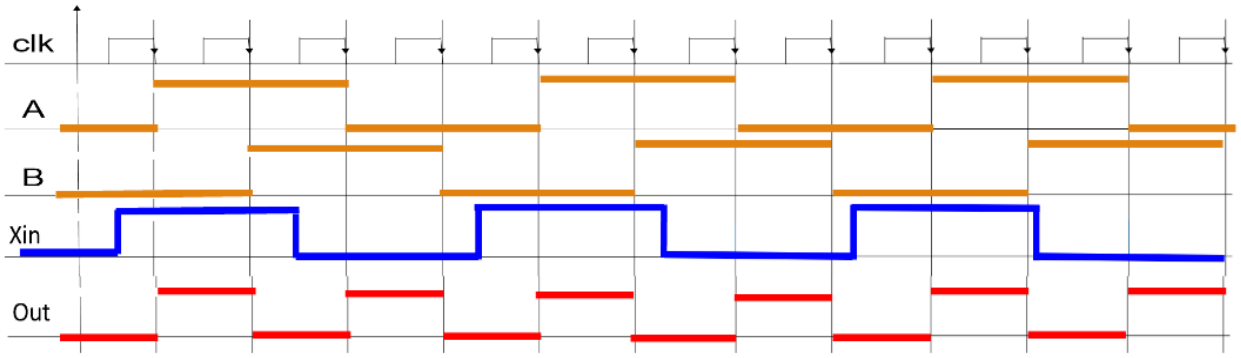
Consider the following circuit, what is the operation of the output?



A. High to Low edge detector
B. Low to High edge detector
C. High to Low and Low to High edge detector
D. 1:4 frequency divider
E. None of them

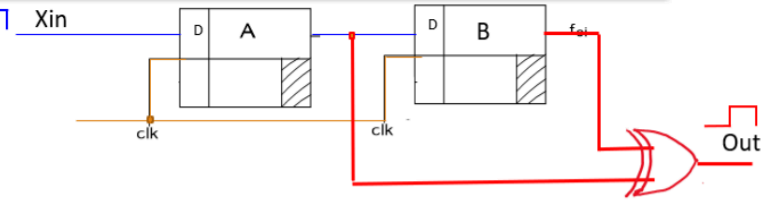
Consider the following circuit, if Xin is input and Out is the output signal, and the following timing graph is considered for the circuit operation, which of the following items in this regard are correct.

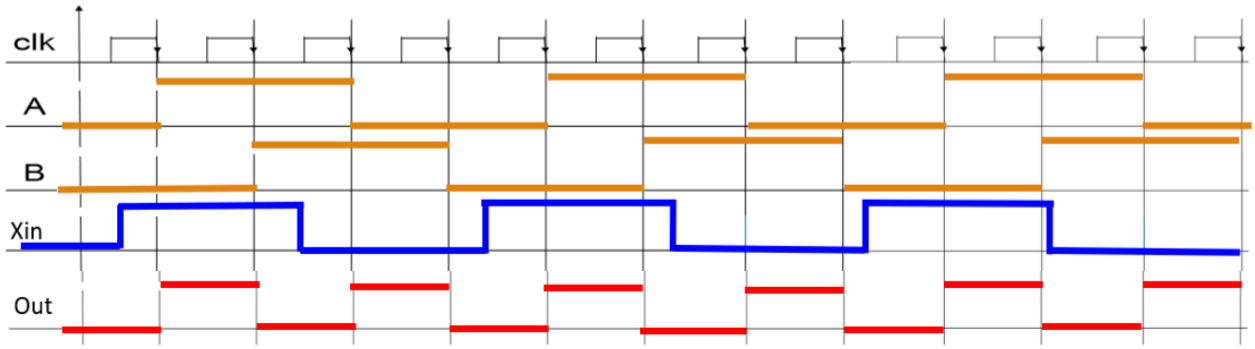




A. Based on Xin signal and clk input, A signal (QA) is incorrect
B. Based on Xin signal and clk input, B signal (QB) is incorrect (Wrong)
C. Based on Xin signal and clk input, Out signal is incorrect
D. All signals (A, B & Out) are correct
E. All signals are incorrect

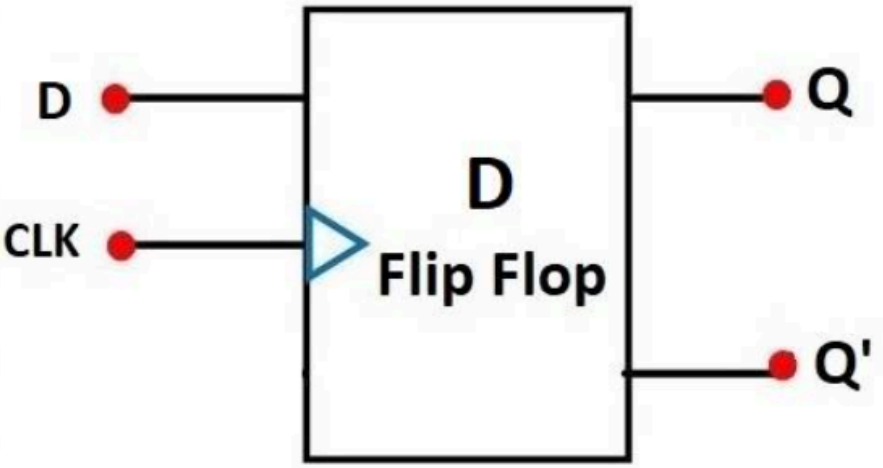
8. Consider the following circuit, if Xin is an input and Out is the output signal, and the following timing graph is considered for the circuit operation, which of the following items in this regard are correct.





Truth Table of DFlip Flop

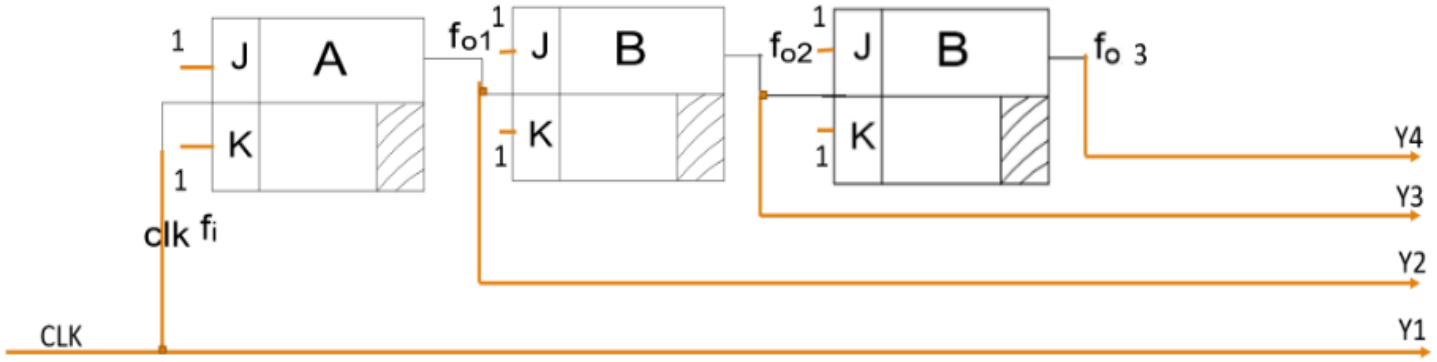
D	CLK	Q	Q`
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



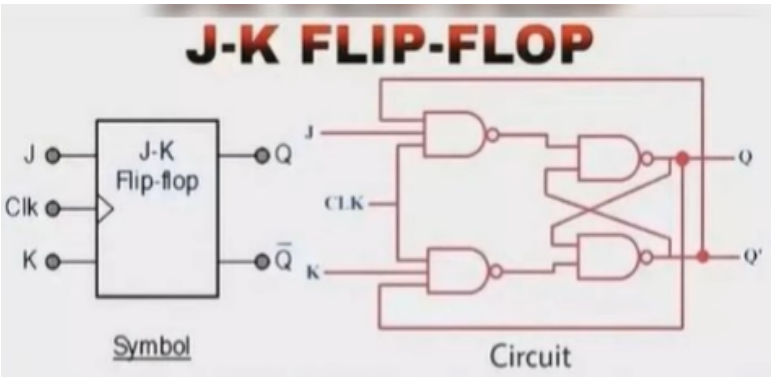
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Consider the following circuit as a frequency divider, it contains three JK-FFs.

Fi is a clk rate of input and fo1, fo2 & f03 are three outputs. Which of the following items are correct regarding clk rate ratio.



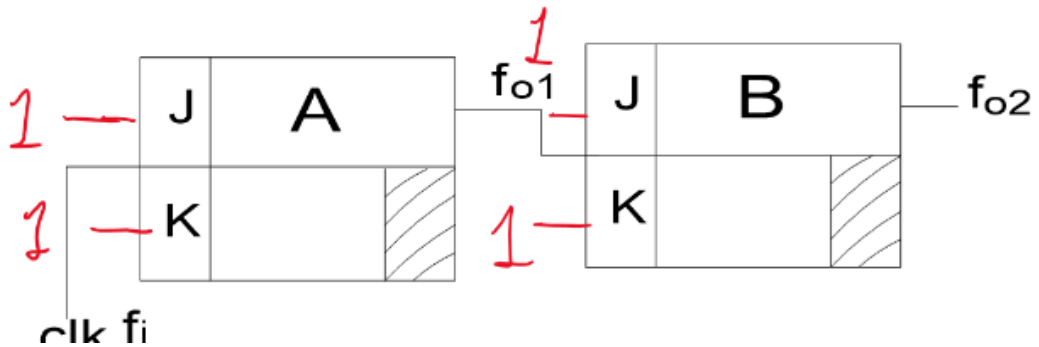
A. A.Fo1/Fi =1/2, Fo2/Fi= 1/4, Fo3/Fi= 1/8
B. Fo1/Fi = 1, Fo2/Fi= 1/2, Fo3/Fi=1/4
C. A.Fo1/Fi = 1/4, Fo2/Fi= 1/2, Fo3/Fi=1/8
D. A.Fo1/Fi = 1/2, Fo2/Fi= 1/8, Fo3/Fi=1/4
E. None of them are correct



Clk	J	K	Q	Q'	State
1	0	0	Q	Q'	No change in state
1	0	1	0	1	Resets Q to 0
1	1	0	1	0	Sets Q to 1
1	1	1	-	-	Toggles

Truth Table

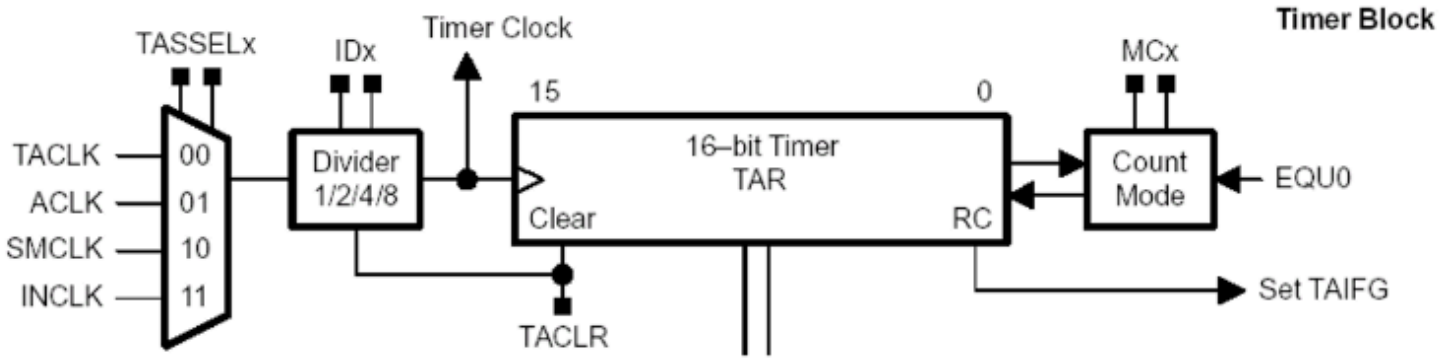
Consider the following circuit as a frequency divider, it contains two JK-FFs.
Fi is a clk rate of input and fo1 & fo2 are two outputs. Which of the following items are correct regarding clk rate ratio.



A. Fo1/Fi = 2
B. Fo2/Fi= 2
C. Fo2/Fi=4
D. Fo1/Fi=4
E. Both A & C are correct

For Timer-A-MSP430x1xx,

In the folowing picture, If MCx=10 what is the operation mode of timer ?

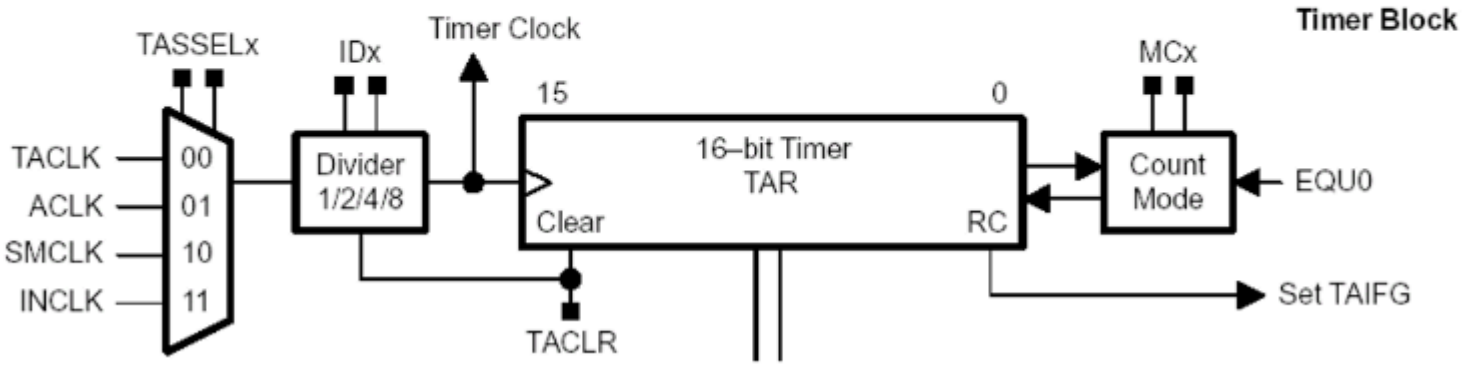


A. Stop/Halt mode
B. up/down mode
C. Up mode
D. Continues mode
E. Both C & D

Answer:
MCx Mode:
00: Stop mode
01: Up mode
10: Continuous mode
11: Up/Down mode

In Timer-A-MSP430x1xx,

In which of the following modes of MCx, CCR is counting up to maximum value (0FFFFh)?



A. Stop/Halt mode
B. up/down mode
C. Up mode (Wrong)
D. Continues mode
E. Both C & D

Answer:
In Continuous mode (MC = 10), the timer repeatedly counts from zero to 0xFFFF

For Timer-A-MSP430x1xx,In the folowing picture, If MCx=01 what is the operation mode of timer ?
A.Stop/Halt mode
B.up/down mode
C.Up mode
D.Continues mode
E.Both C & D

Answer:
00: Stop mode
01: Up mode
10: Continuous mode
11: Up/Down mode
