UART, SPI = Full-Duplex I2C = Half-Duplex

which of the following statements are correct ?
Daisy Chain structure is possible for SPI modules only
Daisy Chain structure is possible for UART modules only
Daisy Chain structure is possible for I2C modules only
Daisy Chain structure is possible for both SPI and I2C modules
A and B are correct

Question 1

SPI systems

which of the following statements are correct ?

- ○ SPI is Half-Duplex
- ◉ SPI is Full Duplex
- ○ SPI is Simplex
- ○ SPI could be Half Duplex and Simplex
- ○ None of them

SPI is Half-Duplex
SPI is Full Duplex
SPI is Simplex
SPI could be Half Duplex and Simplex
None of them

Q10
In I2C systemswhich of the following statements are correct ?
I2C is Half-Duplex
I2C is Full Duplex
I2C is Simplex
I2C could be Half Duplex and Simplex
None of them

Q18
Regarding UART systems. which of the following statements are correct ?
UART is Half-Duplex
UART is Full Duplex
UART is Simplex
UART could be Half Duplex and Simplex
None of them

Q8
In SPI systems which of the following statements are correct ?
SPI is master and slave structure
SPI has only one master and multi slaves
SPI could have multi master multi slaves
A and C are correct
A and B are correct

Q20
Regarding I2C and SPI which of the following statements are correct ?
I2C is a multi-Master protocol
I2C is a single-Master protocol
SPI is a multi-Master protocol
SPI is a single-slave protocol
None of the above

1. "I2C is a multi-Master protocol" - This statement is correct. I2C can support multiple masters, as mentioned in several sources. For example, source 1 states: "The 'multiple masters with multiple slaves' setup in the I2C Communication Protocol is highly flexible and complicated. With several masters and slaves on a single bus, it enables separate subsystem or module communication."
2. "SPI is a multi-Master protocol" - This statement is technically possible but not common or standard. SPI is typically implemented as a single-master protocol, though multi-master configurations are possible with additional complexity.

Q4

Regarding I2Cwhich of the following statements are correct ?

I2C has a resistor as pull up network at the port

I2C has a transistor as pull down network at the port

I2C has a transistor as Pull up network at the port

I2C has a resistor as pull down network at the port

A and B are correct

Answer:

- I2C devices can only pull signals low, not high. The pull-up resistors are needed to pull the signals high when not actively driven low.

I2C has pull up resistor and pull down transistor (switch)

Q13

Regarding UART systemsWhich of the following statements are correct?

The number of bits for each word is fixed by 9 bits without change

each word contains start bit, stop bit, parity bit only

Each word contains date bits, and start bit only

Each word contains, data bit, start bit, stop bit, maybe parity bit

A & B are correct

Answer:

1. **"The number of bits for each word is fixed by 9 bits without change":**
    - This statement is **incorrect**. In UART, the number of bits per word (data bits) can vary depending on configuration. It can typically be set to 5, 6, 7, 8, or 9 bits, so it's not always fixed at 9 bits.
2. **"Each word contains start bit, stop bit, parity bit only":**
    - This statement is **incorrect**. Each word in UART typically contains data bits (along with optional parity bits), a start bit, and stop bits. The data bits are essential, and the parity bit is optional.
3. **"Each word contains data bits and start bit only":**

- This statement is **incorrect**. In UART, each word contains data bits, a start bit, and at least one stop bit. A parity bit may also be present, but the stop bit is mandatory.

4. **"Each word contains data bits, start bit, stop bit, maybe parity bit":**
   - This statement is **correct**. A UART word consists of the following: data bits, a start bit, and at least one stop bit, with an optional parity bit depending on configuration.
5. **"A & B are correct":**
   - This is **incorrect** because both A and B contain inaccuracies.

Conclusion: The correct answer is "Each word contains data bits, start bit, stop bit, maybe parity bit."

Q14
In UART systems,Why in some systems the stop bit has 1.5T of CLK period ?
It can help for synchronization between sender and receive
It is just for testing edge detector circuits
Recognition of previous word from next word
Introducing CLK Period
A & C are correct

Answer:

1. **"It can help for synchronization between sender and receiver":**
   - This is **correct**. The stop bit provides a buffer time between the transmission of consecutive data frames. A longer stop bit (1.5T or 2T) allows more time for the receiver to synchronize and process the incoming data, particularly in systems where timing stability is critical.
2. **"It is just for testing edge detector circuits":**
   - This is **incorrect**. The stop bit's primary purpose is not for testing edge detector circuits but to ensure proper timing and synchronization between sender and receiver.
3. **"Recognition of previous word from next word":**
   - This is **correct**. A longer stop bit can help the receiver differentiate between consecutive data words more clearly, especially in slower

systems where more time is needed to distinguish the start of a new word from the end of the previous one.

4. **"Introducing CLK Period":**
    - This is **incorrect**. The stop bit is not about introducing a clock period but about allowing time for the system to prepare for the next data word.

Conclusion: The correct answer is "A & C are correct."

Q6

Regarding UART systemsWhich of the following statements are correct?

Bit rate means the number of CLK bits per second and it depends on CLK frequency only
Baud Rate means the number of bit per second which is function of CLK rate and coding process
Baud rate ratio could be more than 1 but not lest than 1
Baud rate ratio could be less than 1 not more than 1
A & B are correct

Answer:
B statement is mostly correct. Baud rate is the number of signal changes per second, which can be affected by the clock rate and encoding method. However, it's not always equal to bits per second.

Q3

Regarding UART systems with 7 bit data, 1 bit start bit, 1 bit stop bit, 1 bit parity bit. how much is the maximum error tolerance with CLK shifting ?
%4
%5.5
%6.2
%4.7
None of them

Answer:

N = 7 + 1 + 1 + 1 = 10bits

100 / (2* 10 + 1) = 4.7%

Calculation based on clock delay

- Assume that the receiver clock is slow:

$T + \delta t$ instead of T

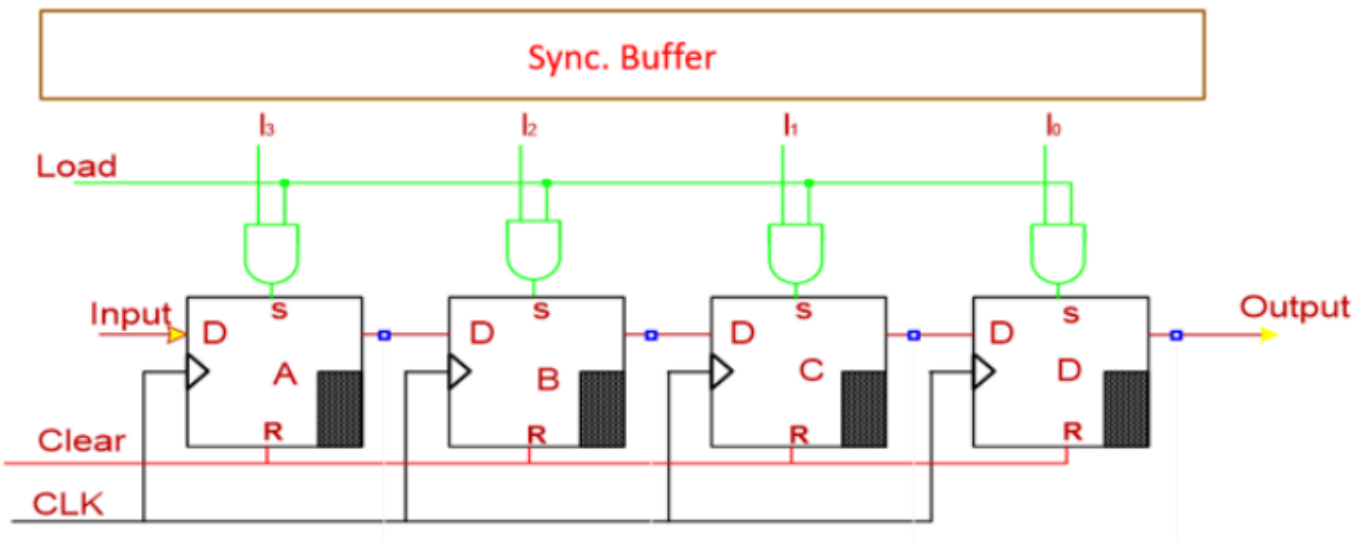
$$\frac{T}{2} > (2N + 1)\frac{\delta t}{2}$$

$$\frac{\delta t}{T} < \frac{1}{(2N+1)}$$

$$\frac{\delta t}{T} < \frac{100}{(2N+1)}\%$$

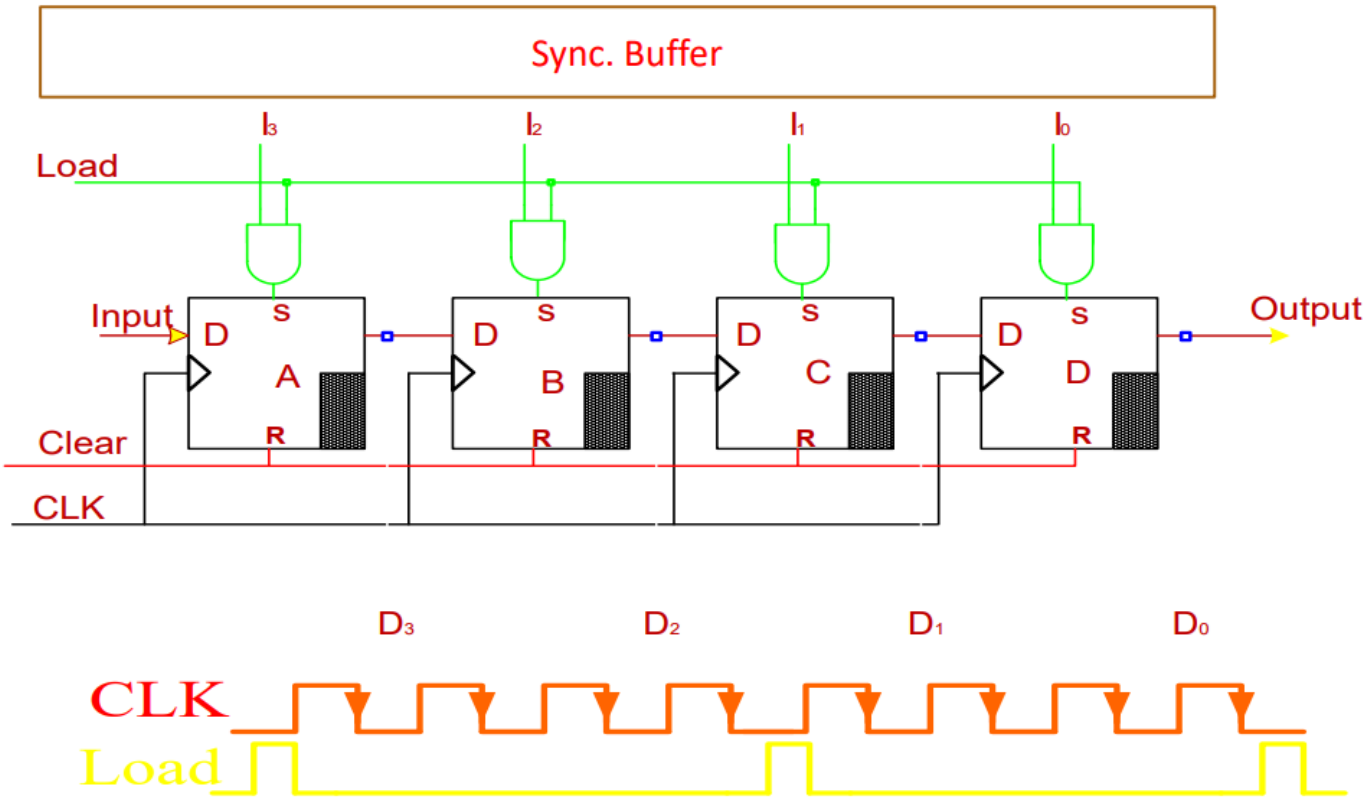
Q2

In a UART system, what is the following circuit ?



Parallel to serial converter, frequency of CLK is 4 times more than Load signal
Parallel to serial converter, frequency of CLK is 1/4 of the Load signal
Serial to Parallel converter, frequency of CLK is 4 times more than Load signal
Serial to Parallel converter, frequency of CLK is 1/4 of the Load signal
None of the above

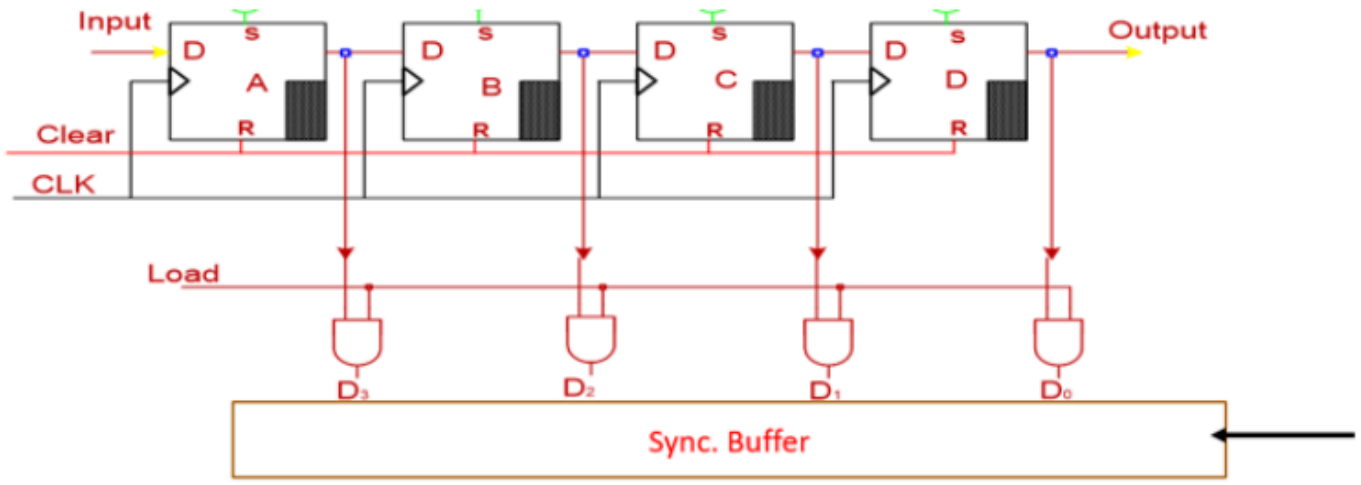
Parallel to serial convertor



1. The clock frequency is typically a multiple of the load signal frequency, with the multiple being equal to or greater than the number of bits in the parallel data.

Question 15

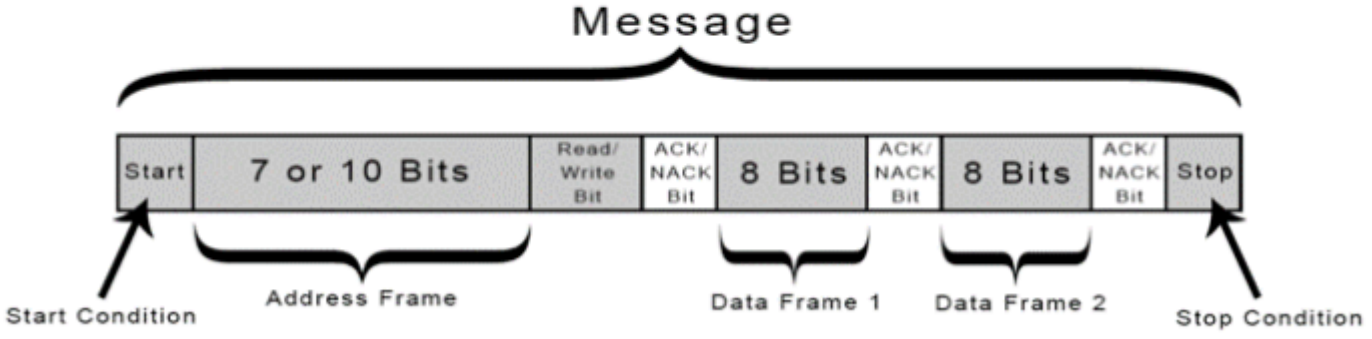
In a UART system, what is the following circuit ?



Parallel to serial converter, frequency of CLK is 4 times more than Load signal
Parallel to serial converter, frequency of CLK is 1/4 of the Load signal
Serial to Parallel converter, frequency of CLK is 4 times more than Load signal
Serial to Parallel converter, frequency of CLK is 1/4 of the Load signal
None of the above

Question 5

In I2C protocol, "1" after Address frame means:



d

Master writes to slave

Master reads from slave

Slave ACK the write request

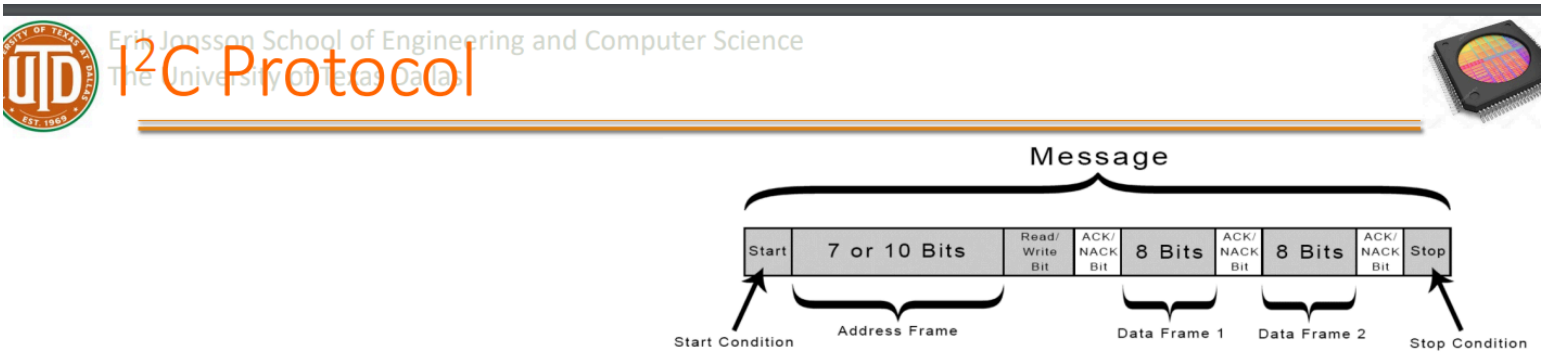
Slave ACK the read request

None of the above

Answer:

If the bit is "0," the master writes to the slave.

If the bit is "1," the master reads from the slave.



1. Master sends start condition (S) and controls the clock signal
2. Master sends a unique 7-bit (or 10-bit) slave device address
3. Master sends read/write bit (R/W) – 0 - slave receive, 1 - slave transmit
4. Receiver sends acknowledge bit (ACK)
5. Transmitter (slave or master) transmits 1 byte of data
6. Receiver issues an ACK bit for the byte received
7. Repeat 5 and 6 if more bytes need to be transmitted.
8. For write transaction (master transmitting), master issues stop condition after last byte of data.
9. For read transaction (master receiving), master does not acknowledge final byte, just issues stop condition to tell the slave the transmission is done

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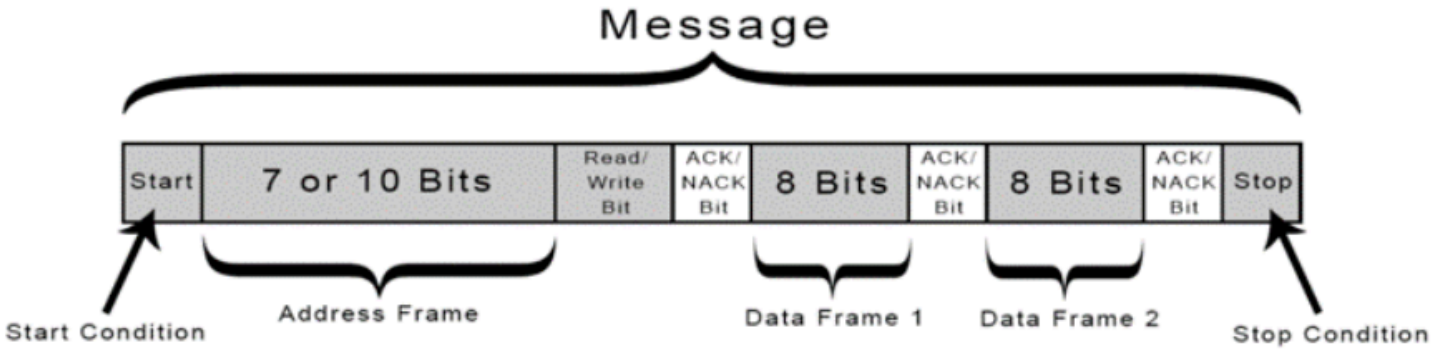
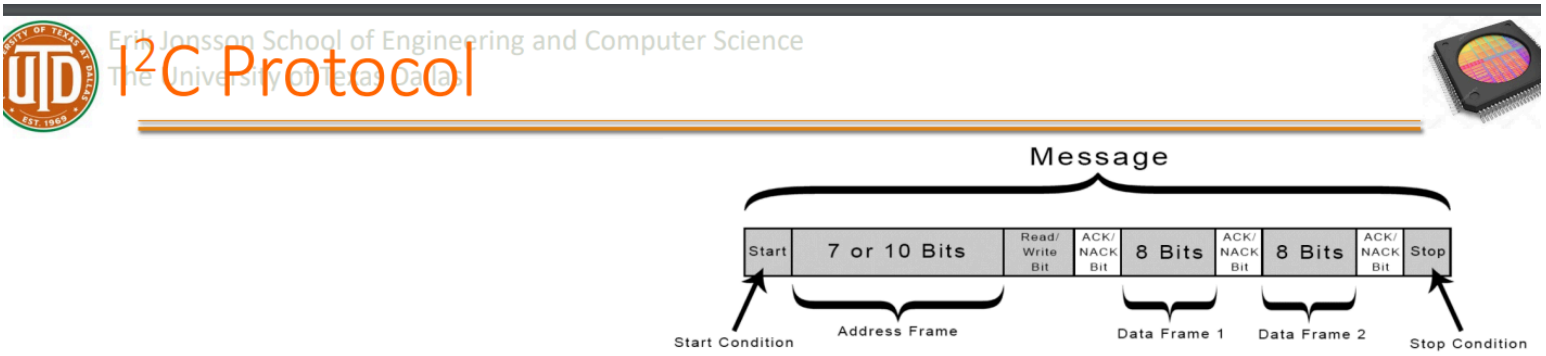
Question 9

In I2C protocol, after each word transfer from master to slave :



Master ACK the write operation
Master ACK the read operation
Slave ACK the write operation
Slave ACK the read operation
None of the above

Answer:



1. Master sends start condition (S) and controls the clock signal
2. Master sends a unique 7-bit (or 10-bit) slave device address
3. Master sends read/write bit (R/W) – 0 - slave receive, 1 - slave transmit
4. Receiver sends acknowledge bit (ACK)
5. Transmitter (slave or master) transmits 1 byte of data
6. Receiver issues an ACK bit for the byte received
7. Repeat 5 and 6 if more bytes need to be transmitted.
8. For write transaction (master transmitting), master issues stop condition after last byte of data.
9. For read transaction (master receiving), master does not acknowledge final byte, just issues stop condition to tell the slave the transmission is done

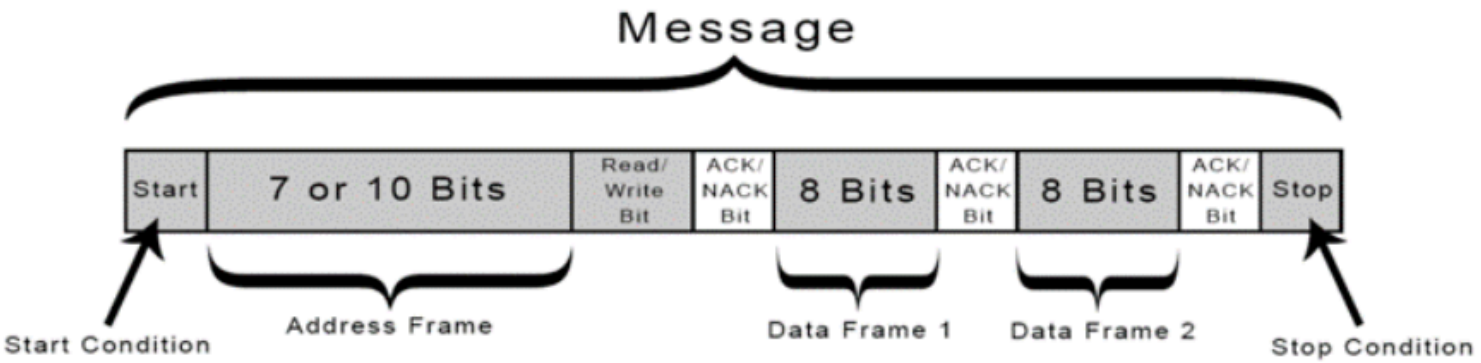
In the I2C protocol, after each word (byte) transfer from the master to the slave, the **slave acknowledges (ACKs) the reception** of the data by pulling the data line (SDA) low.

when the receiver (slave) sends an acknowledge bit (ACK) after a write operation, it means that the **slave has successfully acknowledged the write operation**.

Thus, the correct answer is: **Slave ACK the write operation**.

Question 11

In I2C protocol, address frame :



is a 4 bits
is sometimes from slave to master
is always from slave to master
is always from master to slave
None of the above

Answer:

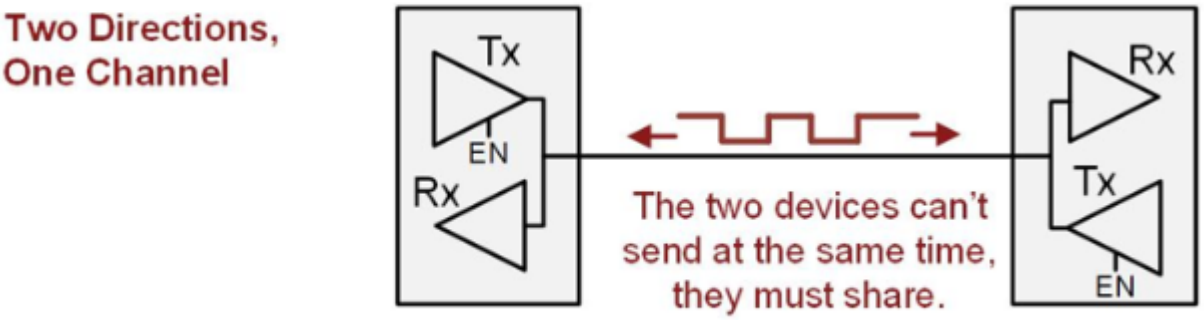
In the I2C protocol, the **address frame** is used to specify the address of the slave device the master wants to communicate with. The address frame:

- Is typically **7 bits** (or sometimes 10 bits, depending on the addressing mode).
- **Is always from the master to the slave**. The master initiates communication by sending the address of the target slave device along with the read/write bit.

Thus, the correct answer is: **is always from master to slave**.

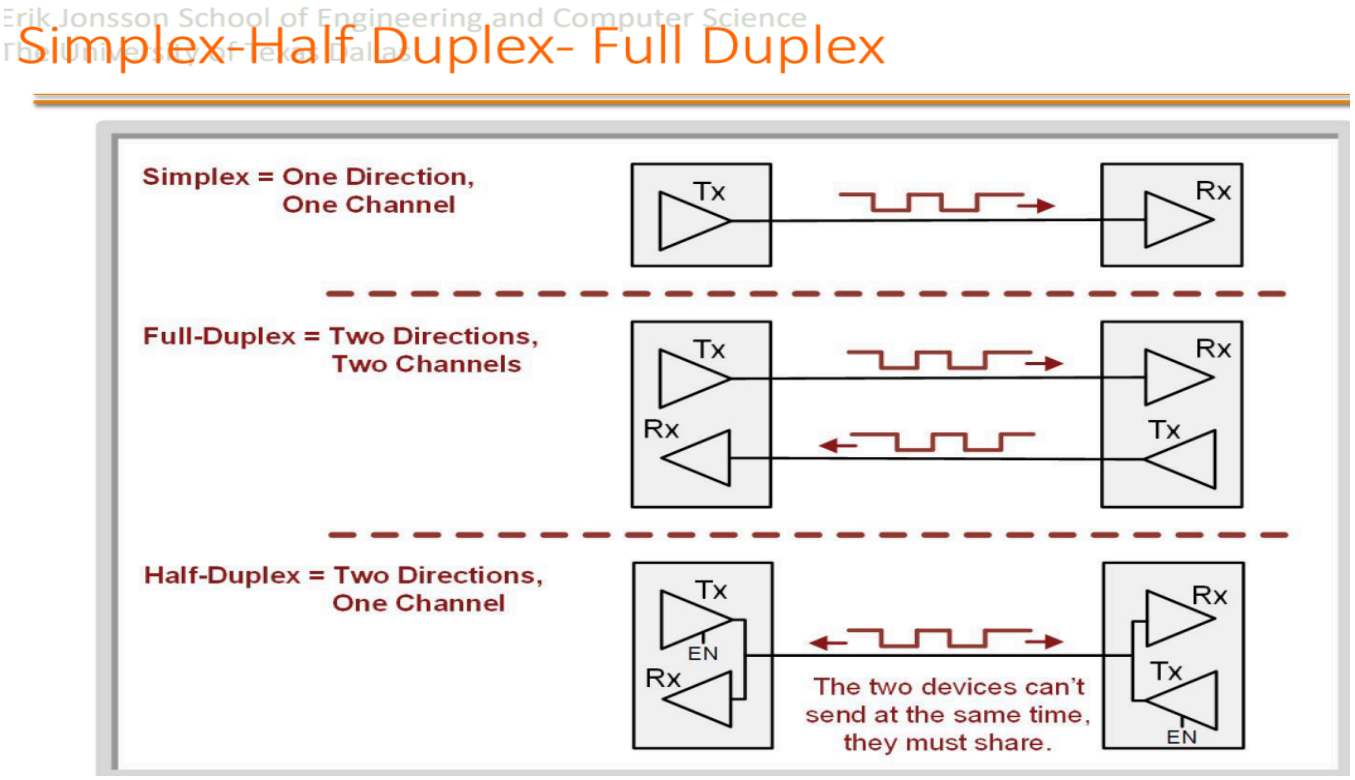
Question 12

Which of the following sentences are correct regarding following picture ?



The system is Simplex
The system is Half Duplex
The system is Full Duplex
All of the above
None of the above\

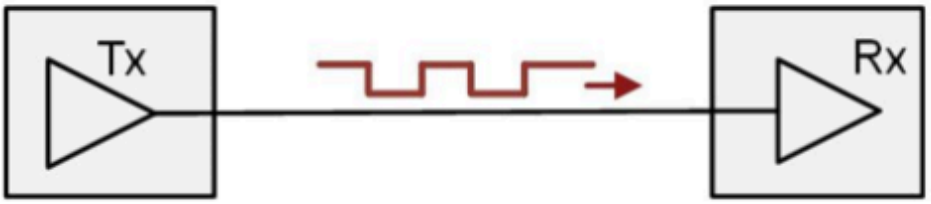
Answer:



Question 19

Which of the following statements are correct regarding following picture ?

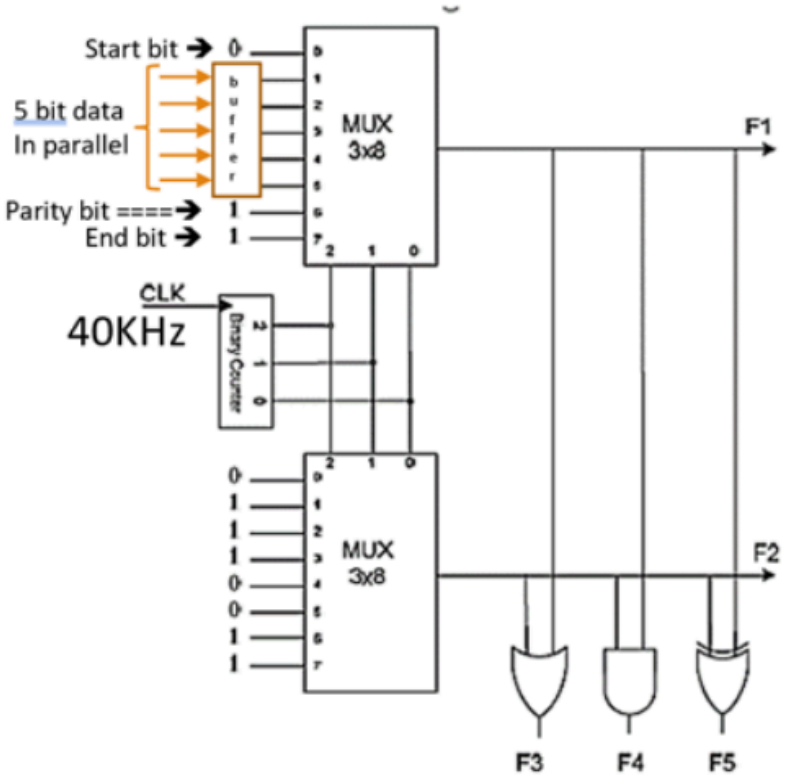
One Direction,
One Channel



- [x] The system is Simplex
- [ ] The system is Half Duplex
- [ ] The system is Full Duplex
- [ ] All of the above are correct
- [ ] None of the above

Question 7

In UART system and the following picture, the counter is 3-bit binary count-up. what is the Baud rate on F1 output line?



10KHZ
25KHZ
30KHZ
40KHZ
None of the above

Answer:

Baud rate may be higher or lower than bit rate
N = clk source / baud rate
N= 5 + 2 = 7 = 40000 / baud rate
Clk = 40000
Baud rate = 40000/7 = 5.7 kHz

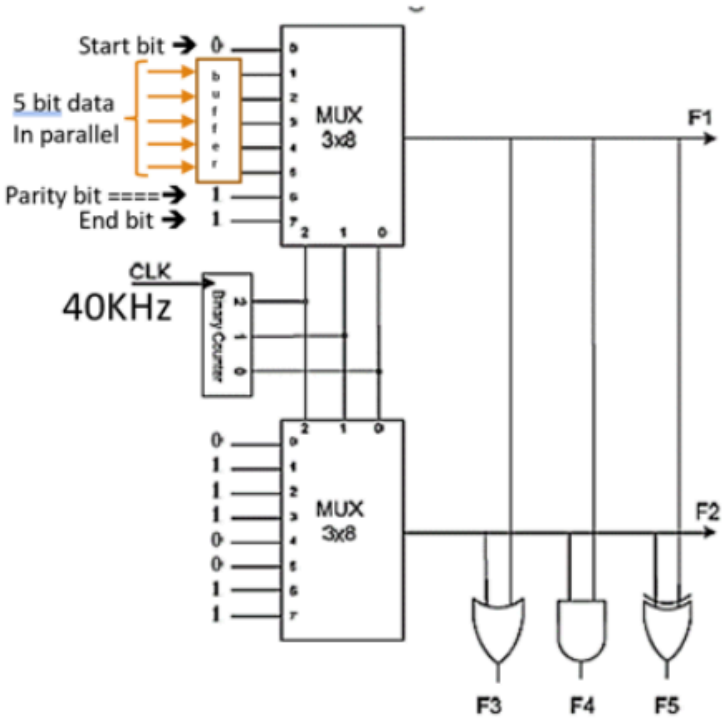
1. Total bits = 1 + 5 + 1 +1 = 8 bits
2. Now, we can calculate how many complete UART frames can be transmitted in one second:
   Frames per second = CLK frequency / Clock cycles per frame
   = 40,000 / 8
   = 5000 frames per second
3. **The Baud rate is defined as the number of signal changes per second**. In this case, it's equivalent to the number of bits transmitted per second:
   Baud rate = Frames per second * Bits per frame

= 5000 * 5
= 25,000 bps round to 25k

11100

Question 16

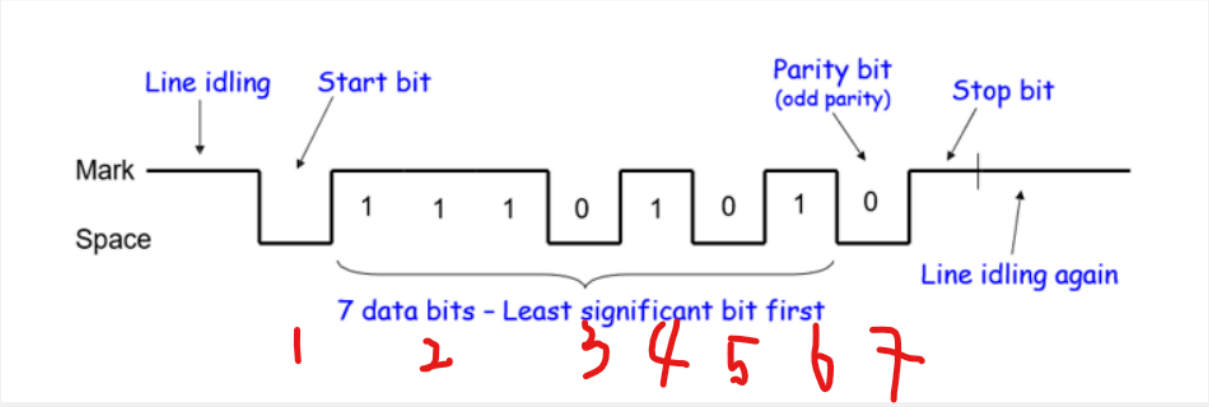
In UART system and the following picture, the counter is 3-bit binary count-up. what is the Bit rate on F1 output line?



10KHZ
25KHZ
30KHZ
40KHZ
None of the above

Question 17

In UART system and the following picture, if the stop bit is 1,5 T, (T is CLK period) . And CLK frequency is 120KHz, what is the Baud rate on output line?



10KHZ
25KHZ
80KHZ
40KHZ
None of the above

Answer:

4. Total bits = 1 + 7 + 1 + 1.5 = 10.5 bits
5. Now, we can calculate how many complete UART frames can be transmitted in one second:
   Frames per second = CLK frequency / Clock cycles per frame
   = 120,000 / 10.5
   = 11428 frames per second
6. **The Baud rate is defined as the number of signal changes per second**. In this case, it's equivalent to the number of bits transmitted per second:
   Baud rate = Frames per second * Bits per frame
   = 11428 * 7
   = 79996 bps round to 80k
