~~a. $T_{clk} \geq T_{clk \to Q} + T_{combinational} + T_{setup}$~~

~~$T_{clk} \geq$~~

a. $T_{clk} \geq T_{pcq} + T_{pd} + T_{setup}$.

$T_{clk} \geq 20ps + 350ps + 35ps = 350ps$.

max frequency $= 1/350ps = 2.86\,GHz$.

Checking for hold time violations,

$T_{hold} = 45ps$

$T_{pcq} + T_{cd} = 20 + 50 = 70ps$

Since $45ps < 70ps$, hold time is not violated.

b. $T_{propagation1} = T_{pcq} + T_{pd1} + T_{setup} = 20ps + 100ps + 30ps = 150ps$.

$T_{propagation2} = T_{pcq} + T_{pd2} + T_{setup} = 20ps + 210ps + 30ps = 260ps$.

The clock period has to be based on the greater of the two delays, hence,

$T_{clk,min} = 260ps, \Rightarrow f_{clk,max} = 1/260ps = 3.85\,GHz$ which is less than $4.8\,GHz$.

$\Rightarrow$ There is a setup violation in stage 2.

$T_{contamination1} = T_{pcq} + T_{cd1} = 20 + 20 = 40ps < 45ps$ (hold time violation).

$T_{contamination2} = T_{pcq} + T_{cd2} = 20 + 50 = 70ps > 45ps$ (no hold time violation).

c. Setup violation can be fixed by decreasing the clock frequency or reducing the propagation delay in stage 2.

Hold violations can be fixed by increasing contamination delay of S1, by, for example, adding buffers to that logic path, or reducing transistor widths.

d. Throughput is proportional to operations per second which is proportional to clock frequency. The max clock frequency in 'a' is $2.9\,GHz$ and the max clock frequency in 'b' is $3.9\,GHz$, therefore, design b has its throughput increased by $\frac{3.9}{2.9} - 1 = 34.5\%$

Latency is the number of stages multiplied by the clock period.

For design 'a', Latency = 1 × 350 ps = 350 PS

for design 'b', Latency = 2 × 260 ps = 520 ps

design b has $\frac{520}{350} - 1 = 48.57\%$ more latency than design a.

e. design a, $T_{clk} \geq T_{pcq} + T_{pd} + T_{setup} + T_{skew} = 20ps + 300ps + 30ps + 30ps = 380ps$

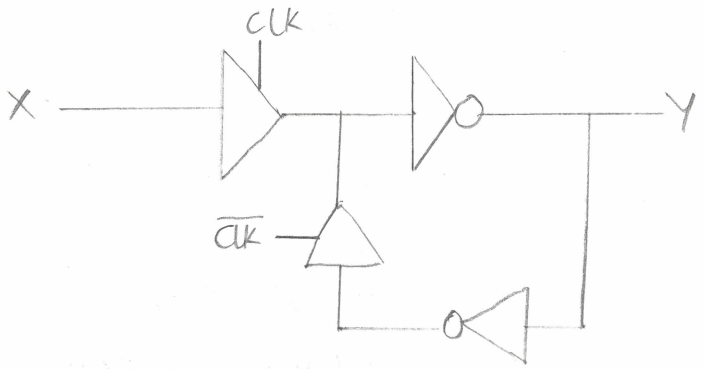
$\Rightarrow f_{max} = 1/380ps = 2.63\ GHz$

design b, $T_{clk} \geq \max(T_{pcq} + T_{pd} + T_{setup} + T_{skew}) = \max(20+100+30+30,\ 20+210+30+30)$

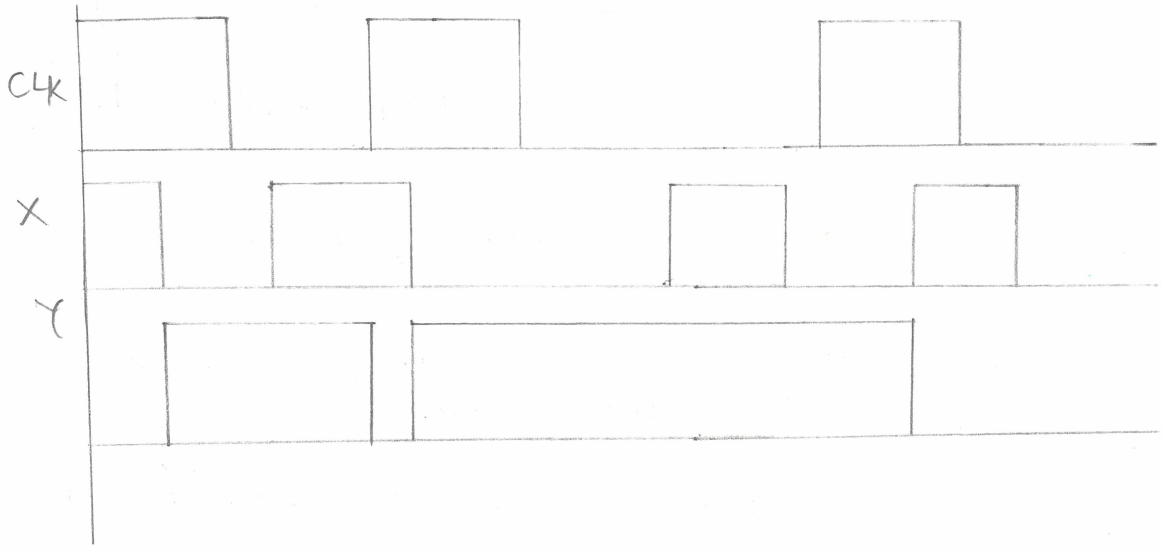
$= \max(180ps, 290ps) = 290ps.$

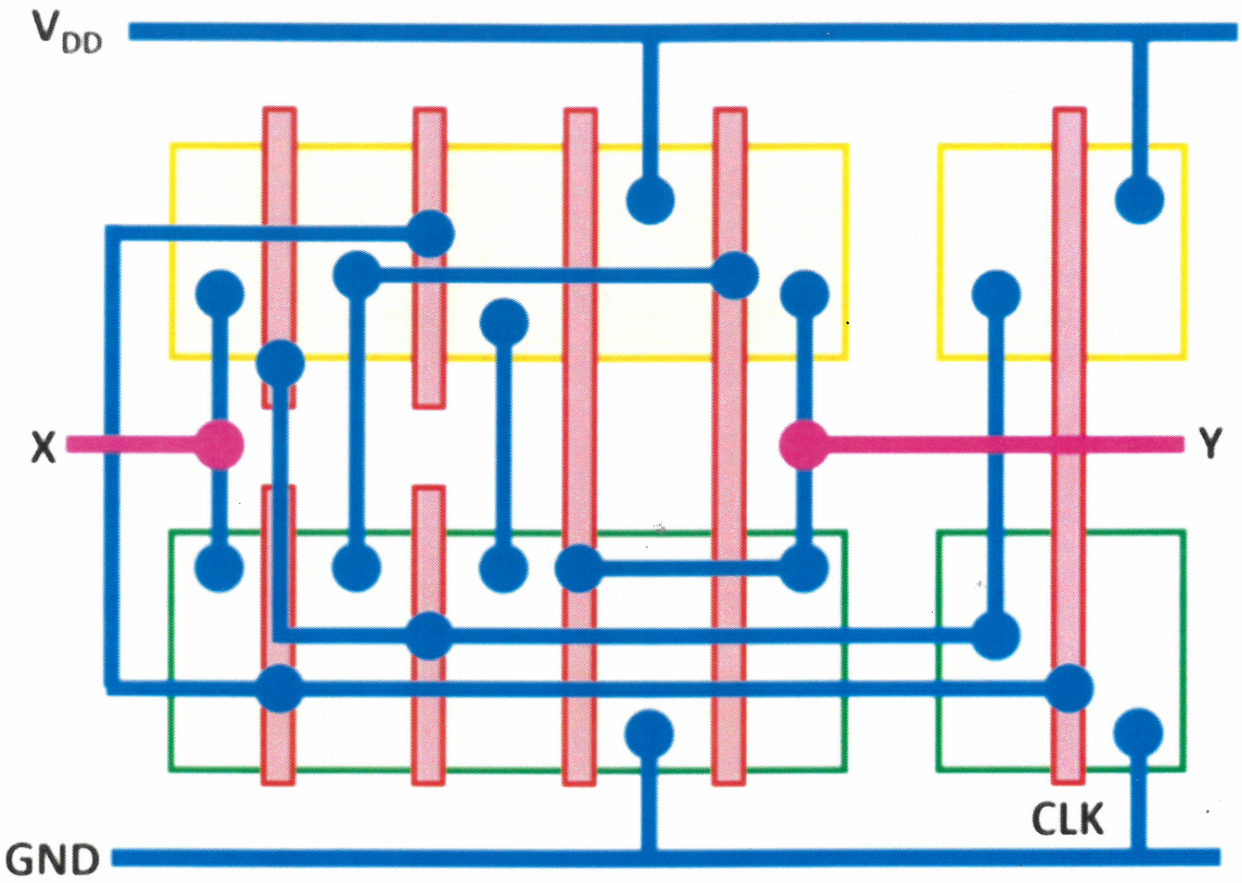
$\Rightarrow f_{max} = 1/290ps = 3.45\ GHz.$

2. a.



b.




V_{DD}
X
Y
CLK
GND