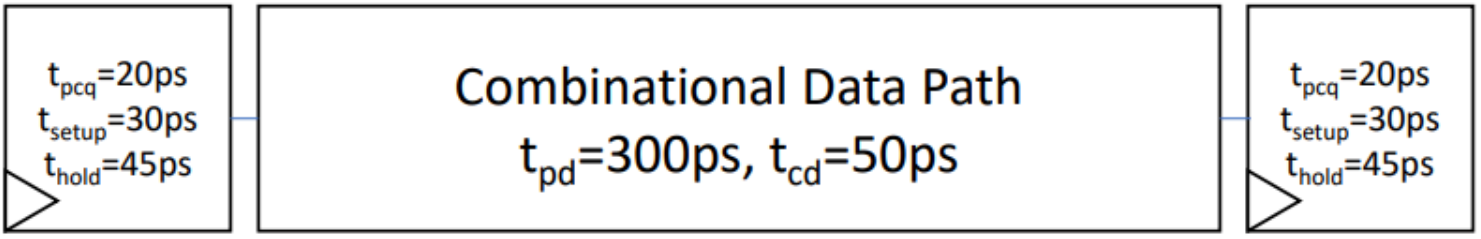
1. Shown below is a combinational path in between two flip-flops.

a) Find the maximum clock frequency this system can operate without violating setup and hold-time constraints.



A young engineer decides to split the combinational block into two stages in order to decrease the propagation delay per stage and increase the clock frequency (shown below). He chooses a clock frequency of 4.8 GHz to support the propagation delay of the longest combinational block.

a. $T_{clk} \geq T_{pcq} + T_{pd} + T_{setup}$.

$T_{clk} \geq 20ps + 300ps + 30ps = 350ps$.

max frequency $= \frac{1}{350ps} = 2.86\,GHz$.

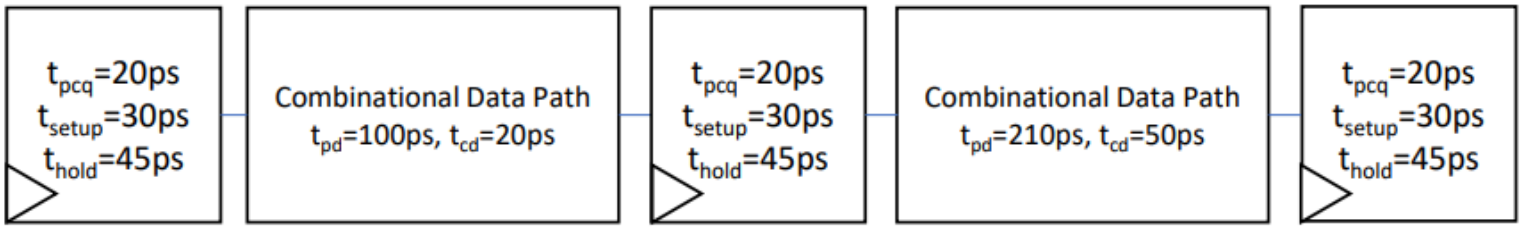
Checking for hold time violations,

$T_{hold} = 45ps$

$T_{pcq} + T_{cd} = 20 + 50 = 70ps$

Since $45ps < 70ps$, hold time is not violated.

b) Find any setup and hold-time violations in this new, pipelined design.



b. $T_{propagation1} = T_{pcq} + T_{pd1} + T_{setup} = 20ps + 100ps + 30ps = 150ps.$

$T_{propagation2} = T_{pcq} + T_{pd2} + T_{setup} = 20ps + 210ps + 30ps = 260ps.$

The clock period has to be based on the greater of the two delays, hence,

$T_{clk,min} = 260ps, \Rightarrow f_{clk,max} = 1/260ps = 3.85GHz$ which is less than 4.8GHz.

$\Rightarrow$ There is a setup violation in stage 2.

$T_{contamination1} = T_{pcq} + T_{cd1} = 20 + 20 = 40ps < 45ps$ (hold time violation).

$T_{contamination2} = T_{pcq} + T_{cd2} = 20 + 50 = 70ps > 45ps$ (no hold time violation).

c) Explain how these timing violations can be resolved?

c. Setup violation can be fixed by decreasing the clock frequency or reducing the propagation delay in stage 2.

Hold violations can be fixed by increasing contamination delay of S1, by, for example, adding buffers to that logic path, or reducing transistor widths.

d) Compare the throughput and latency of the two data-paths.

c. Throughput is proportional to operations per second which is proportional to clock frequency. The max clock frequency in 'a' is 2.9 GHz and the max clock frequency in 'b' is 3.9 GHz, therefore, design b has its throughput increased by $\frac{3.9}{2.9} - 1 = 34.5\%$

Latency is the number of stages multiplied by the clock period.

For design 'a', Latency = 1 x 350 ps = 350 ps

for design 'b', Latency = 2 x 260 ps = 520 ps

design b has $\frac{520}{350} - 1 = 48.57\%$ more latency than design a.

d)

	Original Design	Pipelined Design
latency	300ps	100+210 = 310 ps
Throughput	2.86 GHz	3.85 GHz

Throughput improvement: pipelined design allows for higher frequency, increasing throughput

Latency increases

Pipelined design sacrifices the cost of delay increase by 10 ps but improve throughput

e) Find the maximum clock frequency for both circuits given the clock tree has a maximum skew of 30 ps. Ignore possible hold-time violations.

e. design a, $T_{clk} \geq T_{pcq} + T_{pd} + T_{setup} + T_{skew} = 20ps + 300ps + 30ps + 30ps = 380ps$

$\Rightarrow f_{max} = 1/380ps = 2.63\,GHz$

design b, $T_{clk} \geq \max(T_{pcq} + T_{pd} + T_{setup} + T_{skew}) = \max(20+100+30+30,\ 20+210+30+30)$

$= \max(180ps, 290ps) = 290ps.$

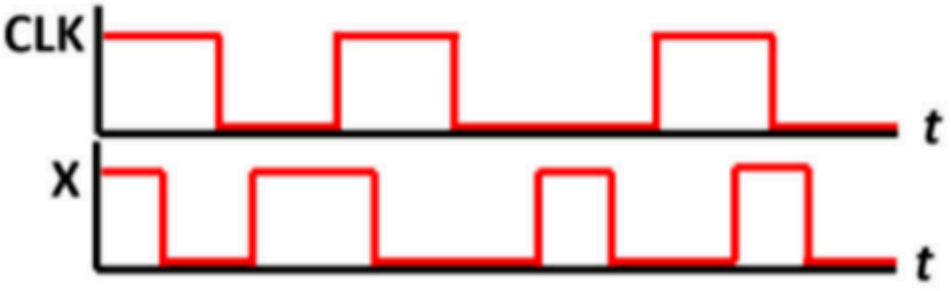
$\Rightarrow f_{max} = 1/290ps = 3.45\,GHz.$

2. Answer the following questions:

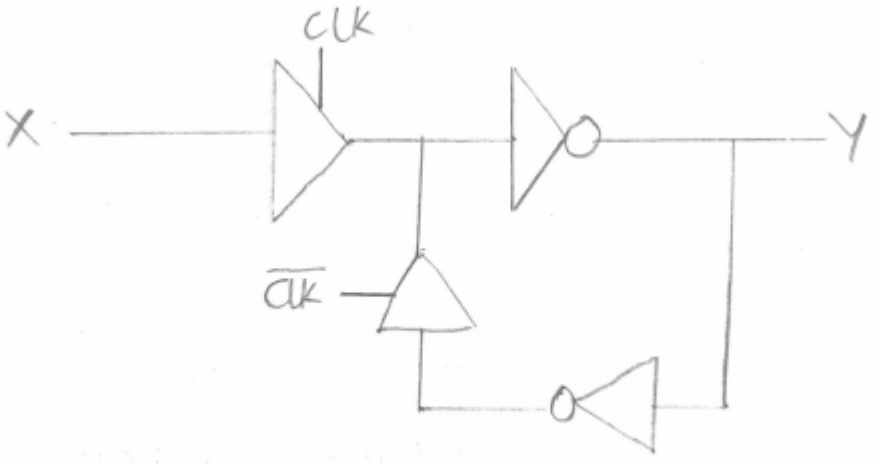
a) Draw the gate-level schematic of an inverting active-high synchronous transparent latch.

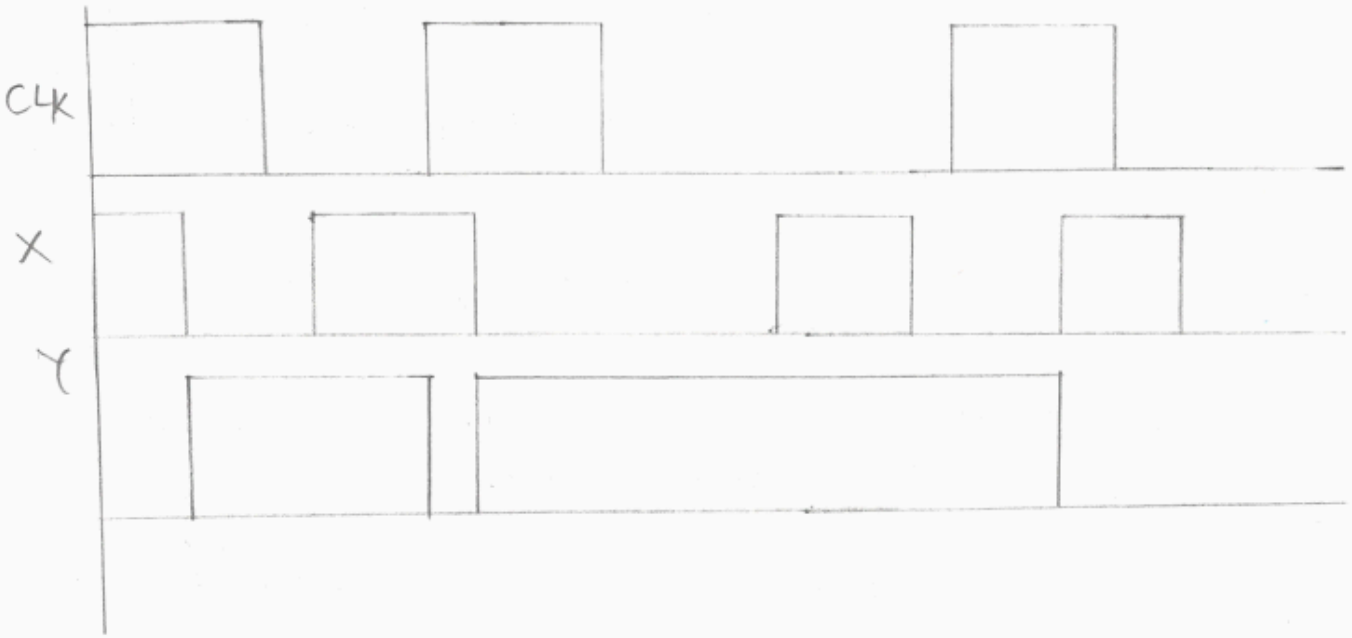
b) Draw the layout for your schematic above.

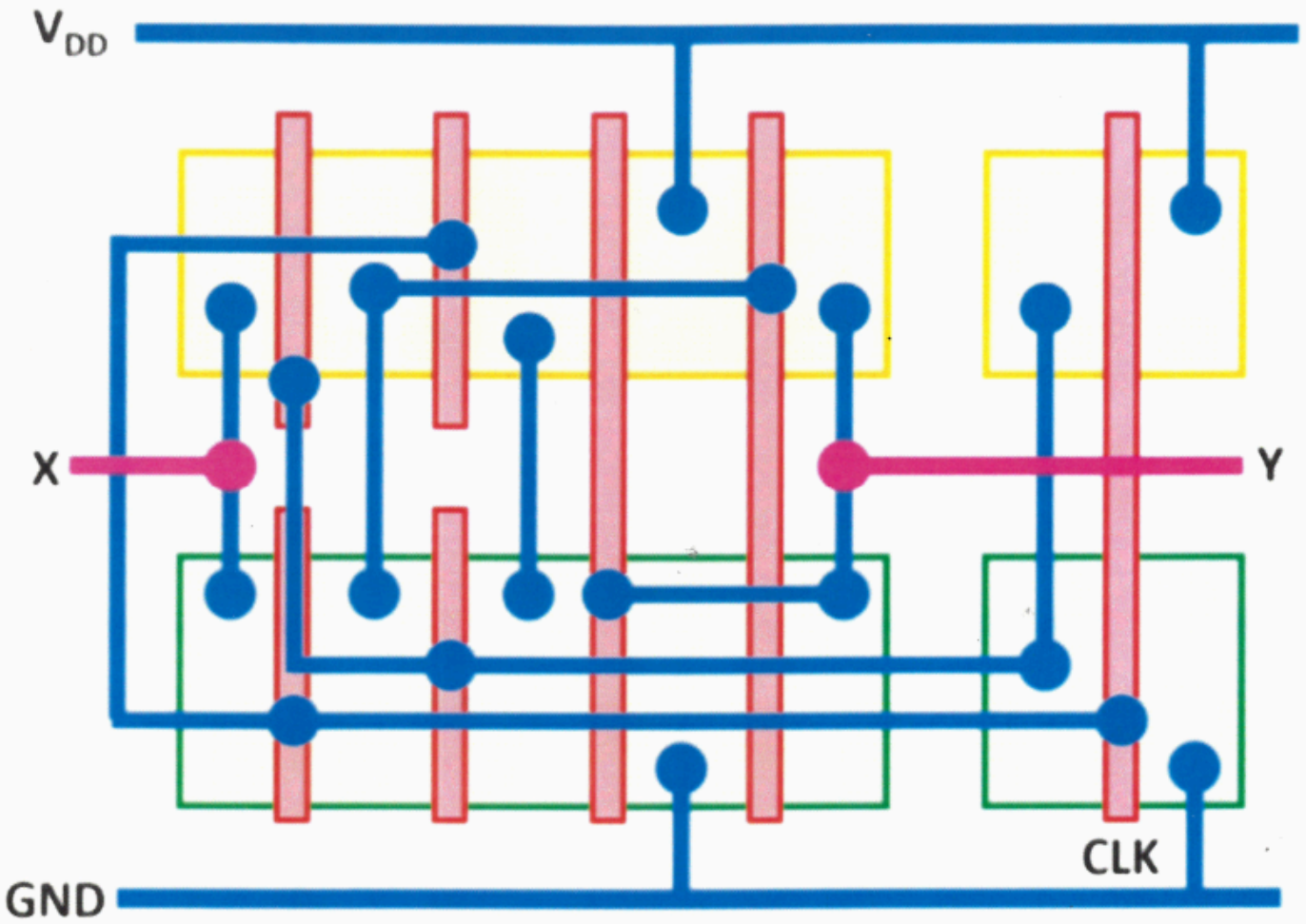
c) Given input waveforms X and CLK, draw the waveform for Y.



2. a.




CLK
X
Y


VDD
X
Y
CLK
GND