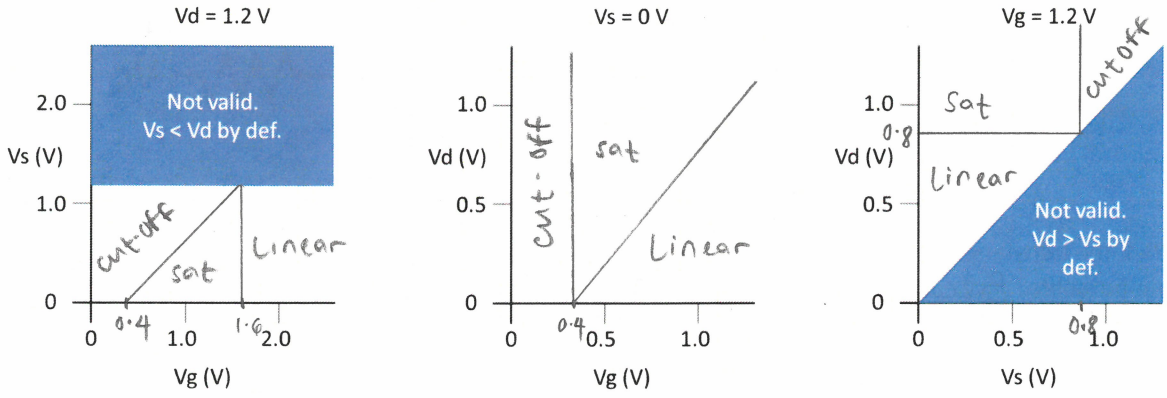
VLSI Spr. 2022, CH2 HW

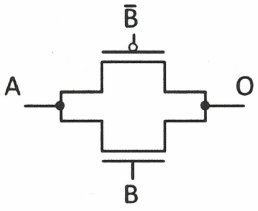
20 1. In an NMOS transistor, Vtn = 0.4 V. Sketch the regions of operation when one of the voltages is held constant. What do you notice?



10 2. N-type Si has better carrier transport properties than P-type Si, so why don't we use NMOS for all of our logic?

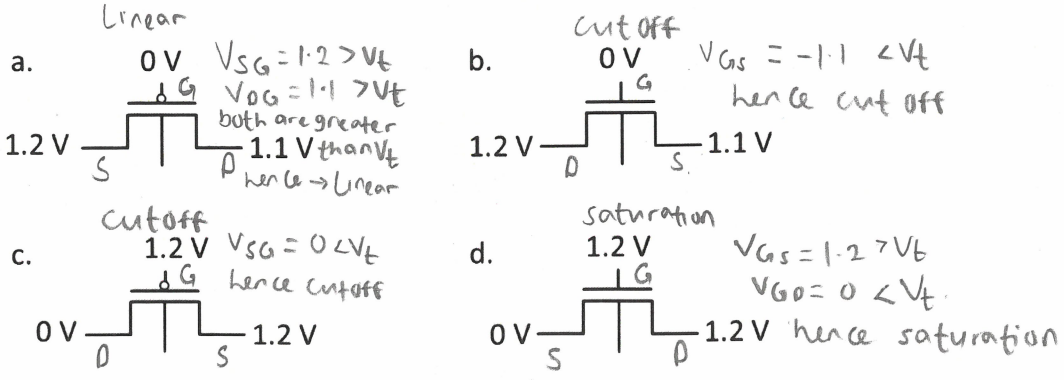
P-type silicon is needed in using PMOS for the pull-up because NMOS is bad in transmitting 1.

10 3. In the following diagram, describe the function of the shown gate (A and B are the inputs)? Why do we need both NMOS and PMOS?



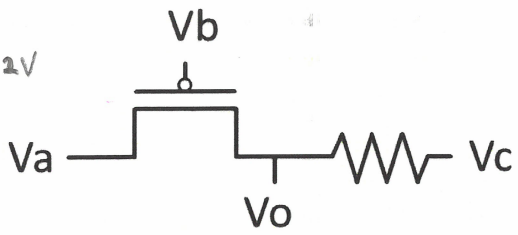
This is a transmission gate or T-gate or Pass gate. The NMOS will be used to pass 0 from 'A' to 'O' when A=0 and the PMOS will be used to pass 1 from 'A' to 'O' when A=1.

10 4. In which operating regions are the following transistors ($v_{tn} = -v_{tp} = 0.4$ V), and identify the terminals (assume there is no leakage and no body effect)?

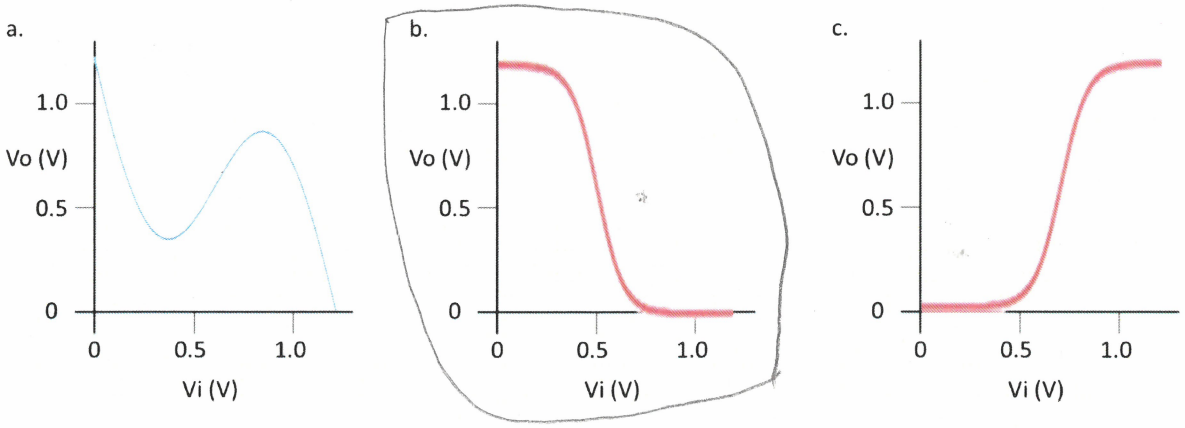


20 5. Calculate Vo in the following circuit when: (assume V_{tp} = 0.4 V and R is large)

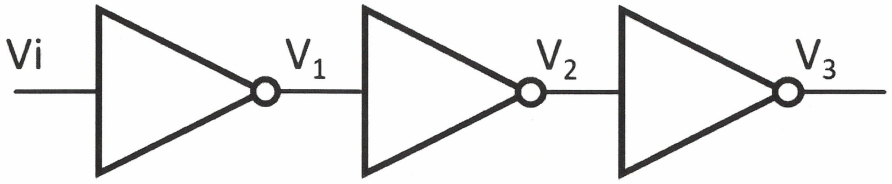
a. Va = 0 V. Vb = 1.2 V. Vc = 1.2 V
cutoff, hence $V_o = V_c = 1.2V$
b. Va = 1.2 V. Vb = 0 V. Vc = 0 V
on, since Pmos passes 1 fully, $V_o = V_a = 1.2V$
c. Va = 0 V. Vb = 0 V. Vc = 1.2 V
$V_o = 0.4V$, when Pmos passes 0, it drops V_{DD} to $V_{tp} = 0.4V$



10 6. Pick the transfer characteristics which describe a stable inverter. Why is it so important that an inverter chain be stable? Because it reduces noise



20 7. In the selected stable graph from Q6 if at Vi an input of '1' is represented by a voltage in [0.8 V, 1.2 V]. and an input '0' is represented by a voltage in [0 V, 0.5 V], then in the inverter chain below, what are the possible output ranges at V_1? What are the possible output ranges at V_2? What are the possible output ranges at V_3.



1 [0.8, 1.2] 0 [0] 1 [1.2] 0 [0]

0 [0, 0.5] 1 [0.6, 1.2] 0 [0, 0.2] 1 [1.19, 1.2]