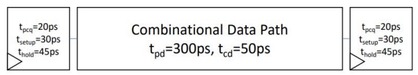
Hw6 vlsi

Thursday, February 27, 2025 11:32 AM

1. Shown below is a combinational path in between two flip-flops.

a) Find the maximum clock frequency this system can operate without violating setup and hold-time constraints.



A young engineer decides to split the combinational block into two stages in order to decrease the propagation delay per stage and increase the clock frequency (shown below). He chooses a clock frequency of 4.8 GHz to support the propagation delay of the longest combinational block.

clock to Q delay $t_{pcq} = 20ps$

setup time $t_{setup} = 30ps$

Hold time $t_{hold} = 45ps$

Propagation delay of combinational path $t_{pd} = 300ps$

Contamination delay of combinational path $t_{cd} = 50ps$

$T_{clk} \geq t_{pcq} + t_{pd} + t_{setup}$

$T_{clk} \geq 20ps + 300ps + 30ps = 350ps$

$t_{pcq} + t_{cd} \geq t_{hold}$

$20ps + 50ps \geq 45ps$

$f_{max} = \frac{1}{T_{clk}} = \frac{1}{350 \times 10^{-12}} = 2.86\ GHz$

b) Find any setup and hold-time violations in this new, pipelined design.

Setup Constraint

$T_{clk} \geq t_{pcq} + t_{pd} + t_{setup}$

First Stage

$t_{pcq} = 20ps$

$t_{pd} = 100ps$

$t_{setup} = 30ps$

$T_{clk} \geq 20 + 100 + 30 = 150ps$

Second Stage

$t_{pcq} = 20ps$

$t_{pd} = 210ps$

$t_{setup} = 30ps$

$T_{clk} \geq 20 + 210 + 30 = 260ps$

The minimum clock period must be at least 260ps

$f_{max} = \frac{1}{260 \times 10^{-12}} = 3.85GHz$

Hold Time Constraint

$t_{pcq} + t_{cd} \geq t_{hold}$

First Stage

$t_{pcq} = 20ps$

$t_{cd} = 20ps$

$t_{hold} = 45ps$

$20 + 20 = 40ps < 45ps$

This violates the hold time constraint

Second Stage

$t_{pcq} = 20ps$

$t_{cd} = 50ps$

$t_{hold} = 45ps$

$20 + 50 = 70ps > 45ps$

This satisfy the hold time constraint

c) Explain how these timing violations can be resolved?

d) Compare the throughput and latency of the two data-paths.

e) Find the maximum clock frequency for both circuits given the clock tree has a maximum skew of 30 ps. Ignore possible hold-time violations.

c) Increase the contamination delay t_{cd} by adding buffer to ensure

$t_{pcq} + t_{cd} \geq t_{hold}$

Reduce t_{hold} by improving flip flop design

Introduce clock skew

(intentional slow down the clock at the second flip flop)

d)

	Original Design	Pipelined Design
latency	300ps	100+210 = 310 ps
Throughput	2.86 GHz	3.85 GHz

Throughput improvement pipelined design allows for higher frequency, increasing throughput

Latency increases

Pipelined design sacrifices the cost of delay increase by 10 ps but improve throughput

e) $t_{skew} = 30ps$

$T_{clk} \geq t_{pcq} + t_{pd} + t_{setup} - t_{skew}$

First Stage

$T_{clk} \geq 20 + 100 + 30 - 30 = 120ps$

$f_{max} = \frac{1}{120 \times 10^{-12}} = 8.33\ GHz$

Second

$T_{clk} \geq 20 + 210 + 30 - 30 = 230ps$

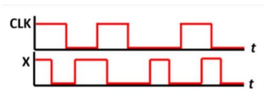
$f_{max} = \frac{1}{230 \times 10^{-12}} = 4.35GHz$

2. Answer the following questions:

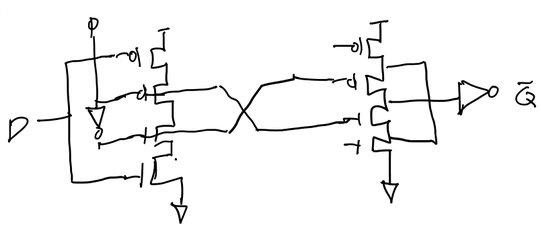
a) Draw the gate-level schematic of an inverting active-high synchronous transparent latch.

b) Draw the layout for your schematic above.

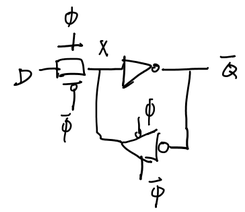
c) Given input waveforms X and CLK, draw the waveform for Y.



a)



b)



c)