VLSI: HW Ch7

1: Assume Dennard constant field scaling. Answer the following: (assume nominal scaling from a 130 nm process to a 32 nm process.) You may use Table 7.4.

a) Assuming the area of a unit inverter before scaling is $0.2\ um^2$, find the area of the unit inverter in the newly scaled technology.
b) Assuming the NMOS gate capacitance in the unit inverter before scaling is $50\ fF$, find the NMOS gate capacitance in the unit inverter in the newly scaled technology.
c) Assuming τ before scaling is $20\ ps$, find τ in the newly scaled technology.
d) Assuming the NMOS ON-resistance in the unit inverter before scaling is 0.1Ω, find R_{ON} in the newly scaled technology.

NOTE: You are expected to bring a copy of whichever tables you anticipate using to the exam, and *reference tables will not be provided during exams.*

2: In a chip, there are 300,000 NAND2 gates, 1,000,000 inverters, 200,000 AOI22 gates and 200,000 NOR2s. If the probability of a defect for NAND2 is 0.000001, the probability of a defect for INV is 0.0000003, the probability of a defective AOI22 is 0.0000045, and the probability of a defective NOR2 is 0.00001. (Assume that if a single gate fails, the entire chip fails.)

a) Find the expected yield of the chip.
b) Suppose the designer wants to increase yield by splitting the design into two separate chips. What is the expected yield of one of these new chips assuming number of gates are divided equally among the two chips.
c) Suppose the designer split the design across three equal chips. What is the expected yield of one of these chips.

3: In a specific manufacturing process, there is approximately one (1) defect for every two (2) square-millimeters.

a) Find the expected yield of a chip that has an area of 2 square-millimeters.
b) Find the expected yield of a chip that has an area of 1 square-millimeter.
c) Find the expected yield of a chip that has an area of 0.5 square-millimeters.

Assume now that the air filter in the clean-room where the wafers are processed has decreased in efficiency and there is now 1 defect per square-millimeter.

d) Re-evaluate the yield for the three chips mentioned above.

4: Solve exercise 7.6 from *Weste, Harris. CMOS VLSI Design: a circuits and systems perspective. 4th edition*. reproduced here: A chip contains 100 11-stage ring oscillators. Each inverter has an average delay of 10 ps with a standard deviation of 1 ps, so the average ring oscillator runs at 4.54 GHZ. The operating frequency of the chip is defined to be the slowest frequency of any of the oscillators on the chip.

a) Find the expected operating frequency of a chip.
b) Find the maximum
target frequency to achieve 99.7% parametric yield.

5: In figure 7.6 in *Weste, Harris. CMOS VLSI Design: a circuits and systems perspective. 4th edition* reproduced below:

a) Label the x and y-axes.
b) Name and explain each of the labeled regions of the chart.
c) Explain the meaning of the chart.