1: Assume Dennard constant field scaling. Answer the following: (assume nominal scaling from a 130 nm process to a 32 nm process.) You may use Table 7.4.

a) Assuming the area of a unit inverter before scaling is $0.2\ um^2$, find the area of the unit inverter in the newly scaled technology.
b) Assuming the NMOS gate capacitance in the unit inverter before scaling is $50\ fF$, find the NMOS gate capacitance in the unit inverter in the newly scaled technology.
c) Assuming τ before scaling is $20\ ps$, find τ in the newly scaled technology.
d) Assuming the NMOS ON-resistance in the unit inverter before scaling is 0.1Ω, find R_{ON} in the newly scaled technology.

NOTE: You are expected to bring a copy of whichever tables you anticipate using to the exam, and *reference tables will not be provided during exams.*

TABLE 7.4 Influence of scaling on MOS device characteristics

Parameter	Sensitivity	Dennard Scaling	Constant Voltage	Lateral Scaling
Scaling Parameters				
Length: L		$1/S$	$1/S$	$1/S$
Width: W		$1/S$	$1/S$	1
Gate oxide thickness: t_{ox}		$1/S$	$1/S$	1
Supply voltage: V_{DD}		$1/S$	1	1
Threshold voltage: V_{tn}, V_{tp}		$1/S$	1	1
Substrate doping: N_A		S	S	1
Device Characteristics				
β	$\frac{W}{L}\frac{1}{t_{ox}}$	S	S	S
Current: I_{ds}	$\beta(V_{DD}-V_t)^2$	$1/S$	S	S
Resistance: R	$\frac{V_{DD}}{I_{ds}}$	1	$1/S$	$1/S$
Gate capacitance: C	$\frac{WL}{t_{ox}}$	$1/S$	$1/S$	$1/S$
Gate delay: τ	RC	$1/S$	$1/S^2$	$1/S^2$
Clock frequency: f	$1/\tau$	S	S^2	S^2
Switching energy (per gate): E	CV_{DD}^2	$1/S^3$	$1/S$	$1/S$
Switching power dissipation (per gate): P	Ef	$1/S^2$	S	S
Area (per gate): A		$1/S^2$	$1/S^2$	1
Switching power density	P/A	1	S^3	S
Switching current density	I_{ds}/A	S	S^3	S

130nm ⇒ 32nm

S (scaling Factor) $= \frac{130}{32} = 4.06$

a) Area of unit inverter

$$A' = \frac{A}{S^2} = \frac{0.2\ \mu m^2}{(4.06)^2} = \frac{0.2}{16.48} \approx \boxed{0.0121\ um^2}$$

b) Scaled NMOS Gate capacitance

$$C' = \frac{C}{S} = \frac{50\ fF}{4.06} \approx \boxed{12.32\ fF}$$

c) Scaled Gate Delay

$$\tau' = \frac{\tau}{S} = \frac{20\ PS}{4.06} = \boxed{4.93\ PS}$$

d) Scaled NMOS R_{ON}

$$R' = R = \boxed{0.1\Omega}$$

a. $S = \frac{130nm}{32nm} = 4.0625$.

Area scales by $1/S^2 = 0.06059$

$A_{new} = 0.06059 \times A_{old} = 0.06059 \times 0.2\,\mu m^2 = 0.012122\,\mu m^2$.

b. Capacitance scales by $1/S = 0.2462$.

$C_{new} = 1/S \times C_{old} = 0.2462 \times 50\,ff = 12.31\,fF$.

c. τ scales by $1/S = 0.2462$

$\tau_{new} = 1/S \times \tau_{old} = 0.2462 \times 20\,ps = 4.92\,ps$.

d. R is constant in Denard scaling $\Rightarrow R_{new} = R_{old} = 0.1\,\Omega$.

2: In a chip, there are 300,000 NAND2 gates, 1,000,000 inverters, 200,000 AOI22 gates and 200,000 NOR2s. If the probability of a defect for NAND2 is 0.000001, the probability of a defect for INV is 0.0000003, the probability of a defective AOI22 is 0.0000045, and the probability of a defective NOR2 is 0.00001. (Assume that if a single gate fails, the entire chip fails.)

a) Find the expected yield of the chip.
b) Suppose the designer wants to increase yield by splitting the design into two separate chips. What is the expected yield of one of these new chips assuming number of gates are divided equally among the two chips.
c) Suppose the designer split the design across three equal chips. What is the expected yield of one of these chips.

NAND2	300000 gates	defect probability (P_d) = 0.00 0001
INV	1000000 gates	P_d = 0.0000003
AOI 22	200 000 gates	P_d = 0.0000045
NOR 2	200000 gates	P_d = 0.00001

$$\sum (N_i P_{di}) = (300000 \cdot 0.000001) + (1000000 * 0.0000003) + (200000 * 0.0000045) + (200000 * 0.00001)$$

$$= 0.3 + 0.3 + 0.9 + 2.0 = 3.5$$

$$Y = e^{-3.5} = \boxed{0.0302}$$

b) Split into 2 chips

$$\sum (N_i P_{di})_{new} = \frac{3.5}{2} = 1.75$$

$$Y = e^{-1.75} \approx \boxed{0.173}$$

c) Split into 3 chips

$$\sum (N_i P_{di})_{new} = \frac{3.5}{3} = 1.167$$

$$Y = e^{-1.167} \approx \boxed{0.311}$$

2a. Prob(all NAND2 are good) $= (1 - 0.000001)^{350,000} = 74.1\%$

Prob(all INV are good) $= (1 - 0.0000003)^{1,000,000} = 74.1\%$

Prob(all AOI22 are good) $= (1 - 0.00000045)^{200,000} = 40.7\%$

Prob(all NOR2 are good) $= (1 - 0.00001)^{200,000} = 13.5\%$

Yield = $\prod$ Prob $= 3.02\%$.

b. Prob(NAND2) $= (1 - 0.000001)^{150,000} = 86.1\%$

Prob(INV) $= (1 - 0.0000003)^{500,000} = 86.1\%$

Prob(AOI22) $= (1 - 0.00000045)^{100,000} = 63.8\%$

Prob(NOR2) $= (1 - 0.00001)^{100,000} = 36.8\%$

Yield $= 17.4\%$

c. Prob(NAND2) $= (1 - 0.000001)^{100,000} = 90.5\%$

Prob(INV) $= (1 - 0.0000003)^{333,333} = 90.5\%$

Prob(AOI22) $= (1 - 0.00000045)^{66,667} = 74.1\%$

Prob(NOR2) $= (1 - 0.00001)^{66,667} = 51.3\%$

Yield $= 31.1\%$.

3: In a specific manufacturing process, there is approximately one (1) defect for every two (2) square-millimeters.

a) Find the expected yield of a chip that has an area of 2 square-millimeters.
b) Find the expected yield of a chip that has an area of 1 square-millimeter.
c) Find the expected yield of a chip that has an area of 0.5 square-millimeters.

Assume now that the air filter in the clean-room where the wafers are processed has decreased in efficiency and there is now 1 defect per square-millimeter.

d) Re-evaluate the yield for the three chips mentioned above.

Defect rate before air filter inefficiency

$D = 1$ defect per $2mm^2$

Defect rate after air filter inefficiency

$D = 1$ defect per $1mm^2$

$$Y = e^{-DA}$$

a) $2mm^2$

$$Y = e^{-(\frac{1}{2})2} = \boxed{0.3679}$$

b) $1mm^2$

$$Y = e^{-(\frac{1}{2})1} \simeq \boxed{0.6065}$$

c) $0.5mm^2$

$$Y = e^{-(\frac{1}{2})0.5} \simeq \boxed{0.7788}$$

d) recevaluat with Defect rate $D' = 1$ defect per mm^2

i) $Y = e^{-1 \cdot 2} = \boxed{0.1353}$ ($2mm^2$)

ii) $Y = e^{-1.1} = \boxed{0.3679}$ ($1mm^2$)

iii) $Y = e^{-1.0.5} = \boxed{0.6065}$ ($0.6mm^2$)

The reduced efficiency of the air filter decreases chip yield

39. Using Poisson's model.

Yield $= e^{-AD} = e^{-2mm^2 \times 1/2mm^2} = e^{-1} = 36.8\%$

b. Yield $= e^{-1mm^2 \times 1/2mm^2} = e^{-1/2} = 60.65\%$.

c. Yield $= e^{-0.5mm^2 \times 1/2mm^2} = e^{-1/4} = 77.88\%$.

d.

a. Yield $= e^{-2mm^2 \cdot 1/1mm^2} = e^{-2} = 13.53\%$

b. Yield $= e^{-1mm^2 \times 1/1mm^2} = e^{-1} = 36.8\%$.

c. Yield $= e^{-0.5mm^2 \times 1/1mm^2} = e^{-0.5} = 60.65\%$.

4: Solve exercise 7.6 from *Weste, Harris. CMOS VLSI Design: a circuits and systems perspective. 4th edition*. reproduced here: A chip contains 100 11-stage ring oscillators. Each inverter has an average delay of 10 ps with a standard deviation of 1 ps, so the average ring oscillator runs at 4.54 GHZ. The operating frequency of the chip is defined to be the slowest frequency of any of the oscillators on the chip.

a) Find the expected operating frequency of a chip.
b) Find the maximum
target frequency to achieve 99.7% parametric yield.

TABLE 7.9 Behavior of maximum of normal variables

N	E[M]	σ(M)
2	0.56	0.82
10	1.54	0.59
100	2.50	0.43
1000	3.24	0.35
10,000	3.85	0.30
100,000	4.40	0.28

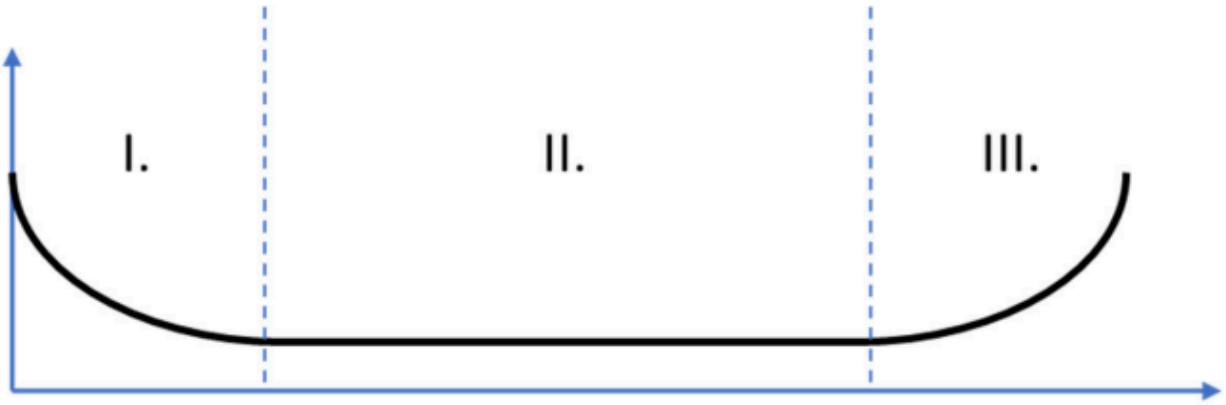
4. Inverter Variance = (standard deviation)^2 = (1ps)^2 = 1 ps^2
Expected delay of ring oscillator has a mean of 11 x 10ps = 110ps.
Ring Oscillator also has a variance of 11 x 1ps^2 = 11 ps^2
⇒RO standard deviation = $\sqrt{11 ps^2}$ = 3.317ps.
From table 7.9, Maximum of 100 ROs will have a mean of 110ps + (2.5 x 3.22ps)
= 118ps.
and standard deviation = 0.43 x 3.22ps
= 1.38ps

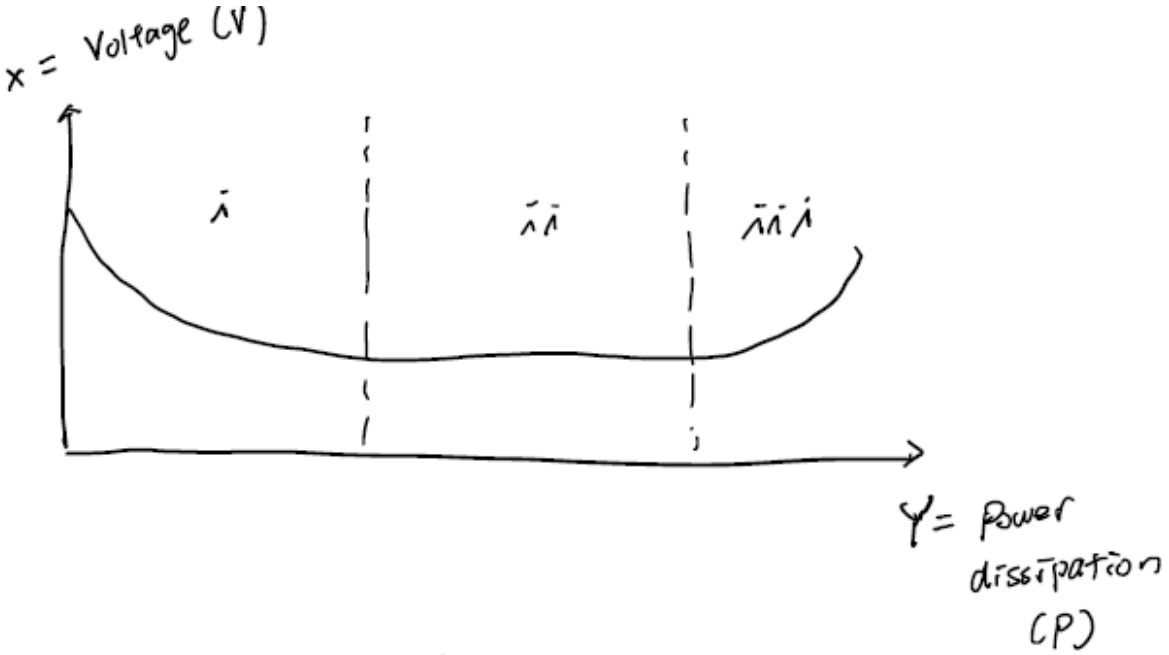
a. Period = 2x118ps = 236ps (Positive & negative edge).
frequency = 1/236ps = 4.24 GHz.

b. 99.7% is μ + 3σ (mean + [3 x standard deviation]) ⇒ Delay = 118 + (3x1.38)
= 122ps.
Period = 2 x 122 = 244ps ⇒ f = 1/244ps = 4.10 GHz.

5: In figure 7.6 in *Weste, Harris. CMOS VLSI Design: a circuits and systems perspective. 4th edition* reproduced below:

a) Label the x and y-axes.
b) Name and explain each of the labeled regions of the chart.
c) Explain the meaning of the chart.





I = Sub threshold leakage Region

low Voltage

Power dissipation ↑ due to leakage

II = ideal operating Region

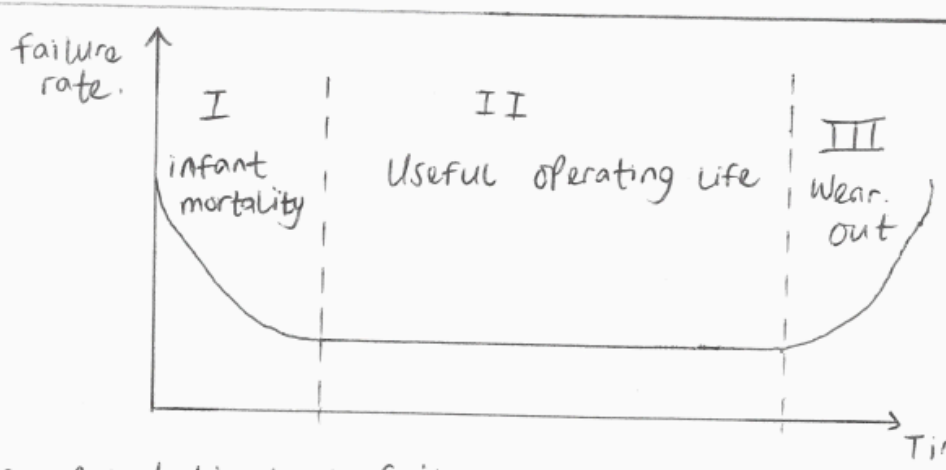
optimal for CMOS

$P = CV^2f$

c)

This chart illustrates the trade-off between **power dissipation and supply voltage** in CMOS circuits.
Lowering voltage reduces power consumption but can lead to **subthreshold leakage** issues.
Increasing voltage improves performance but causes excessive power dissipation.
The **optimal region (Region II)** represents the best balance between **power efficiency and performance**.

5.



Chips are most likely to fail really early or have a long life. A good idea to weed out chips that will fail early is to stress chips during testing.