Homework 3

1)a) $P(C_1) = P(a) \cdot P(b) = 0.5 \times 0.25 = 0.125$

~~$P(C_2) = P(c) \mid -(P(c) \cdot P(d)) = 1 - (0.75 \times 0.5) =$~~

$P(C_2) = 1 - (\overline{P(c)} \cdot \overline{P(d)}) = 1 - ((1-0.75)(1-0.5)) = 0.875$

$P(C_3) = P(C_1) \cdot P(C_2) = 0.125 \times 0.875 = 0.109375$

$P(C_4) = 1 - P(C_3) = 1 - 0.109375 = 0.890625$

b.) $\alpha(C_1) = P(C_1) \cdot \overline{P(C_1)} = 0.109375$

$\alpha(C_2) = P(C_2) \cdot \overline{P(C_2)} = 0.109375$

$\alpha(C_3) = P(C_3) \cdot \overline{P(C_3)} = 0.0974$

$\alpha(C_4) = P(C_4) \cdot \overline{P(C_4)} = 0.0974$

c.) $P_{switching}(C_1) = \alpha(C_1) \cdot C_1 \cdot V_{DD}^2 \cdot f$

$= 0.109375 \times 2 \times 10^{-6} \times 1.2^2 \times 2.5 \times 10^9 = 787.5\,W$

$P_{switching}(C_2) = 0.109375 \times 5 \times 10^{-6} \times 1.2^2 \times 2.5 \times 10^9 = 1968.75\,W$

~~P.S~~ $P_{switching}(C_3) = 0.0974 \times 0.5 \times 10^{-6} \times 1.2^2 \times 2.5 \times 10^9 = 175.32\,W$

$P_{switching}(C_4) = 0.0974 \times 17 \times 10^{-6} \times 1.2^2 \times 2.5 \times 10^9 = 5960.88\,W$

d) $P_{total} = 787.5\,W + 1968.75\,W + 175.32\,W + 5960.88\,W = 8892.45\,W$

2.a) You can either use Power gating ~~or clock gating~~ to disconnect the voltage ~~or clock source~~ from the circuit when it is dormant. or operate at a lower voltage (e.g 50% of V_{dd}) or reduce the transistor width.

b.) By operating at a lower V_{dd}, e.g 50% of V_{dd} → Power $\propto \frac{\text{Voltage}^2}{R}$

$$\frac{\text{Power}_{new}}{\text{Power}_{old}} = \frac{\text{Voltage}_{new}^2}{\text{Voltage}_{old}^2} = \frac{(0.5\,V_{old})^2}{V_{old}^2} = 0.5^2 = 0.25$$

Power savings $= 1 - 0.25 = 0.75$ (75%)

Assuming the circuit is idle 50% of the time, savings = (75%)(50%) = 37.5%

c.) Power gating circuit is needed leading to added area and delay. Also, for the operation at 50% of V_{dd} requires voltage domain crossing circuitry. Finally, by reducing the transistor width, you have less drive for the transistor leading to longer latency.

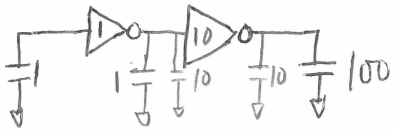
3.) 1 stage

$D = 1 \times 100 + 1 = 101$

$E \propto C_{tot} = (2 \times 1) + 100 = 102$

$EDP \propto 101 \times 102 = 10302$

2 stages

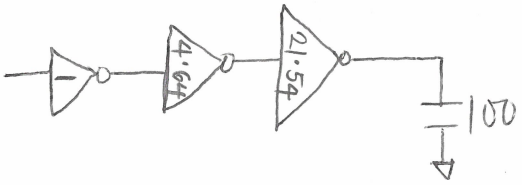


$D = 2 \times \sqrt[2]{100} + 2 = 22$

$E \propto C_{tot} = (2 \times 1) + (2 \times 10) + 100 = 122$

$EDP \propto 22 \times 122 = 2684$

3 stages

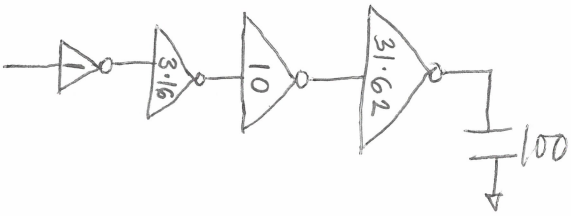


$D = 3 \times \sqrt[3]{100} + 3 = 16.92$

$E \propto C_{tot} = 2(1 + 4.64 + 21.54) + 100 = 154.36$

$EDP \propto 16.92 \times 154.36 = \boxed{2611.77}$

4 stages



$D = 4 \times \sqrt[4]{100} + 4 = 16.65$

$E \propto C_{tot} = 2(1 + 3.16 + 10 + 31.62) + 100 = 191.56$

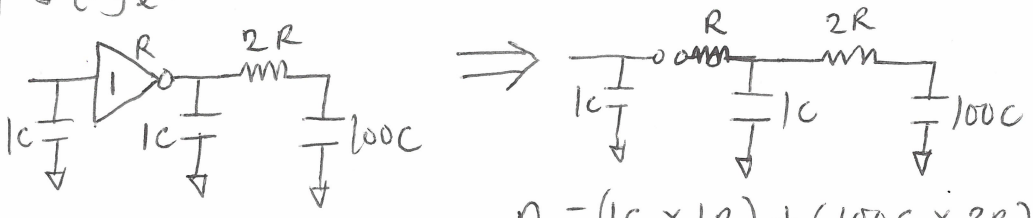
$EDP \propto 16.62 \times 191.56 = 3183.73$

Minimum EDP occurs for 3 stages.

4.)

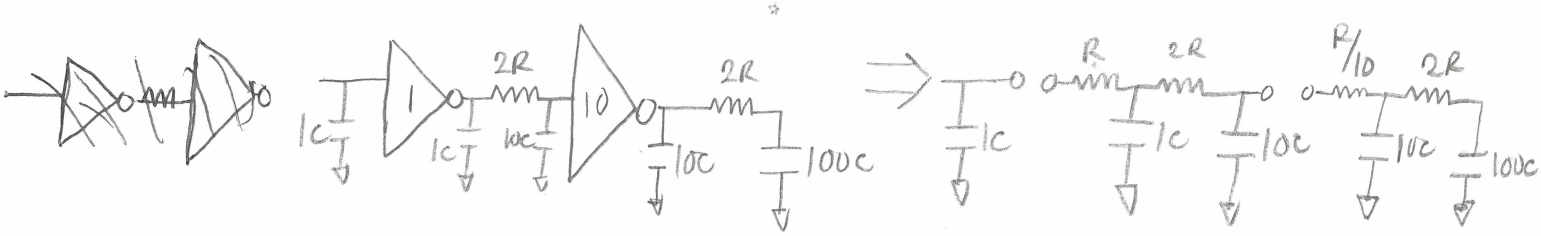
	L doubles	W doubles	d doubles	h doubles	E doubles	S doubles
R	doubles	halves	–	halves	–	doubles
L	doubles	non-linear	–	non-linear	–	–
C	doubles	–	halves	doubles	doubles	–

5.) 1 stage.



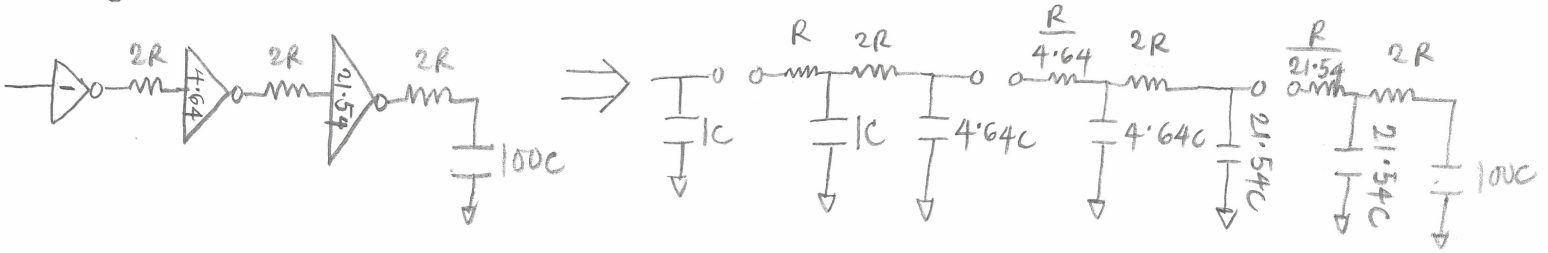
$D = (1C \times 1R) + (100C \times 3R) = RC + 300RC = 301RC$
$= 301\tau$

2 stages



$D = (1C \times 1R) + (10C \times 3R) + (10C \times \frac{R}{10}) + (100C \times \frac{21}{10}R) = RC + 30RC + RC + 210RC$
$= 242RC = \boxed{242\tau}$

3 stages



$\text{Delay} = RC\left[(1\times1) + (3\times4\cdot64) + (4\cdot64\times\frac{1}{4\cdot64}) + (21\cdot54\times2\cdot216) + (21\cdot54\times\frac{1}{21\cdot54}) + (100\times2\cdot046)\right]$

$= 269\cdot25RC = 269\cdot25\tau$

Minimum $\overset{\text{delay}}{=}$ 2 stages.