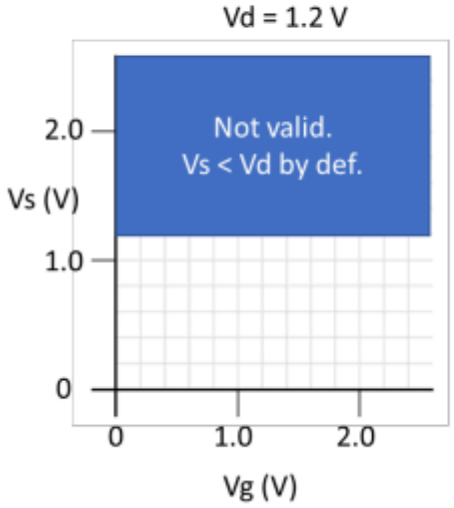
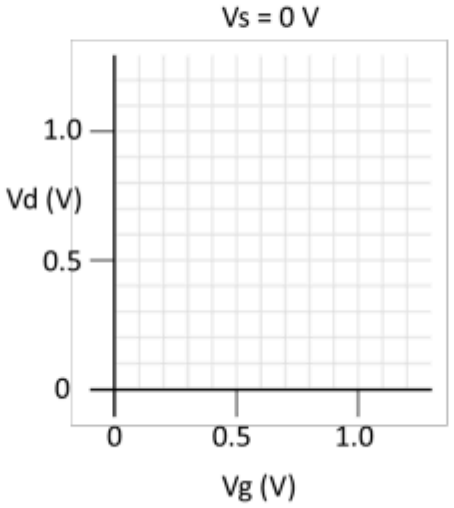
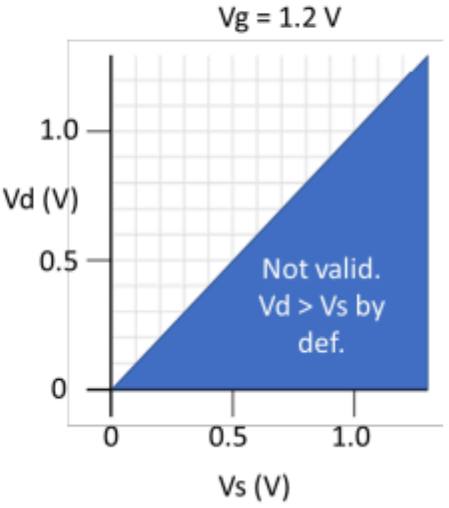
1. In an NMOS transistor, Vtn = 0.4 V. Sketch the regions of operation when one of the voltages is held constant. What do you notice?







NMOS

cutoff regions: $V_{GS} < V_{tn}$ OFF

Linear regions: $V_{GS} \geq V_{tn}$ and $V_{DS} < V_{GS} - V_{tn}$ ON

Saturation regions: $V_{GS} \geq V_{tn}$ and $V_{DS} \geq V_{GS} - V_{tn}$ ON = V_S

$V_{tn} = 0.4V$ Not valid when $V_D > V_S$

$V_D = 1.2V$ V_S has to be $< 1.2V$

V_G can be any

a.

Cutoff: $V_G < V_S + 0.4V$

Saturation: $V_S + 0.4V \leq V_G \leq 1.6V$

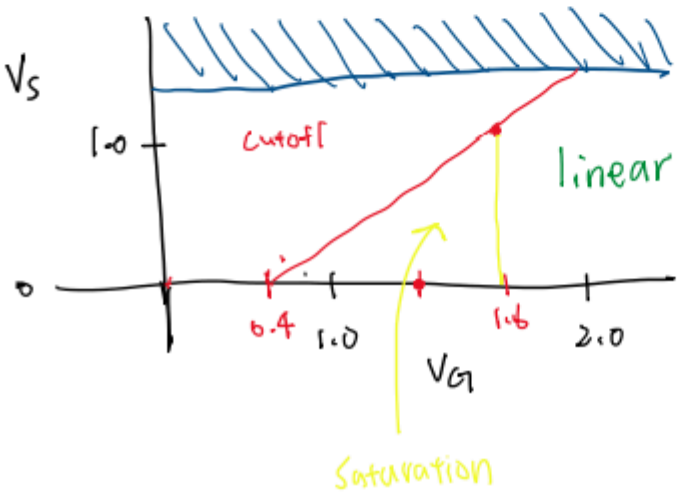
Linear: $V_G > 1.6V$

V_S: $0 \sim 1.19$

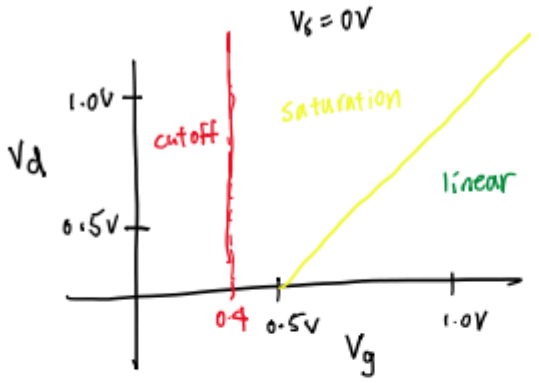
V_D: 1.2

V_G: any

$0 \sim \infty$



b.



$V_G - V_S < 0.4V$

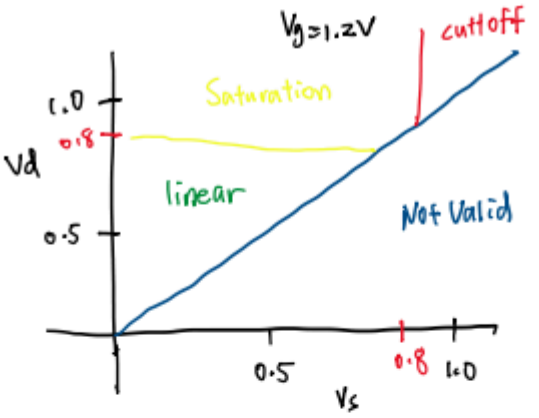
$V_S = 0V$

$V_G < 0.4V \Rightarrow$ cuttoff

$V_{DS} < V_{GS} - V_{th}$

$V_D < V_G - 0.4$

c.



$V_G - V_S < 0.4V$

$1.2 - V_S < 0.4V$

$-V_S < -0.8V$

$V_S > 0.8V$ Cuttoff

$V_{DS} < V_{GS} - V_{th}$

$V_D < V_G - 0.4$

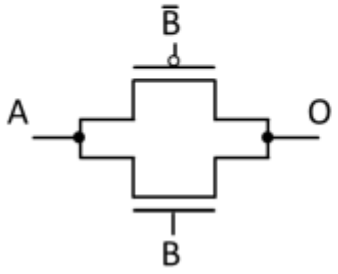
$V_D < 1.2 - 0.4 = 0.8$

$V_D < 0.8$ linear

2. N-type Si has better carrier transport properties than P-type Si, so why don't we use NMOS for all of our logic?

Base on what I had read in ch1 and ch2, NMOS has better transport properties due to higher mobility of electrons compare to holes, which are primary charge carriers in PMOS. PMOS was suffering from poor performance, yield, and reliability. However, nMOS was also suffering from power consumption since NMOS draws static power. This is cause by the logic of NMOS transistor pull it down effectively when low (0), but if the output is high (1), PMOS will be needed to connect the output to the power supply. Hence, CMOS (NMOS + PMOS) is the prefered choice for modern logic circuit. It offers low power consumption, high speed and high performance, and noise robustness.

3. In the following diagram, describe the function of the shown gate (A and B are the inputs)? Why do we need both NMOS and PMOS?



This is a CMOS Logic gate

A and B are the inputs

O is the output

pull-down

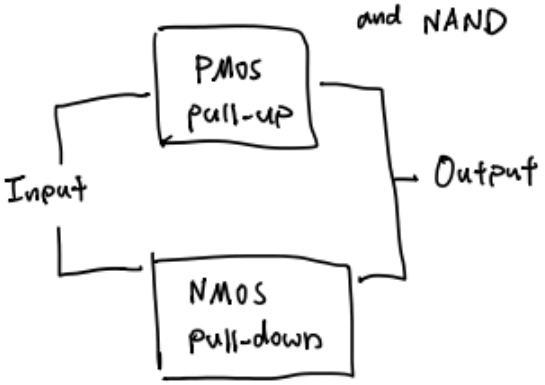
		g=0	g=1	
nMOS	s—d	OFF	ON	s—d
PMOS	s—d	ON	OFF	s—d

pull-up

The nMOS transistors is connecting at the bottom to ground

The pMOS transistors is connecting at the top to power supply (VDD)

This is the inverter (NOT gate) and NAND



O = 0 GND

O = 1 VDD

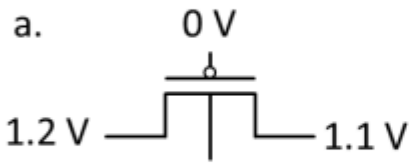
	Pull-up OFF	Pull-up ON
pull-down OFF	Z	1 (VDD)
pull-down ON	0 (GND)	crowbarred ($V_{DD} \rightarrow$ GND)

CMOS provide lower power consumption, high speed, and high performance

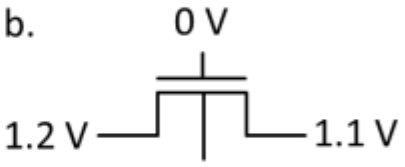
This is why we need both NMOS and PMOS for CMOS

4. In which operating regions are the following transistors ($v_{tn} = -v_{tp} = 0.4$ V), and identify the terminals (assume there is no leakage and no body effect)?

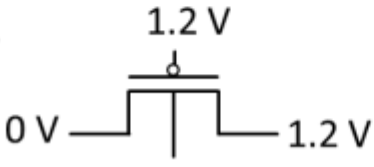
a.



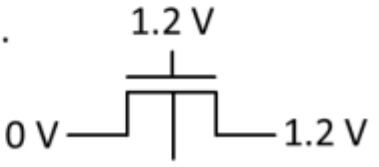
b.

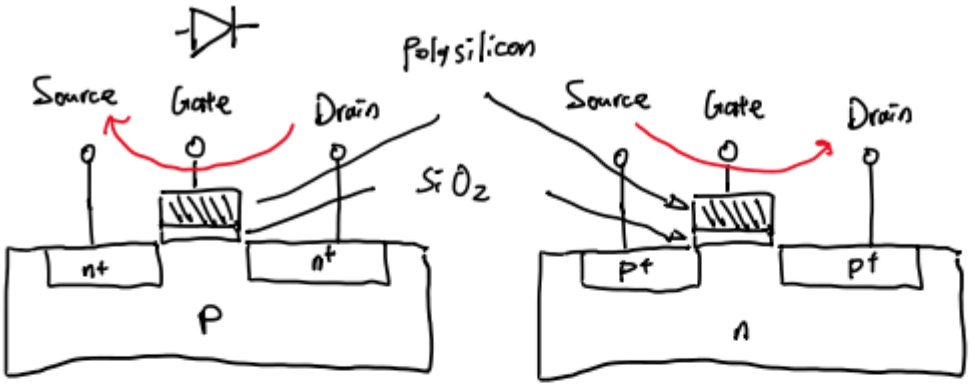


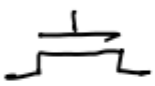
c.



d.





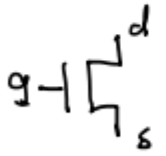


nMOS

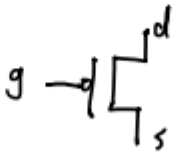
I from drain to source

PMOS

I from Source to drain



Typical connect to ground (GND)



Typical connect to supply voltage (V_{CC})

assume $V_{tn} = 0.4\,V$ for NMOS

$V_{tp} = -0.4\,V$ for PMOS

a.

Terminals: $S = 1.2V$, $G = 0V$, $D = 1.1V$

PMOS

cutoff regions: $V_{SG} < |V_{tp}|$

Linear regions: $V_{SG} \geq |V_{tp}|$ and $V_{SD} < V_{SG} - |V_{tp}|$

Saturation regions: $V_{SG} \geq |V_{tp}|$ and $V_{SD} \geq V_{SG} - |V_{tp}|$

$V_{SG} = V_S - V_G = 1.2V - 0V = 1.2V$

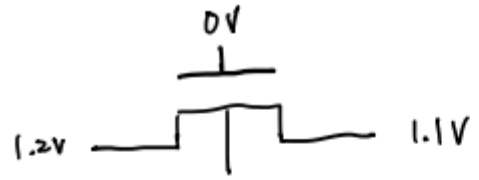
$1.2V > 0.4V$ ✗ cutoff

$V_{SD} = V_S - V_D = 1.2V - 1.1V = 0.1V$

$0.1V < 1.2V - 0.4 = 0.8V$

option A is PMOS and is in linear regions

b.



Terminals: $S = 1.2V$, $G = 0V$, $D = 1.1V$

NMOS

cutoff regions: $V_{GS} < V_{tn}$

Linear regions: $V_{GS} \geq V_{tn}$ and $V_{DS} < V_{GS} - V_{tn}$

Saturation regions: $V_{GS} \geq V_{tn}$ and $V_{DS} \geq V_{GS} - V_{tn}$

$$V_{GS} = V_G - V_S = 0 - 1.2V = -1.2V$$

$$-1.2V < 0.4V$$

Option B is NMOS and it is in cutoff regions

C.

Terminals: S = 0V, G = 1.2V, D = 1.2V

PMOS

$$V_{SG} = V_S - V_G = 0V - 1.2V = -1.2V$$

$$-1.2V < |-0.4|$$

option C is PMOS and is in cutoff regions

D.

Terminals: S = 0V, G = 1.2V, D = 1.2V

NMOS

$V_{GS} = V_G - V_S = 1.2V - 0V = 1.2V$

$V_{GS} < V_{tn}$ $1.2V > 0.4V$ (X cutoff)

$V_{DS} = V_D - V_S = 1.2V - 0V = 1.2V$

$V_{DS} = 1.2V > V_{GS} - V_{tn} = 1.2V - 0.4V = 0.8V$

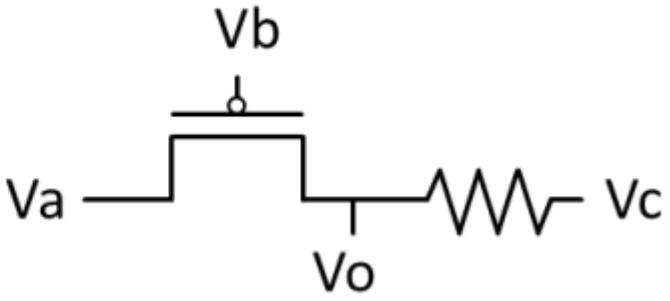
option D is NMOS and it is in saturation regions

5. Calculate Vo in the following circuit when: (assume $V_{tp} = 0.4$ V and R is large)

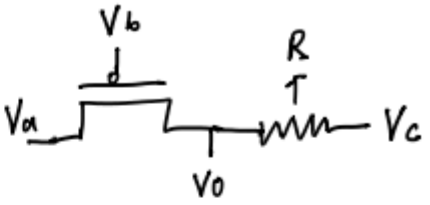
a. Va = 0 V. Vb = 1.2 V. Vc = 1.2 V

b. Va = 1.2 V. Vb = 0 V. Vc = 0 V

c. Va = 0 V. Vb = 0 V. Vc = 1.2 V



a. $V_a = 0V$, $V_b = 1.2V$, $V_C = 1.2V$



Terminals: $S = 0V$, $G = 1.2V$, $D = 1.2V$

R is large so current flow is minimal

$V_{tp} = -0.4V$

PMOS

ON: $V_{SG} \geq |V_{tp}|$

OFF: $V_{SG} < |V_{tp}|$

$V_{SG} = V_S - V_G = 0V - 1.2V = -1.2V$

$-1.2V < 0.4V$ (OFF)

When PMOS is OFF, $V_O = V_D = V_C$

$\boxed{V_O = 1.2V}$

b.

Terminals: $S = 1.2V$, $G = 0V$, $D = 0V$

$V_{SG} = 1.2V - 0V = 1.2V$

$1.2V > 0.4V$ (ON)

when PMOS is ON, $V_O = V_S = V_a$

$\boxed{V_O = 1.2V}$

c.

Terminals: $S = 0V$, $G = 0V$, $D = 1.2V$

$V_{SG} = 0V - 0V = 0$

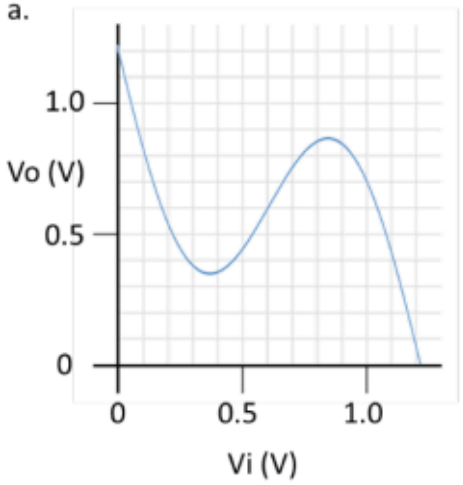
$0V < 0.4V$ (OFF)

when PMOS is OFF, $V_O = V_D = V_c$

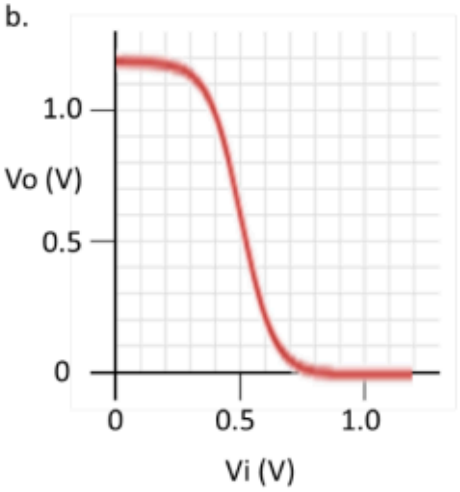
$\boxed{V_O = 1.2V}$

6. Pick the transfer characteristics which describe a stable inverter. Why is it so important that an inverter chain be stable?

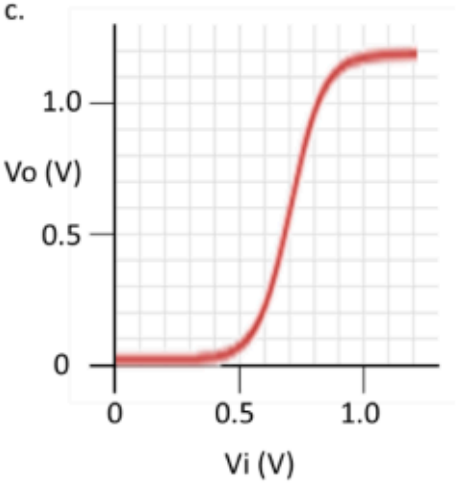
a.

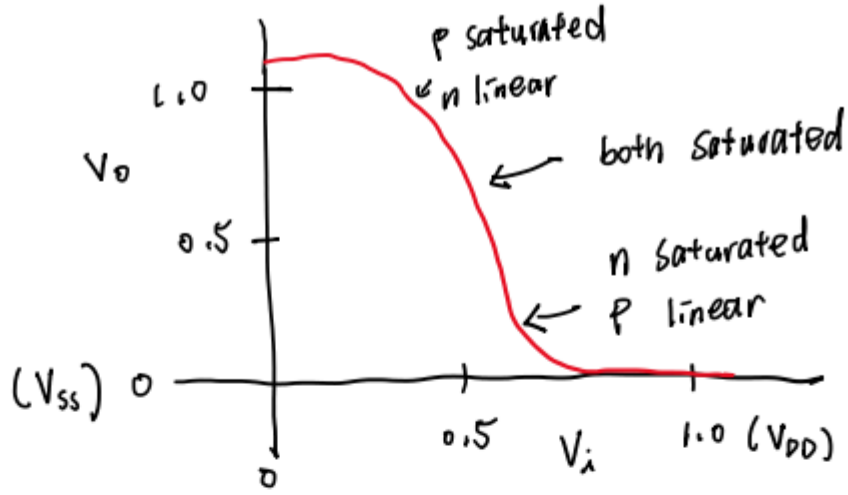


b.



c.





option A seems highly nonlinear and unstable

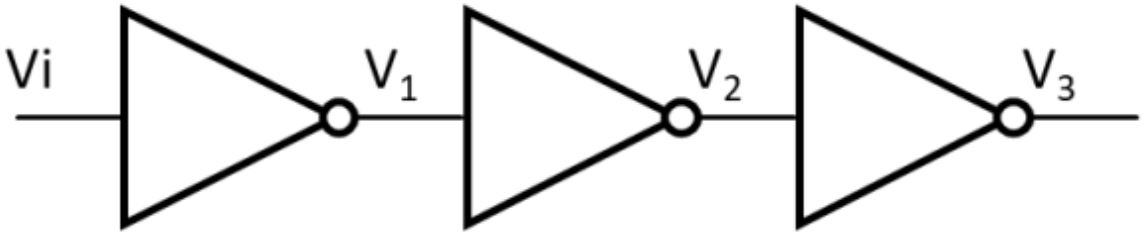
option C seems stable but not ideal for an inverter

option B is a stable inverter. As we can see that at a low input voltage we have a high output votage and high input votage we have a low input voltage. and these correspond to different combination of states of those pull up and pull down transistors. For example, with low input voltages the p-type transistor is saturated and n-type is linear.

Why is it important that an inverter chain be stable?

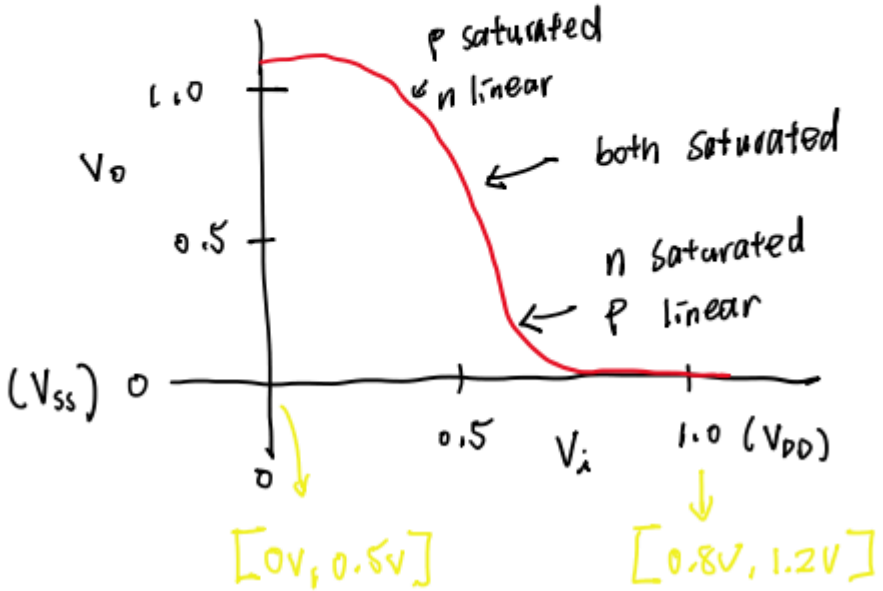
Stability ensures reliable, efficient, and predictable performance in digital circuits

7. In the selected stable graph from Q6 if at Vi an input of '1' is represented by a voltage in [0.8 V, 1.2 V] and an input '0' is represented by a voltage in [0 V, 0.5 V], then in the inverter chain below, what are the possible output ranges at V_1? What are the possible output ranges at V_2? What are the possible output ranges at V_3.



V_{in} ⇒ 1 (High) [0.8 V, 1.2V]

0 (Low) [0V, 0.5V]



① Input = V_i , output = V_1

If V_i = [0.8, 1.2], V_1 will output [0V, 0.5V]

If V_i = [0 V, 0.5V] V_1 will output [0.8V, 1.2V]

② Input = V_1 , output = V_2

If V_1 = [0.8V, 1.2V] V_2 will output [0V, 0.5V]

If V_1 = [0 V, 0.5V] V_2 will output [0.8V, 1.2V]

③ Input = V_2 , output = V_3

If V_2 = [0.8V, 1.2V] V_3 will output [0V, 0.5V]

If V_2 = [0 V, 0.5V] V_3 will output [0.8V, 1.2V]