1. Implement the following function:

$$Y = \overline{AB + C}$$

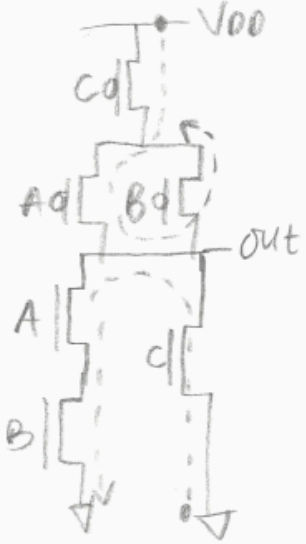
a) Draw a stick diagram implementing the function in the CMOS logic family.
b) Draw an optimized schematic of this function implemented in Pass-Transistor Logic (PTL) with an output inverter.
c) Draw a schematic of the function implemented in pseudo-NMOS.

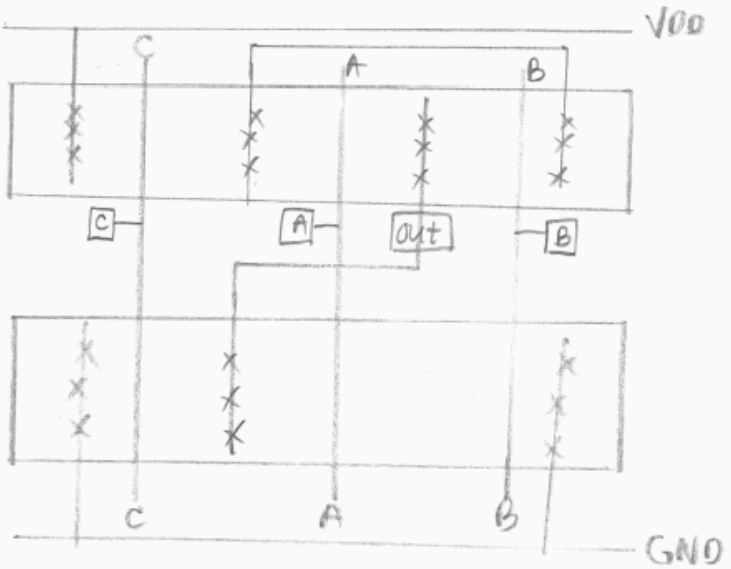
NMOS: + parallel
· → series

PMOS · → parallel
+ → series

1a. $\overline{AB+C}$

DET = CAB





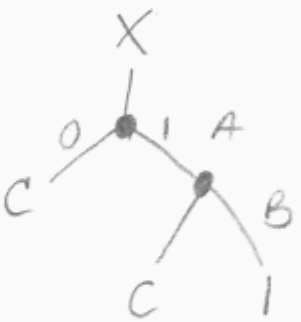
Pass Transistor Logic with an inverter

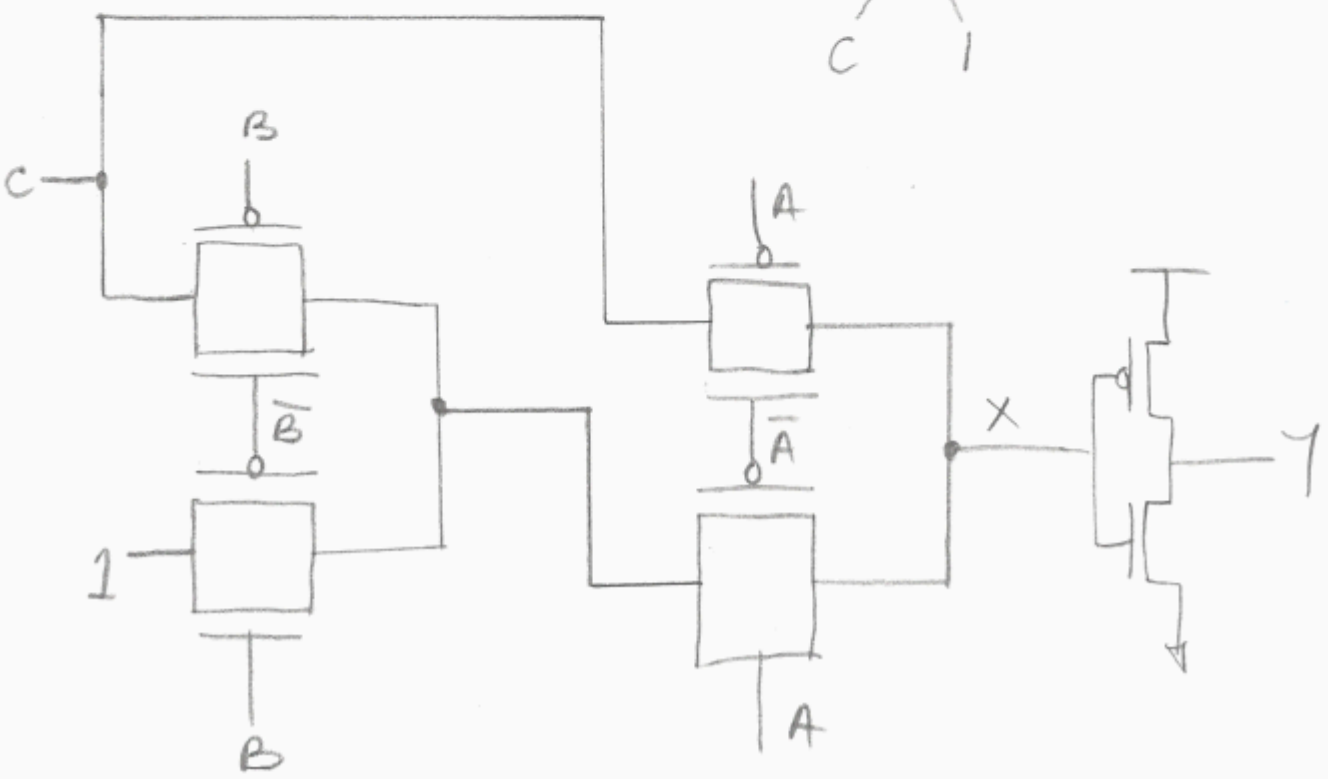
↳ low power circuit

avoid leakage

b. $Y = \overline{AB+C} \rightarrow X = \bar{Y} = AB+C$

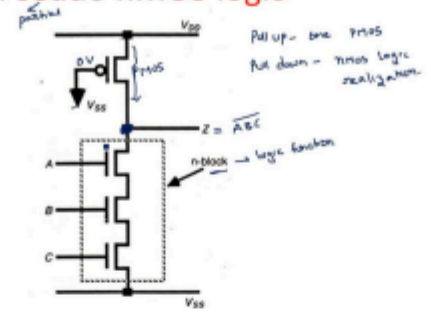
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

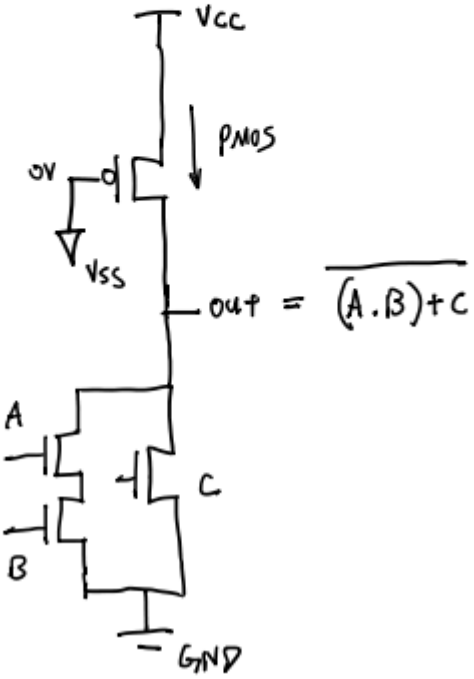




c)

Pseudo nMOS logic





2. For the functions in **a** and **b**:

i) Draw the schematic that performs the function
ii) Use **dual Euler paths** to find the minimum number of diffusion breaks, clearly show your work
iii) Draw **stick diagram** providing best layout with minimum number of diffusion breaks
iv) Draw the exact corresponding schematic for your layout in **'iii'** (if this is same as **'i'** don't redraw but mention **'same as i'**)

a $out = (A+B+C)(D+E(F+G))(H+I)J$

b $out = \overline{ABC+D(E+FG)+HIJK+LM}$

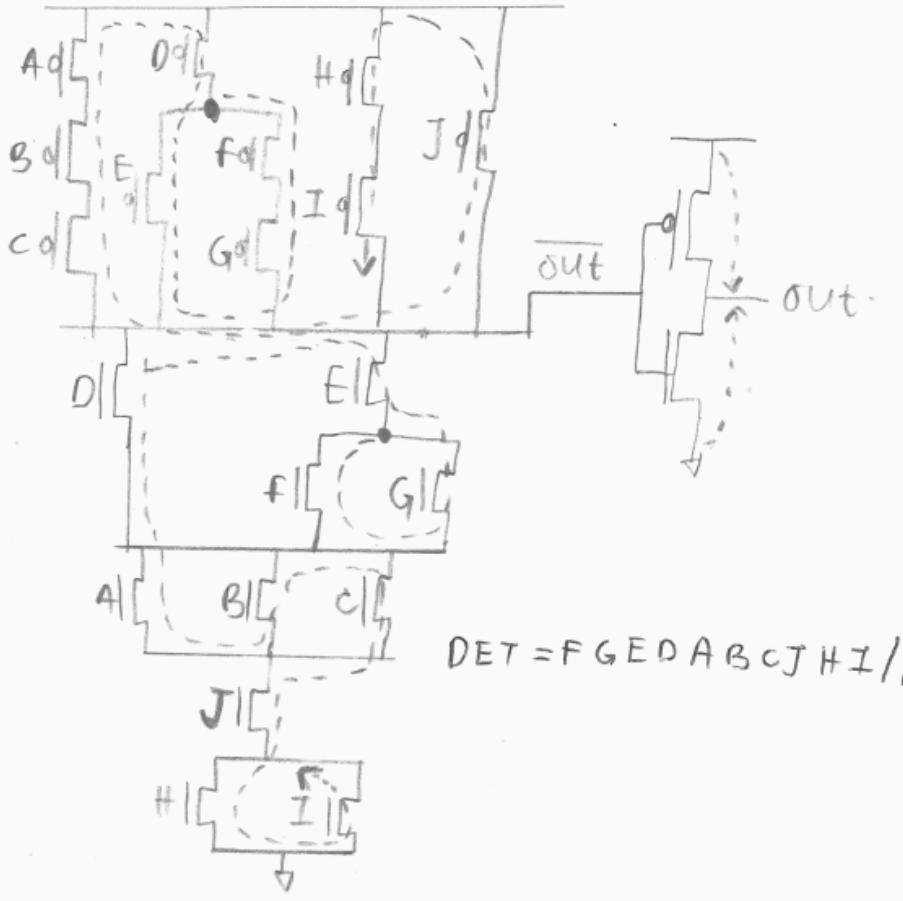
$$(A+B+C)(D+E(F+G)(H+I)J$$

NMOS: + parallel
· → series

PMOS · → parallel
+ → series

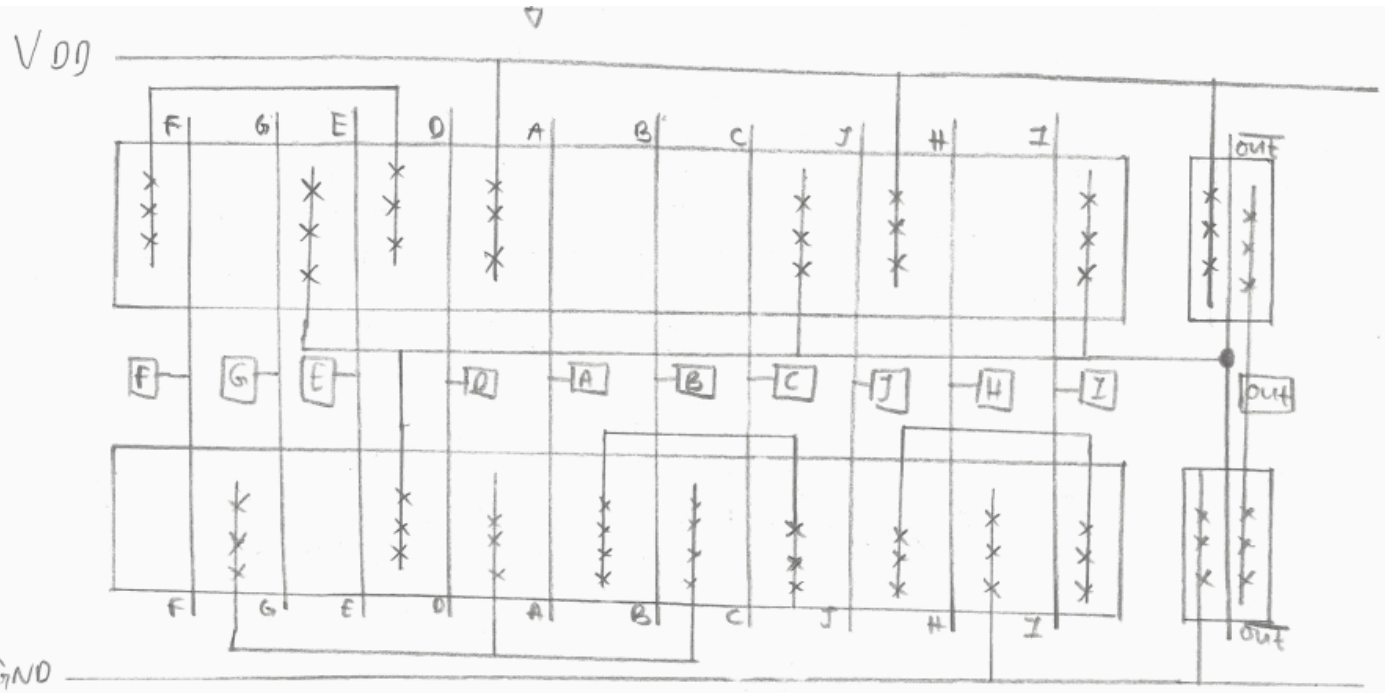
2a.
i
8
ii

$$Out = \overline{(A+B+C)(D+E(F+G))(H+I)J}$$



DET = FGEDABCJHI // $\overline{out}$

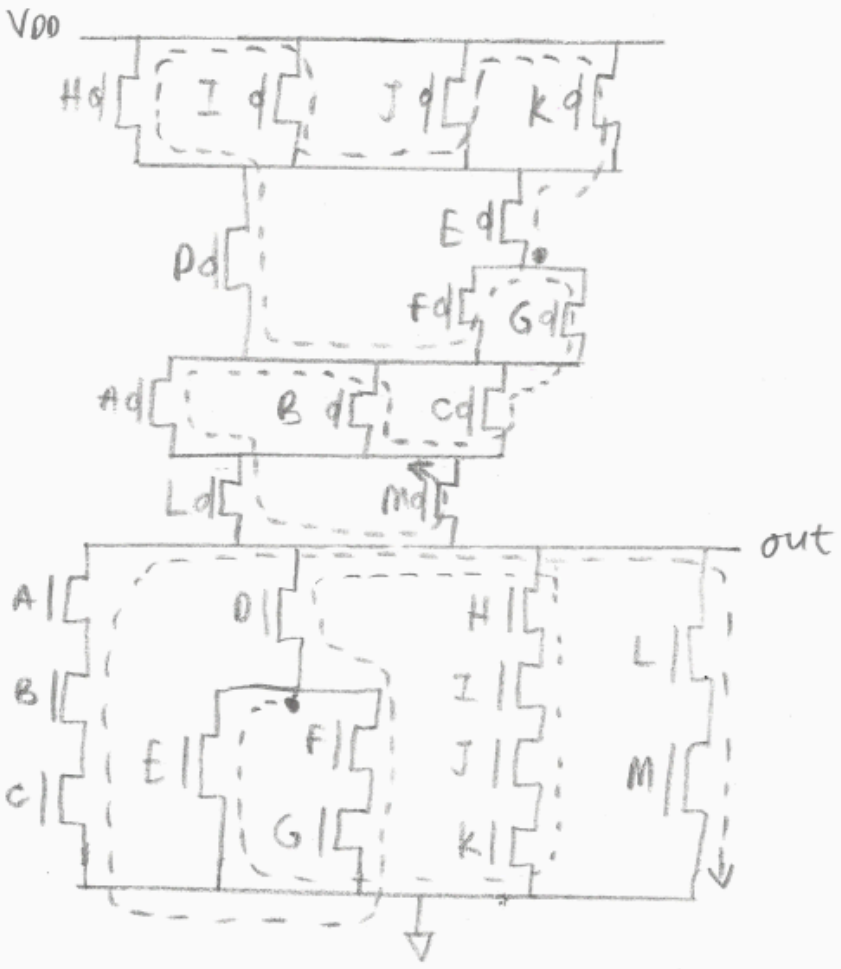
iii



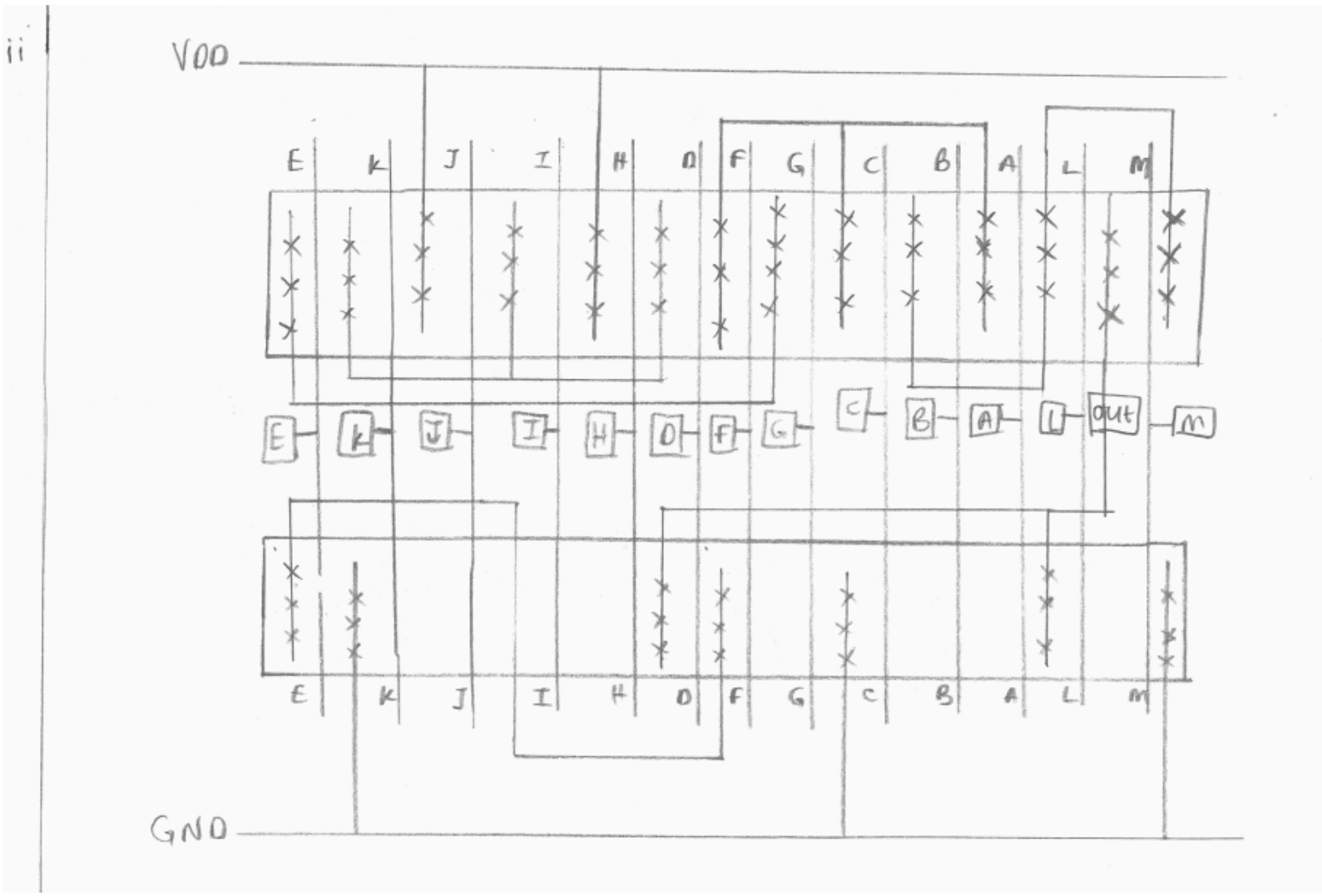
2b)

i&

ii

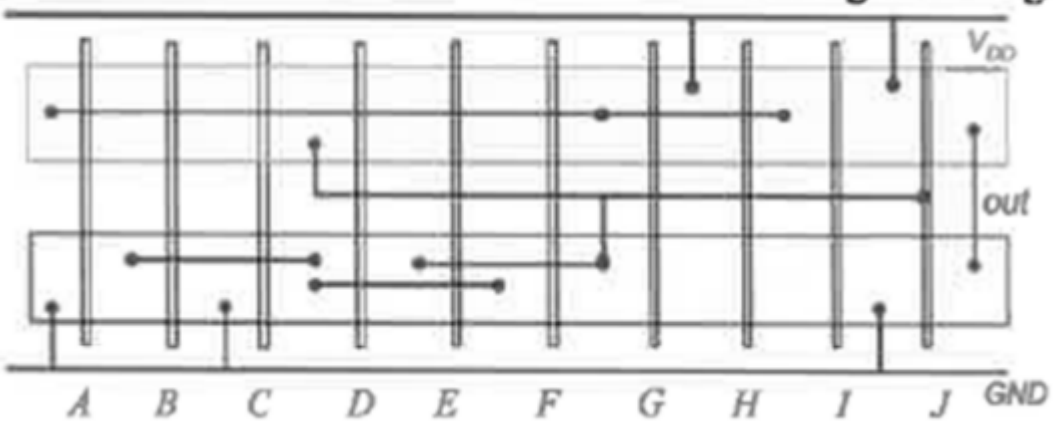


DET = EkJIHDFGCBALM

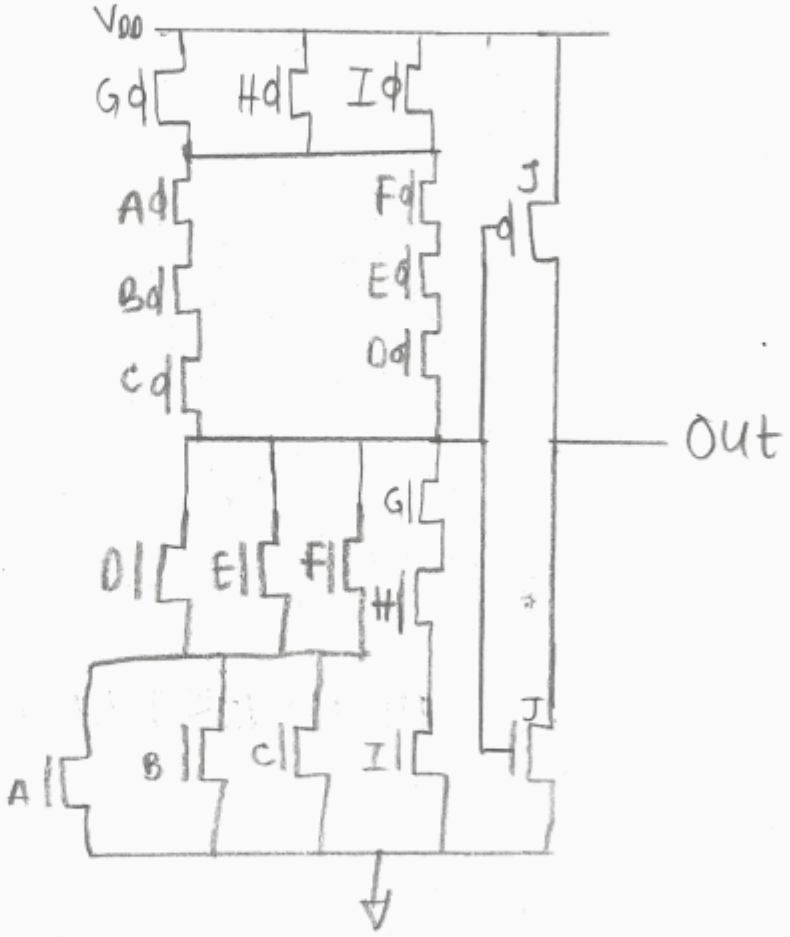


3. **Write down the Boolean functions for the following stick diagrams:**

a.



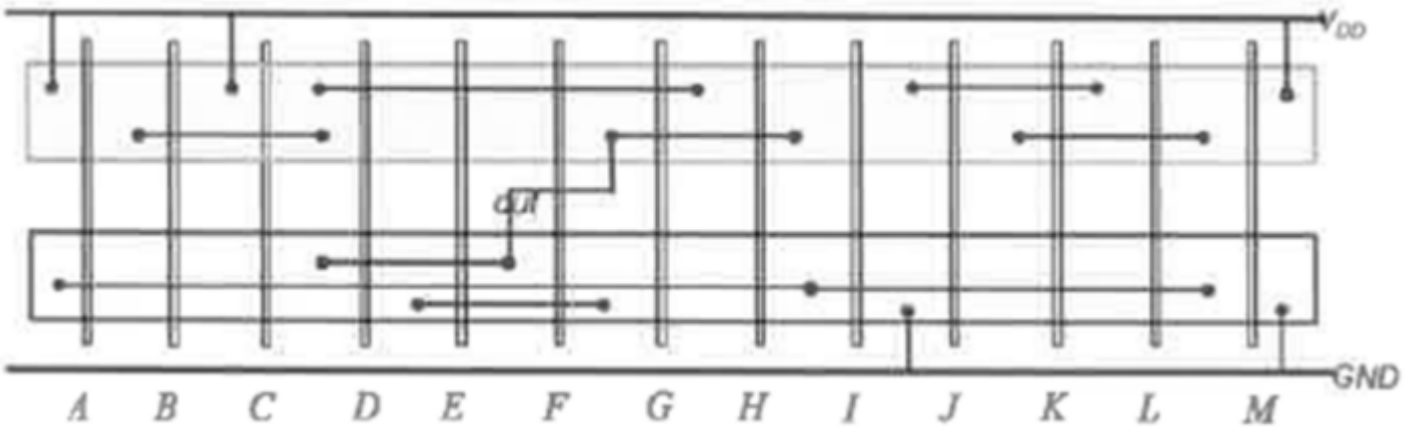
3.
a.



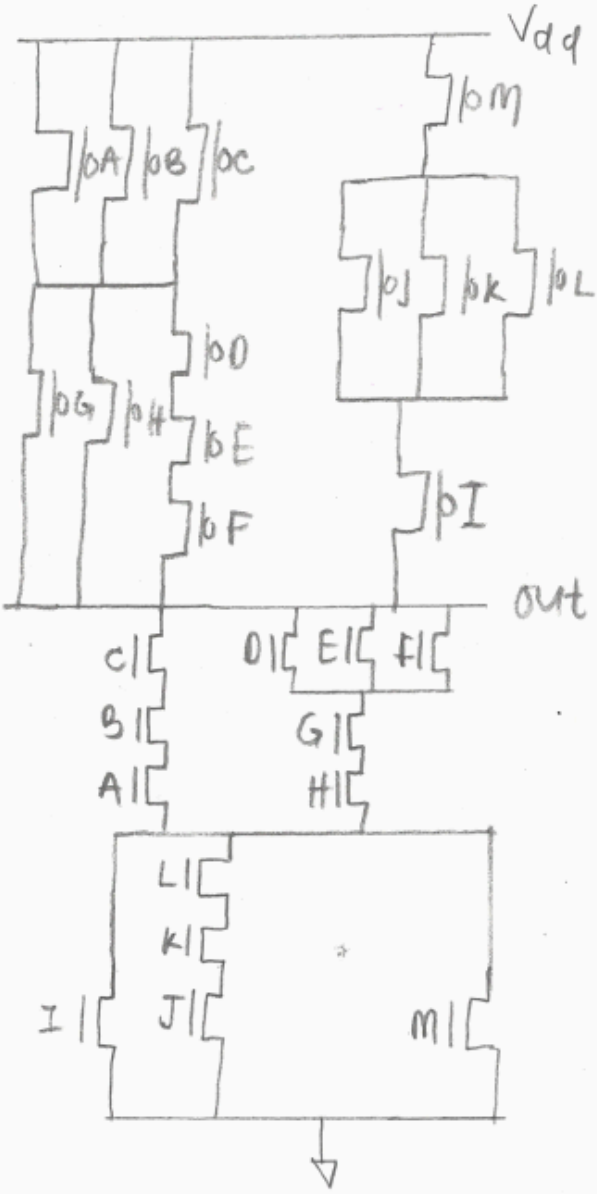
$$Out = \overline{(A+B+C)(D+E+F)+GHI} + inv$$

$$= (A+B+C)(D+E+F)+GHI$$

b.



3b'



$$Out = \overline{(ABC + (DEF)GH)(I + JKL + M)}$$