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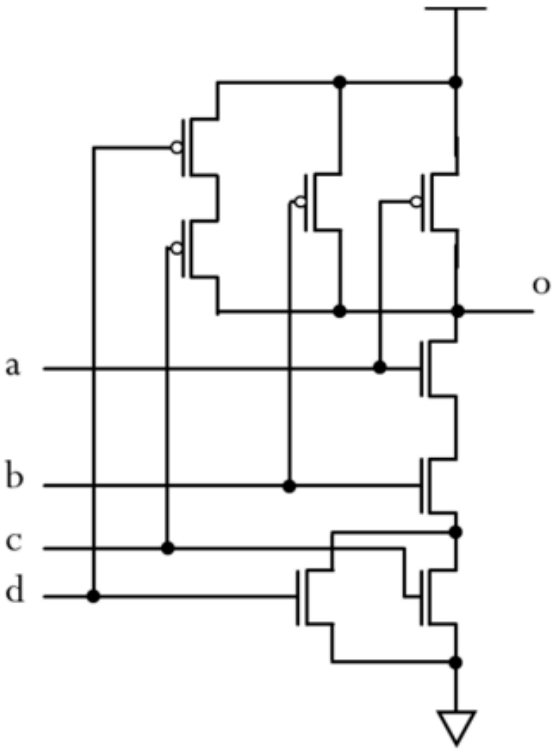
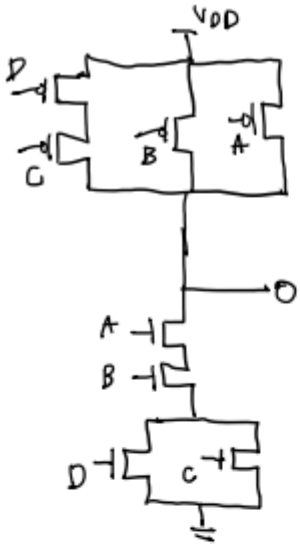
1: Answer the following about the shown gate:

a. Describe the function of the gate.
b. Size the transistors of the gate so it has equal worst-case drive to a unit inverter where Wp = 2Wn.
c. Using the Elmore delay method, calculate the worst-case parasitic ***pull-up*** delay of the gate when there is no load connected.
d. Using the Elmore delay method, calculate the worst-case parasitic ***pull-down*** delay of the gate when there is no load connected.
e. Using the Elmore delay method, calculate the worst-case pull-up and pull-down delays of the gate when it is driving four unit-inverters.
f. Calculate the logical effort at inputs a, b, c, and d and explain why they are different.



a)

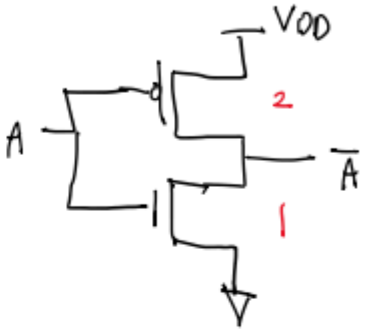


$$O = (A+B)+C\cdot D = \overline{A\cdot B\cdot (C+D)}$$

(PMOS) Pull up

(NMOS) Pull down

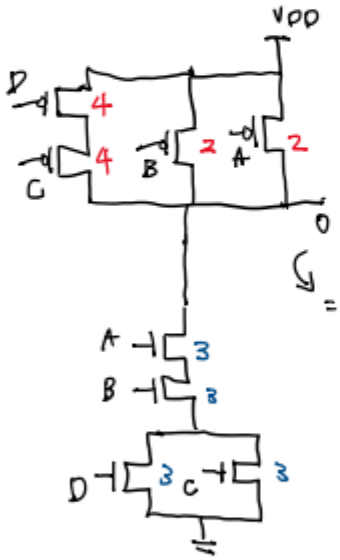
unit CMOS Inverter



$(W/L)_P = 2$

$(W/L)_N = 1$

b)



$$O = (A+B)+C\cdot D = \overline{A\cdot B\cdot (C+D)}$$

(PMOS) Pull up

(NMOS) Pull down

$k = \left(\frac{W}{L}\right)_P$

$\frac{2R}{K} = \frac{2R}{2} = \left[\frac{2R}{K} + \frac{2R}{K}\right]$

$R = \frac{4R}{K}$

$K = 4$

$k = \left(\frac{W}{L}\right)_N$

$\frac{R}{K} + \frac{R}{K} + \frac{R}{K} = R$

$\frac{3R}{K} = R$

$K = 3$

c)

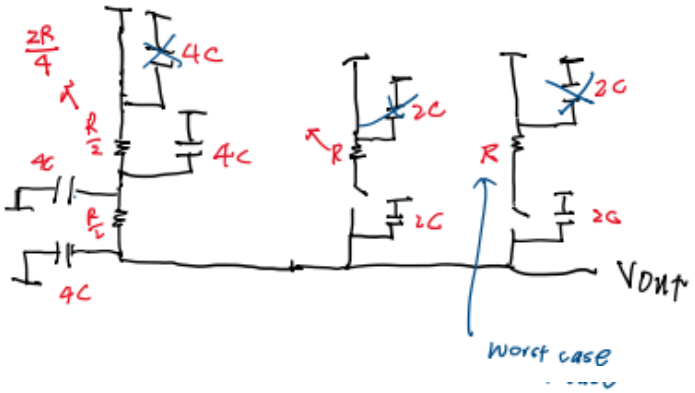
Elmore Delay

$$t_{pd} = \sum_{i} R_{ki} C_i = \sum_{i=1}^{n} C_i \sum_{j=1}^{i} R_j$$

t_{pd}: propagation delay; R_{ki}: sum resister in series

$R_{series} = R_1 + R_2$

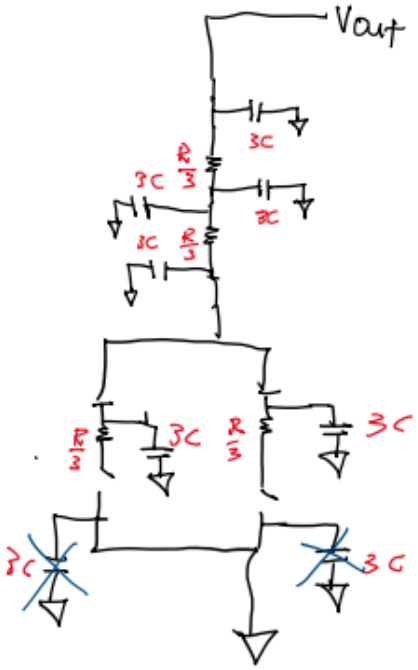
$R_{parallel} = R$



$$\overbrace{4C\left(\frac{R}{2}\right)}^{2} + \overbrace{8C\left(\frac{R}{8}\times 2\right)}^{8} + 2RC + 2RC$$

$$= \boxed{14RC}$$

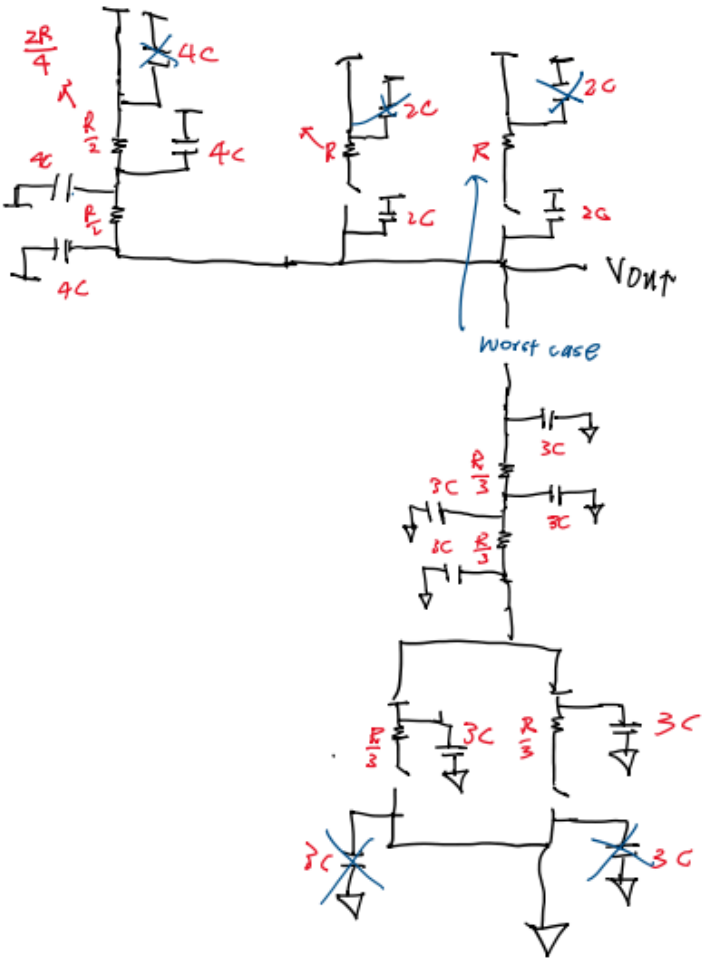
d)



$$\overbrace{3C\left(\frac{R}{3}\right)}^{R} + \overbrace{3C\left(\frac{R}{3}\right)}^{R} + \overbrace{3C\left(\frac{R}{3}\right)}^{R} + \overbrace{6C\left(\frac{R}{3}\times 2\right)}^{4R}$$

$$= \boxed{7RC}$$

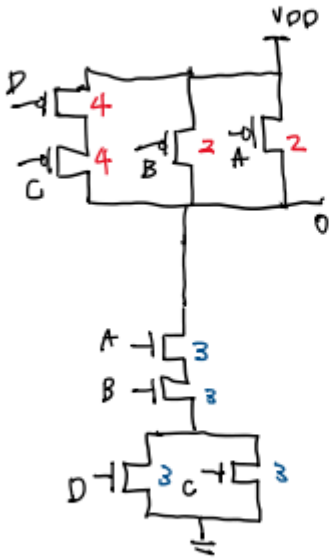
e)



$14RC + 7RC = \boxed{21RC}$

f)

$g = C_{in\ gate} / C_{in\ inverter}$



$g_A = \frac{2+3}{3} = \frac{5}{3}$

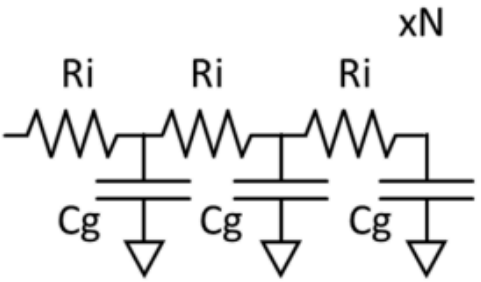
$g_B = \frac{2+3}{3} = \frac{5}{3}$

$g_C = \frac{3+4}{3} = \frac{7}{3}$

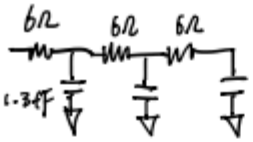
$g_D = \frac{3+4}{3} = \frac{7}{3}$

↑ logic effort ↑ resistance

2: In some systems a clock is used to drive a large number of transistors synchronously. In the shown RC clock system, the gates of N transistors are connected in parallel via resistive interconnect which has a resistance Ri between each pair of gates. If $R_i = 6\ \Omega$ and $C_g = 1.3fF$:



a. Calculate the delay of the circuit when N = 3 (as shown) using Elmore delay.
b. Calculate the delay for arbitrary N.
c. How does the delay scale with N?
d. What effect would this have on maximum clock frequency?
e. Would all capacitors in the circuit receive the same amount of current?
f. Would there be a difference in the timing of the charging of the capacitors?
g. Instead of the linear arrangement of these transistor gates, can you think of alternatives that would mitigate drive strength, timing, and delay issues that could arise?



a)

$$\tau = \sum_{i=1}^{N} R_i C_i = (C_g \cdot R_i) + (C_g \cdot 2R_i) + (C_g + 3R_i)$$

$$= 1.3(6) + (1.3)(\overset{12}{6\times 2}) + (1.3)(\overset{18}{6\times 3}) = \boxed{46.8\ RC}$$

b)

$$\tau = R_i \cdot C_g \cdot \sum_{K=1}^{N} K$$

K is the position index (1 to N)

$$\sum_{K=1}^{N} K = \frac{N(N+1)}{2}$$

c)

The delay scales quadratically with N

$$\tau \propto N(N+1)/2 \simeq N^2$$

d)

A larger delay reduces the max clock freq f_{clk}

$$f_{clk} \propto \frac{1}{\tau}$$

$N \uparrow$ clock freq $\downarrow$

e) No,

The first capacitor in the chain charge more quickly, as the driving resistance is lower. later capacitors have higher resistance, causing a time-dependent variation in current

f) capacitor closer to the clock source charge faster due to lower resistance

capacitors farther away have slower charging due to higher cumulative resistance, causing skew (not straight) in the charging time

G) Alterate to Mitigate issue

1. Tree structures instead of linear can minimize delay
   ↓ distribute evenly
2. insert buffer between groups of gates can reduce resistive delay
3. lower resistance
4. Divide the clock distribution into smaller segments

3: The path marked in the blue dashed line is the critical path of the circuit (the path with the longest delay). Because of this, we want to minimize the delay on this path. The input inverter has already been sized such that the input load see's 9λ worth of capacitance, and the output load is 24λ (hint follow the steps in example 4.13):

a. Using the logical effort method, find G, H, B, F, and f.
b. Calculate the parasitic delay for each gate based on table 4.3. And compute P.
c. Calculate the minimum delay D of the circuit.
d. Based on your results from part *a*, calculate the drives *x* and *y* and size the transistors in each gate to achieve the circuit with the minimum delay.
e. Verify you have achieved the minimum delay by calculating the delay for each gate.

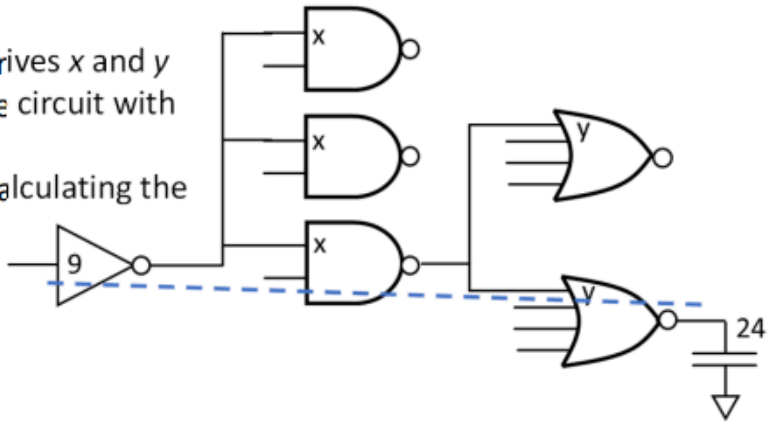


TABLE 4.2 Logical effort of common gates

Gate Type	Number of Inputs				
	1	2	3	4	*n*
inverter	1				
NAND		4/3	5/3	6/3	$(n+2)/3$
NOR		5/3	7/3	9/3	$(2n+1)/3$
tristate, multiplexer	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

a)

$G_T = (1)\left(\frac{4}{3}\right)\left(\frac{9}{3}\right) = \frac{36}{3} = 12$

$H = \frac{24}{9} = \frac{8}{3}$

$B = \pi bi = \frac{C_{\text{off path}} + C_{\text{ON path}}}{C_{\text{off path}}}$

$\frac{X+X}{X} = 2 \qquad \frac{3X+X}{X} = 4$

$= 2 \times 4 = 8$

$F = GBH = (\cancel{12}^{4})\left(\frac{8}{\cancel{3}}\right)(8) = 256$

$f = \sqrt[3]{256} = 6.34$

b) $P = 1 + 2 + 3 = 6$

c) $D = N(GB \cdot H)^{1/N} + P$

$N = 3$ stages

Inverter → NOR → NAND

$3(256)^{\frac{1}{3}} + 6 = \boxed{25}$

d) $F = g \cdot h$

$= g \cdot \frac{C_{out}}{C_{in}}$

$= \frac{9}{3} \cdot \frac{24}{Y} \Rightarrow Y = \frac{9}{3} \cdot \frac{24}{f(6.34)}$

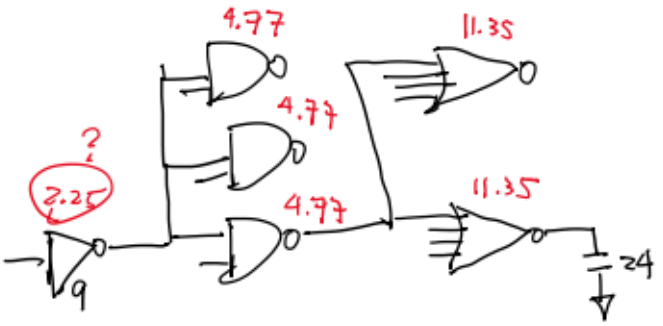
$Y = 11.35$

$6.34 = \frac{4}{3} \cdot \frac{(11.35)_2}{X} \Rightarrow X = \frac{4}{3} \cdot \frac{22.7}{6.34}$

$= 4.77$

$6.34 = 1 \cdot \frac{(4.77)3}{z} \Rightarrow z = 1 \cdot \frac{14.31}{6.34}$

$= 2.25$



z should be 9 not sure why it is 2.25

c) $d_1 = 1 \times \frac{14.31}{2.25} + 1 = 7.84$

$d_2 = \frac{4}{3} \cdot \frac{22.7}{4.77} + 2 = 8.54$

$d_3 = \frac{9}{3} \cdot \frac{24}{11.35} + 4 = 10.34$

4: You have a unit inverter and you need to drive 100 unit-sized loads. Find the optimal number of inverters (including the unit inverter) to minimize delay including parasitics as listed in table 4.3, and size the inverters appropriately.

n	$h = \sqrt[n]{100}$	$D = n.(h+1)$	
2	$\sqrt{100} = 10$	$2(10+1) = 22$	
3	$\sqrt[3]{100} \approx 4.64$	$3(4.64+1) = 16.92$	
4	$\sqrt[4]{100} \approx 3.16$	$4(3.16+1) = 16.64$	✓
5	$\sqrt[5]{100} \approx 2.51$	$5(2.51+1) \approx 17.55$	

Stage 4 size = 100 $h = \sqrt[4]{100}$

Stage 3 size = $\frac{100}{h} = \frac{100}{3.16} = 31.6$

Stage 2 size = $\frac{31.6}{3.16} = 10$

Stage 1 size = $\frac{10}{3.16} = 3.16$