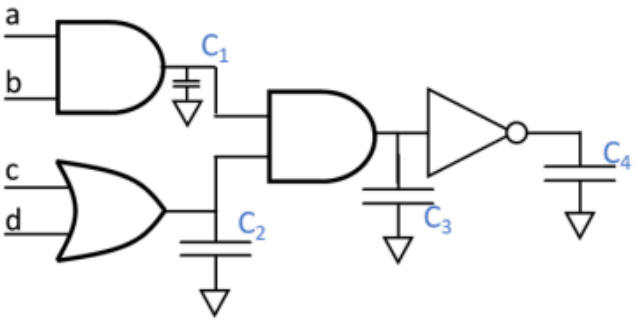
1: **In the circuit shown, assume all switching activity is uncorrelated.** Pa (the probability that at any clock cycle input *a* is a logic '1') = 0.5. Pb = 0.25. Pc = 0.75. Pd = 0.5.



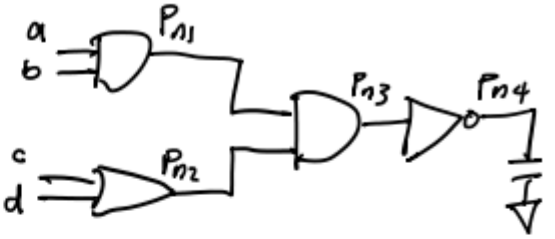
a) Calculate the probabilities of all nodes in the circuit.
b) Calculate the activity factor (α) of every node in the circuit.
c) Assuming the clock frequency is 2.5 Ghz, Vdd = 1.2 V, $C_1 = 2\ \mu F$, $C_2 = 5\ \mu F$, $C_3 = 0.5\ \mu F$, $C_4 = 17\ \mu F$, calculate the average switching power used to drive each capacitor.
d) Calculate the overall switching power consumed by the circuit.

TABLE 5.1 Switching probabilities

Gate	P_Y
AND2	$P_A P_B$
AND3	$P_A P_B P_C$
OR2	$1 - \overline{P}_A \overline{P}_B$
NAND2	$1 - P_A P_B$
NOR2	$\overline{P}_A \overline{P}_B$
XOR2	$P_A \overline{P}_B + \overline{P}_A P_B$

$P_a = 0.5$ $P_c = 0.75$

$P_b = 0.25$ $P_d = 0.5$



$P_{n1} = P_a$ and P_b

$= 0.5(0.25) = \boxed{0.125}$

$P_{n2} = P_c$ or $P_d = 1 - \overline{P_c}\,\overline{P_d}$

$= 1 - (1-0.75)(1-0.5) = 1 - (0.25)(0.5) = \boxed{0.875}$

$P_{n3} = P_{n1}$ and P_{n2}

$= 0.125(0.875) = \boxed{0.109375}$

$P_{n4} = 1 - P_{n3}$

$= 1 - 0.109375 = \boxed{0.890625}$

b) $\alpha = \bar{P} \cdot P$

$\alpha_{Pn1} = (0.125)(1-0.125) = \boxed{0.109375}$

$\alpha_{Pn2} = (0.875)(1-0.875) = \boxed{0.109375}$

$\alpha_{Pn3} = (0.109375)(1-0.109375) = \boxed{0.097412109}$

$\alpha_{Pn4} = (0.890625)(1-0.890625) = \boxed{0.097412109}$

c) $P = \alpha \cdot f \cdot C \cdot V^2$

$C_1 = 2\text{MF}$, $C_2 = 5\text{MF}$, $C_3 = 0.5\text{MF}$, $C_4 = 17\text{MF}$,

$V_{dd} = 1.2V$, clock freq. $= 2.5\text{GHz} = 25 \cdot 10^9\ \text{Hz}$

$P_{C1} = (0.109375)(2.5\times10^9)(2\cdot10^{-6})(1.2)^2$

$= \boxed{787.5\ \text{W}}$

$P_{C2} = (0.109375)(2.5\times10^9)(5*10^{-6})(1.2)^2$

$= \boxed{1968.75\ \text{W}}$

$P_{C3} = (0.097412109)(2.5\times10^9)(0.5\cdot10^{-6})(1.2)^2$

$= \boxed{175.34\ \text{W}}$

$P_{C4} = (0.097412109)(2.5\times10^9)(17\cdot10^{-6})(1.2)^2$

$= \boxed{5961.62\ \text{W}}$

d)

$$P_{total} = P_{C_1} + P_{C_2} + P_{C_3} + P_{C_4}$$

$$= 787.5 + 1968.75 + 175.34 + 5961.62$$

$$= \boxed{8893.2\ W}$$

2: In a given computer, block X consumes 50% of the total static power, but it is only operational in bursts 10% of the time.

a) Describe two methods for reducing the static power used by block X.
b) Estimate the power savings for your chosen methods.
c) Describe any drawbacks for your methods.

a) You can either use Power gating ~~or clock gating~~ to disconnect the voltage ~~of clock source~~ from the circuit when it is dormant. or operate at a lower voltage (e.g 50% of V_{dd}) or reduce the transistor width.

b) By operating at a lower V_{dd}, e.g 50% of V_{dd} → Power $\propto \frac{Voltage^2}{R}$

$$\frac{Power_{new}}{Power_{old}} = \frac{Voltage_{new}^2}{Voltage_{old}^2} = \frac{(0.5\,V_{old})^2}{V_{old}^2} = 0.5^2 = 0.25$$

Power savings $= 1 - 0.25 = 0.75\ (75\%)$

Assuming the circuit is idle 50% of the time, savings $= (75\%)(50\%) = 37.5\%$

c) Power gating circuit is needed leading to added area and delay. Also, for the operation at 50% of V_{dd} requires Voltage domain crossing circuitry. Finally, by reducing the transistor width, you have less drive for the transistor leading to longer latency.

3: In HW2 Q4, we asked you to find the optimal number of inverters minimize delay to drive a 100-unit load starting with a unit inverter. Repeat the problem now minimizing the switching energy delay product (EDP) under a constant Vdd, f, and α. The diffusion nodes are disconnected because the inverters in the cascade are sized differently.

3)

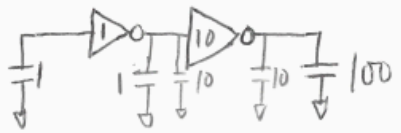
1 stage

$D = 1 \times 100 + 1 = 101$

$E \propto C_{tot} = (2 \times 1) + 100 = 102$

$EDP \propto 101 \times 102 = 10302$

2 stages

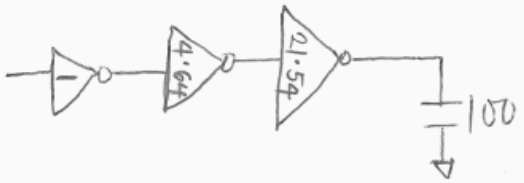


$D = 2 \times \sqrt[2]{100} + 2 = 22$

$E \propto C_{tot} = (2 \times 1) + (2 \times 10) + 100 = 122$

$EDP \propto 22 \times 122 = 2684$

3 stages

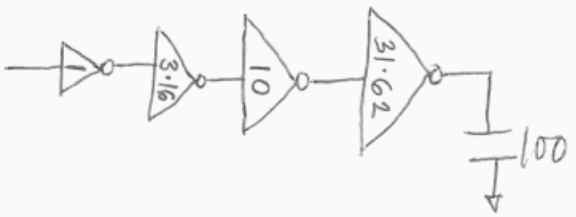


$D = 3 \times \sqrt[3]{100} + 3 = 16.92$

$E \propto C_{tot} = 2(1 + 4.64 + 21.54) + 100 = 154.36$

$EDP \propto 16.92 \times 154.36 = \boxed{2611.77}$

4 stages



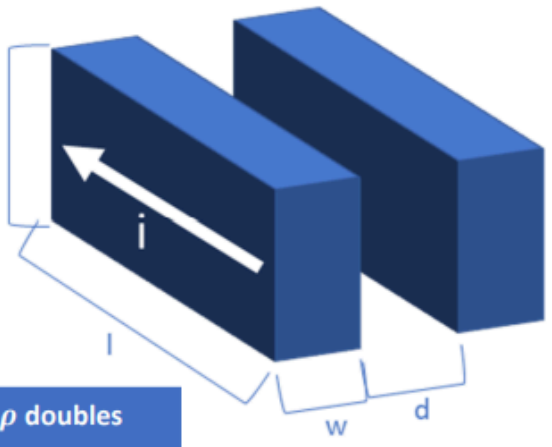
$D = 4 \times \sqrt[4]{100} + 4 = 16.65$

$E \propto C_{tot} = 2(1 + 3.16 + 10 + 31.62) + 100 = 191.56$

$EDP \propto 16.62 \times 191.56 = 3183.73$

Minimum EDP occurs for 3 stages.

4: In the shown interconnect model, two wires are placed adjacent to each other with length l, thickness h, width w, and are space a distance of d apart. A dielectric of permittivity ϵ encases the wires which have a resistivity of ρ. Current flows along the length of the conductor as shown. **Fill in the table analyzing the effect of material parameters and dimensions on resistance (R), capacitance (C), and inductance (L)** *(assuming all parameters are constant except for the one listed).*



	l doubles	w doubles	d doubles	h doubles	ϵ doubles	ρ doubles
R:						
L:						
C:						

$R = \rho \cdot \frac{l}{w \cdot h}$ P, l double R↑ h, w double R↓

$C \propto \frac{\epsilon \cdot l}{d}$ L, ϵ double C↑ d double C↓

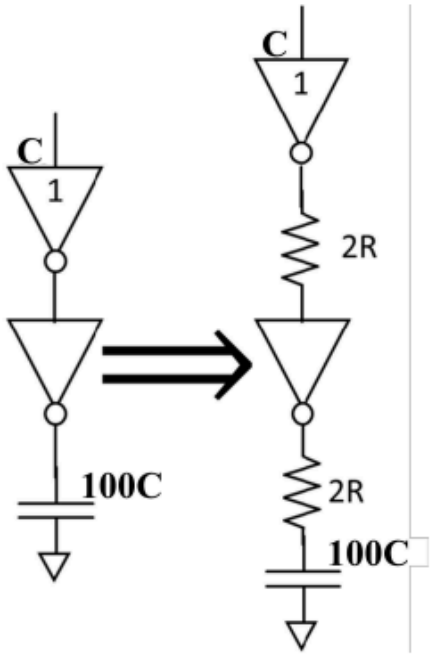
$L \propto \ln(\frac{d}{w}) \cdot l$ d double L increases w double L decreases l double L doubles

ϵ = dielectric permittivity

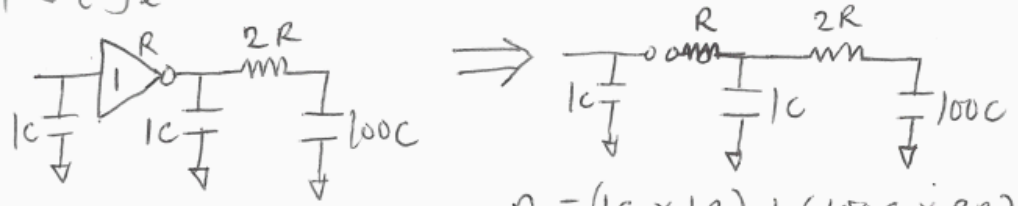
4)

	l doubles	w doubles	d doubles	h doubles	ϵ doubles	ρ doubles
R	doubles	halves	–	halves	–	doubles
L	doubles	non-linear	–	non-linear	–	–
C	doubles	–	halves	doubles	doubles	–

5: In HW2 Q4, we asked you to find the optimal number of inverters to drive a 100-unit load starting with a unit inverter. Repeat the problem minimizing delay using the Elmore delay model assuming now that due to interconnect, there is a 2R *(where R is the unit NMOS ON resistance)* resistor between each inverter and its load as depicted below: *(recall that a unit inverter has input capacitance C and thus a 100-unit load is equivalent to 100C of capacitance)*

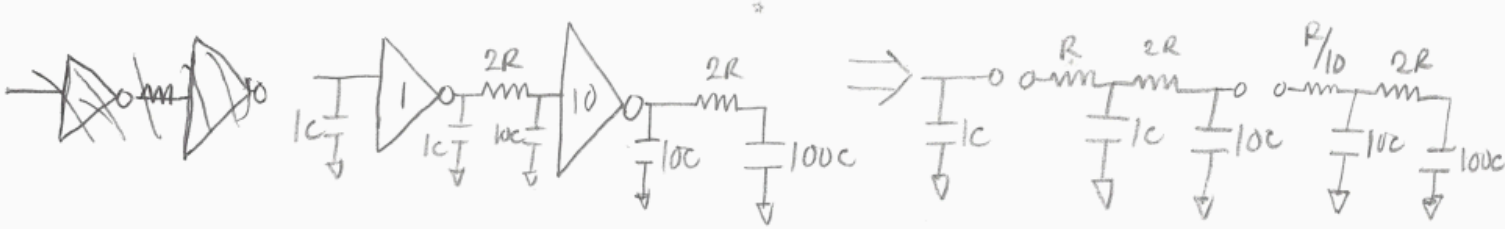


5.) 1 stage



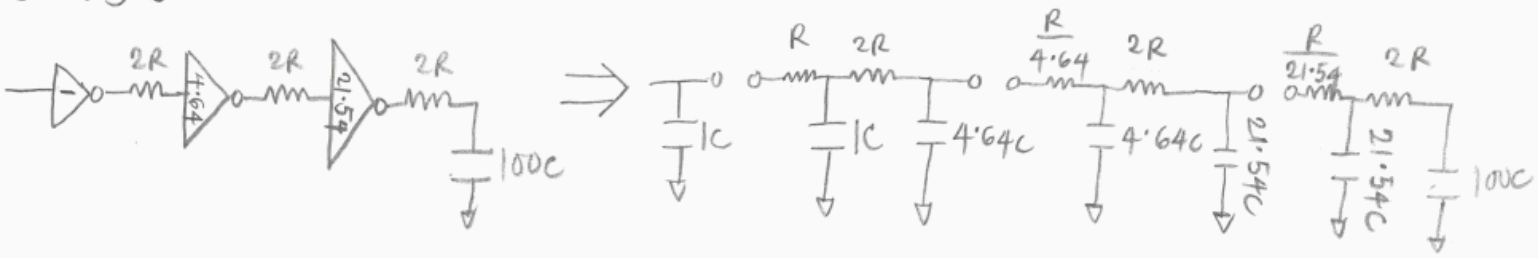
$D = (1C \times 1R) + (100C \times 3R) = RC + 300RC = 301RC$
$= 301\tau$

2 stages



$D = (1C \times 1R) + (10C \times 3R) + (10C \times \frac{R}{10}) + (100C \times \frac{21}{10}R) = RC + 30RC + RC + 210RC$
$= 242RC = \boxed{242\tau}$

3 stages



$$\text{Delay} = RC\left[(1\times1)+(3\times4\cdot64)+\left(4\cdot64\times\frac{1}{4\cdot64}\right)+(21\cdot54\times2\cdot216)+\left(21\cdot54\times\frac{1}{21\cdot54}\right)+(100\times2\cdot046)\right]$$

$$= 269\cdot25RC = 269\cdot25\,\tau$$

Minimum $\overset{\text{delay}}{\wedge}$ = 2 stages.