P2: INVERTER LAYOUT AND SIMULATION COMPETITION

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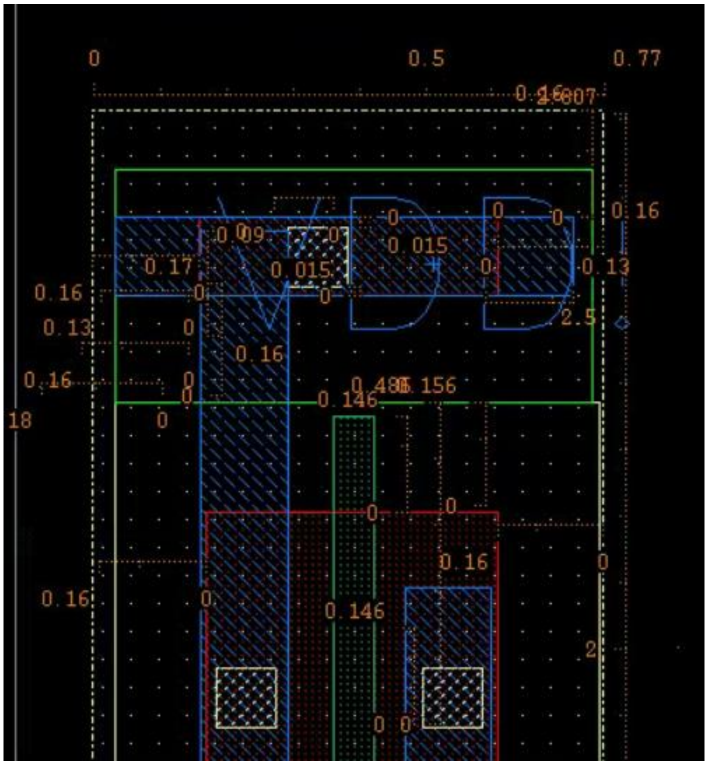
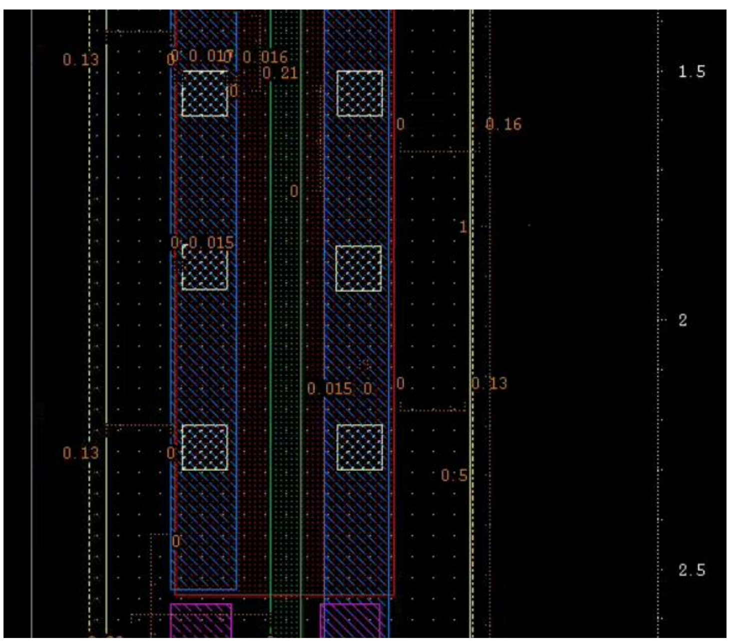
Clearly state the results as in the template table

PMOS Width (nm)	PMOS Length (nm)	NMOS Width (nm)	NMOS Length (nm)	Layout Width (nm)	Layout Height (nm)
60nm	1944nm	60nm	1000nm	770nm	4450nm
Propagation Delay (Rising) t_{pdr}(ps)	Propagation Delay (Falling) t_{pdf} (ps)	Average delay t_{avg} (ps) (t_{pdr}+ t_{pdf})/2	Output Rise Time t_r (ps)	Output Fall Time t_f (ps)	Transitional Energy **E**(fj)
118 ps	108 ps	113 ps	222ps	191ps	113 fj
EDP (E* t_{avg}) (fJ ps)	Layout Area, ***A*** (nm^2)	AEDP (**EDP***A*) (fJ ps nm^2)			
12769ps	3342190	4.26×10^{10}			

↓

770(2804) + 720(1.647)


0
0.5
0.77
0.16
0.13
0.17
0.09
0.015
0.146
0.156
0.16
2.5
18
2


1.5
2
2.5
0.13
0.16
0.21
0.015
0.5
1

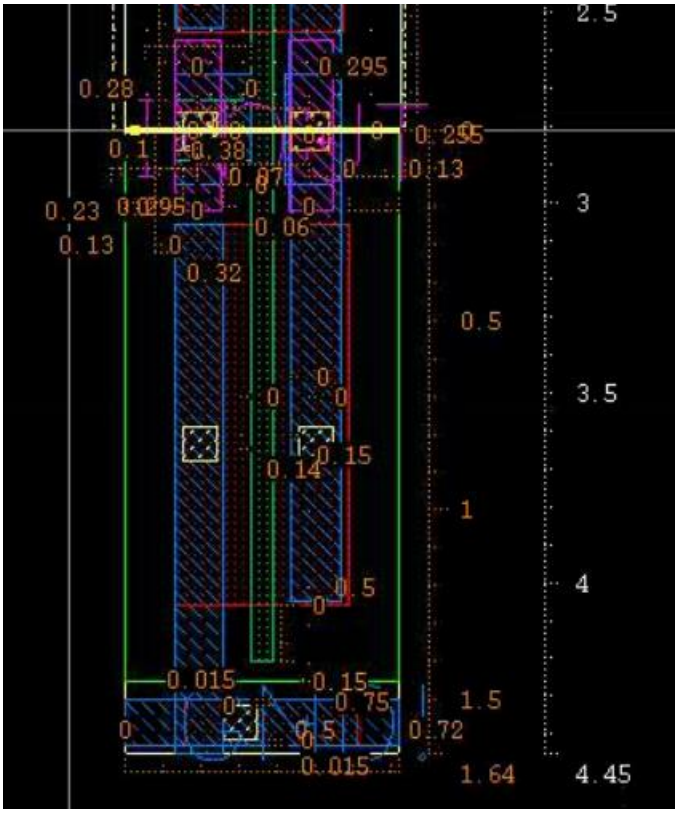


Fig1: Layout

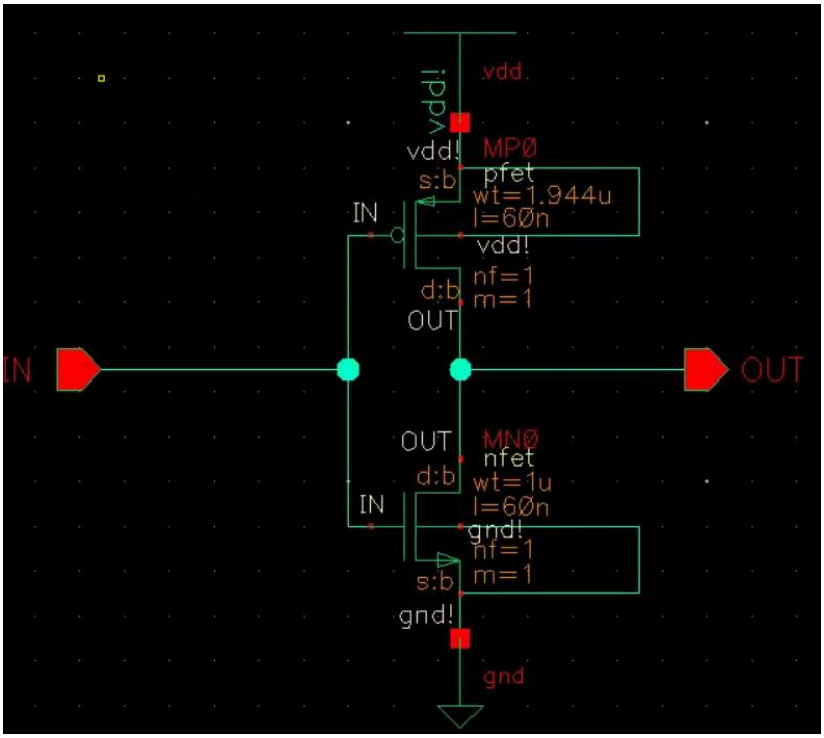


Fig2: Schematic

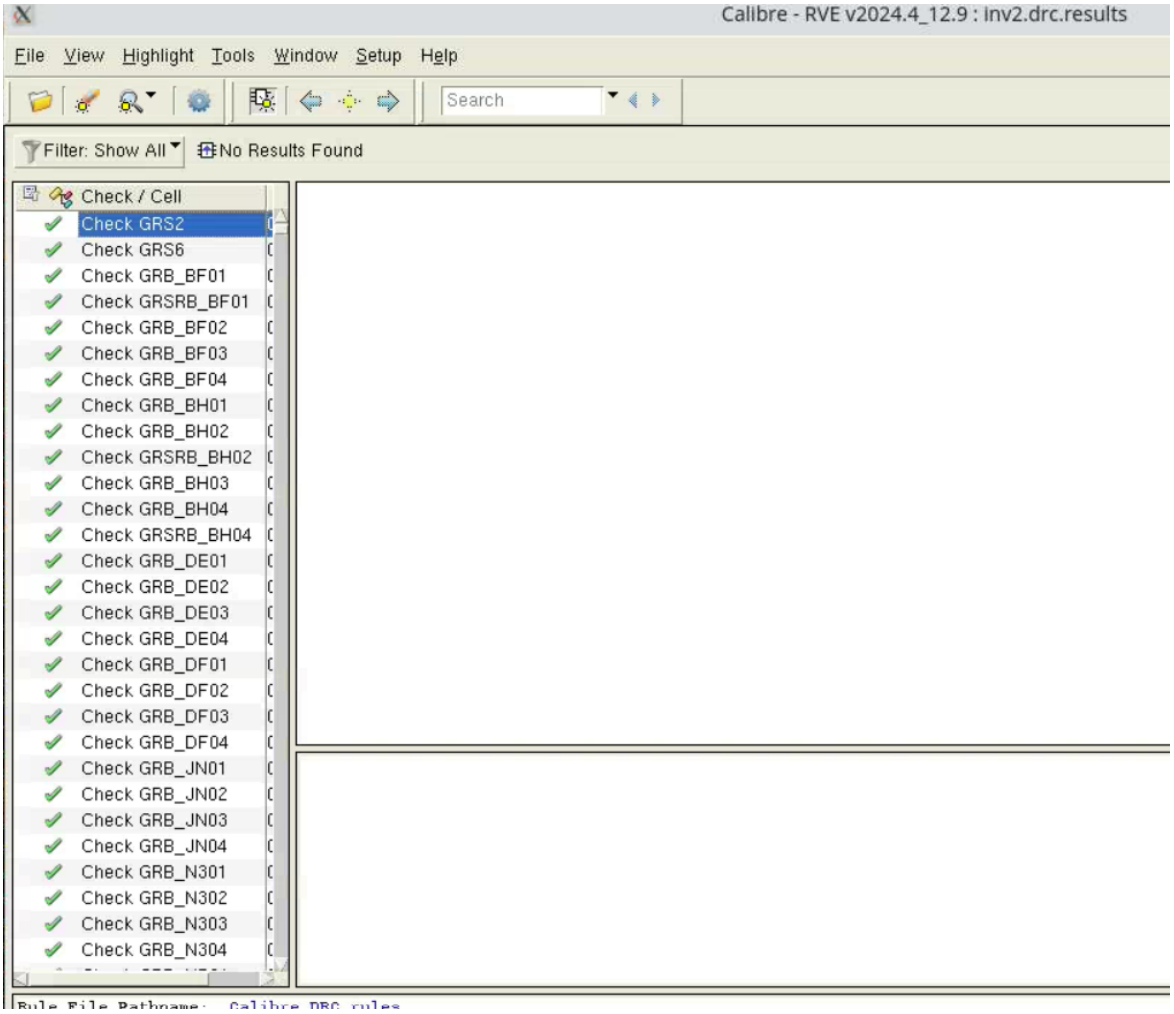

Calibre - RVE v2024.4_12.9 : inv2.drc.results
File View Highlight Tools Window Setup Help
Search
Filter: Show All
No Results Found
Check / Cell
Check GRS2
Check GRS6
Check GRB_BF01
Check GRSRB_BF01
Check GRB_BF02
Check GRB_BF03
Check GRB_BF04
Check GRB_BH01
Check GRB_BH02
Check GRSRB_BH02
Check GRB_BH03
Check GRB_BH04
Check GRSRB_BH04
Check GRB_DE01
Check GRB_DE02
Check GRB_DE03
Check GRB_DE04
Check GRB_DF01
Check GRB_DF02
Check GRB_DF03
Check GRB_DF04
Check GRB_JN01
Check GRB_JN02
Check GRB_JN03
Check GRB_JN04
Check GRB_N301
Check GRB_N302
Check GRB_N303
Check GRB_N304

Fig3: DRC

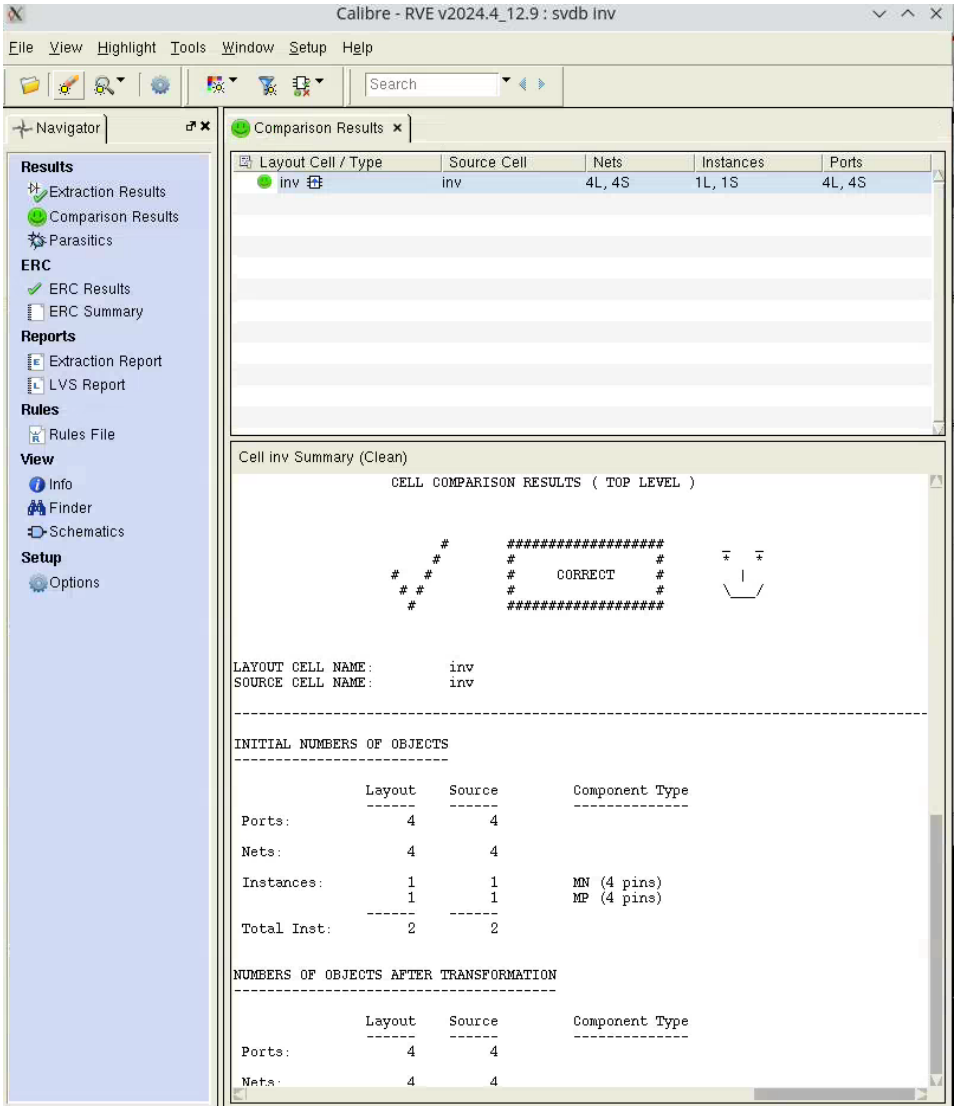

Calibre - RVE v2024.4_12.9 : svdb inv
File View Highlight Tools Window Setup Help
Search
Navigator
Results
Extraction Results
Comparison Results
Parasitics
ERC
ERC Results
ERC Summary
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
inv
inv
4L, 4S
1L, 1S
4L, 4S
Cell inv Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: inv
SOURCE CELL NAME: inv
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 4 4
Nets: 4 4
Instances: 1 1 NN (4 pins)
1 1 MP (4 pins)
Total Inst: 2 2
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 4 4
Nets: 4 4

Fig4: LVS

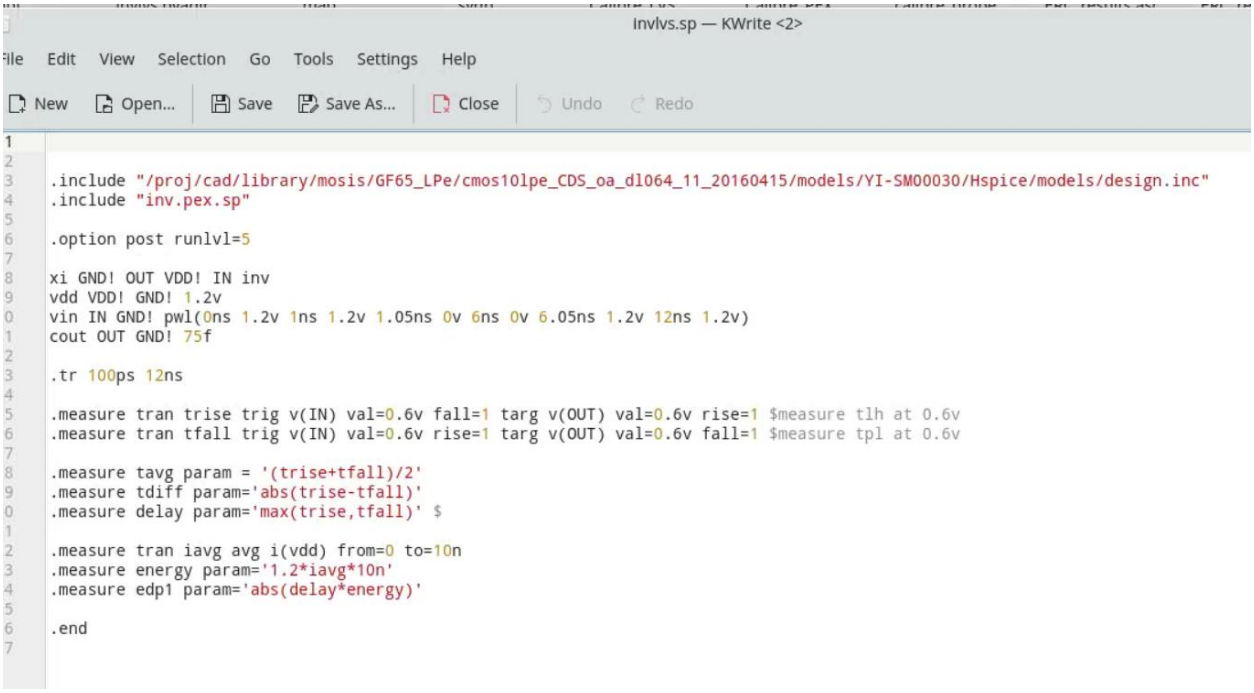


Fig5: HSpice test setup file

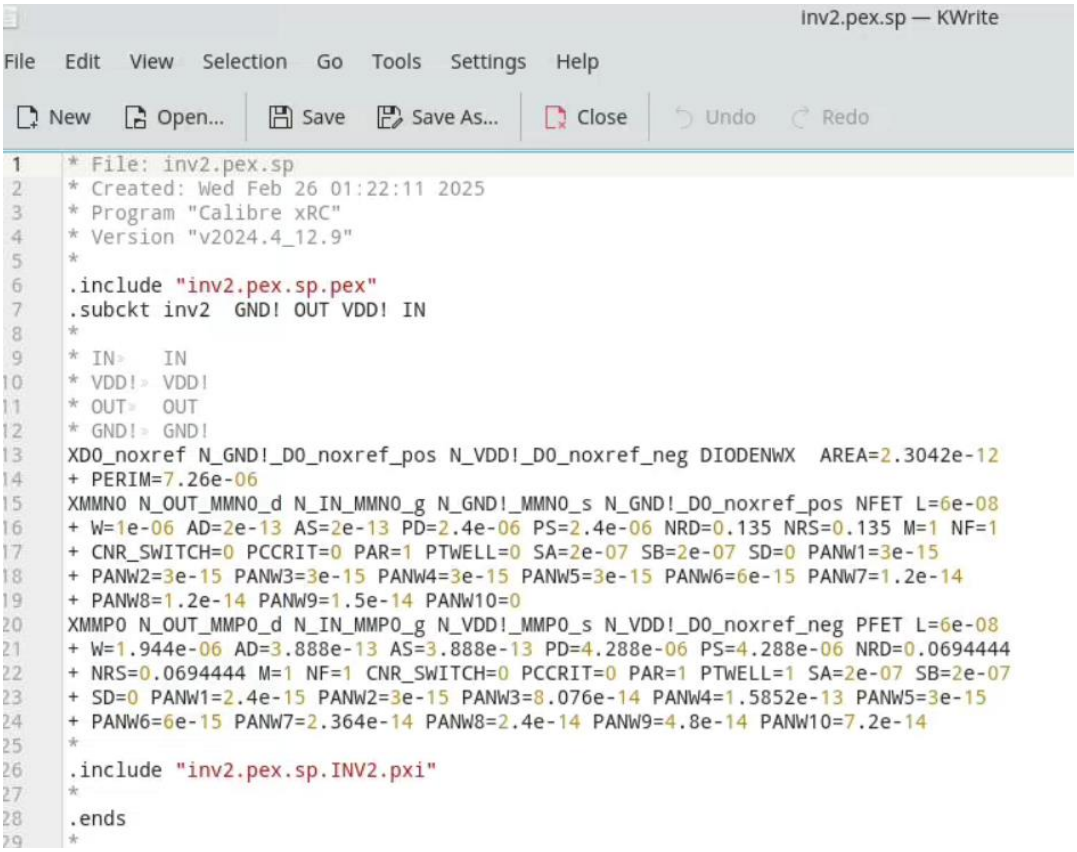


Fig6: Netlist file

Detailed explanation on how you achieved the minimum AEDP:

The formula for AEDP is given by:

AEDP=E×tavg×layout area (nm2)

During the optimization process, I noticed that reducing the layout area did not significantly affect the energy consumption. The energy only decreased from 113 jF to 110 jF. However, I also observed trade-offs. For example, when I changed the PMOS:NMOS ratio from 2:1 to 1:0.5, the delay increased from 113 ps to 215 ps.

I tested the AEDP for both the 2:1 and 1:0.5 ratios, and the 2:1 configuration still resulted in a smaller AEDP. Specifically, the AEDP was 5.37×10^10 compared to 4.09×10^10 for the 1:0.5 ratio.

Additionally, I tried the 1.414:1 ratio, which I read in a textbook as the optimal ratio for minimizing tavg delay. However, the time difference between tpdr and tpdf was 40 ps. Therefore, I chose the 1.944:1 ratio to achieve a lower delay, despite a slightly larger area, with a tdiff of only 9.36 ps.
For widthof layout, smallest I can get to is 0.77um 0.45 +0.16 *2 = 0.77 for Pmos since RX's area has to be at least 0.45 *0.12 >= 0.054 um^2 and 0.72um for Nmos
For Height of layout, RX to JZ drawing has to be >= 0.16um so I just make it as small as possible and getting 4.45um total in height.

Hence, a 2:1 ratio can minimize delay, but it increases the layout area and may slightly increase energy consumption. There are certainly better ways to reduce AEDP to 2×10^10, but I am unsure how to achieve that, so I have decided to stick with my current approach.

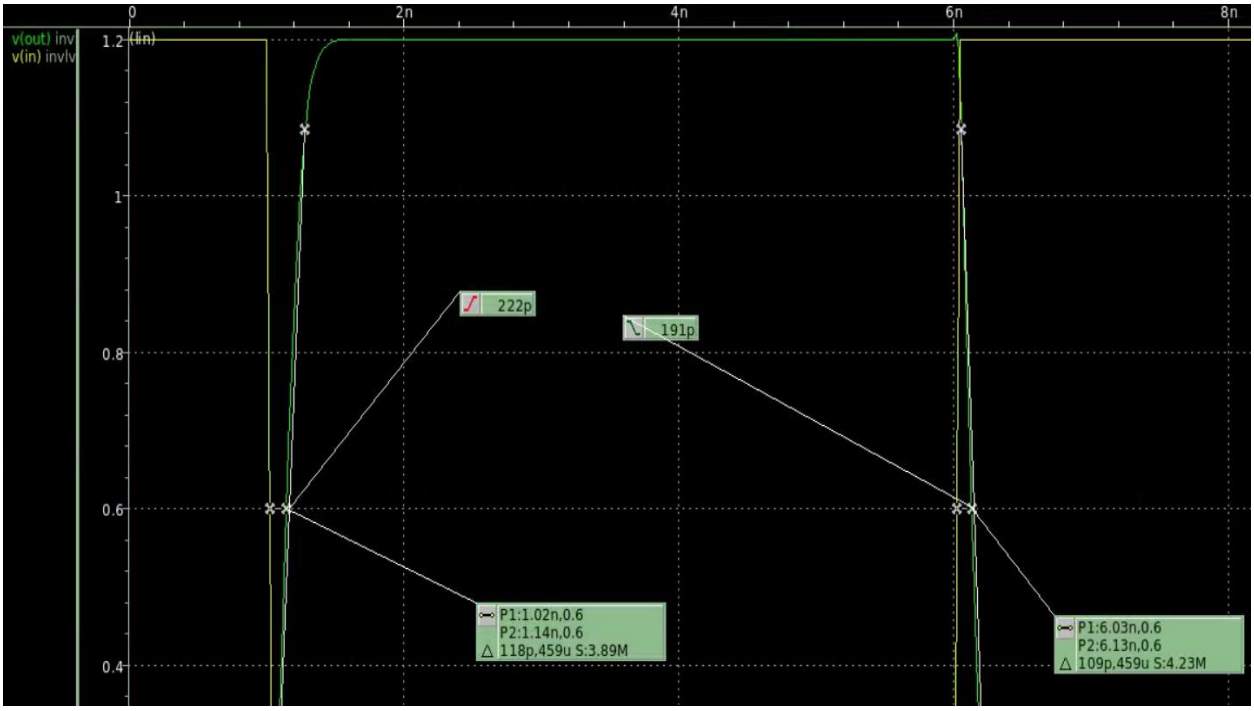


Fig6: Waveforms from WaveView

invlvs2.out — KWrite

File Edit View Selection Go Tools Settings Help

New Open... Save Save As... Close Undo Redo

```
Using: /proj/cad/synopsys/synopsys_2018/hspice_vO-2018.09-2/hspice/linux64/hspice invlvs2.sp
 ****** HSPICE -- O-2018.09-2 linux64 (Oct 18 2018) ******
  Copyright (c) 1986 - 2025 by Synopsys, Inc. All Rights Reserved.
  This software and the associated documentation are proprietary
  to Synopsys, Inc. This software may only be used in accordance
  with the terms and conditions of a written license agreement with
  Synopsys, Inc. All other use, reproduction, or distribution of
  this software is strictly prohibited.
  Input File: invlvs2.sp
  Command line options: /proj/cad/synopsys/synopsys_2018/hspice_vO-2018.09-2/hspice/linux64/hspice invlvs2.sp
 lic:
 lic: FLEXlm: SDK_11.6.9.6
 lic: USER:   yxh230019           HOSTNAME: engnx04a.utdallas.edu
 lic: HOSTID: "b02628e85784"      PID:      2653364
 lic: Using FLEXlm license file:
 lic: 1700@engdmv.utdallas.edu
 lic: Checkout 1 hspice
 lic: License/Maintenance for hspice will expire on 30-jun-2025/2023.12
 lic: 1(in_use)/50(total) FLOATING license(s) on SERVER 1700@engdmv.utdallas.edu
 lic:

*pvaI* current limit stacksize=8388608, set new limit stacksize=62914560
 ------------------------------------------------------
|                                                      |
|             Synopsys Unified Verilog-A (pVA)         |
|                                                      |
|           Machine Name: engnx04a.utdallas.edu        |
| Copyright (c) 2015 Synopsys Inc., All Rights Reserved. |
|                                                      |
 ------------------------------------------------------
```

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
trise= 117.9760p  targ=   1.1430n   trig=   1.0250n
tfall= 108.5795p  targ=   6.1336n   trig=   6.0250n
tavg= 113.2778p
tdiff=   9.3964p
delay= 117.9760p
iavg=  -9.4438u  from=   0.             to=  10.0000n
energy=-113.3251f
edp1= 1.3370e-23

          ***** job concluded
******
```

```
  ******  Circuit Statistics  ******
  # nodes       =      45 # elements   =     124
  # resistors   =      38 # capacitors =      81 # inductors   =       0
  # mutual_inds =       0 # vccs       =       0 # vcvs        =       0
  # cccs        =       0 # ccvs       =       0 # volt_srcs   =       2
  # curr_srcs   =       0 # diodes     =       1 # bjts        =       0
  # jfets       =       0 # mosfets    =       2 # U elements  =       0
  # T elements  =       0 # W elements =       0 # B elements  =       0
  # S elements  =       0 # P elements =       0 # va device   =       0
  # vector_srcs =       0 # N elements =       0


  ******  Runtime Statistics (seconds)  ******

  analysis           time    # points   tot. iter  conv.iter
  op point           0.02           1           8
  transient          0.00         121         267         120 rev=        22
  readin             1.67
  errchk             0.04
  setup              0.00
  output             0.00


          peak memory used        381.38 megabytes
          total cpu time            1.72 seconds
          total elapsed time        7.29 seconds
          job started at     01:22:20 02/26/2025
          job ended   at     01:22:28 02/26/2025



>info:         ***** hspice job concluded
 lic: Release hspice token(s)
 lic: total license checkout elapse time:        0.02(s)

End of pVA simulation reached at time 0 on Wed Feb 26 01:22:28 2025     GTM/In-use: 61.0000/49.6117 MB


                      pVA malloc          4.840 Mbytes       100792 times
                      pVA calloc         79.544 Mbytes       547191 times
                      pVA realloc         3.622 Mbytes         1826 times
                      pVA valloc          0.000 Mbytes            0 times
                      pVA alloca          0.000 Mbytes            0 times

                      pVA TOT-MEM        88.006 Mbytes       649809 times
                      pVA free                               132695 times
                      pVA strdup          0.000 Mbytes            0 times


pVA concluded on Wed Feb 26 01:22:28 2025       GTM/In-use: 61.0000/49.6117 MB
```

Fig7: Screenshot of HSPICE output terminal showing the simulation results

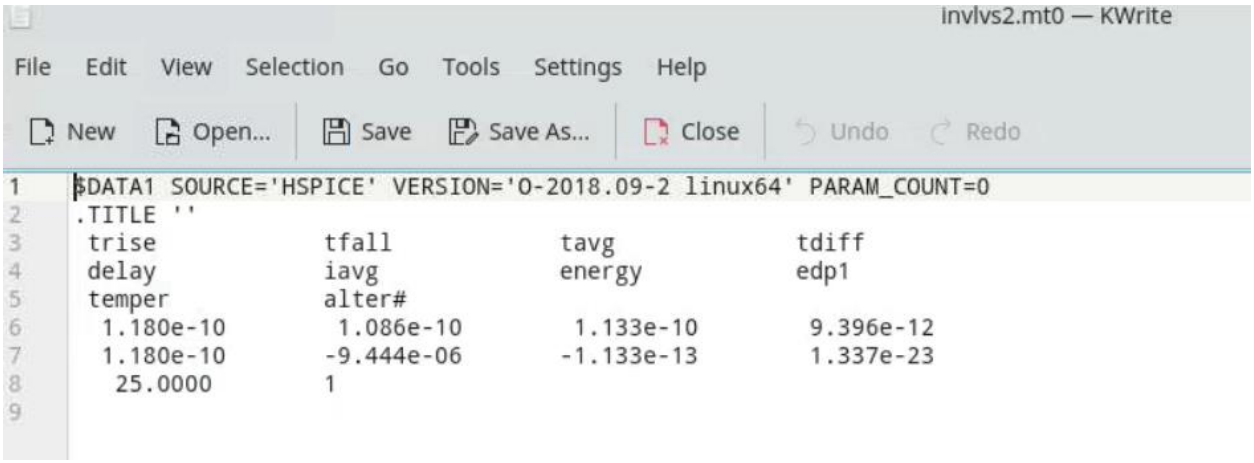


Fig8: .mt0 file