P3: NAND2/NOR2 Design Competition

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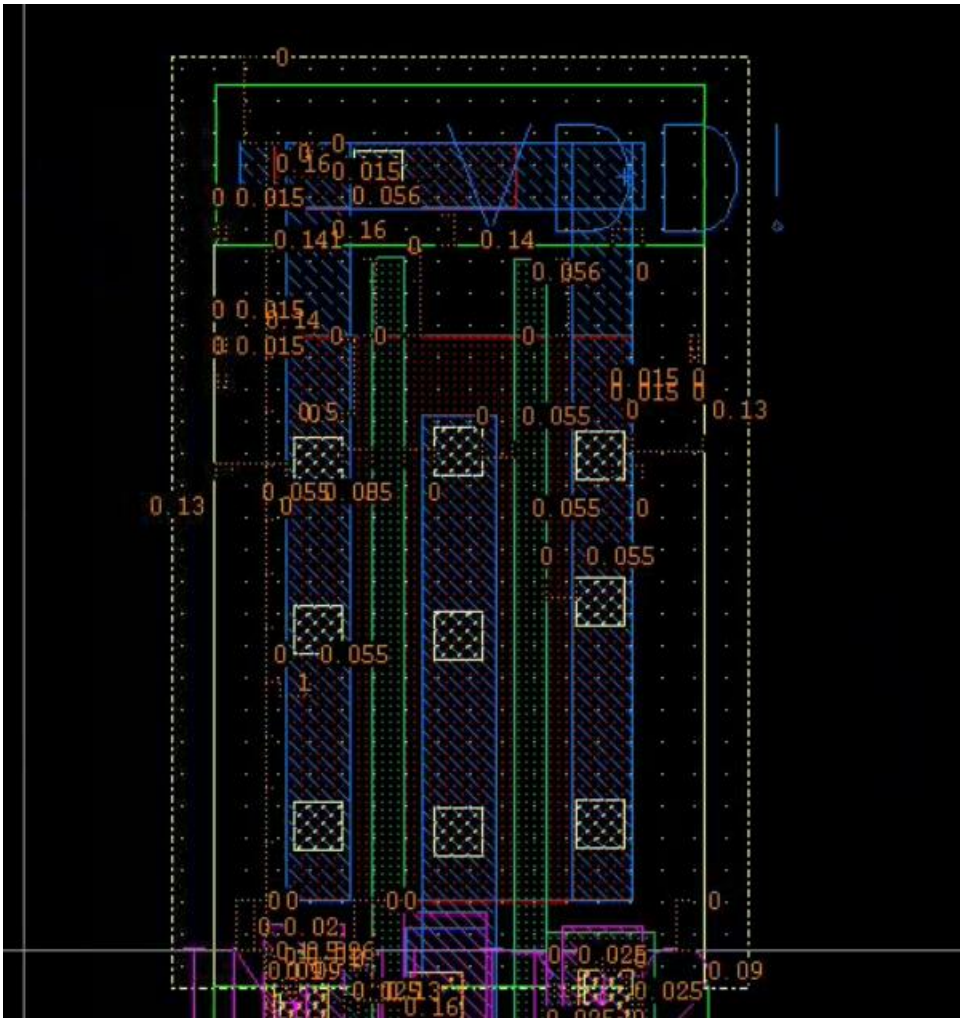
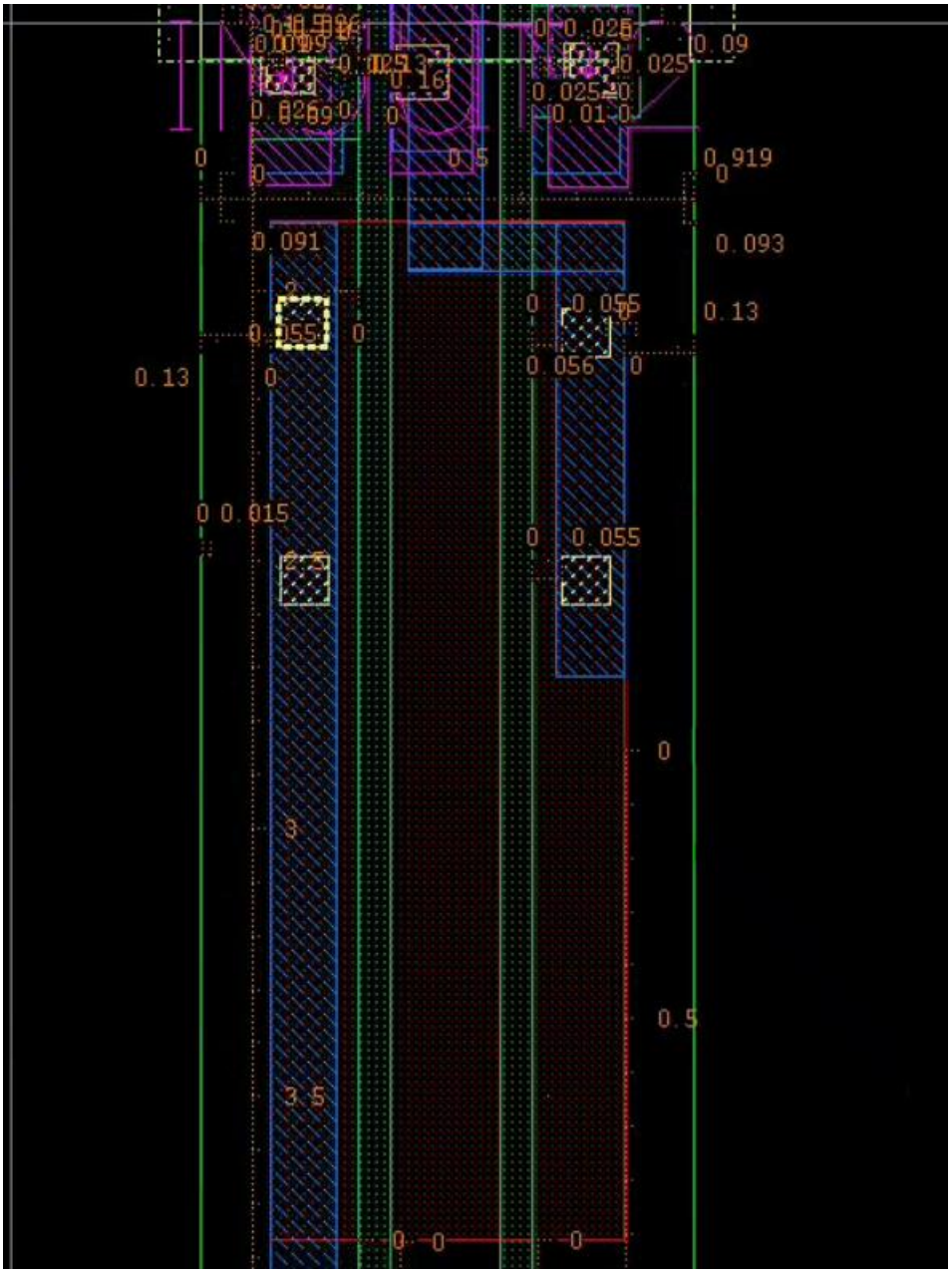
Name of the designed Cell: NAND2

Clearly state the results as in the template table

PMOS Width (um)	PMOS Length (um)	NMOS Width (um)	NMOS Length (um)	Layout Width (um)	Layout Height (um)
1.05um	0.06 um	1.9 um	0.06um	0.919um	4.11 um
Propagation Delay (Rising) t_{pdr}(ps)	Propagation Delay (Falling) t_{pdf} (ps)	Worst-Case Propagation Delay (ps)	Energy **E**(fJ)	**EDP** (E× $t_{worst-case}$) (fJ.ps)	Layout Area, ***A*** (um^2)
142PS	133 PS	142PS	3.00 fj	42600 fj.ps	3.77 um^2
AEDP (**EDP**× ***A***) (fJ.ps.um^2)	= (42600 fJ.ps)(3.77 um^2) = 1.6×10^5 fJ.ps. um^2				


VDD!


0.09
0.025
0.16
0.5
0.919
0.091
0.093
0.055
0.13
0.056
0.13
0.015
0.055
0
3
0.5
3.5

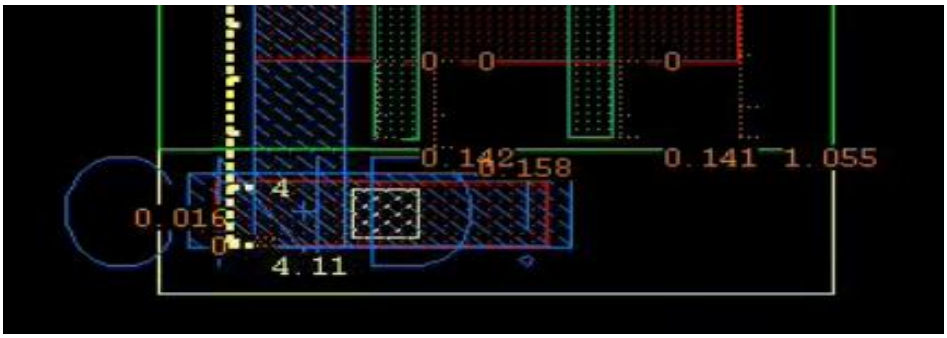

0.142
0.158
0.141
1.055
4
0.016
4.11

Fig1: Layout

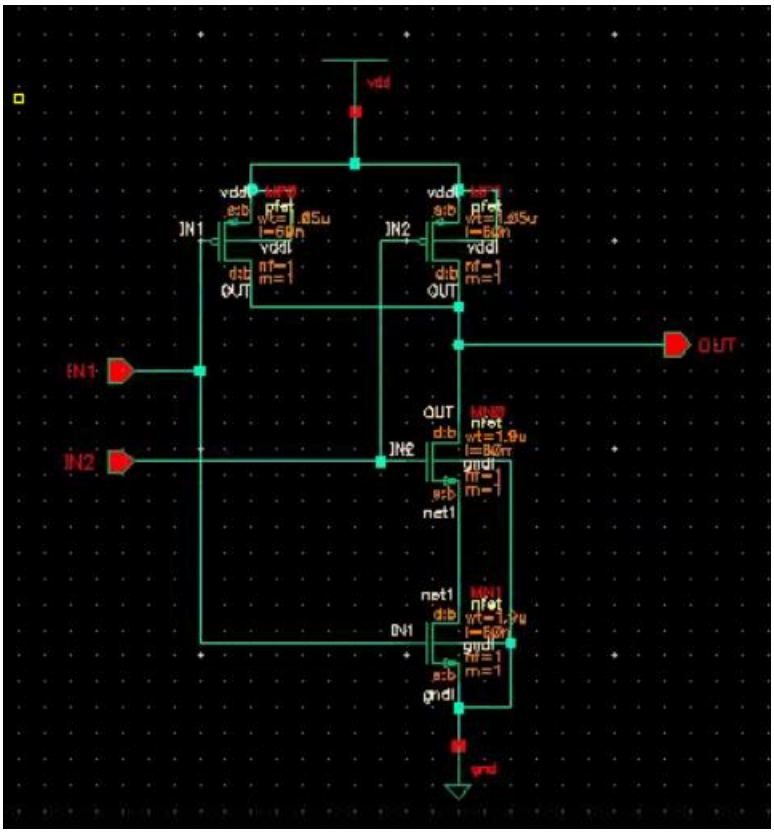


Fig2: Schematic

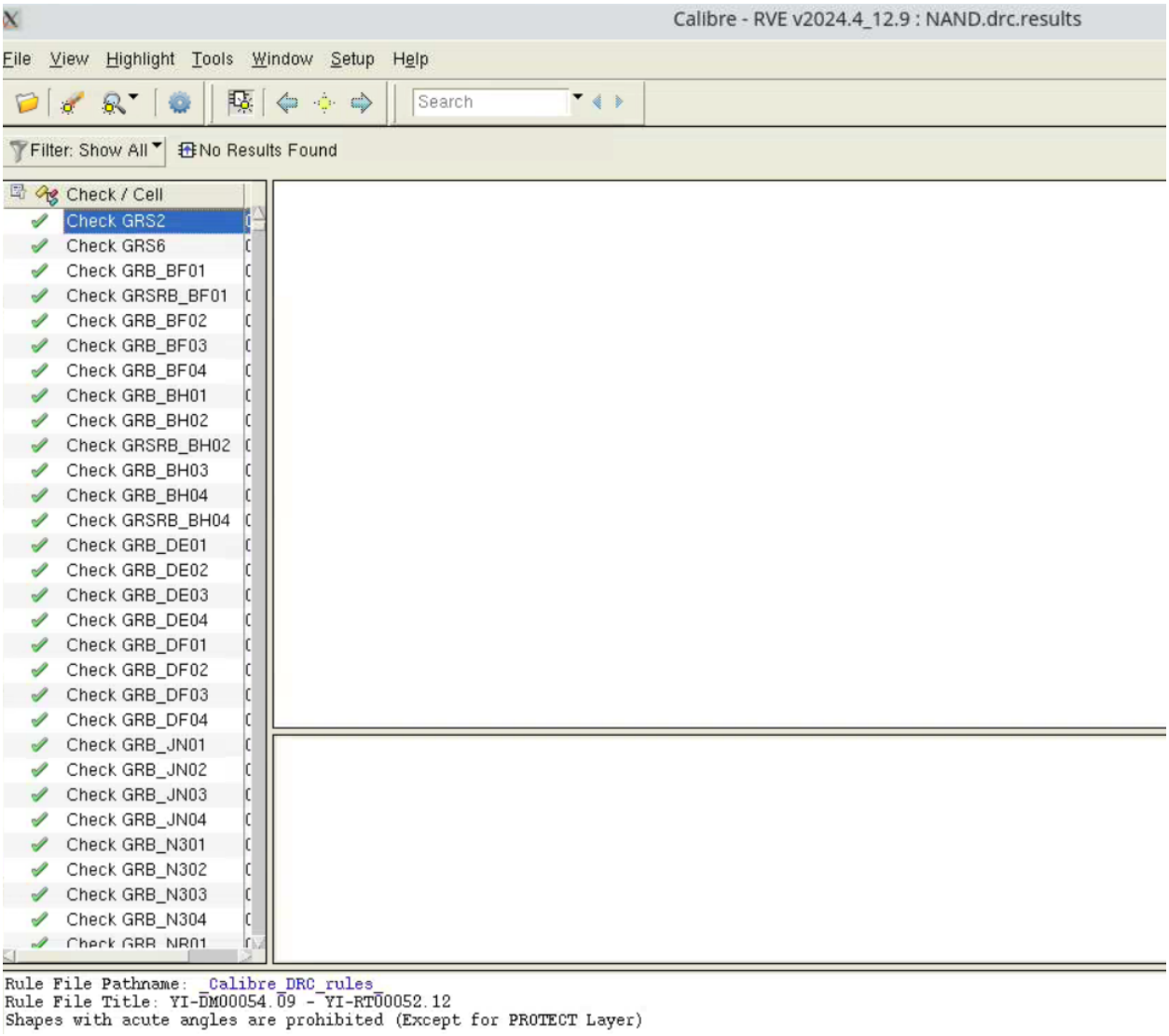

Calibre - RVE v2024.4_12.9 : NAND.drc.results
File View Highlight Tools Window Setup Help
Search
Filter: Show All
No Results Found
Check / Cell
Check GRS2
Check GRS6
Check GRB_BF01
Check GRSRB_BF01
Check GRB_BF02
Check GRB_BF03
Check GRB_BF04
Check GRB_BH01
Check GRB_BH02
Check GRSRB_BH02
Check GRB_BH03
Check GRB_BH04
Check GRSRB_BH04
Check GRB_DE01
Check GRB_DE02
Check GRB_DE03
Check GRB_DE04
Check GRB_DF01
Check GRB_DF02
Check GRB_DF03
Check GRB_DF04
Check GRB_JN01
Check GRB_JN02
Check GRB_JN03
Check GRB_JN04
Check GRB_N301
Check GRB_N302
Check GRB_N303
Check GRB_N304
Rule File Pathname: _Calibre_DRC_rules_
Rule File Title: YI-DM00054.09 - YI-RT00052.12
Shapes with acute angles are prohibited (Except for PROTECT Layer)

Fig3: DRC

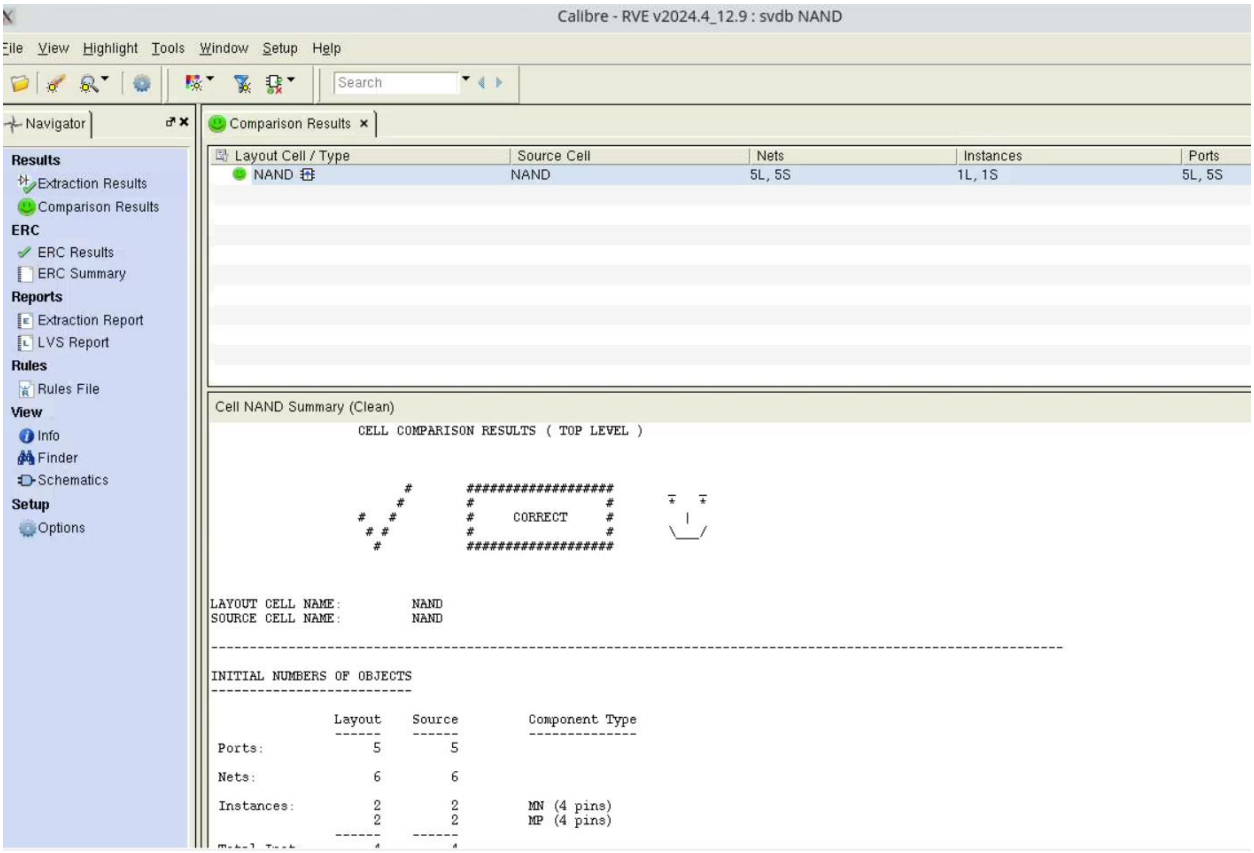


Fig4: LVS

```
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "NAND.pex.sp"

.option post runlvl=5

xi GND! OUT VDD! IN1 IN1 NAND
vdd VDD! GND! 1.2v
vin1 IN1 GND pwl(0ns 0v 1.15ns 0v 1.2ns 1.2v 2.35ns 1.2v 2.4ns 0v 3.55ns 0v 3.6ns 1.2v 4.75ns 1.2v 4.8ns 1.2v 5.55ns 1.2v 6ns 1.2v 7.15ns 1.2v 7.2ns 0v 8.35ns 0v 8.4ns 0v)
vin2 IN2 GND pwl(0ns 0v 1.15ns 0v 1.2ns 1.2v 2.35ns 1.2v 2.4ns 1.2v 3.55ns 1.2v 3.6ns 1.2v 4.75ns 1.2v 4.8ns 0v 5.95ns 0v 6ns 1.2v 7.15ns 1.2v 7.2ns 0v 8.35ns 0v 8.4ns 0v)
cout OUT GND! 100f
```

```
.tr 100ps 12ns
*.tr 100ps 12ns sweep WP 2u 4u 0.5u

.measure tran trise trig v(IN1) val=0.6v fall=1 targ v(OUT) val=0.6v rise=1 $propagation delay
.measure tran tfall trig v(IN1) val=0.6v rise=1 targ v(OUT) val=0.6v fall=1

.measure tavg param = '(trise+tfall)/2'
.measure tdiff param = 'abs(trise-tfall)'
.measure delay param = 'max(trise,tfall)'
```

```
.measure tran iavg avg i(vdd) from=0 to=10n
.measure energy param = 1.2*iavg*10n
.measure edp1 param = 'abs(delay*energy)'

.measure tran t1 when v(IN1)=1.19 fall=1
.measure tran t2 when v(OUT)=1.19 rise=1
.measure tran t3 when v(IN1)=0.01 rise=1
.measure tran t4 when v(OUT)=0.01 fall=1
.measure tran i1 avg i(vdd) from=t1 to=t2
.measure tran i2 avg i(vdd) from=t3 to=t4
.measure energy1 param='1.2*i1*(t2-t1)'
.measure energy2 param='1.2*i2*(t4-t3)'
.measure energysum param='energy1 + energy2'
.measure edp2 param='abs(tavg*energysum)' *calculation is based on the average delay, rather than the worst-case delay

.end
```

Fig5: HSpice test setup file

NAND.pex.sp –

File Edit View Selection Go Tools Settings Help

New Open... Save Save As... Close Undo Redo

```
* File: NAND.pex.sp
* Created: Thu Mar  6 23:49:37 2025
* Program "Calibre xRC"
* Version "v2024.4_12.9"
*
.include "NAND.pex.sp.pex"
.subckt NAND  GND! OUT VDD! IN1 IN2
*
* IN2>  IN2
* IN1>  IN1
* VDD!> VDD!
* OUT>  OUT
* GND!> GND!
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX  AREA=1.85003e-12
+ PERIM=5.598e-06
XMMN1 NET1 N_IN1_MMN1_g N_GND!_MMN1_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=1.9e-06 AD=1.9285e-13 AS=3.135e-13 PD=2.103e-06 PS=4.13e-06 NRD=0.0534211
+ NRS=0.0542105 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.65e-07
+ SB=4.34e-07 SD=0 PANW1=1.2e-16 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMN0 N_OUT_MMN0_d N_IN2_MMN0_g NET1 N_GND!_D0_noxref_pos NFET L=6e-08 W=1.9e-06
+ AD=3.249e-13 AS=1.9285e-13 PD=4.142e-06 PS=2.103e-06 NRD=0.0531579
+ NRS=0.0534211 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=4.28e-07
+ SB=1.71e-07 SD=0 PANW1=1.2e-16 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15 PANW5=3e-15
+ PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=2.4e-14 PANW10=3.6e-14
XMMP0 N_OUT_MMP0_d N_IN1_MMP0_g N_VDD!_MMP0_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=1.05e-06 AD=1.06575e-13 AS=1.68e-13 PD=1.253e-06 PS=2.42e-06 NRD=0.0961905
+ NRS=0.0952381 M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=1 SA=1.6e-07
+ SB=4.24e-07 SD=0 PANW1=8.22e-15 PANW2=3e-15 PANW3=3.24e-14 PANW4=3.66e-14
+ PANW5=3e-15 PANW6=1.104e-14 PANW7=8.7e-14 PANW8=2.4e-14 PANW9=3.678e-14
+ PANW10=9.96e-15
XMMP1 N_OUT_MMP0_d N_IN2_MMP1_g N_VDD!_MMP1_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=1.05e-06 AD=1.06575e-13 AS=1.6905e-13 PD=1.253e-06 PS=2.422e-06
+ NRD=0.0971429 NRS=0.0961905 M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=1
+ SA=4.23e-07 SB=1.61e-07 SD=0 PANW1=8.22e-15 PANW2=3e-15 PANW3=2.925e-14
+ PANW4=3.975e-14 PANW5=3e-15 PANW6=1.104e-14 PANW7=8.7e-14 PANW8=2.4e-14
+ PANW9=3.678e-14 PANW10=9.96e-15
*
.include "NAND.pex.sp.NAND.pxi"
```

Fig6: Netlist file

Detailed explanation on how you achieved the minimum AEDP:

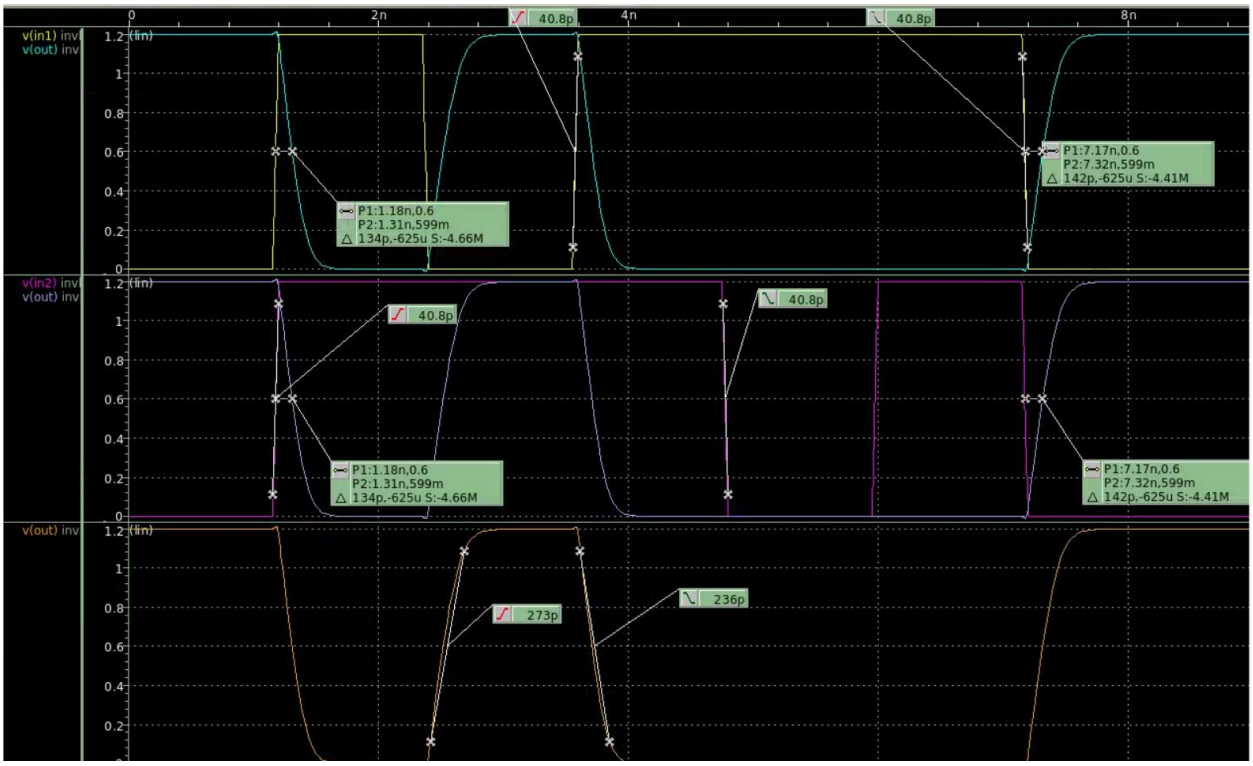
During the optimization process, I initially used a 2:1 pMOS:nMOS width ratio for a NAND2 gate. With this configuration, I observed a rise time (t_rise) of 79 ps and a fall time (t_fall) of 241 ps, resulting in a large t_diff (rise-fall delay difference). Since the delay difference was too high, I needed to optimize the transistor sizing.

Optimization Process:

1. Changing the pMOS:nMOS Ratio to 1.5:1:
    - This adjustment led to t_rise = 101 ps and t_fall = 239 ps.
    - The results indicated that reducing the pMOS width alone increases overall delay, rather than effectively balancing rise and fall times.
2. Increasing the nMOS Ratio (1:1.5 pMOS:nMOS):
    - This configuration resulted in t_rise = 144 ps and t_fall = 163 ps.
    - Although the delay difference decreased, it was still greater than 10 ps, which was my target.
3. Final Optimal Ratio (1.05:1.9 pMOS:nMOS):
    - After further tuning, I determined that a 1.05:1.9 pMOS:nMOS ratio provided the best trade-off between rise and fall times.
    - Interestingly, this ratio is the opposite of the typical inverter sizing ratio.
    - While this configuration minimized the delay difference, it also increased the layout area and slightly increased energy consumption.

Final Result:

With the 1.05:1.9 pMOS:nMOS ratio, I achieved an AEDP of 1.6×10^5 fJ·ps·μm². This indicates that the optimized transistor sizing significantly improved timing balance while still maintaining a reasonable energy-area tradeoff.



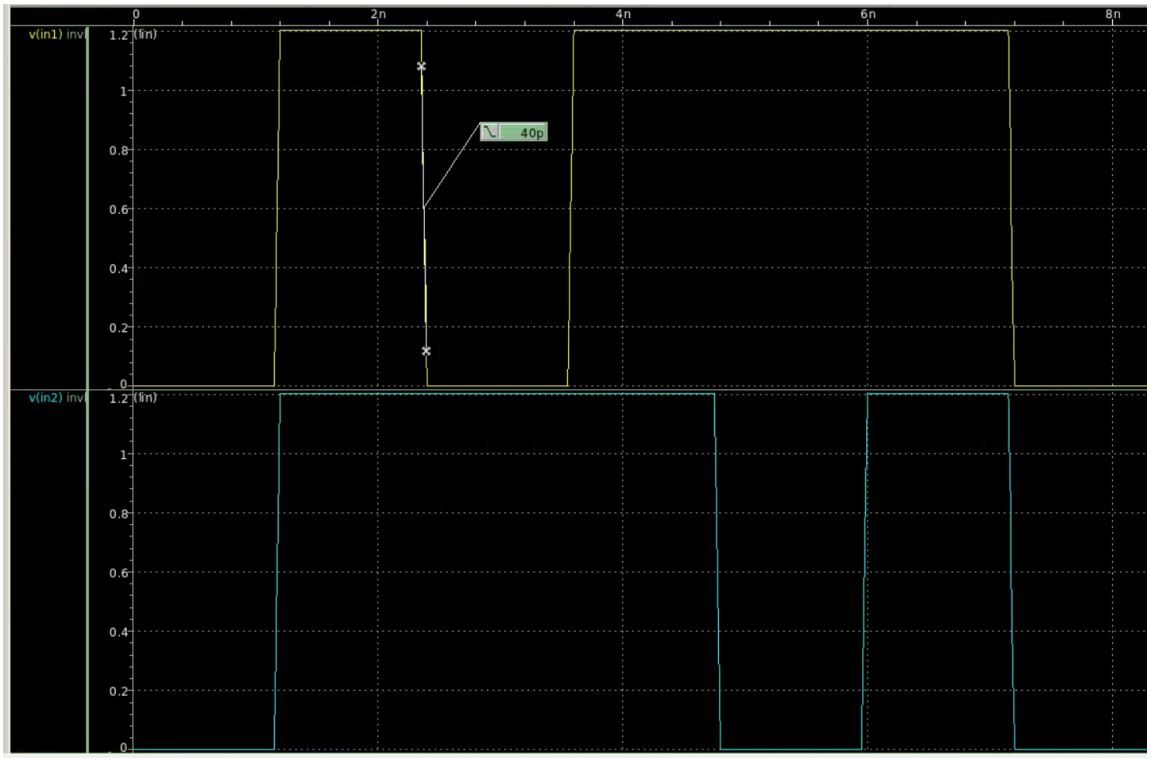


Fig6: Waveforms from WaveView

```
 errchk             0.04
 setup              0.00
 output             0.00


          peak memory used        381.50 megabytes
          total cpu time            1.71 seconds
          total elapsed time        7.17 seconds
          job started at     14:35:35 03/04/2025
          job ended   at     14:35:43 03/04/2025



info:         ***** hspice job concluded
 lic: Release hspice token(s)
 lic: total license checkout elapse time:        0.02(s)

nd of pVA simulation reached at time 0 on Tue Mar  4 14:35:43 2025     GTM/In-use: 61.0000/49.6117 MB


                       pVA malloc          4.840 Mbytes       100792 times
                       pVA calloc         79.544 Mbytes       547191 times
                       pVA realloc         3.622 Mbytes         1826 times
                       pVA valloc          0.000 Mbytes            0 times
                       pVA alloca          0.000 Mbytes            0 times

                       pVA TOT-MEM        88.006 Mbytes       649809 times
                       pVA free                               132695 times
                       pVA strdup          0.000 Mbytes            0 times


VA concluded on Tue Mar  4 14:35:43 2025       GTM/In-use: 61.0000/49.6117 MB
```

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
trise= 141.9889p  targ=   2.5170n   trig=   2.3750n
tfall= 133.9920p  targ=   1.3090n   trig=   1.1750n
tavg= 137.9905p
tdiff=   7.9969p
delay= 141.9889p
iavg= -25.2261u  from=   0.             to=  10.0000n
energy=-302.7127f
edp1= 4.2982e-23
t1=   2.3504n
t2=   2.8651n
t3=   1.1504n
t4=   1.5968n
i1=-243.9817u  from=   2.3504n     to=   2.8651n
i2=   1.1509u  from=   1.1504n     to=   1.5968n
energy1=-150.6854f
energy2= 616.4541a
energysum=-150.0690f
edp2= 2.0708e-23

         ***** job concluded
******
```

Fig7: Screenshot of HSPICE output terminal showing the simulation results

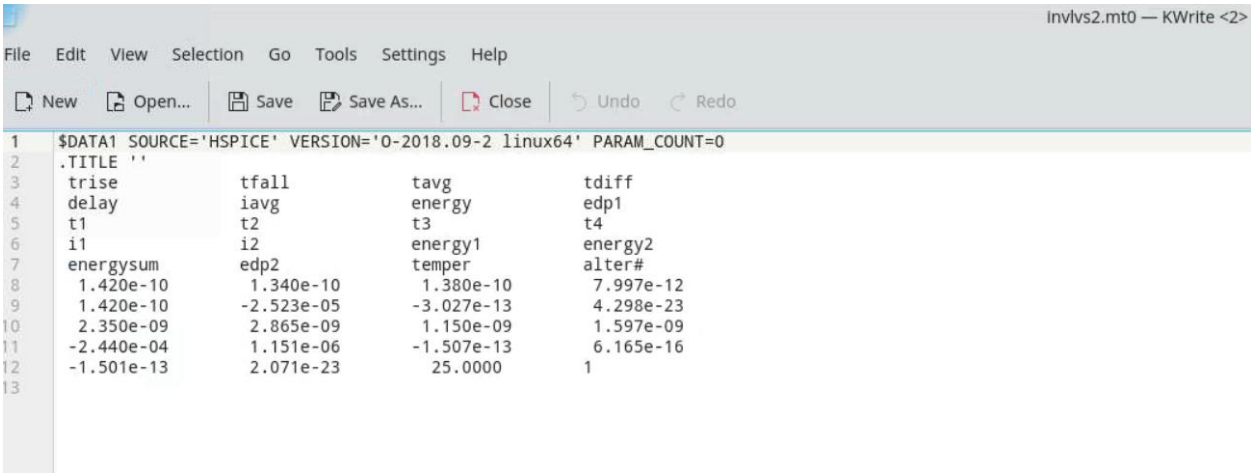


Fig8: .mt0 file