

1. For the following 4-bit addition operations use equations 11.4-11.7 and fig. 11.12 to

a) compute $G_0, G_1, G_2, G_3, G_4, P_0, P_1, P_2, P_3$, and P_4 .

b) use the results from a) to compute $G_{0:0}, G_{1:0}, G_{2:0}$, and $G_{3:0}$.

c) use the results from a) and b) to compute the sum bits, $S_1 - S_4$, and carry-out (overflow) bit, C_{out} , of the operations and verify by converting to decimal.

$$\begin{array}{r} 1011 \\ +0111 \\ \hline \end{array}$$

$$\begin{array}{r} 1000 \\ +1111 \\ \hline \end{array}$$

$$\begin{array}{r} 0011 \\ +1010 \\ \hline \end{array}$$

1.

$$\begin{array}{r} 1011 \\ +0111 \\ \hline 10010 \end{array}$$

↓

$$\begin{array}{r} 11 \\ +7 \\ \hline 18 \end{array}$$

a.

$$\begin{aligned} G_0 &= C_{in} = 0 & P_0 &= 0 \\ G_1 &= 1 \cdot 1 = 1 & P_1 &= 1 \oplus 1 = 0 \\ G_2 &= 1 \cdot 1 = 1 & P_2 &= 1 \oplus 1 = 0 \\ G_3 &= 0 \cdot 1 = 0 & P_3 &= 0 \oplus 1 = 1 \\ G_4 &= 1 \cdot 0 = 0 & P_4 &= 1 \oplus 0 = 1 \end{aligned}$$

b.

$$\begin{aligned} G_{0:0} &= G_0 = 0 \\ G_{1:0} &= G_{1:1} + P_{1:1} \cdot G_{0:0} = 1 \\ G_{2:0} &= G_{2:2} + P_{2:2} \cdot G_{1:0} = 1 \\ G_{3:0} &= G_{3:3} + P_{3:3} \cdot G_{2:0} = 0 + 1 = 1 \\ G_{4:0} &= G_{4:4} + P_{4:4} \cdot G_{3:0} = 0 + 1 = 1 \end{aligned}$$

$$c. S_1 = P_1 \oplus G_{0:0} = 0 \oplus 0 = 0$$

$$S_2 = P_2 \oplus G_{1:0} = 0 \oplus 1 = 1$$

$$S_3 = P_3 \oplus G_{2:0} = 1 \oplus 1 = 0$$

$$S_4 = P_4 \oplus G_{3:0} = 1 \oplus 1 = 0$$

$$C_{out} = G_{4:0} = 1$$

$$ans = 10010 = 18$$

$$\begin{array}{r} 1000 \\ + 1111 \\ \hline 10111 \end{array}$$

↓

$$\begin{array}{r} 8 \\ + 15 \\ \hline 23 \end{array}$$

$$a. G_0 = C_{in} = 0$$

$$P_0 = 0$$

$$G_1 = 0 \cdot 1 = 0$$

$$P_1 = 0 \oplus 1 = 1$$

$$G_2 = 0 \cdot 1 = 0$$

$$P_2 = 0 \oplus 1 = 1$$

$$G_3 = 0 \cdot 1 = 0$$

$$P_3 = 0 \oplus 1 = 1$$

$$G_4 = 1 \cdot 1 = 1$$

$$P_4 = 1 \oplus 1 = 0$$

$$b. G_{0:0} = 0$$

$$G_{1:0} = 0$$

$$G_{2:0} = 0$$

$$G_{3:0} = 0$$

$$G_{4:0} = 1$$

$$C \cdot S_1 = 1$$

$$S_2 = 1$$

$$S_3 = 1$$

$$S_4 = 0$$

$$\text{Count} = 1$$

$$\text{ans} = 1011$$

$$\begin{array}{r} 0011 \\ 1010 \\ \hline 1101 \end{array}$$

↓

$$\begin{array}{r} 3 \\ + 10 \\ \hline 13 \end{array}$$

$$a. \quad G_0 = 0 \quad P_0 = 0$$

$$G_1 = 0 \quad P_1 = 1$$

$$G_2 = 1 \quad P_2 = 0$$

$$G_3 = 0 \quad P_3 = 0$$

$$G_4 = 0 \quad P_4 = 1$$

$$b. \quad G_{0:0} = 0$$

$$G_{1:0} = 0$$

$$G_{2:0} = 1$$

$$G_{3:0} = 0$$

$$G_{4:0} = 0$$

$$C \cdot S_1 = 1$$

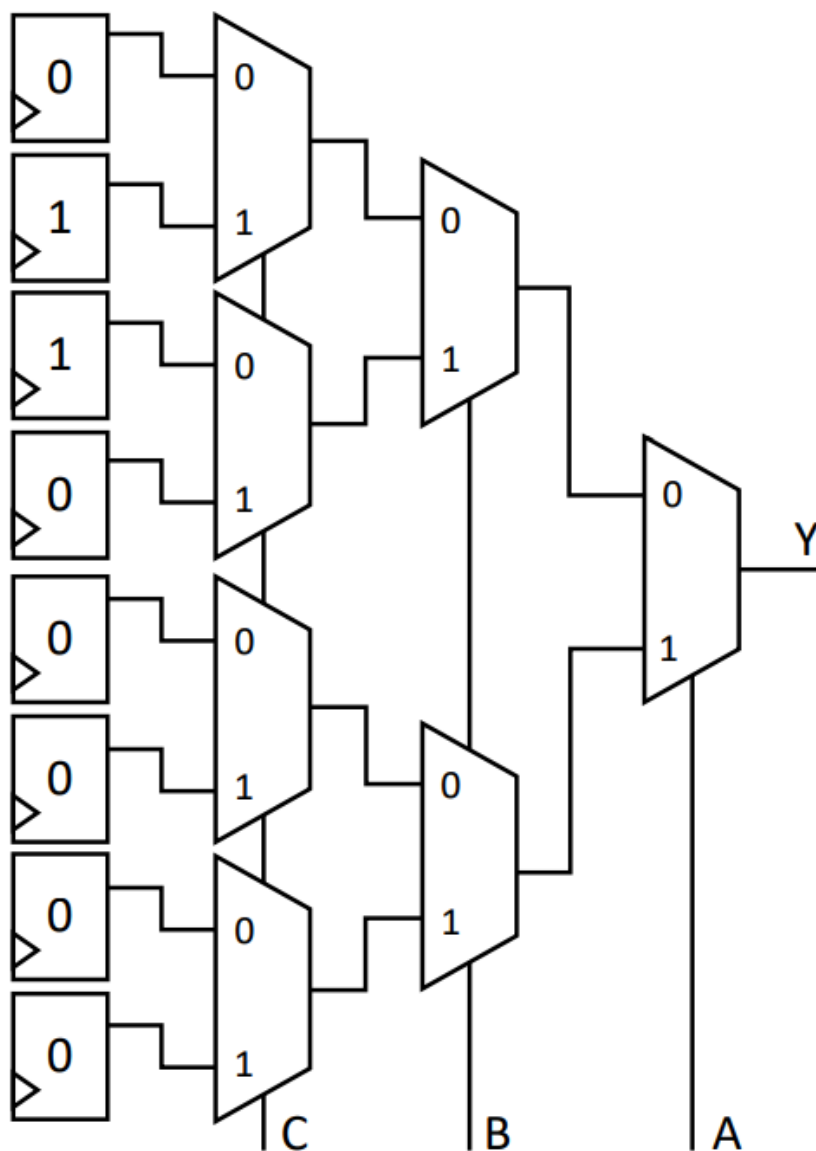
$$S_2 = 0$$

$$S_3 = 1$$

$$S_4 = 1$$

$$\text{Count} = 0 \quad \text{ans} = 1101$$

2. Find the logic operation implemented by the lookup table (LUT) depicted. A value inside a memory cell, indicates that that is the value stored in that cell.



2.

Truth Table.

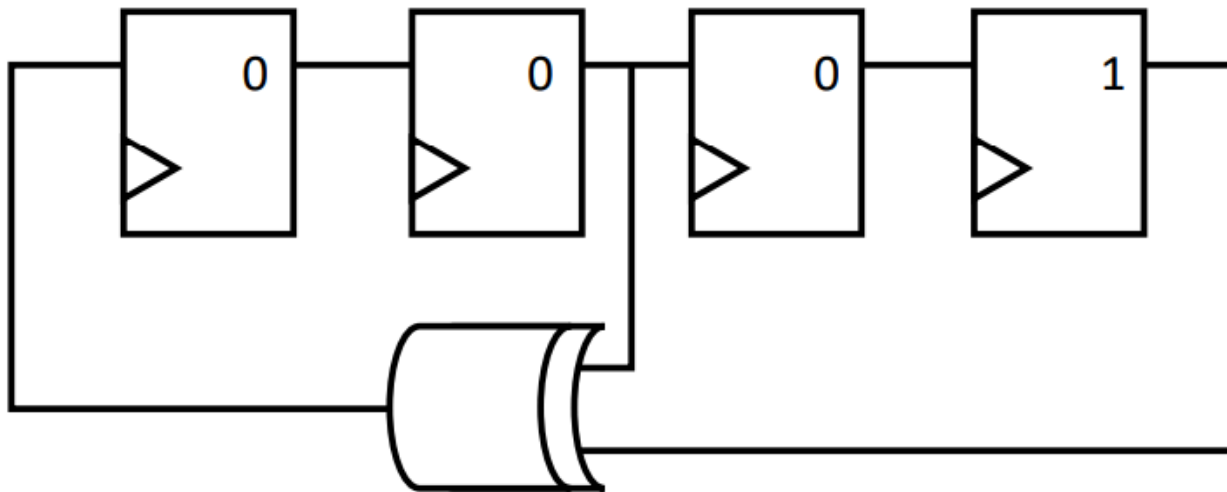
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

looks like xor (B, C)

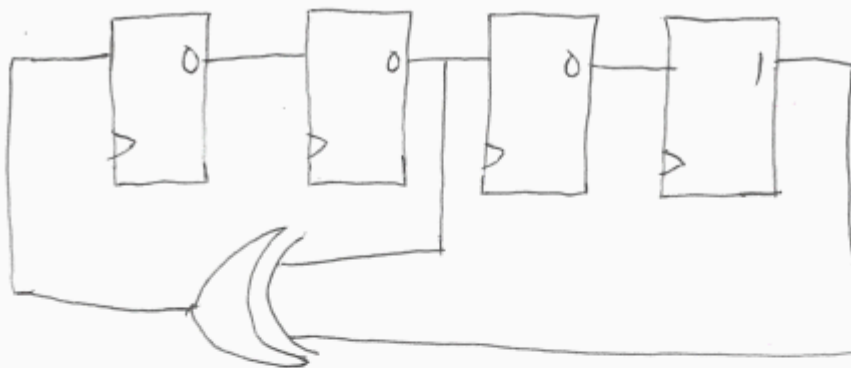
looks like \bar{A} Answer $\rightarrow \bar{A}(B \oplus C)$ [just one expression]

Other forms exist such as the minterm expression ($\bar{A}\bar{B}C + \bar{A}B\bar{C}$),
 Maxterm expression, etc.

3. Predict the output of the following LFSR assuming it starts in the 0001 state and has a steady clock input. What is the cycle length of this LFSR? Redesign the circuit so it has a cycle of maximal-length (length 15). (The weird-looking gate is an XOR)



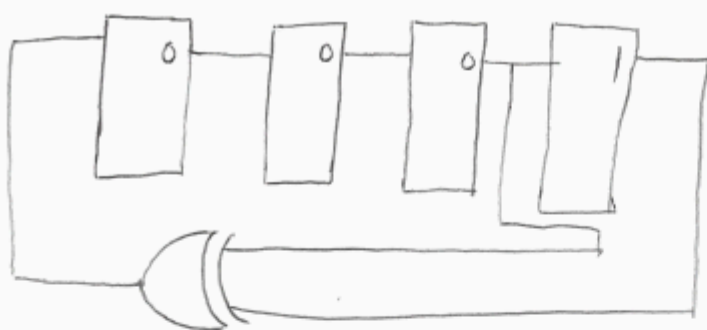
3.



→ 0 0 0 1
 1 0 0 0
 0 1 0 0
 1 0 1 0
 0 1 0 1
 0 0 1 0
 → 0 0 0 1

6 steps to get back to the start

cycle length = 6



~~0000~~ 0001
 1000
 0100
 0010
 1001
 1100
 0110
 1011
 0101
 1010
 1101
 1110
 1111

0111
 0011
 0001

Cycle length = 15