EECT/CE 6325 VLSI DESIGN

PR#4 D Flip-Flop Design Competition

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Partner Name: Xiongtao Zhang

Minimum Clock Period TMIN	Maximum Clock Period TMAX	Layout Width (nm)	Layout Height (nm)	Worst-Case Setup Time, tsetup (ps)
0.8ns	infinity	1970	4189	50
Worst-Case Clock-to output delay, tc2q (ps)	Average Overall Transition Energy, E (fJ)	EDP(E×(tsetup+tc2q)) (fJ.ps)	Layout Area, A (nm2)	AEDP (EDP× A) (fJ.ps.nm2)
102.58	115.9	17,684.022	8,252,330	145,934,203,720 or $1.45x10^{11}$

1. Description:

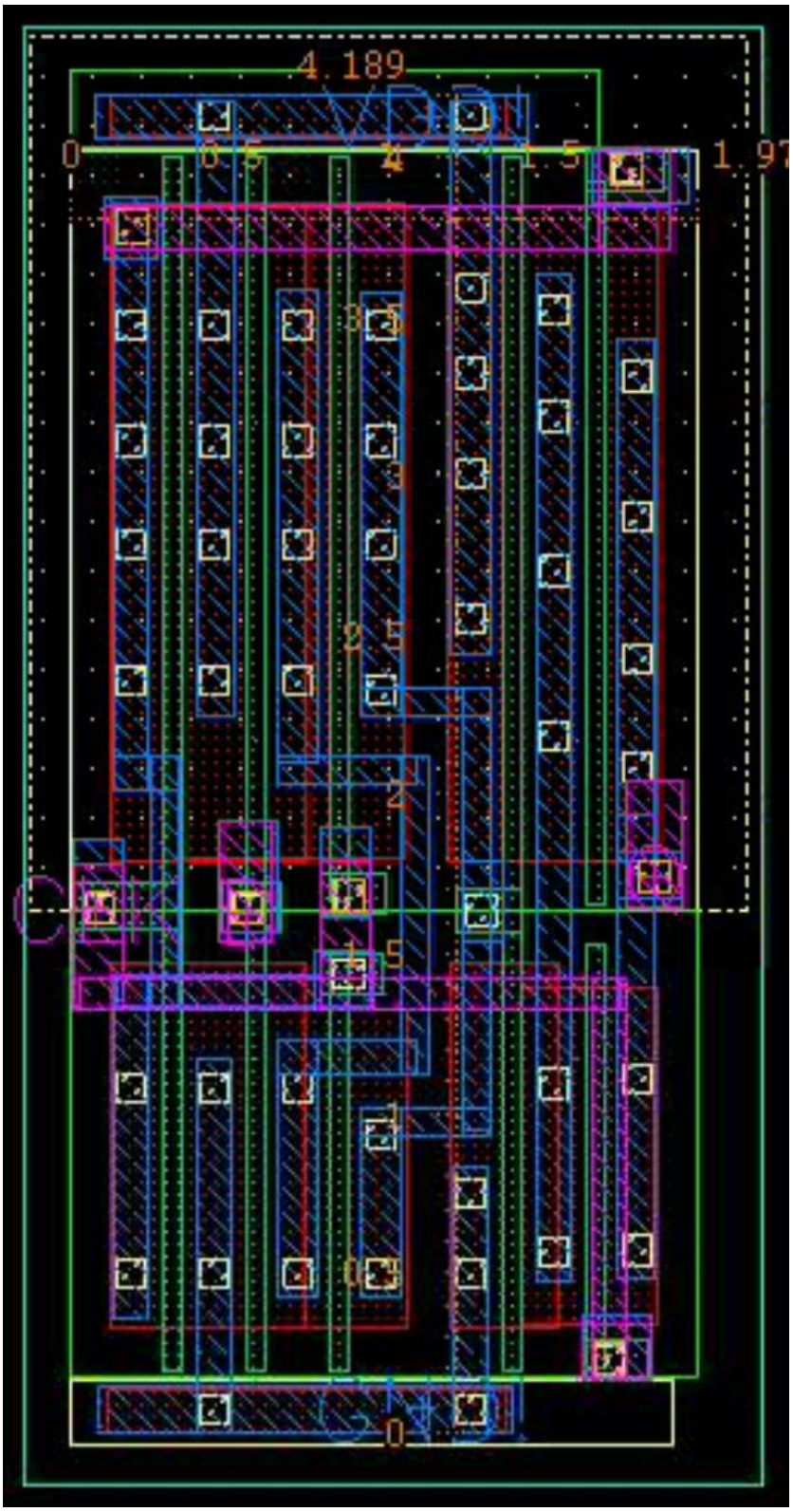

Figure 1.1 Overall Layout (with cell height=4.189 width=1.97 (um))

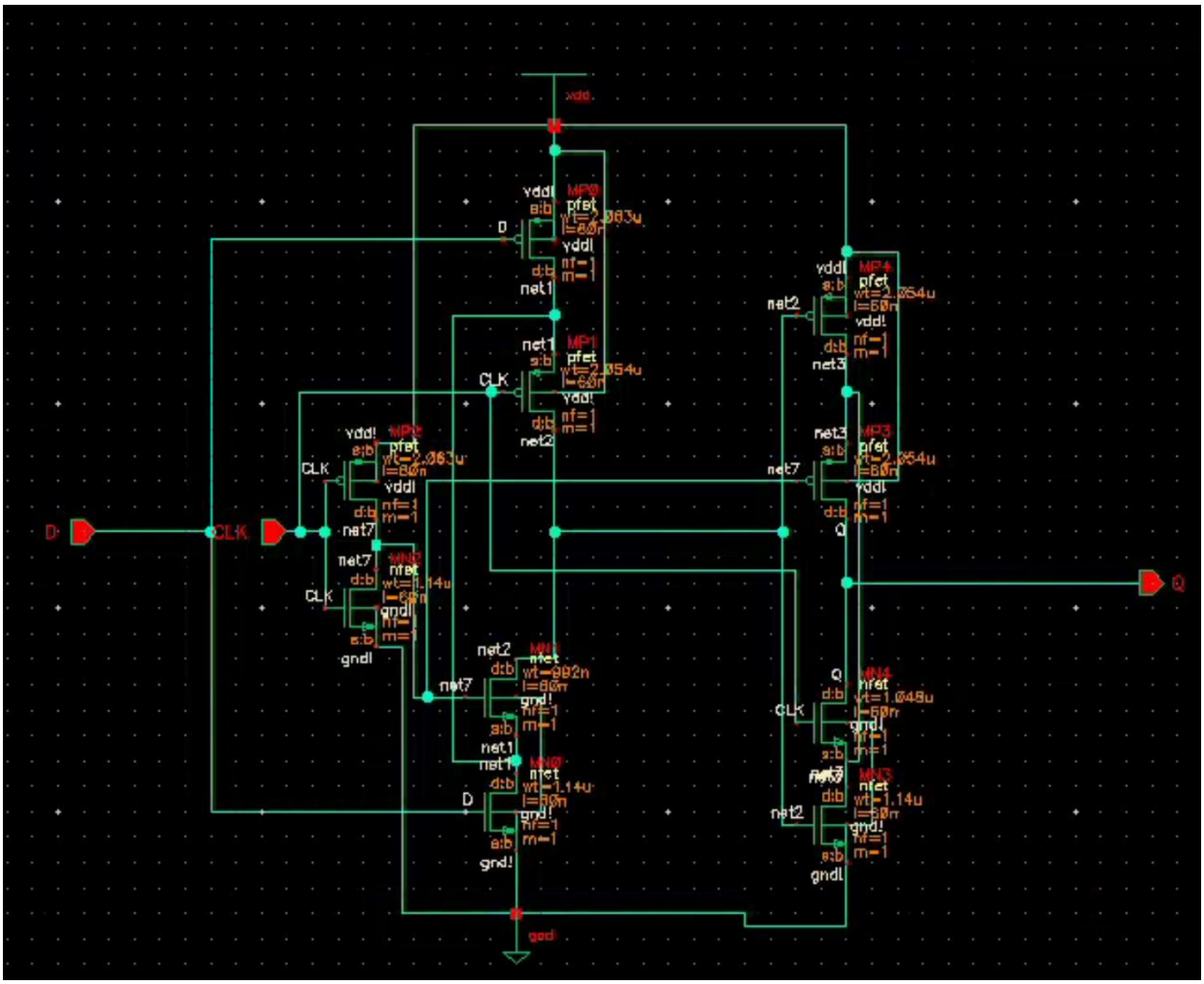

Figure 2.1 Schematic

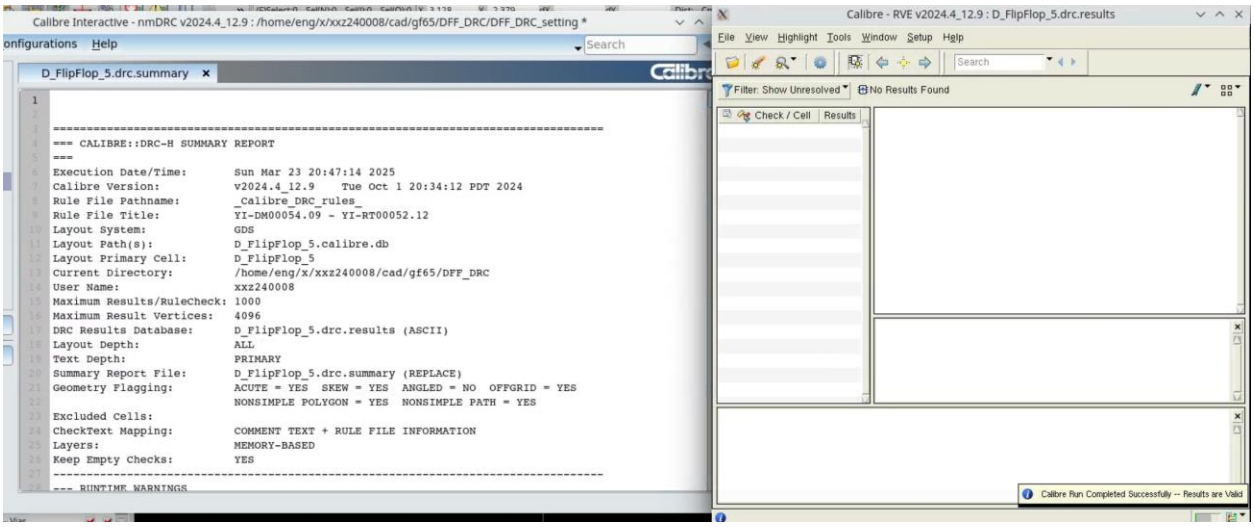

Figure 3 DRC report

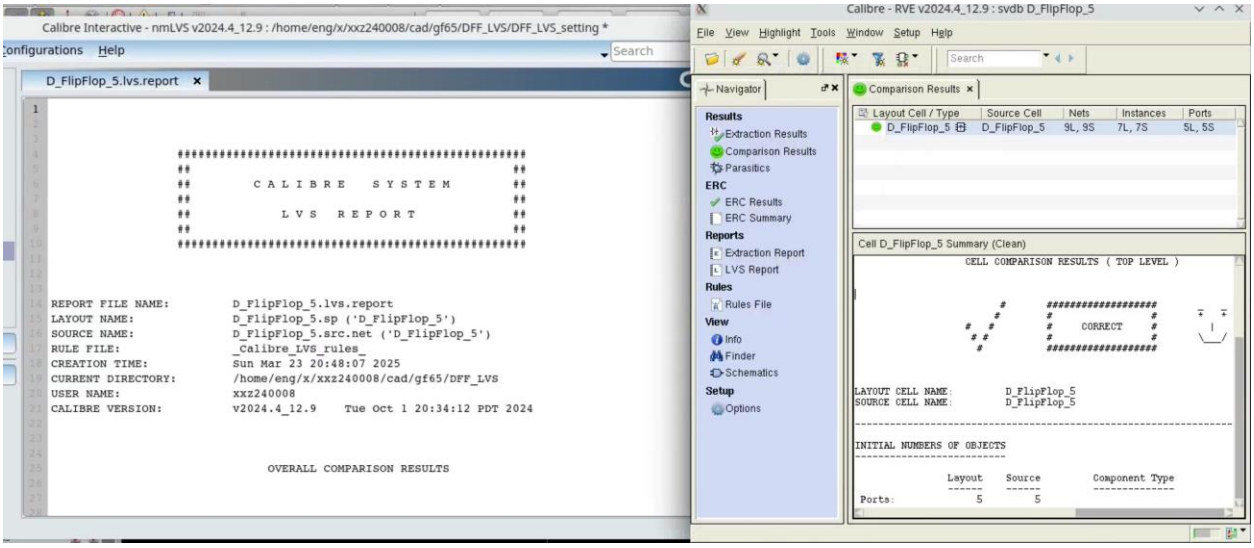

Figure 4 LVS report

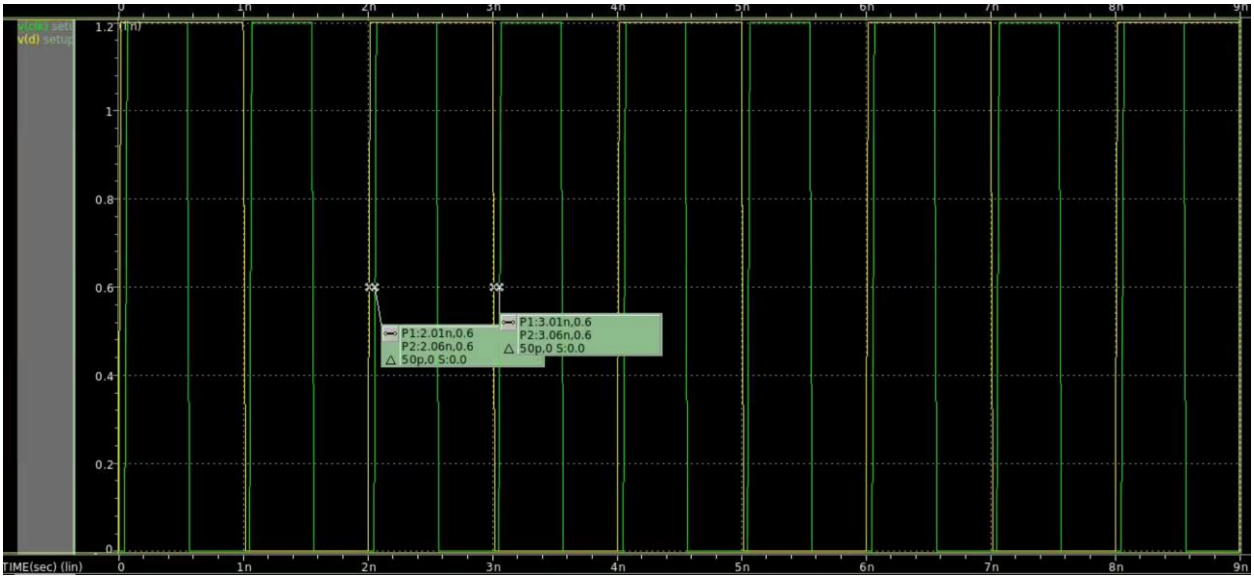

Figure 5 Waveform of clk, d, showing tsetup

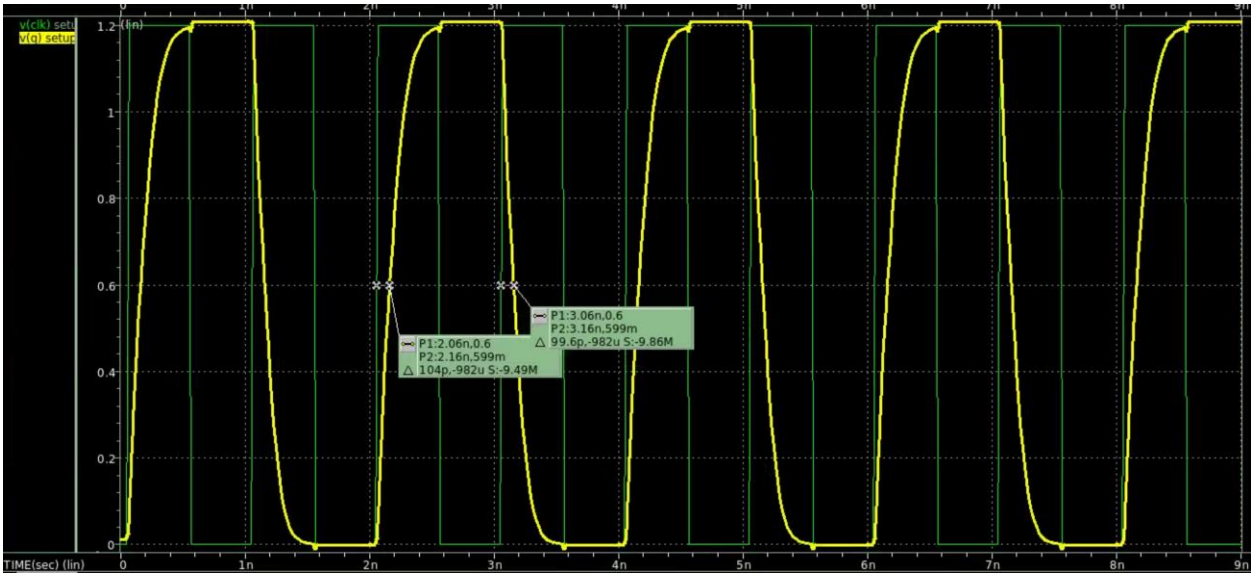

Figure 6 Waveform of clk, q, showing tpcq

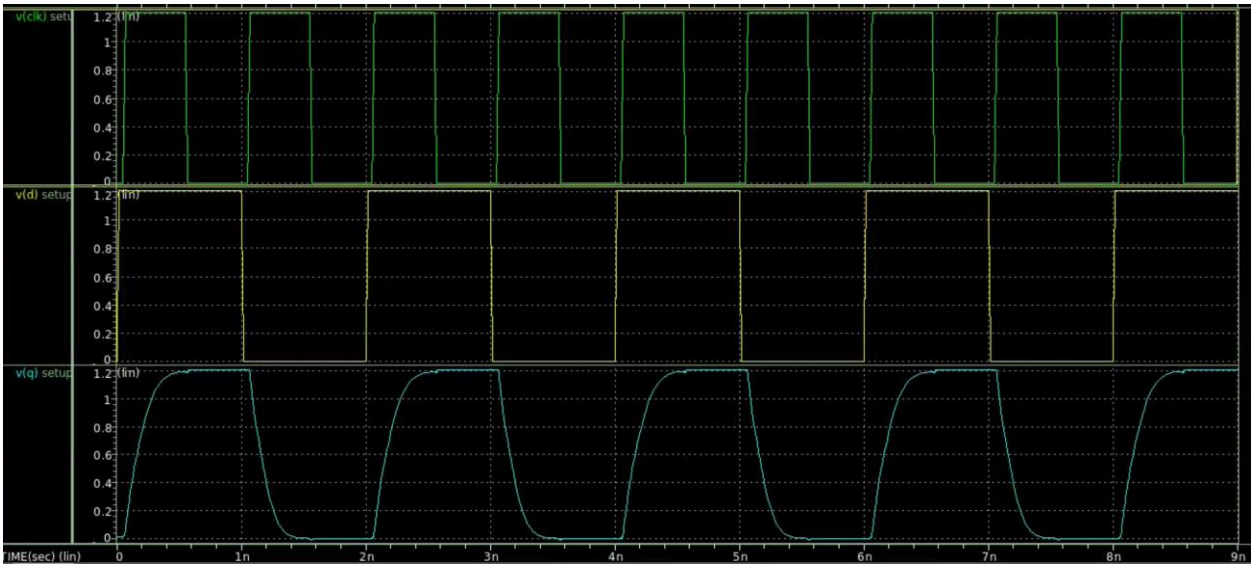

Figure 7 Waveform of clk, d, q (T=1ns, Tall=2*T=2ns, Phase of D = 50ps)

```
* File: D_FlipFlop_5.pex.netlist Untitled-1 ●
.include "D_FlipFlop_5.pex.netlist.pex"
.subckt D_FlipFlop_5  GND! Q VDD! CLK D
*
* D D
* CLK   CLK
* VDD!  VDD!
* Q Q
* GND!  GND!
XD0_noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENWX  AREA=6.14107e-12
+ PERIM=9.964e-06
XMMN2 N_NET7_MMN2_d N_CLK_MMN2_g N_GND!_MMN2_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=1.14e-06 AD=1.8696e-13 AS=1.1457e-13 PD=2.608e-06 PS=1.341e-06 NRD=0.0885965
+ NRS=0.0885965 M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=0 SA=1.64e-07
+ SB=6.65807e-07 SD=0 PANW1=8.4e-15 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15
+ PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=1.8e-14 PANW10=0
XMMN0 N_NET1_MMN0_d N_D_MMN0_g N_GND!_MMN2_s N_GND!_D0_noxref_pos NFET L=6e-08
+ W=1.14e-06 AD=1.15741e-13 AS=1.1457e-13 PD=1.43302e-06 PS=1.341e-06
+ NRD=0.0877193 NRS=0.0877193 M=1 NF=1 CNR_SWITCH=2 PCCRIT=0 PAR=1 PTWELL=0
+ SA=4.25e-07 SB=4.04807e-07 SD=0 PANW1=8.4e-15 PANW2=3e-15 PANW3=3e-15
+ PANW4=3e-15 PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=1.8e-14
+ PANW10=0
XMMN1 N_NET2_MMN1_d N_NET7_MMN1_g N_NET1_MMN0_d N_GND!_D0_noxref_pos NFET
+ L=6e-08 W=9.92e-07 AD=1.85504e-13 AS=1.00715e-13 PD=2.358e-06 PS=1.24698e-06
+ NRD=0.10131 NRS=0.100806 M=1 NF=1 CNR_SWITCH=2 PCCRIT=0 PAR=1 PTWELL=0
+ SA=6.85e-07 SB=1.87e-07 SD=0 PANW1=0 PANW2=2.52e-15 PANW3=3e-15 PANW4=3e-15
+ PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=1.8e-14 PANW10=0
XMMN3 N_NET3_MMN3_d N_NET2_MMN3_g N_GND!_MMN3_s N_GND!_D0_noxref_pos NFET
+ L=6e-08 W=1.14e-06 AD=1.16405e-13 AS=1.8696e-13 PD=1.39947e-06 PS=2.608e-06
+ NRD=0.0894737 NRS=0.0877193 M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=0
+ SA=1.64e-07 SB=3.98225e-07 SD=0 PANW1=8.4e-15 PANW2=3e-15 PANW3=3e-15
+ PANW4=3e-15 PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=1.8e-14
+ PANW10=0
XMMN4 N_Q_MMN4_d N_CLK_MMN4_g N_NET3_MMN3_d N_GND!_D0_noxref_pos NFET L=6e-08
+ W=1.048e-06 AD=1.6768e-13 AS=1.07011e-13 PD=2.416e-06 PS=1.28653e-06
+ NRD=0.0954198 NRS=0.096374 M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=0
+ SA=4.27e-07 SB=1.6e-07 SD=0 PANW1=3.54e-15 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15
+ PANW5=3e-15 PANW6=6e-15 PANW7=1.2e-14 PANW8=1.2e-14 PANW9=1.734e-14 PANW10=0
XMMP2 N_NET7_MMP2_d N_CLK_MMP2_g N_VDD!_MMP2_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=2.063e-06 AD=3.38332e-13 AS=2.07331e-13 PD=4.454e-06 PS=2.264e-06
+ NRD=0.0484731 NRS=0.0489578 M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=1
+ SA=1.64e-07 SB=6.94626e-07 SD=0 PANW1=8.34e-15 PANW2=3e-15 PANW3=3e-15
+ PANW4=8.1394e-14 PANW5=4.8386e-14 PANW6=1.08e-14 PANW7=2.4e-14 PANW8=2.4e-14
+ PANW9=4.8e-14 PANW10=1.9578e-13
XMMP0 N_NET1_MMP0_d N_D_MMP0_g N_VDD!_MMP2_s N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=2.063e-06 AD=2.0639e-13 AS=2.07331e-13 PD=2.26795e-06 PS=2.264e-06
+ NRD=0.0484731 NRS=0.0484731 M=1 NF=1 CNR_SWITCH=2 PCCRIT=0 PAR=1 PTWELL=1
+ SA=4.25e-07 SB=4.33626e-07 SD=0 PANW1=8.34e-15 PANW2=3e-15 PANW3=3e-15
+ PANW4=3e-15 PANW5=3e-15 PANW6=1.08e-14 PANW7=1.4778e-13 PANW8=2.4e-14
+ PANW9=4.8e-14 PANW10=1.9578e-13
XMMP1 N_NET2_MMP1_d N_CLK_MMP1_g N_NET1_MMP0_d N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=2.054e-06 AD=3.5945e-13 AS=2.0549e-13 PD=4.458e-06 PS=2.25805e-06
+ NRD=0.0486855 NRS=0.0486855 M=1 NF=1 CNR_SWITCH=2 PCCRIT=0 PAR=1 PTWELL=1
+ SA=6.85e-07 SB=1.75e-07 SD=0 PANW1=7.8e-15 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15
+ PANW5=3e-15 PANW6=1.08e-14 PANW7=2.4e-14 PANW8=1.4724e-13 PANW9=1.7124e-13
+ PANW10=7.2e-14
XMMP4 N_NET3_MMP4_d N_NET2_MMP4_g N_VDD!_MMP4_s N_VDD!_D0_noxref_neg PFET
+ L=6e-08 W=2.054e-06 AD=2.08481e-13 AS=3.61504e-13 PD=2.257e-06 PS=4.46e-06
+ NRD=0.0491723 NRS=0.0491723 M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=1
+ SA=1.76e-07 SB=4.23e-07 SD=0 PANW1=8.4e-15 PANW2=3e-15 PANW3=3e-15 PANW4=3e-15
+ PANW5=3e-15 PANW6=1.02e-14 PANW7=1.4724e-13 PANW8=2.4e-14 PANW9=4.8e-14
+ PANW10=1.9524e-13
XMMP3 N_Q_MMP3_d N_NET7_MMP3_g N_NET3_MMP4_d N_VDD!_D0_noxref_neg PFET L=6e-08
+ W=2.054e-06 AD=3.2864e-13 AS=2.08481e-13 PD=4.428e-06 PS=2.257e-06
+ NRD=0.0486855 NRS=0.0496592 M=1 NF=1 CNR_SWITCH=1 PCCRIT=0 PAR=1 PTWELL=1
+ SA=4.39e-07 SB=1.6e-07 SD=0 PANW1=8.4e-15 PANW2=3e-15 PANW3=3e-15
+ PANW4=2.1486e-14 PANW5=1.057e-13 PANW6=1.2254e-14 PANW7=2.4e-14 PANW8=2.4e-14
+ PANW9=4.8e-14 PANW10=1.9524e-13
*
.include "D_FlipFlop_5.pex.netlist.D_FLIPFLOP_5.pxi"
*
.ends
*
```

Figure 8 Extracted Spice Netlist

```
* File: D_FlipFlop
* Created: Mon Feb 24 00:11:17 2025
* Program "Calibre xRC"
* Version "v2024.4_12.9"
*
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "D_FlipFlop_5.pex.netlist"
.option post runlvl=5

X2 GND! Q VDD! CLK D D_FlipFlop_5


vdd VDD! GND! 1.2v
*                  1              0         clk 3.2n rise              1                      0

vin1 D GND PULSE(0v 1.2v 0ps 20ps 20ps 0.98ns 2ns)
vin2 CLK GND PULSE(0v 1.2v 50ps 20ps 20ps 0.48ns 1ns)
cout Q GND! 50f

.tr 0.1ps 9ns
*.tr 1ps 9ns sweep W 0.5u 1.5u 0.025u

.measure tran tpcq trig v(CLK) val=0.6v rise=1 targ v(Q) val=0.6v rise=1 $tpcq
.measure tran tsetup trig v(D) val=0.6v fall=1 targ v(CLK) val=0.6v rise=1 from=0.9n




.measure tran iavg avg i(vdd) from=2n to=4n
.measure energy param = 1.2*iavg*2n



.end

*
*
```

Figure 9 SPICE setup.sp file

```
******
* file: d_flipflop

****** transient analysis tnom=  25.000 temp=  25.000 ******
tpcq= 102.5860p  targ= 162.5860p   trig=  60.0000p
tsetup=  50.0000p  targ=   1.0600n   trig=   1.0100n
iavg= -48.3096u  from=   2.0000n     to=   4.0000n
energy=-115.9430f

         ***** job concluded
******
* file: d_flipflop

****** job statistics summary tnom=  25.000 temp=  25.000 ******
```

Figure 10 SPICE measurement (tsetup=50ps, tpcq=102.58ps, energy=115.9fJ)

```
$DATA1 SOURCE='HSPICE' VERSION='O-2018.09-2 linux64' PARAM_COUNT=0
.TITLE '* file: d_flipflop'
 tpcq              tsetup           iavg             energy
 temper            alter#
  1.026e-10         5.000e-11       -4.831e-05       -1.159e-13
   25.0000         1
```

Figure 11 mt0 file

2. Achieved the minimum AEDP:

1. Adjust the ratio between width of NMOS and PMOS. In this case, the P/N MOS width ratio = 1.8 achieves the minimum AEDP.

2. Optimize layout. The D Flipflop designed contains 10 transistors, the routing of the metal wire and the placement of VIAs are optimized to make full use of the area.

3. Apply different width of different transistor to optimize area. Some transistors, e.g. the clock inverter, affect the overall delay less, some transistors e.g. the output transmission gate, affect the overall performance more. Balance the width of different transistor achieves the minimum AEDP.