

Task	Assigned to	Time(hours)		Due date
learn assembly	Team	2		13/11/2015
design CPU test bench	Team	1		14/11/2015
code in assembly	Team?	1.5		
Write a README	Yuzhong	0.5		
understand	Team	1.5		20/11/2015
PC Design		0.5		17/11/2015
PC test		0.25		
Memory Design		1		
Memory Test		0.5		
RegFile Design		0.5		
RegFile Test		0.5		
IR		0.5		
IR Test		0.5		
32-bit Reg		0.5		
32-bit Reg Test		0.5		
Concat		0.25		
Concat Test		0.25		
SE		0.25		
SE Test		0.25		
MUXs		0.25		
MUXs Test		0.25		
Shifter Design		0.5		
Shifter Test		0.5		
Behavioral ALU		1		
FSM Design	Team	1.5		10/11/2015
FSM Test	Team	2		10/11/2015
Combine test cases	Team	1		18/11/2015
Report	Team	2		19/11/2015
Upload to FPGA	Team	1		18/11/2015
Everything		22.75		20/11/2015