

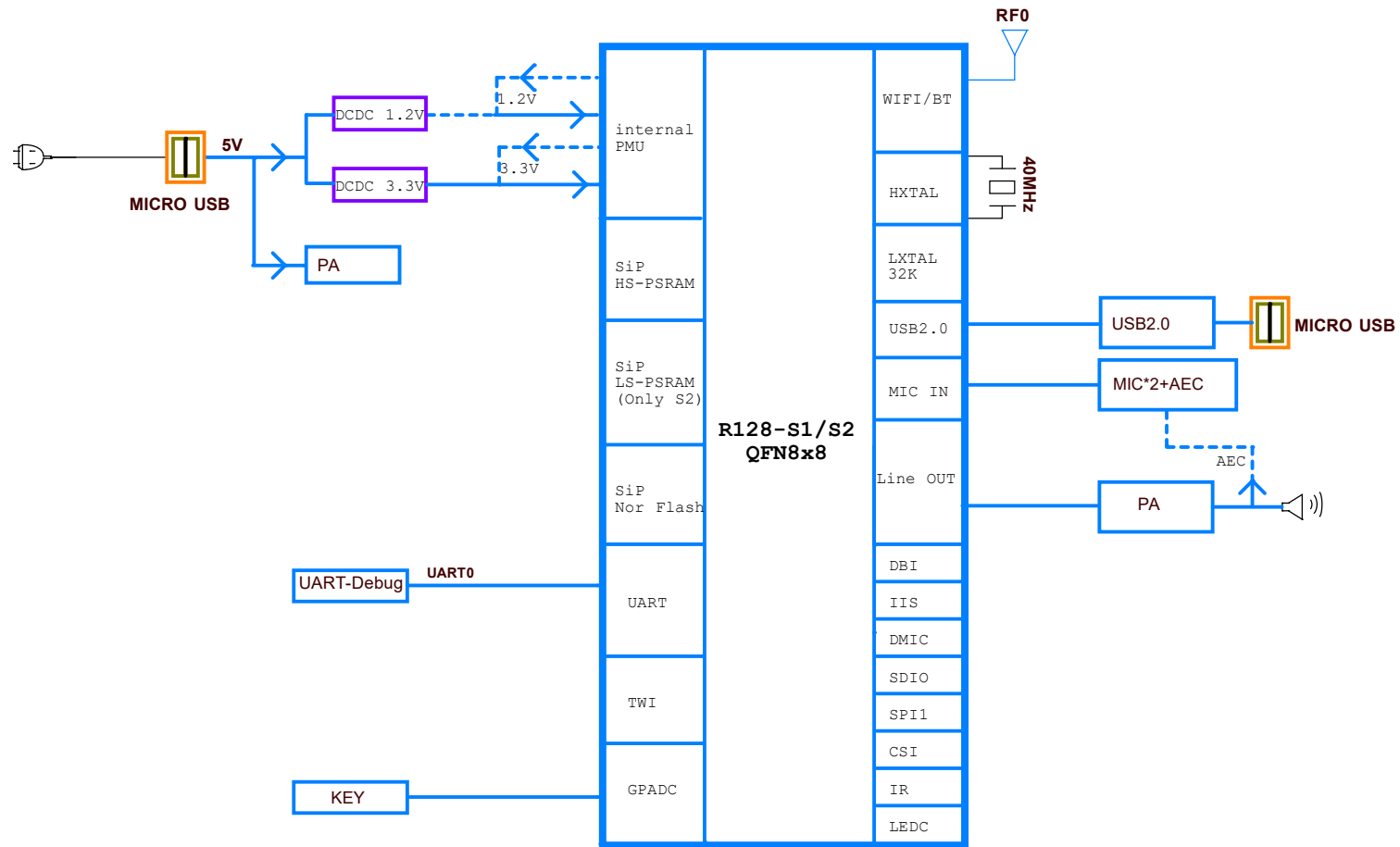
VERSION HISTORY

Index:

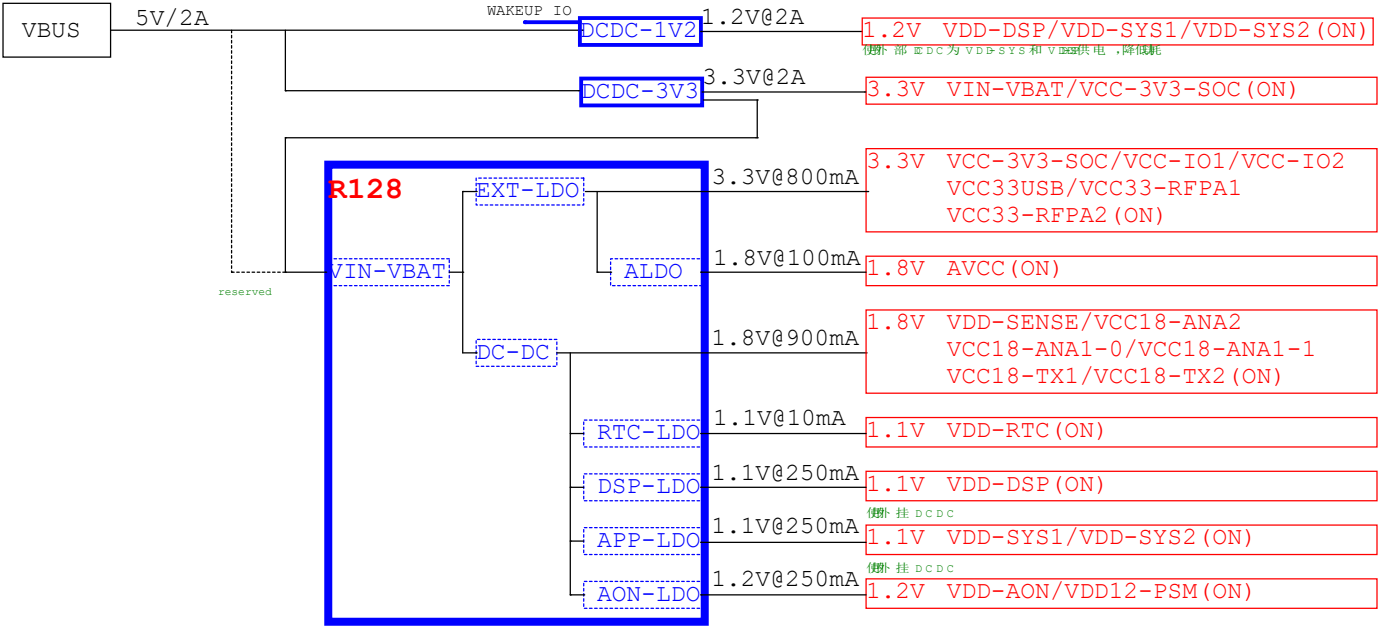
- P01 REVISION HISTORY
- P02 BLOCK DIAGRAM
- P03 POWER TREE
- P04 IO ASSIGNMENT
- P05 POWER
- P06 R128-S2
- P07 AUDIO
- P08 UART/KEY
- P09 WIFI&BT

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0		20221206	AWA1822		

BLOCK



POWER TREE

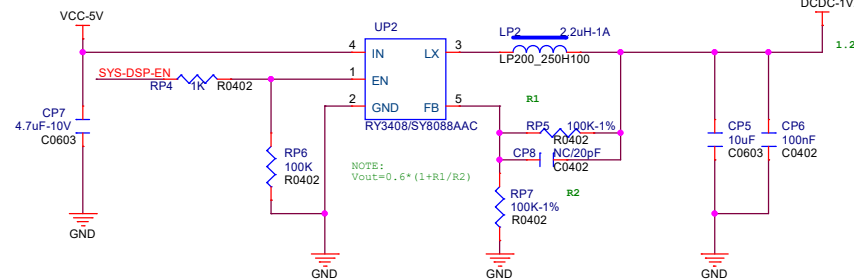


IO ASSIGNMENT

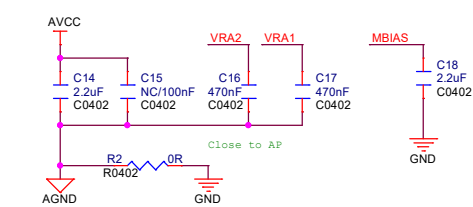
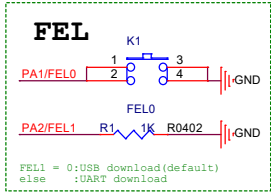
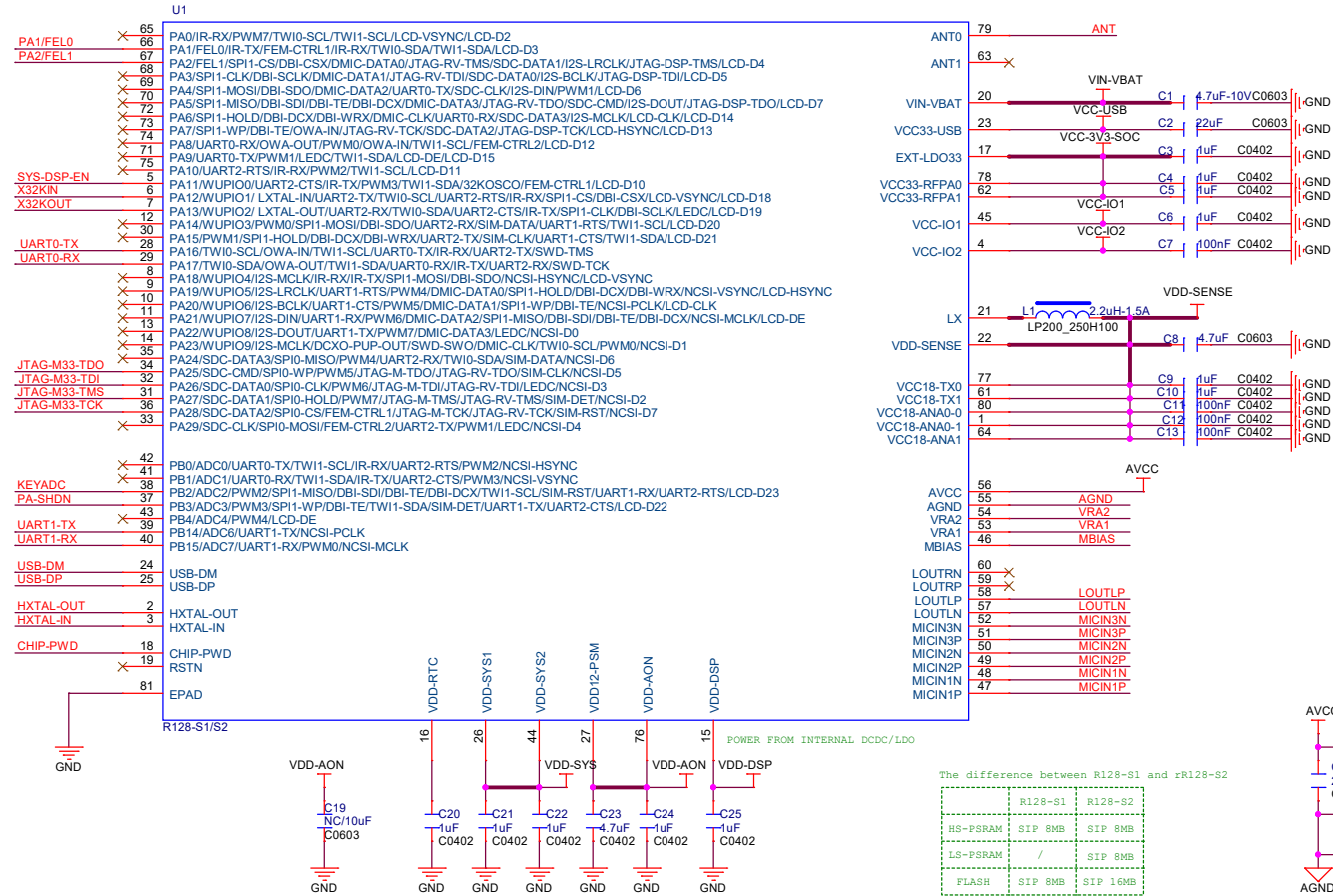
PIN	Define1	CFG	Function
PA0			FEL
PA1	FEL0		
PA2	FEL1		
PA3			
PA4			
PA5			
PA6			
PA7			
PA8			
PA9			
PA10			
PA11	DSP-SYS-EN	1	
PA12	X32KIN		
PA13	X32KOUT		
PA14			
PA15			
PA16	UART0-TX	5	DEBUG
PA17	UART0-RX	5	
PA18			
PA19			
PA20			
PA21			
PA22			
PA23			
PA24			
PA25	JTAG-M33-TDO	8	DEBUG
PA26	JTAG-M33-TDI	8	
PA27	JTAG-M33-TMS	8	
PA28	JTAG-M33-TCK	8	
PA29			

PIN	Define	CFG	Function
PB0/ADC0			KEY
PB1/ADC1			
PB2/ADC2	KEYADC		
PB3/ADC3	PA-SHDN	1	PA
PB4/ADC4			DEBUG
PB14/ADC6	UART1-TX	2	
PB15/ADC7	UART1-RX	2	

DCDC 1.2V

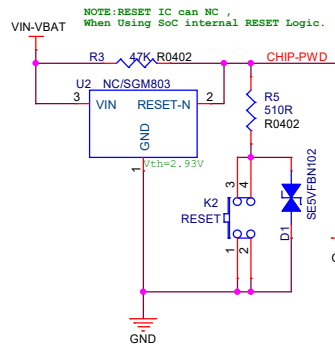


SOC

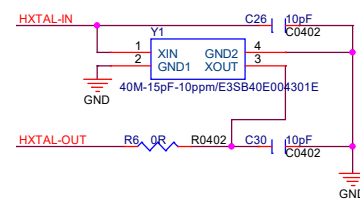


RESET

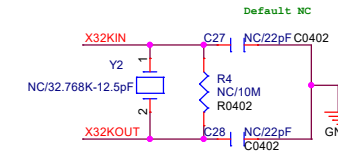
- 1.AP=RESETN signal shall be far away from the edge of the board and interference signal.
- 2.AP=RESETN signal shall be surrounded by GND trace



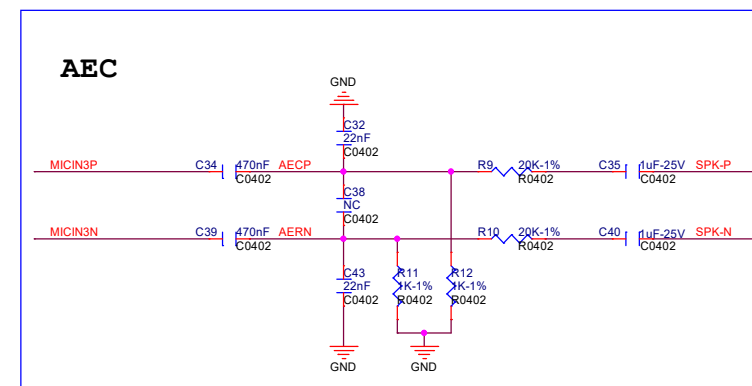
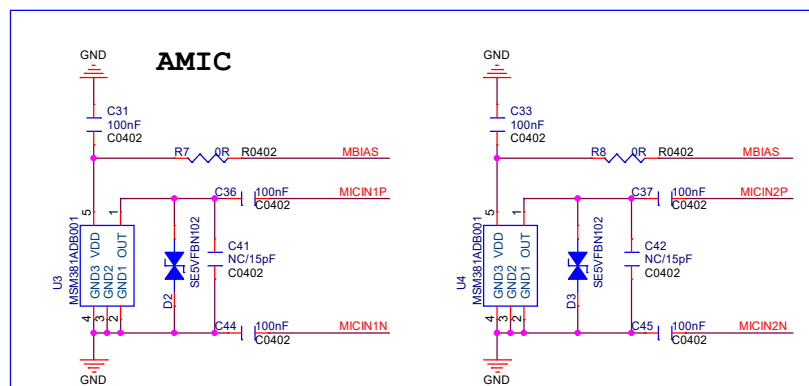
XTAL 40M



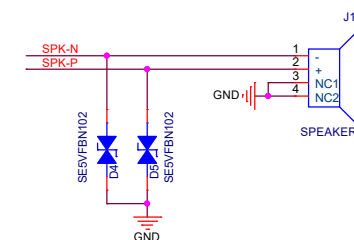
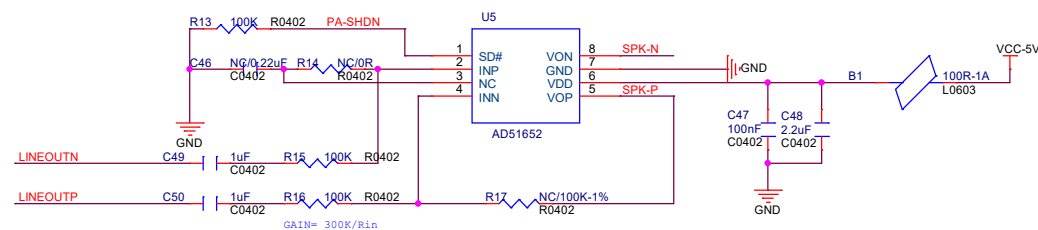
XTAL 32K



AllWinner Technology Co., Ltd			
Design Name	R128_S1/S2_REF		
Size A3	Page Name	R128-S2	
Date:	Friday, December 23, 2022	Sheet	6 of 9
Rev		RevCode	



PA



6	LOUTLP	LINEOUTP
6	LOUTLN	LINEOUTN
6	PA-SHDN	PA-SHDN
6	MBIAS	MBIAS
6	MICIN2N	MICIN2N
6	MICIN2P	MICIN2P
6	MICIN1N	MICIN1N
6	MICIN1P	MICIN1P
6	MICIN3N	MICIN3N
6	MICIN3P	MICIN3P



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Design Name

R128_S1/S2_REF

Size

Page Name

AUDIO

Rev

<RevCode>

Date:

Saturday, December 10, 2022

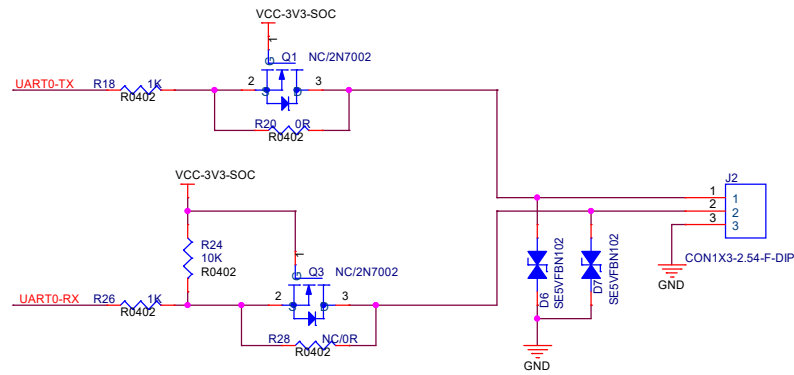
Sheet

7

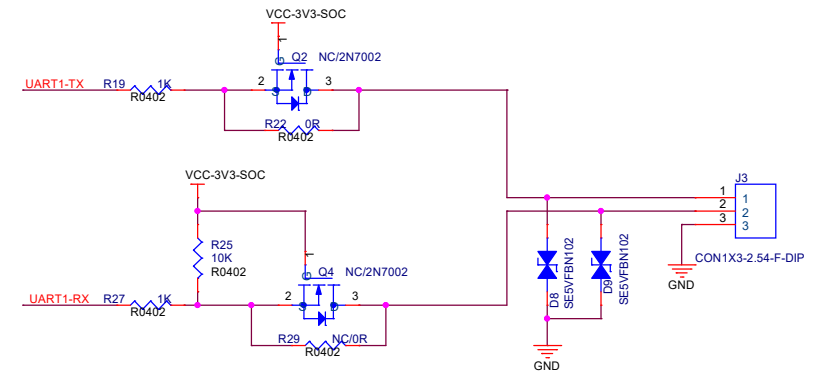
of

9

Debug UART0

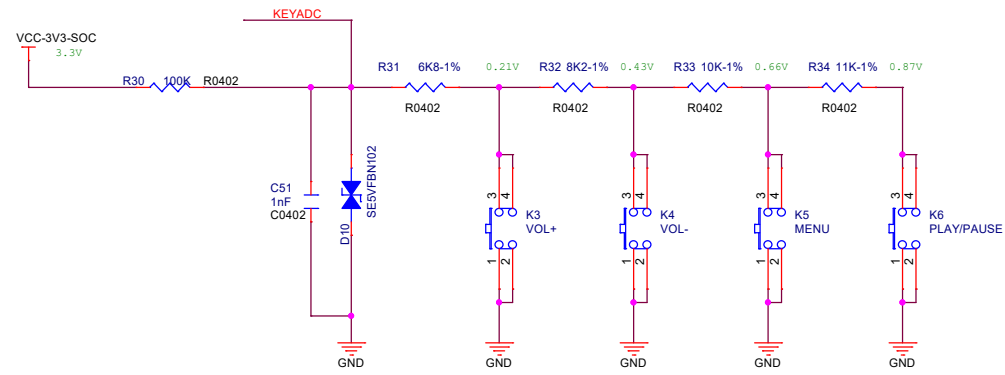


UART1



6 UART0-TX <<< UART0-TX
 6 UART0-RX <<< UART0-RX
 6 UART1-TX <<< UART1-TX
 6 UART1-RX <<< UART1-RX
 6 KEYADC <<< KEYADC

KEY



PCB MARK Signal Net

WIFI/BT

6 ANT << ANT

