

# MODULE 2

# Fundamentals of Electronic Circuits

CpE AC2

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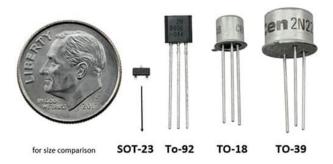
## **Objectives:**

- 1. Explain how a transistor works.
- 2. Solve Bipolar Junction Transistor circuits.

## **INTRODUCTION**

Much of the progress in the past 60 years has been because of the success of the transistor. Invented in the 1940s, it replaced vacuum tubes in televisions, radios and other electronic equipment. Its ruggedness, small size and low power consumption produced a wave of miniaturization resulting in home computers, digital cameras, cell phones and other devices. Research in transistors is ongoing; the capability of electronics will continue to improve for the foreseeable future. (Papiewski, 2017)

Transistors are like two diodes connected with each other. This yield to a three terminal component namely: emitter terminal, base terminal, and collector terminal. The emitter layer is the source of charge carriers and it is heavily doped with a moderate cross-sectional area. The collector collects the charge carriers emitted by the emitter region and hence has a moderate doping and a large cross-sectional area. The base region is in between these and it acts as a path for the movement of charge carriers. In order to reduce the recombination of electrons and holes in the base region, this region is lightly doped and is of narrow cross-sectional area. This three terminal device is called a Bipolar Junction Transistor or BJT. (Poorachandra, Sasikala, & Khan, 2005)



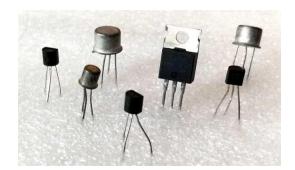


Figure 2.1 Figure 2.2

## **Bipolar Junction Transistor**

BJT can be classified into two types based on the type of semiconductor construction.

## npn-Transistor

In an npn transistor, p-type semiconductor is sandwiched between two n-type semiconductors. Therefore, the emitter region is made up of n-type semiconductor where in majority carriers is electrons, which results in electron current and minority carrier is holes, which results in hole current. The base region is made up of p-type semiconductor where in majority carrier is holes, which results in hole current and minority carrier is electrons, which results in electron current. The collector region is made up of n-type semiconductor where in majority carriers is electrons, which results in electron current and minority carrier is holes, which results in hole current. Refer to figure 2.3 for the diagram of an npn-transistor and 2.4 for its schematic symbol.

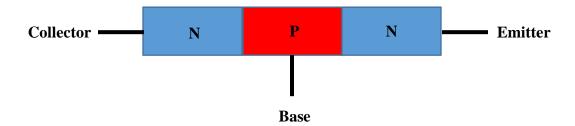


Figure 2.3

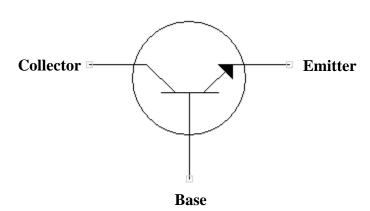


Figure 2.4

## pnp-Transistor

In a pnp transistor, n-type semiconductor is sandwiched between two p-type semiconductors. Therefore, the emitter region is made up of p-type semiconductors where in majority carrier is holes, which results in hole current and minority carrier is electrons, which results in electron current. The base region is made up of n-type semiconductor where in majority carrier is electrons, which results in electron current and minority carrier is holes, which results in hole current. The collector region is made up of p-type semiconductor where in majority carrier is holes, which results in hole current and minority carrier is electrons, which results in electron current. Refer to figure 2.5 for the diagram of an npn-transistor and 2.6 for its schematic symbol.

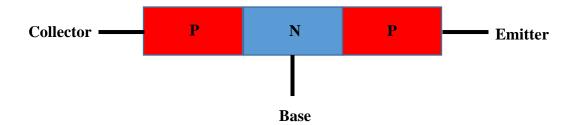
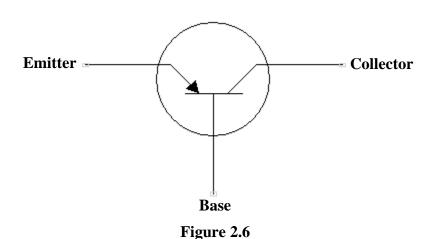


Figure 2.5



*Note: The arrow indicate the conventional current flow* 

# **NPN vs. PNP Transistors**

In terms of circuit, below is the common circuit diagram for each type of transistor.

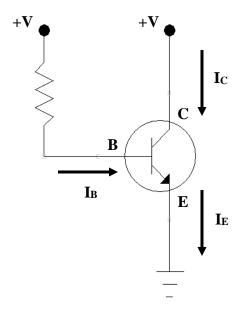
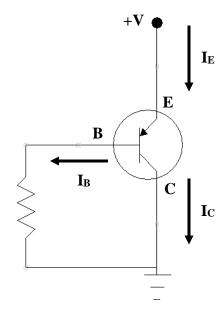


Figure 2.6 NPN Transistor



**Figure 2.6 PNP Transistor** 

For our circuit analysis we will focus more on NPN Transistor on this discussion.

Here are some of the formulas we need to take note in solving transistors.

$$I_C = \beta I_B$$
 Eq. 2.1

$$\beta = hfe$$
 Eq. 2.2

Applying KCL on Figure 2.6 and 2.7 we can get,

$$I_E = I_C + I_B$$
 Eq. 2.3

Substitute Eq. 2.1 into Eq. 2.3,

$$I_E = \beta I_B + I_B$$
 Eq. 2.4

Factor out  $I_B$ ,

$$I_E = I_B(\beta + 1)$$
 Eq. 2.5

**Example 2.1** Using an NPN Transistor with a base current of 50  $\mu$ A and hfe of 200. Determine the collector and emitter current.

Answer:  $I_C = 10 \text{ mA}$  and  $I_E = 10.05 \text{ mA}$ 

*Note:* If hfe is greater than 100 we can say that  $I_C$  and  $I_E$  are approximately equal.

Now let's consider the circuit below using an NPN Transistor,

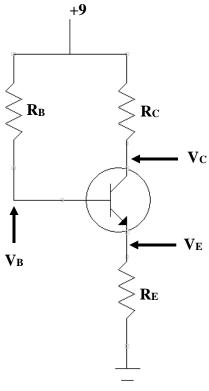


Figure 2.7

 $V_C$ ,  $V_B$ , and  $V_E$  are voltages from collector, emitter, and base respectively with respect to ground. Meaning if you use a multi-tester placing the positive probe to emitter then the negative probe to ground you will get  $V_C$  and the same goes for collector and base. Consider the following relationship of voltages.

$$V_{CE} = V_C - V_E$$
 Eq. 2.6
$$V_{BE} = V_B - V_E$$
 Eq. 2.7
$$V_{BE} = 0.6V \text{ to } 0.7V$$
 Eq. 2.8
$$V_{CB} = V_C - V_B$$
 Eq. 2.9
$$V_{CC} = Source Voltage = 9V$$
 Eq. 2.10
$$V_{EE} = 0V$$
 Eq. 2.11

Consider the circuit below.

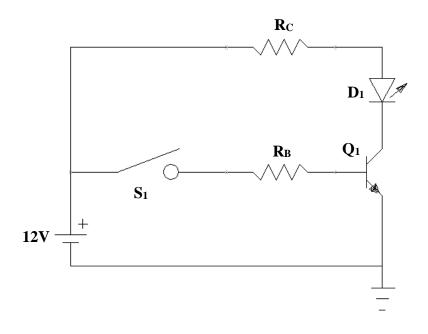


Figure 2.8

When the switch  $S_1$  is open, no current will flow on  $R_B$  so voltage on Base will be 0 and if the voltage on Base is not greater than or equal to 0.6 V or 0.7 V depending on the type of semiconductor material used no current will flow from collector to emitter therefore no current flow also on the Diode and the circuit is open. But when the switch  $S_1$  is closed current will flow on  $R_B$  and voltage on Base will also rise leading to conduct current from collector to emitter therefore current will also flow on the Diode and the circuit is now close.

**Example 2.2** Find the maximum  $I_C$  current in the circuit shown in Figure 2.8 with  $R_C = 1 \text{ k}\Omega$  and  $R_B = 100 \text{ k}\Omega$ .

Answer: 12 mA, this is the Saturation Current of the circuit.

**Example 2.3** Using the same circuit in Figure 2.8 with  $R_C = 220 \Omega$ ,  $R_B = 100 k\Omega$ , hfe = 100, and with  $D_1$  as a green LED with 2V of voltage drop across it, find  $I_B$ ,  $I_C$ ,  $I_E$ , and  $V_{CE}$ .

Answer: 0.114 mA, 11.4 mA, 11.514 mA, and 7.49 V respectively.

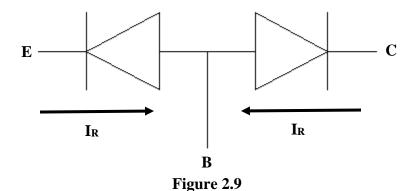
In designing an amplifier to get its maximum benefits take to consider this relationship of  $V_{CC}$  and  $V_{CE}$ .

$$V_{CE} = \frac{1}{2}V_{CC}$$
 Eq. 2.12

This is known as midpoint biased.

There are 3 important regions you have to consider when dealing with transistors.

**Cutoff Region** – during the cutoff region the transistor is off. The emitter potential is greater than the potential of the base the same goes with the potential of collector as compared to the potential of base. Having greater potential than the base will yield to reverse bias operation of the transistor.



From the condition during a cutoff region the following equation can be expressed:

$$V_B < V_E$$
 Eq. 2.13 
$$V_{BE} < 0.6 V$$
 Eq. 2.14 
$$V_{CE} = V_{CC}$$
 Eq. 2.15

$$I_C = 0A Eq. 2.16$$

**Active Region** – the transistor is in the active state. The potential at the base is greater than the potential at the emitter but the collector potential is still greater than the base potential. This yield to forward bias on the emitter side and reverse bias on the collector side.

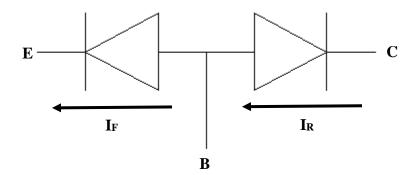


Figure 2.10

From the condition above the following equation can be expressed:

$$V_{BE} \ge 0.6 V$$
 Eq. 2.17  $0 < V_{CE} < V_{CC}$ 

**Saturation Region** – the potential at the base is still higher than the emitter potential but the potential at collector is greater than the potential at the base. This yield to both emitter and collector in forward biased mode. In active region if you increase the I<sub>B</sub> the value of I<sub>C</sub> also increases, in saturation region even if the I<sub>B</sub> increases the I<sub>C</sub> which is in its saturation value of I<sub>S</sub> it will not rise up anymore.

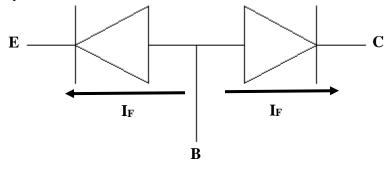


Figure 2.11

From the condition above the **following equation** can be expressed:

$$V_{BE} \ge 0.6 V$$
 Eq. 2.19

$$V_{CE} = 0 Eq. 2.20$$

These shows the importance of getting the value of  $V_{CE}$ , to determine whether the transistor operates in cutoff region, active region or saturation region. Another way to determine this is by using the value of  $I_{C}$ .

If

$$I_C = 0 Eq. 2.21$$

It is in the cutoff region.

If

$$0 < I_C < I_S$$
 Eq. 2.22

It is in the active region.

If

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E}$$
 Eq. 2.23

It is in the saturation region. If there is an LED connected to transistor you need to include the voltage drop across the LED to get the saturation current of the circuit.

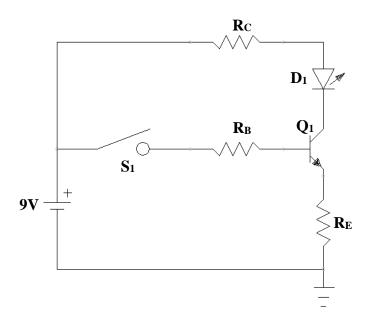
$$I_{C(sat)} = \frac{V_{CC} - V_D}{R_C + R_E}$$
 Eq. 2.23

In designing an amplifier if you want to create an almost ideal amplifier you want to create a midpoint biased transistor, this is achieved by having your  $V_{CE}$  half of your  $V_{CC}$  and when  $I_C$  is one half of the saturation current.

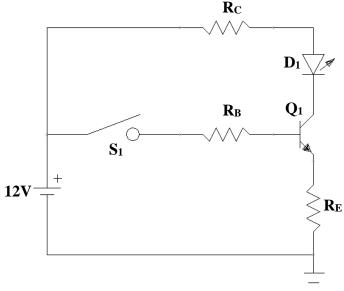
# **Activity 2**

Solve the following problem. Round off your FINAL ANSWERS ONLY to 5 decimal place.

- 1. With  $I_B=60~\mu A$  and hfe = 10, find the value of  $I_C$  and  $I_E$  of the transistor.
- 2. Find the saturation current of  $I_C$  with  $R_C$  = 1.5 k $\Omega$ ,  $R_B$  =126 k $\Omega$ ,  $R_E$  =1 k $\Omega$ , and green LED with a voltage drop across it of 2V.



3. You were tasked to design an amplifier using an NPN Transistor. With  $R_B = 100 \ k\Omega$ , hfe = 100, and green LED as your existing components. Find the value of  $R_C$  to achieve midpoint bias.



# **Objectives:**

- 1. Explain how FETs works.
- 2. Differentiate types of FETs.
- 3. Solve some voltage divider bias circuit.

On our previous topic on transistor we solve two types of circuit the first one without resistor Re is called FIXED BIAS and the other one that has resistor Re is called EMITTER BIAS. Now we will discuss another one and it is derived from basic principles in solving electrical circuits, voltage divider.

## **VOLTAGE DIVIDER BIAS**

The circuit below is the circuit diagram for a voltage divider bias.

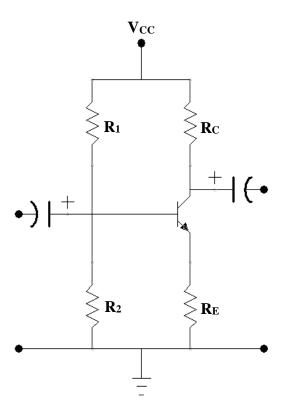


Figure 3.1

To solve this you have to solve for I<sub>B</sub> first, and to get I<sub>B</sub> use the formula below:

$$I_{B} = \frac{V_{CC} x \frac{R_{2}}{R_{1} + R_{2}} - V_{BE}}{\frac{R_{1}R_{2}}{R_{1} + R_{2}} + (\beta + 1)R_{E}}$$
 Eq. 3.1

And after finding the value of  $I_B$  the formula and process are similar to previous calculations that we did.

**Example 3.1** Calculate the values of  $I_B$ ,  $I_C$ ,  $I_1$ ,  $I_2$ ,  $V_B$ ,  $V_C$ ,  $V_E$ , and  $V_{CE}$  using the circuit on Figure 3.1 with  $R_1 = 30 \text{ k}\Omega$ ,  $R_2 = 20.9 \text{ k}\Omega$ ,  $R_C = 150 \Omega$ , and  $R_E = 150 \Omega$ . Is the transistor amplifier midpoint bias? ( $\beta = 200$ ) ( $V_{CC} = 12 \text{ V}$ )

Answer: Yes

#### FIELD EFFECT TRANSISTORS (FET)

Below is the comparison of FETs with BJTs and some of its important information.

- 1. Both BJT and FET has 3 terminals. If BJT has collector denoted C for FET it has drain denoted as D, for base in BJT there is gate denoted G for FET, and for emitter in BJT there is source denoted S for FET. In terms of application BJTs and FETS are almost the same.
- 2. For BJT it is current controlled device while in FET it is voltage controlled device.
- 3. BJT is a bipolar device meaning it depends both the electron and hole flow while on the other hand FET is unipolar meaning it depends on either electron or hole flow only. If the FET is dependent on electron flow it is called **n-channel** and if it is dependent on hole flow it is called **p-channel**.

#### 4. FET Heirarchy

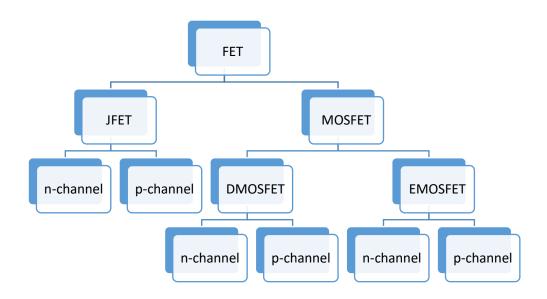


Figure 3.2

5. FET was first patented by Julius Edgar Lilienfeld in 1926 and Oskar Heil in 1934 but these patents are not the actual FETs but the concept. In 1947 William Shockley and his team tried to make an FET but failed, while diagnosing the reason for failure they discovered point-contact transistor this was the first type of transistor to be successfully demonstrated. After one decade the first JFET was made and MOSFET which is better than JFET was invented by Dawon Kahng in 1959.

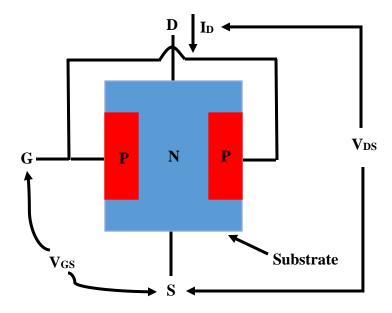
- 6. In "Field Effet" an electric field is develop by the charge present. The flow of current is controlled by utilizing the electric field induced to the gate.
- 7. FETs have high input impedance compared to BJTs.
- 8. FETs are more temperature stable.
- 9. FETs are smaller than BJTs.
- 10. BJTs are more sensitive to the applied signal compared to FETs.

#### **Junction Field Effect Transistor (JFET)**

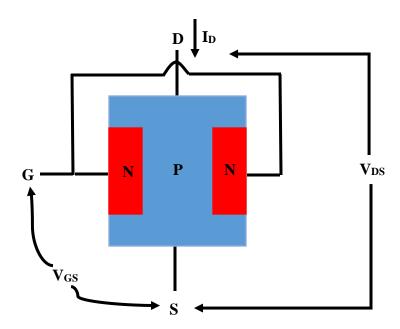
Also called Junction-gate Field Effect Transistor (JUGFET) is unlike transistor that is a current controlled device this type of FET is a voltage controlled device. It has the same function as a transistor, their difference is the construction and the principle behind their working. FETs is a unipolar device therefore it is only working either by means of electron flow or hole flow unlike a transistor that is a bipolar. (Gupta, 2019)

# **Construction and working of JFET**

It has 3 terminal like the transistor the drain (D), source (S), and gate (G). JFET has a substrate which is the base material over which FET is built. Substrate can be a p-type or n-type material, if the substrate is n-type the FET is called an n-channel if it is p-type it is called p-channel this is applicable to both JFET and MOSFET. (Kiross, 2017)



**Figure 3.3 N-Channel JFET Construction** 



**Figure 3.4 P-Channel JFET Construction** 

From the construction above, we have n-channel and p-channel JFET. The type of material of substrate dictates what channel it is. The flow of current from drain to source is controlled by the voltage supplied on the gate. Again the point where n-type material and p-type material meets is called p-n junction and from the figure above we can see that we have two p-n junction. And these junctions has depletion region and we all know that in depletion region conduction or flow of current is difficult because it does not have/too little amount of free charge carriers that is essential in conduction. The difference of voltage between gate and source is called  $V_{GS}$  and the voltage difference between drain and source is  $V_{DS}$ .

Basically when  $V_{DS}$  rises  $I_D$  rises because it is the one that pushes the current from drain to source. But there is a critical value of  $V_{DS}$  where in even if you continue to raise the value of  $V_{DS}$  the value of  $I_D$  will no longer increase, this is called **Pinch-off Voltage**.

For those wondering, this is how an n-channel JFET is connected to a voltage supply. And the voltage source is called  $V_{DD}$ . This is similar to  $V_{CC}$  of the transistor if you can remember.

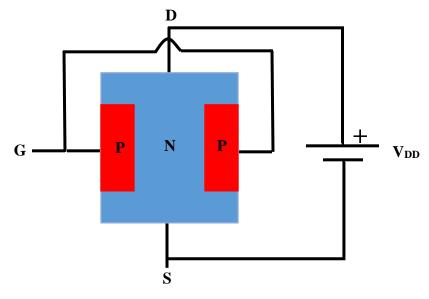


Figure 3.5

# **Schematic Symbol of JFET**

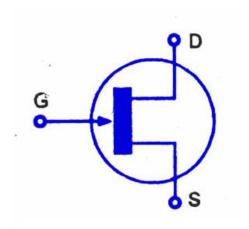


Figure 3.6 N-Channel JFET

https://electrovo.com/jfet-junction-field-effect-transistor-n-channel-p-channel/

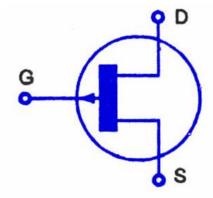


Figure 3.7 P-Channel JFET

https://electrovo.com/jfet-junction-field-effect-transistor-n-channel-p-channel/

#### Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

A MOSFET is a four-terminal device having source (S), gate (G), drain (D) and body (B) terminals. In general, the body of the MOSFET is in connection with the source terminal thus forming a three-terminal device such as a field-effect transistor. MOSFET is generally considered as a transistor and employed in both the analog and digital circuits. Its application is almost the same as the transistor. MOSFET is an active device. Active device are devices that can control the flow of electrons such as BJT, JFET, and MOSFET. Passive device are the devices that cannot control the flow of electrons such as diode, capacitor, transformer and etc. MOSFET can operate in two mode, Enhancement Mode and Depletion Mode. And each mode can be classify as n-channel or p-channel. (Agarwal, 2021)

# **Construction and working of MOSFET**

Basic MOSFET has a substrate of a p-type semiconductor as its base. And then two portion of n-type that is highly dope with n-type impurity. And from these two n-type materials brought out the source (S) and drain (D) terminal of the MOSFET. Then the entire surface of the substrate is covered with silicon dioxide that will serve as insulation. Then on this silicon dioxide a metal plate is attached and will serve as the gate (G) terminal. Take note that this gate terminal will not touch the substrate because of the insulation provided by the silicon dioxide. Please refer to the figure below for further information.

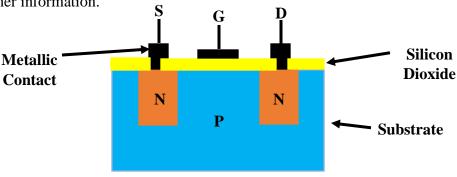


Figure 3.8

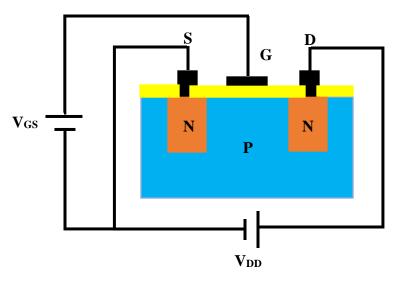


Figure 3.9

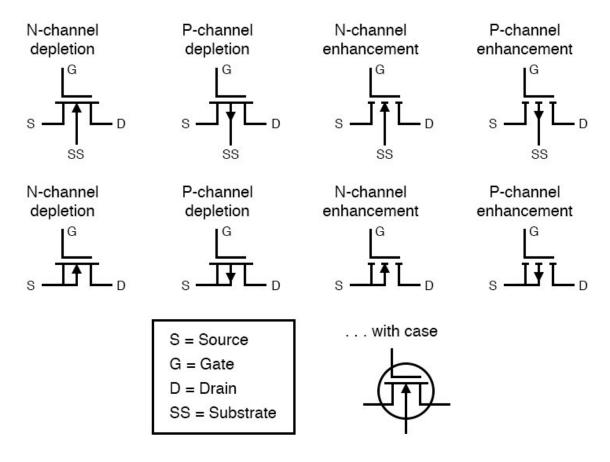
When the MOSFET is attached to a source, that source is called  $V_{DD}$  that is the voltage difference of drain voltage with respect to ground or negative terminal of the source. The difference between gate (G) and source (S) is called  $V_{GS}$  also just like in JFET. Figure 3.9 is an N-channel EMOSFET. Unlike in JFET where in the type of semiconductor used as substrate dictates what channel it is in MOSFET if the substrate is P-type then the channel will be N-channel and if the substrate is N-Type then the channel will be P-channel. It works as the opposite of JFET with regards to substrate and channel relationship.

## A MOSFET can function in two ways

**Depletion Mode** – where initially there is connection already between source and drain and when voltage is applied on gate the conductance between source and drain decreases relative to the value of  $V_{\rm GS}$ .

**Enhancement Mode** – where initially there is no connection between source and drain and when the voltage is applied on gate the conductance between source and drain increases relative to the value of  $V_{GS}$ .

# **Schematic Symbol of MOSFET**



**Figure 3.10** 

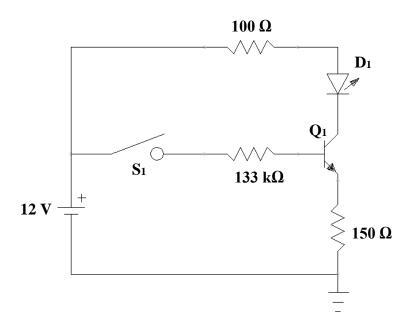
https://www.allaboutcircuits.com/textbook/reference/chpt-9/transistors-insulated-gate-field-effect-igfet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-field-effet-or-mosfet/super-fi

Substrate (SS) again are usually connected to source as stated at the start of this topic that is why you can see on the second layer of the schematic the arrow is connected to source (S) terminal on the other hand if the substrate is connected to external source the symbol will be the 1<sup>st</sup> layer of the schematic symbol. The circle correspond to its enclosure, but usually in a schematic diagram you will not see MOSFET, JFET, and BJT with circle.

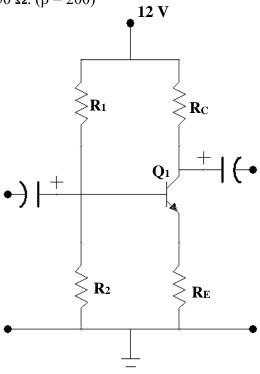
# **Activity 3**

Solve the following problems. Round off your FINAL ANSER ONLY to 5 decimal place.

1. Find the value of  $V_{CE}$  with hfe = 60, and LED voltage drop of 2V.



2. Calculate for  $V_{CE}$ ,  $I_1$ , and  $I_2$  of the circuit below. With  $R1=30~k\Omega$ ,  $R2=25~k\Omega$ ,  $RC=150~\Omega$ , and  $RE=150~\Omega$ . ( $\beta=200$ )



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