The University of Nottingham
Department of Electrical and Electronic Engineering
Electronic Processing and Communications (EEEE2044 UNUK) (FYR1 22-23)

LTspice Simulation of Sequential Circuits

EEEE2044 – Digital Coursework

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Question 1:

Based on the given relationship between state and state description, Figure 1.1 is drawn as the State Diagram to detect the sequence “101”. When the initial state or last two bits are '00', the state is S_0 and the output is 0. When the most recent bit is “1”, the state is S_1 and the output is 0. When the most recent two bits are “10”, the state is S_2 and the output is 0. When the most recent three bits are “101”, the state is S_3 and the output is 1.

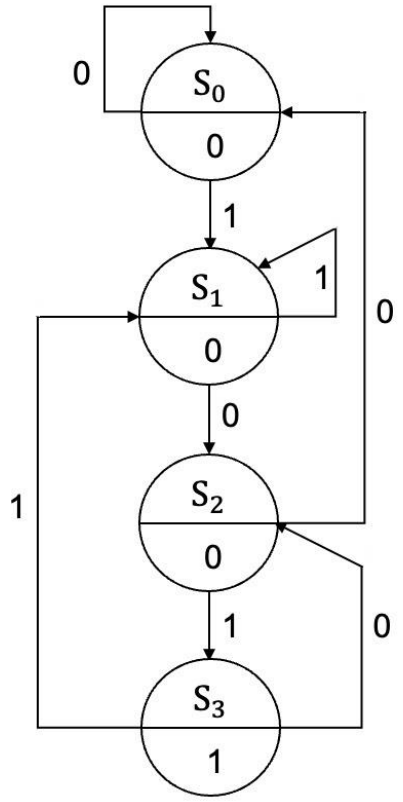

Figure 1.1: State Diagram to detect the sequence “101”

Question 2:

To construct a state table, a table representing the above transitions in Figure 1.1 is created, as shown in Table 2.1. X is the input and Z is the output.

Table 2.1: Transition table for detecting the sequence "101"

Present State (n)	Next State (n+1)		Present Output
	X=0	X=1	Z
S_0	S_0	S_1	0
S_1	S_2	S_1	0
S_3	S_2	S_1	1
S_2	S_0	S_3	0

According to the allocation requirements in the title, the state table is rewritten as Table 2.2. Four states are represented by the outputs of the two flip-flops, which are S_0 = 00; S_1 = 01; S_2 =10; S_3 =11.

For this state table, D_A is the input for Flip-flop A and D_B is the input for Flip-flop B. Q_A is the output for Flip-flop A. Q_B is the output for Flip-flop B. Next state is equal to D-inputs required and the expression for the D type Flip-flop is shown below. (D is the input of flip-flop and Q_{n+1} is the output of flip-flop at next clock period.)

$$Q_{n+1} = D \qquad \textbf{Eqn.1}$$

Table 2.2: Rewritten state table for detecting the sequence "101"

Present State (n)		Next State (n+1)				D-inputs required				Output
		X=0		X=1		X=0		X=1		
Q_n^A	Q_n^B	Q_{n+1}^A	Q_{n+1}^B	Q_{n+1}^A	Q_{n+1}^B	D_A	D_B	D_A	D_B	Z
0	0	0	0	0	1	0	0	0	1	0
0	1	1	0	0	1	1	0	0	1	0
1	1	1	0	0	1	1	0	0	1	1
1	0	0	0	1	1	0	0	1	1	0

Question 3:

To obtain three logical relationships for two Flip-Flop inputs and for the output from the circuit, three Karnaugh maps based on Table 2.2 are drawn. The red parts of three maps are minterms. Minterms can be used to find the minimized expression for these three maps.

Figure 3.1 and Figure 3.2 are used to find the inputs of Flip-Flops (D_A, D_B) based on the outputs of the Flip-Flops (Q_A, Q_B) and the input of the circuit (X). Figure 3.3 is used to find the output of the circuit (Z) based on the outputs of the Flip-Flops (Q_A, Q_B).

Q_AQ_B \ X	**0**	**1**
00	0	0
01	1	0
11	1	0
10	0	1

Figure 3.1: Karnaugh map for Flip-Flop A, Input D_A.

According to Figure 3.1, the minimized expression for D_A is shown below:

$$D_A = Q_B\bar{X} + Q_A\overline{Q_B}\,X \qquad \textbf{Eqn.2}$$

Q_AQ_B \ X	0	1
00	0	1
01	0	1
11	0	1
10	0	1

Figure 3.2: Karnaugh map for Flip-Flop B, Input D_B.

According to Figure 3.2, the minimized expression for D_B is shown below:

$$D_B = X \qquad \textbf{Eqn.3}$$

Q_A \ Q_B	0	1
0	0	0
1	0	1

Figure 3.3: Karnaugh map for Z

According to Figure 3.3, the minimized expression for Z is shown below:

$$Z = Q_A Q_B \qquad \textbf{Eqn.4}$$

Question 4:

Based on the requirements of the components selected in the title and the relational expressions obtained in Q3, Figure 4.1 shows the circuit implemented by LTspice.

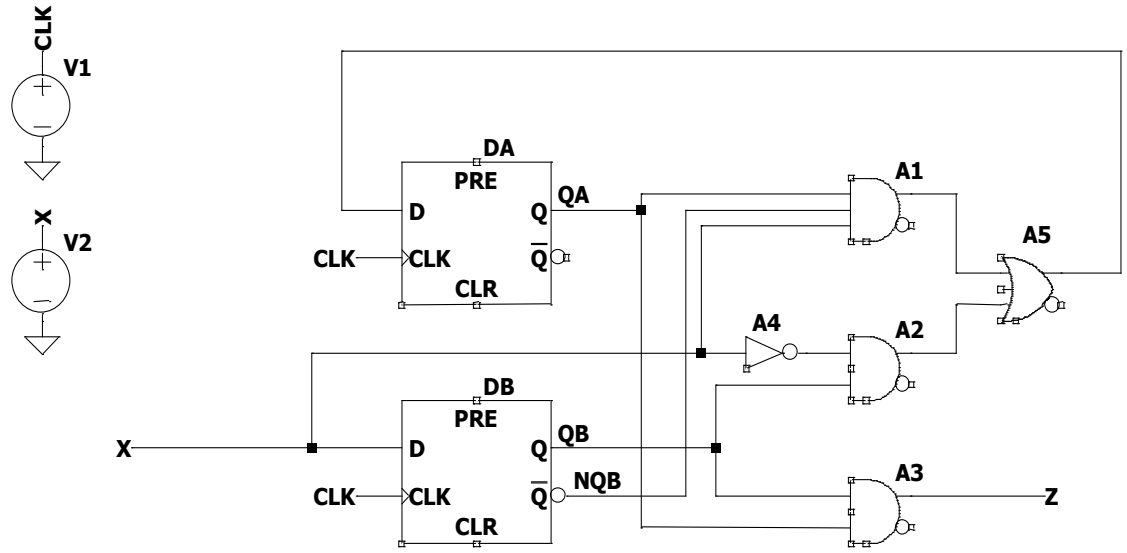

Figure 4.1: Circuit to implement detector of '101' sequence in input stream

Question 5:

Figure 5.1 shows the voltage change for each trace. The result for output Z is correct. When the input signal X sends "101" and is accepted, the output Z becomes "1". The change is also not immediate, it only occurs on the next clock cycle after the last "1" has been received. These are all consistent with the results mentioned in the title.

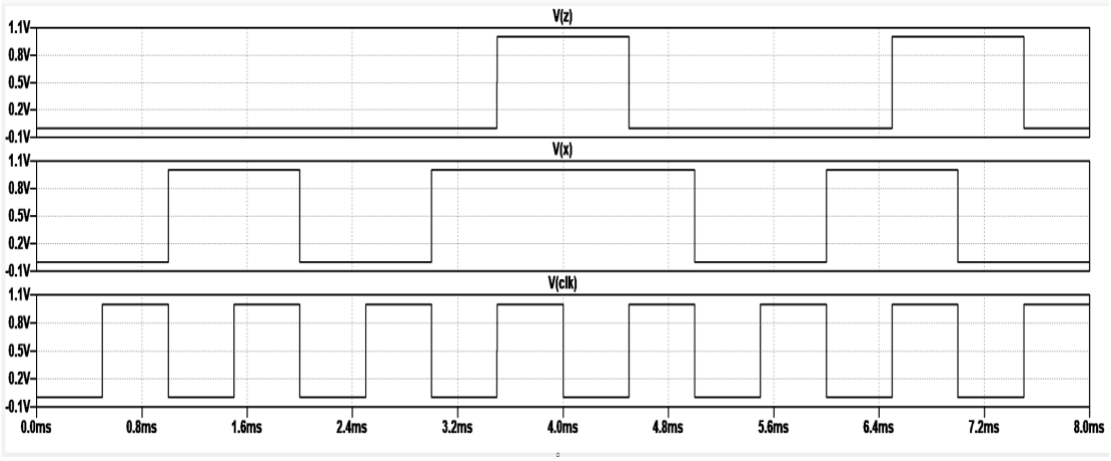

Figure 5.1: Simulation result for each pane (Clock period = 1 ms)

Question 6:

To facilitate the calculation of the delays for each path in the sequential circuit, the figure from the title is introduced and shown as Figure 6.1

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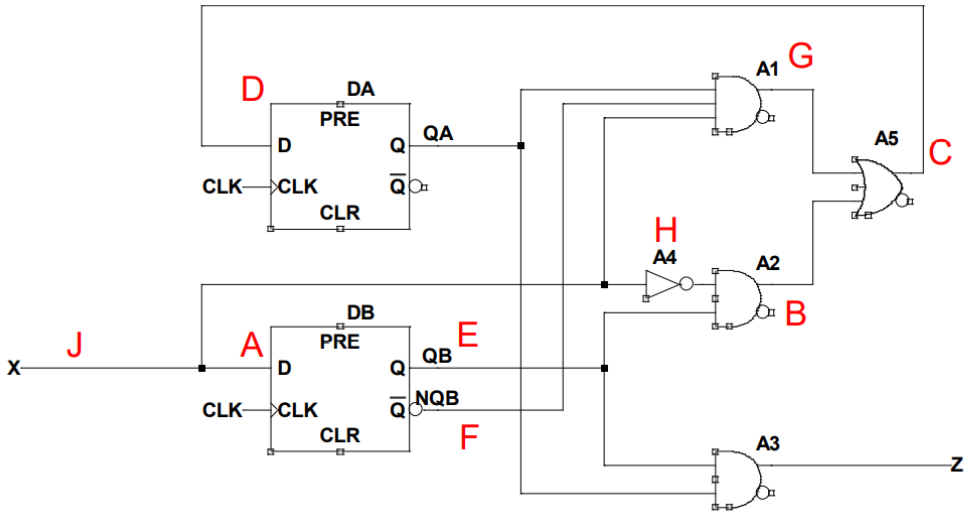

Figure 6.1: Circuit with annotated components for determining delays

For the AFGCD path, it has three different delays in one clock period. At the edge of the clock rise, the signal is output from A through the Flip-Flop (DB) to $\overline{Q}$ to F. The time used to pass this Flip-Flop is the propagation delay, denoted t_{pd}.

The signal then reaches G through the three inputs AND gate (A1). The delay through this gate is denoted as t_{A1}.

Then, the signal travels through the two inputs OR gate (A5) to C. The delay through this gate is denoted as t_{A5}.

Finally, the signal travels to the input D of the Flip-Flop (DA) and has to wait for a set-up time t_{su} of Flip-Flop. Due to the LTspice not simulating t_{su}, it can be ignored.

The sum of these delays is the expression for the delay t_{AFGCD}.

$$t_{AFGCD} = t_{pd} + t_{A1} + t_{A5} \qquad \textbf{Eqn.5}$$

For the DGCD path, it also has three different delays in one clock period like in the AFGCD path. The signal first travels through Flip-Flop (DA) from the input D, it costs

the propagation delay as t_{pd}. Then, the signal reaches G through the three inputs AND gate (A1) and then through the two-input OR gate (A5) to C then to the input D of the upper Flip-flop (DA). The delays used to pass through the two doors are recorded as t_{A1} and t_{A5}. The expression for the delay t_{DGCD} is the sum of these delays.

$$t_{DGCD} = t_{pd} + t_{A1} + t_{A5} \qquad \textbf{Eqn.6}$$

Question 7:

For the JGCD path, the signal from J first travels through the three inputs AND gate (A1) to G and then through the two-input OR gate (A5) to C. The delays used to pass through the two doors are t_{A1} and t_{A5}. The expression for the delay t_{JGCD} is the sum of these delays.

$$t_{JGCD} = t_{A1} + t_{A5} \qquad \textbf{Eqn.7}$$

Question 8:

The expression for t_{AEBCD} is mentioned by the title:

$$t_{AEBCD} = t_{pd} + t_{A2} + t_{A5} \qquad \textbf{Eqn.8}$$

According to the data given by the title and the expression from Q6, t_{AEBCD}, t_{AFGCD} and t_{DGCD} can be calculated as:

$$t_{AEBCD} = 40\ ns + 27\ ns + 22\ ns = 89ns$$

$$t_{AFGCD} = 40\ ns + 27\ ns + 22\ ns = 89\ ns$$

$$t_{DGCD} = 40\ ns + 27\ ns + 22\ ns = 89\ ns$$

These three numbers are the same, so t_{min} is:

$$t_{min} = t_{AEBCD} = t_{AFGCD} = t_{DGCD} = 89\ ns$$

Question 9:

The expression for t_{JHBCD} is mentioned by the title:

$$t_{JHBCD} = t_{A4} + t_{A2} + t_{A5} \qquad \textbf{Eqn.9}$$

According to the data given by the title and the expression from Q7, t_{JHBCD} and t_{JGCD} can be calculated as:

$$t_{JHBCD} = 22\ ns + 27\ ns + 22\ ns = 71\ ns$$

$$t_{JGCD} = 27\ ns + 22\ ns = 49\ ns$$

Question 10:

Figure 10.1 shows the voltage change for each trace after the clock period has changed to 200 ns. The analysis in Figure 10.2 shows that the output Z changes to "1" when a change of "101" in the input signal X is received at the upper edge of the clock signal. This proves that output Z is correct.

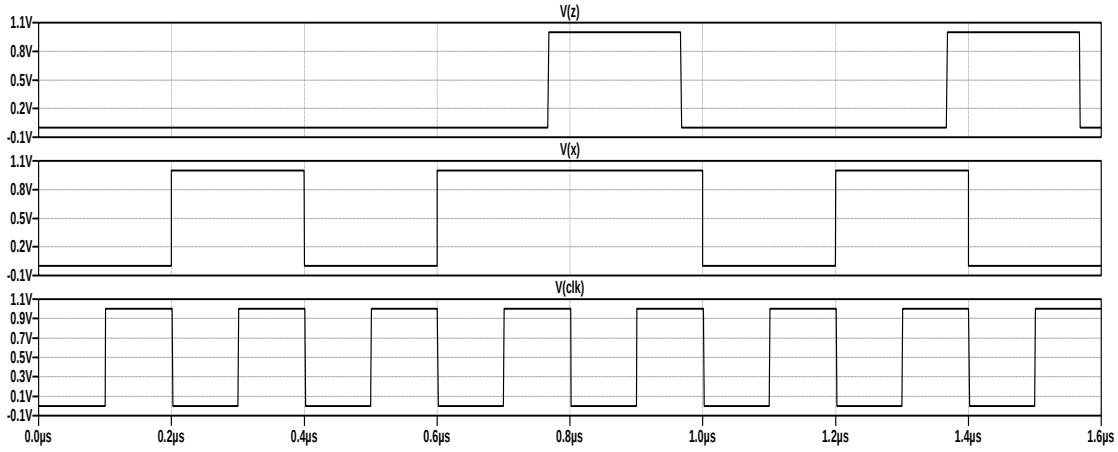

Figure 10.1: Simulation result for each pane (Clock period = 200 ns)

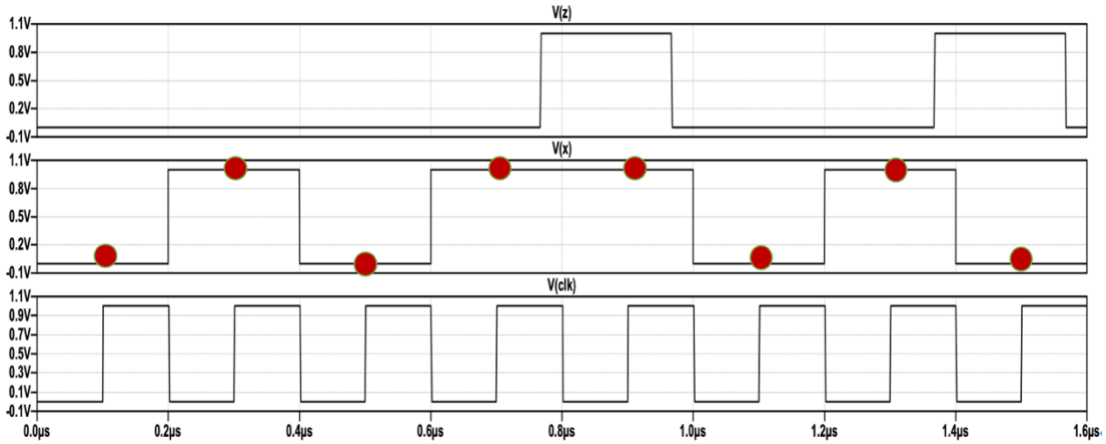

Figure 10.2: The analysis for rising edge

Another point that can be noted is that the output Z does not change immediately in the next clock cycle after the last "1" is received. This is because the input signal X to the output signal Z still has to pass through the Flip-Flop (DA) and AND gate (A3). Delays occur as the signal passes through these two components, the size of which is:

$$t_{delay} = t_{pd} + t_{A3} \qquad \textbf{Eqn.10}$$

$$t_{delay} = 40\ ns + 27\ ns = 67\ ns$$

This delay should also occur in Q5 and is not apparent in the diagram as the clock period of 1ms is much greater than 67 ns.

Question 11 :

Figure 11.1 shows the voltage change for each trace after the clock period has changed to 120 ns. As can be seen from this figure, the result for output Z is wrong despite the clock period (120 ns) being greater than t_{min} (89 ns).

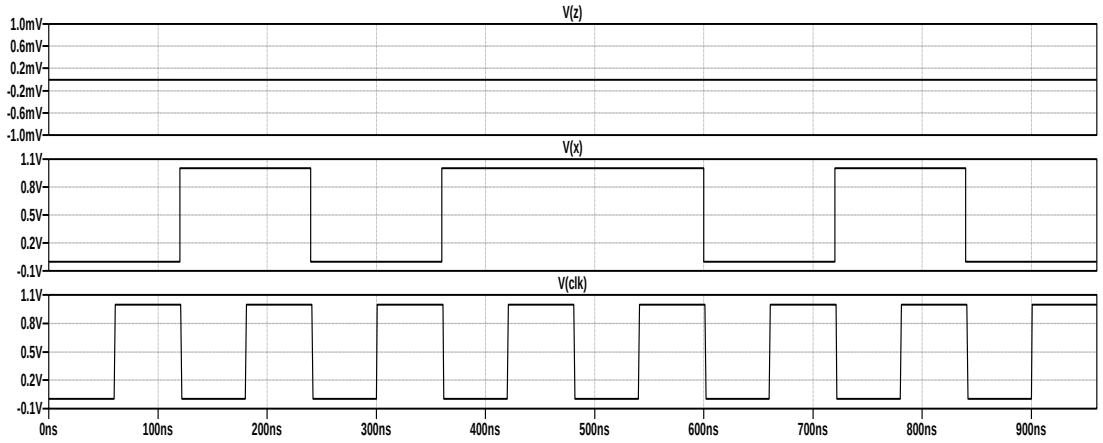

Figure 11.1: Simulation result for each pane (Clock period = 120 ns)

It is mentioned in the title that for the circuit to work well, the input signal X should change within one clock cycle, and it should be at least t_X before the next rising edge of the clock. If this requirement is not met, the circuit is working incorrectly. In this question, the t_X that meets the requirement is the maximum of t_{JHBCD} and t_{JGCD}, which is t_{JHBCD} = 71 ns. For the current circuit, this t_X is 61 ns as seen in Figure 11.2, which is less than 71 ns, so the output of the circuit is incorrect.

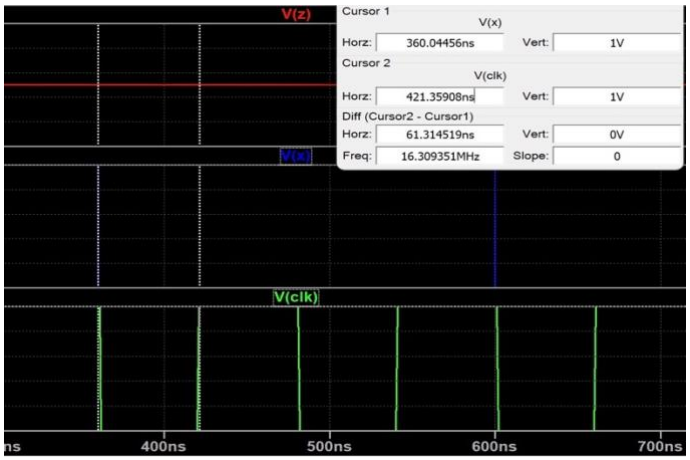

Figure 11.2: The analysis for t_X

Question 12:

Figure 12.1 shows how the voltage of each trace changes when T is added.

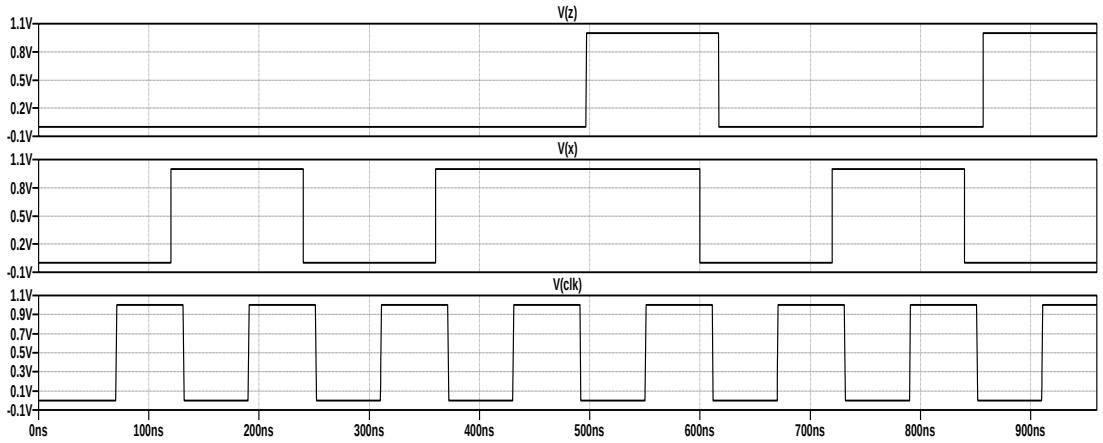

Figure 12.1: Simulation result for each pane after increasing T_{delay} (Clock period = 120 ns)

The analysis in Figure 12.2 shows that the output Z changes to "1" when the input signal X is received with a change of "101". This proves that output Z is correct.

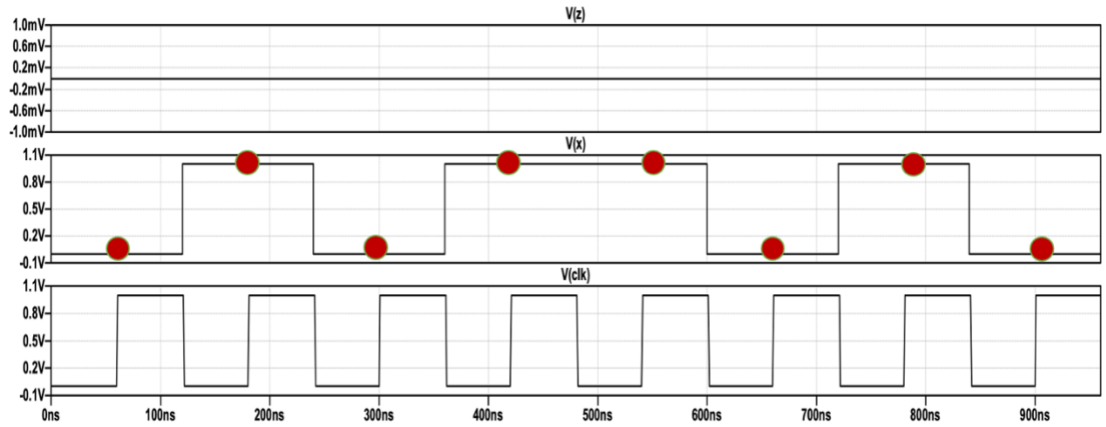

Figure 12.2: The analysis for rising edge

After T_{delay} has been increased by 10 ns, the circuit now has $t_X = t_{JHBCD} = 71$ ns, which meets the requirements mentioned in Q11, so the circuit works properly, and the output becomes correct. Figure 12.3 shows the magnitude of t_X .

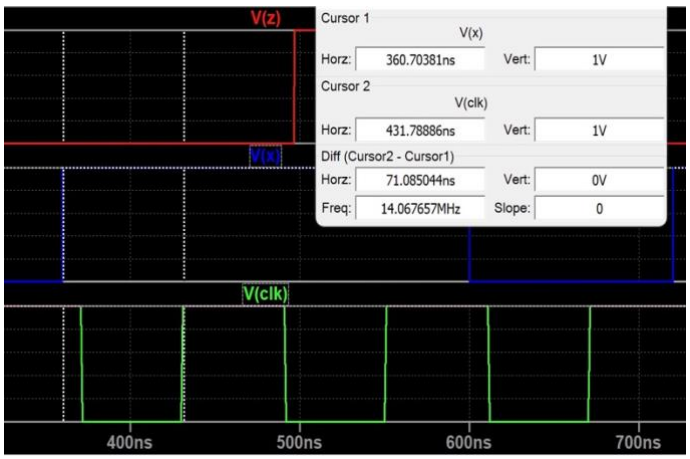

Figure 12.2: The analysis for t_X

Question 13:

For this Mealy design implementation, the sequence to be detected is '10010', which has five bits, so five states are required. Table 13.1 shows six states and their corresponding descriptions.

Table 13.1: State table

State	Description of state
S_0	Initial State/Last three bits are '000'
S_1	Last bit is '1'
S_2	Last 2 bits are '10'
S_3	Last 3 bits are '100'
S_4	Last 4 bits are '1001'

Question 14:

My sequence is ‘10010’ and the test stream is ‘111111001001110010011100 0’.

Based on the state description in Q13, Figure 14.1 shows the state diagram for detecting the sequence ‘10010’.

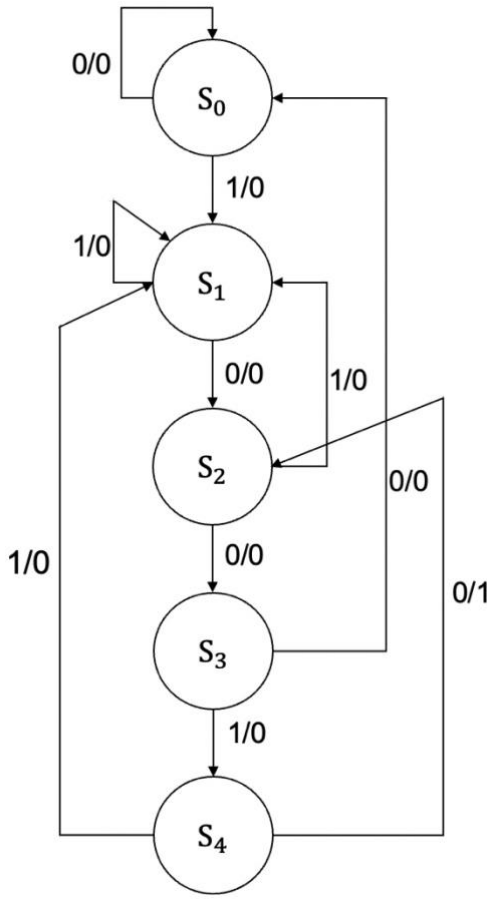

Figure 14.1: State Diagram to detect the sequence ‘10010’

Question 15:

As there are 5 states, this designed circuit needs 3 flip-flops. The outputs of these flip-flops are allocated as follows:

$S_0 = 000$; $S_1 = 001$; $S_2 = 010$; $S_3 = 011$; $S_4 = 100$

Question 16:

Table 16.1 shows the transition table created from the states in Figure 14.1.

Table 16.1: Transition table for detecting '10010'

Present State (n)	Next State (n+1)		Output Z (n)	
	X=0	X=1	X=0	X=1
S_0	S_0	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_3	S_1	0	0
S_3	S_0	S_4	0	0
S_4	S_2	S_1	1	0

Table 16.2 is created based on the output allocation relationship of flip-flops in Q15. Since D Flip-Flops are still used here, the input of D Flip-Flops is equal to its output. "Next State" is used to present the output of flip-flops.

Table 16.2: State table for detecting '10010'

Present State (n)			Next State/D Flip-Flop input						Output Z(n)	
			X=0			X=1			X=0	X=1
Q_n^A	Q_n^B	Q_n^C	Q_{n+1}^A	Q_{n+1}^B	Q_{n+1}^C	Q_{n+1}^A	Q_{n+1}^B	Q_{n+1}^C	Z	
0	0	0	0	0	0	0	0	1	0	0
0	0	1	0	1	0	0	0	1	0	0
0	1	0	0	1	1	0	0	1	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	1	1	0
1	0	1	X	X	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X

Question 17:

According to Table 16.2, four Karnaugh maps are drawn to represent the inputs of the three flip-flops (D_A, D_B, D_C) and the output Z of the whole circuit. By means of minterms in four Karnaugh maps, four resulting expressions are represented by the three flip-flop outputs (Q_A, Q_B, Q_C) and the input X of the whole circuit.

Q_AQ_B \ Q_CX	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	0	0	X	X

Figure 17.1: Karnaugh map for Flip-Flop A, Input D_A.

Q_AQ_B \ Q_CX	00	01	11	10
00	0	0	0	1
01	1	0	0	0
11	X	X	X	X
10	1	0	X	X

Figure 17.2: Karnaugh map for Flip-Flop B, Input D_B.

Q_AQ_B \ Q_CX	00	01	11	10
00	0	1	1	0
01	1	1	0	0
11	X	X	X	X
10	0	1	X	X

Figure 17.3: Karnaugh map for Flip-Flop C, Input D_C

Q_AQ_B \ Q_CX	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	X	X	X	X
10	1	0	X	X

Figure 17.4: Karnaugh map for output Z

Four expressions are shown below:

$$D_A = Q_B Q_C \, X \qquad \textbf{Eqn.11}$$

$$D_B = Q_A \bar{X} + Q_B \overline{Q_C} \bar{X} + \overline{Q_B} \, Q_C X \qquad \textbf{Eqn.12}$$

$$D_C = Q_B\overline{Q_C} + \overline{Q_B}\,X \qquad \textbf{Eqn.13}$$

$$Z = Q_A\bar{X} \qquad \textbf{Eqn.14}$$

Question 18:

PWL file content:
0m 1
0.999999m 1
1m 1
1.999999m 1
2m 1
2.999999m 1
3m 1
3.999999m 1
4m 1
4.999999m 1
5m 1
5.999999m 1
6m 0
6.999999m 0
7m 0
7.999999m 0
8m 1
8.999999m 1
9m 0
9.999999m 0
10m 0
10.999999m 0
11m 1
11.999999m 1
12m 1
12.999999m 1
13m 1
13.999999m 1
14m 0
14.999999m 0
15m 0
15.999999m 0

16m 1
16.999999m 1
17m 0
17.999999m 0
18m 0
18.999999m 0
19m 1
19.999999m 1
20m 1
20.999999m 1
21m 1
21.999999m 1
22m 0
22.999999m 0
23m 0
23.999999m 0
24m 0

Question 19:

Figure 19.1 shows the schematic of the designed circuit.

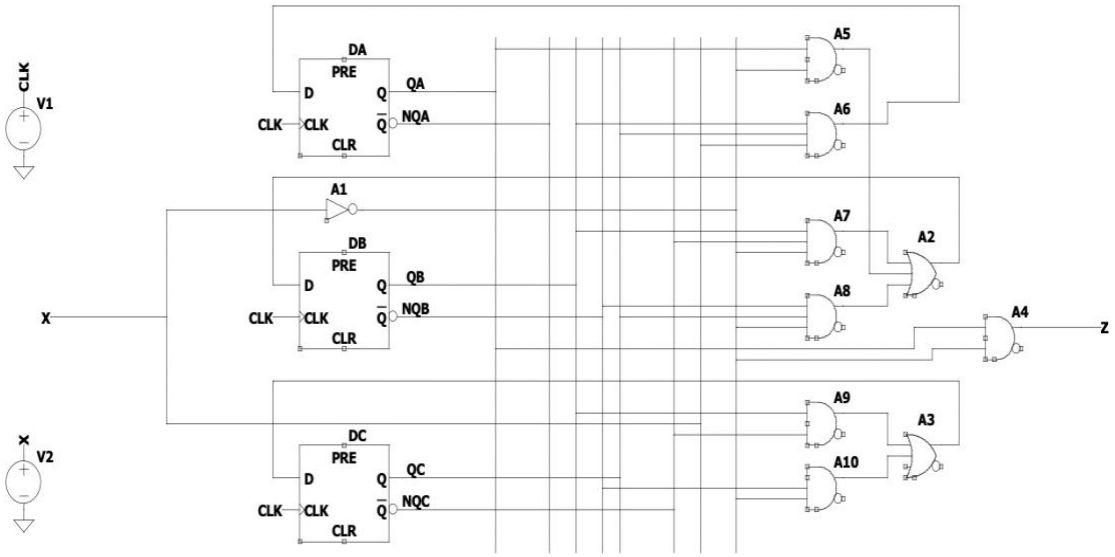

Figure 19.1: Circuit to implement detector of '10010' sequencze in input stream

Question 20:

Figure 20.1 illustrates the transient simulation of the design circuit for each trace. In this figure, it can be observed that the output Z changes to "1" after being received "10010" change in the input signal, which is consistent with the original design, and the result is correct.

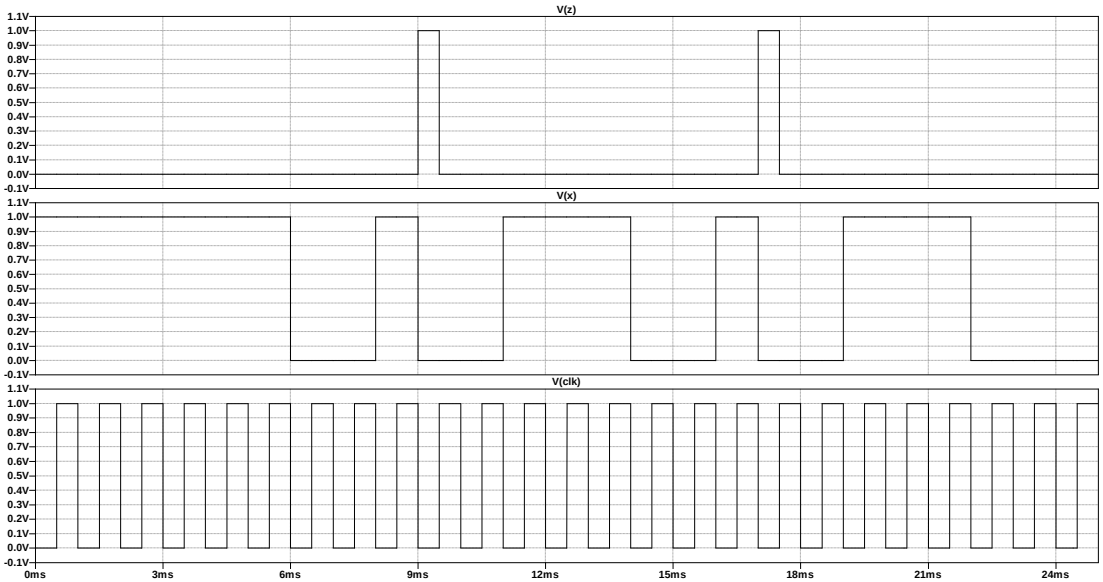

Figure 20.1: Simulation result for each pane