Arrangement of heatsinks

This design has four heatsinks, two next to the N-MOSFETs in the main converter. Because they need to be turned on and off repeatedly to operate, heatsinks are needed to prevent overheating caused by this process. Two heatsinks are next to the diodes at the output of the main converter. Due to the high current at the output, the diodes may overheat and heatsinks were also required.

Inductance of the track (Current calculation)

The inductance of the track is determined by the width and length of the track. The width of the track is determined by the thickness of the board, the temperature rise, and the current. According to the datasheet, the gate driver circuit is rated up to 3A. Since the output power in the main converter is 50 W and the output voltage is 8 V, the output current is calculated as follows:

$$I_{omax} = \frac{P_{max}}{V_o} = \frac{50\ \text{W}}{8\ \text{V}} = 6.25\ \text{A}$$

According to the ppt in last semester's lesson, with an output current of 6.25 A and a magnetisation current of less than 10% of the reflected load current, and a duty cycle estimated at 0.4, the current at the input of the converter can be estimated as follows:

$$\frac{N_2}{N_1} = \frac{V_o}{V_S} \times \frac{1}{d} = \frac{8}{30} \times \frac{1}{40\%} = 0.67$$

$$I_1 = \frac{N_2}{N_1} I_2 + I_{MAG} = \frac{N_2}{N_1} I_{omax} + 10\% I_{load} = 0.67 \times 6.25 + 0.1 \times 6.25 = 4.8125\ \text{A}$$

Table 1 shows the track widths calculated by the PCB calculator for different current cases. This width is calculated for a temperature rise of 20℃. The inductance of the track has the greatest influence on the circuit when the track is the thinnest (0.9 mm) and longest (3.4 cm). In this case, the track inductance is approximately 32.5 nH, which is almost negligible, indicating that the design track results in no effect of additional inductance on each circuit connection.

Table 1: Correspondence between current and wiring width

Current (A)	3	5	6.25
Track Width (mm)	0.90	1.81	2.47

Decoupling capacitance

As the gate driver consumes a large amount of high frequency switching current, the voltage ripple causes the gate driver to switch quickly, and the switching losses then get hot. By adding two decoupling capacitors, the voltage ripple is smoothed out to resolve this phenomenon. If the capacitors were too far away from this supply side, they would be useless, so two capacitors with values of 0.1 uF and 1 uF are placed near the input side.

Layout for easy connection and testing

The PCB has been designed in such a way that the shortest possible trace between each component is achieved. In one area, many GND connections are made, so a filled zone was used here instead of tracks. Four additional vias were added to the design to facilitate the connection of the tracks and to avoid long tracks. There is generally a combination of several small vias at high current connections. Various inputs, outputs, and test points of the circuit were placed on the periphery to facilitate testing. The names of the different components on the circuit were labeled accordingly. Some components were also labeled with positive and negative terminals. Proper clearance between components and tracks to avoid interference.

Warning explanation

Many warnings for “Silkscreen clipped by solder mask”: This is caused by the screen layer overlapping the pad, has no effect on the circuit, and can be ignored.