Part 1 – Inverter Analysis:

Task 1:

Figure 1.1 shows the circuit diagram of a CMOS inverter.

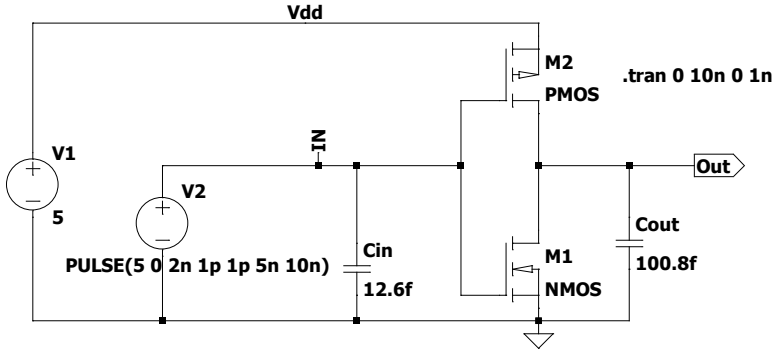

Figure 1.1: CMOS inverter circuit diagram

Task 2:

The input capacitance can be calculated by Eqn 1.1, where C_{ox} is 9×10^{-4} pF · µm^{-2}, W_n/W_p is 3.5 µm and L_n/L_p is 2 µm.

$$C_{in} = C_g + C_w \approx C_g = C_{gp} + C_{gn} = C_{ox}(W_n L_n + W_p L_p) \qquad \textbf{Eqn 1.1}$$

$$C_{in} = 9 \times 10^{-4}\ \text{pF} \cdot \mu\text{m}^{-2}(3.5\ \mu\text{m} \times 2\ \mu\text{m} + 3.5\ \mu\text{m} \times 2\ \mu\text{m}) = 12.6\ \text{fF}$$

Therefore, it can be verified that the input capacitance in the netlist is 12.6 fF.

Task 3:

Figure 1.2 shows the transient plots of "inverterpre.cir". Charging gate delays (τ_{gc}) is the time it takes for the output to rise from 0 to 0.9 V_{dd}, in this case from 0 to 4.5 V. Discharging gate delays (τ_{gd}) is the time it takes for the output to fall from V_{dd} to 0.1V_{dd}, in this case from 5 V to 0.5 V. The figure on the left shows the results of precise point measurements with cursor, and on the right is an indication of τ_{gc} and τ_{gd}. From the figure, the output starts to rise from 2 ns and reaches 4.5 V at 5.3 ns, so τ_{gc} is 3.3 ns. The output starts to fall from 7 ns and reaches 4.5 V at 7.96 ns, so τ_{gd} is 0.96 ns.

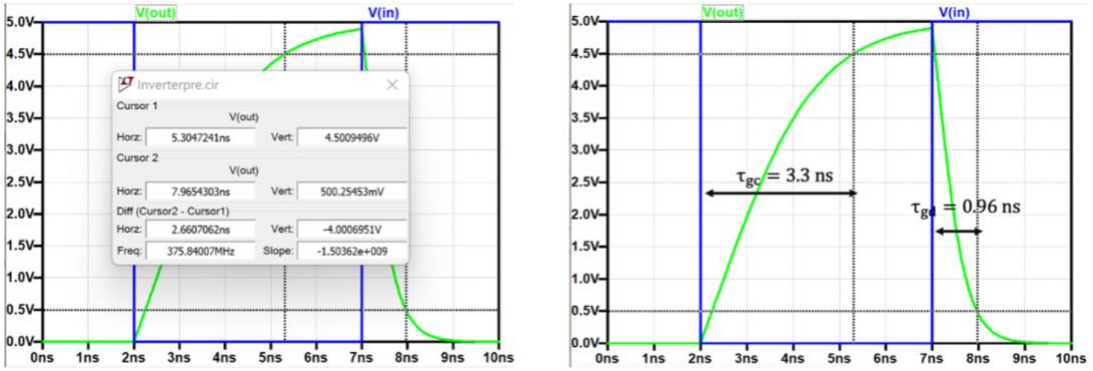

Figure 1.2: Transient plot of "inverterpre.cir"

Task 4:

Eqn 1.2 and 1.3 show the functions to calculate τ_{gc} and τ_{gd}, where V_{dd} is 5 V, $|V_{TP}| = V_{TN} =$ 0.8 V, C_L is 100.8 fF. NMOS gain factor (K_P) and NMOS gain factor (K_N) can be calculated by Eqn 1.4 and 1.5, where PMOS process factor (K_p') is 13 µA · V^{-2} and NMOS process factor

(K_N') is 44 $\mu A \cdot V^{-2}$. With these values, τ_{gc} and τ_{gd} can be calcultated as follows:

$$\tau_{gc} = \frac{2C_L}{K_P(V_{dd}-|V_{TP}|)}\left[\frac{|V_{TP}|}{V_{dd}-|V_{TP}|} + \frac{1}{2}\ln\left(\frac{19V_{dd}-20|V_{TP}|}{V_{dd}}\right)\right] \quad \textbf{Eqn 1.2}$$

$$\tau_{gd} = \frac{2C_L}{K_N(V_{dd}-V_{TN})}\left[\frac{V_{TN}}{V_{dd}-V_{TN}} + \frac{1}{2}\ln\left(\frac{19V_{dd}-20V_{TN}}{V_{dd}}\right)\right] \quad \textbf{Eqn 1.3}$$

$$K_P = K_P{}'\frac{W_p}{L_p} = 13\ \mu A \cdot V^{-2} \times \frac{3.5\ \mu m}{2\ \mu m} = 22.75\ \mu A \cdot V^{-2} \quad \textbf{Eqn 1.4}$$

$$K_N = K_N{}'\frac{W_n}{L_n} = 44\ \mu A \cdot V^{-2} \times \frac{3.5\ \mu m}{2\ \mu m} = 77\ \mu A \cdot V^{-2} \quad \textbf{Eqn 1.5}$$

$$\tau_{gc} = \frac{2\times100.8\ fF}{22.75\ \mu A\cdot V^{-2}\times(5\ V-0.8\ V)} \times \left[\frac{0.8\ V}{5\ V-0.8\ V} + \frac{1}{2}\ln\left(\frac{19\times5\ V-20\times0.8\ V}{5\ V}\right)\right] = 3.31\ ns$$

$$\tau_{gd} = \frac{2\times100.8\ fF}{77\ \mu A\cdot V^{-2}\times(5\ V-0.8\ V)} \times \left[\frac{0.8\ V}{5\ V-0.8\ V} + \frac{1}{2}\ln\left(\frac{19\times5\ V-20\times0.8\ V}{5\ V}\right)\right] = 0.98\ ns$$

Table 1 records the calculated values, spice simulated values and their errors for τ_{gc} and τ_{gd}. Comparison shows that the calculated values are almost the same as the simulated values, and the error between them is very small, -0.3% and -2.4% respectively, which indicates that the spice simulation has a very good accuracy.

Table 1: Comparison between the calculated values and spice simulated values for τ_{gc} and τ_{gd}

Time Type	Calculated Result (ns)	Simulated Result (ns)	Error (%)
τ_{gc}	3.31	3.3	-0.30
τ_{gd}	0.98	0.96	-2.04

Task 5:

Eqn 1.6 and 1.7 show the functions to calculate C_{in} and C_{out} . Since $C_{jpp/n}$ and C_{mp} are neglected, the two equations can be simplified as Eqn 1.8 and 1.9. There are 4 different areas need to find, ploy-field oxide area (A_p), metal-field oxide area (A_{mf}) and diffusion junction area (A_{jan} and A_{jap}). Figures 1.3 shows the inverter layout and the desired layout with different areas that are marked highlight. By counting the lengths and widths of the different regions, areas are calculated as Eqn 1.10, 1.11, 1.12, 1.13, 1.14 and 1.15, where A_p is split into three parts for ease of calculation (A_{p1}, A_{p2},and A_{p3}). With the area values, C_{in} and C_{out} can also be calculated as follows.

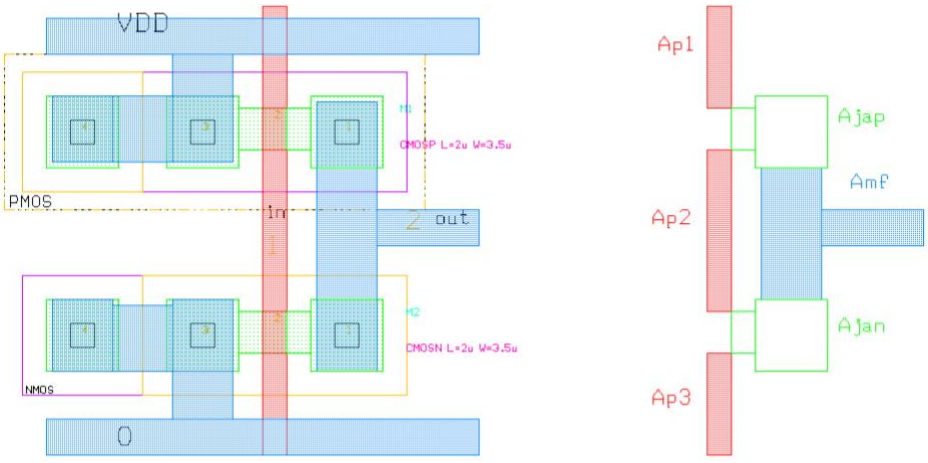

Figure 1.3: Inverter layout with highlight areas

$$C_{in} = C_{poly} + C_{gate} + C_{metal-poly} \quad \textbf{Eqn 1.6}$$

$$C_{out} = C_{metal-fox} + C_{diffarea} + C_{diffperiph} + C_{metal-poly} \quad \textbf{Eqn 1.7}$$

$$C_{in} = C_{poly} + C_{gate} = C_p A_p + C_{gp} + C_{gn} \quad \textbf{Eqn 1.8}$$

$$C_{out} = C_{metal-fox} + C_{diffarea} = C_{mf} A_{mf} + C_{jap} A_{jap} + C_{jan} A_{jan} \quad \textbf{Eqn 1.9}$$

$$A_{p1} = 2\ \mu m \times 8.5\ \mu m = 17\ \mu m^2 \quad \textbf{Eqn 1.10}$$

$$A_{p2} = 2\ \mu m \times 13.5\ \mu m = 27\ \mu m^2 \quad \textbf{Eqn 1.11}$$

$$A_{p3} = 2\ \mu m \times 8.5\ \mu m = 17\ \mu m^2 \quad \textbf{Eqn 1.12}$$

$$A_{mf} = 5\ \mu m \times 11\ \mu m + 3\ \mu m \times 8.5\ \mu m = 80.5\ \mu m^2 \quad \textbf{Eqn 1.13}$$

$$A_{jap} = 6\ \mu m \times 6\ \mu m + 2\ \mu m \times 3.5\ \mu m = 43\ \mu m^2 \quad \textbf{Eqn 1.14}$$

$$A_{jan} = 6\ \mu m \times 6\ \mu m + 2\ \mu m \times 3.5\ \mu m = 43\ \mu m^2 \quad \textbf{Eqn 1.15}$$

$$C_{in} = C_p A_p + C_{gp} + C_{gn} = C_p(A_{p1} + A_{p2} + A_{p3}) + C_{gp} + C_{gn}$$

$$C_{in} = 0.6 \times 10^{-4}\ \text{pF} \cdot \mu m^{-2} \times (17\ \mu m^2 + 27\ \mu m^2 + 17\ \mu m^2) + 12.6\ \text{fF} = 16.26\ \text{fF}$$

$$C_{out} = 0.3 \times 10^{-4}\ \text{pF} \cdot \mu m^{-2} \times 80.5\ \mu m^2 + 2 \times 10^{-4}\ \text{pF} \cdot \mu m^{-2} \times (43\ \mu m^2 + 43\ \mu m^2)$$

$$C_{out} = 19.615\ \text{fF}$$

Therefore, C_{in} is 16.26 fF and C_{out} is 19.615 fF. These two values are consistent with those calculated by the software.

Task 6:

Figure 1.4 shows the transient plots of unloaded "inverter.cir". The left figure shows the results of precise point measurements with cursor, and on the right is an indication of τ_{gc} and τ_{gd}. From the figure, the output starts to rise from 2 ns and reaches 4.5 V at 2.64 ns, so τ_{gc} is 0.64 ns. The output starts to fall from 7 ns and reaches 4.5 V at 7.19 ns, so τ_{gd} is 0.19 ns.

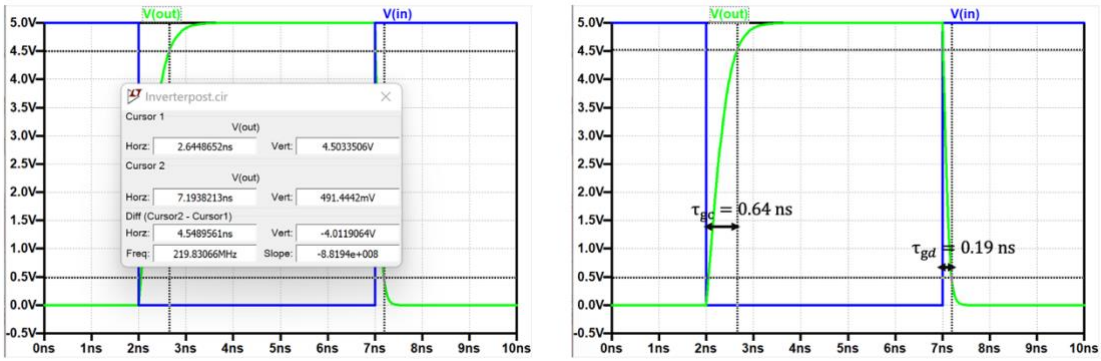

Figure 1.4: Transient plot of unloaded "inverter.cir"

Task 7:

Figure 1.5 shows the transient plots of loaded "inverter.cir". The left figure shows the results of precise point measurements with cursor, and on the right is an indication of τ_{gc} and τ_{gd}. From the figure, the output starts to rise from 2 ns and reaches 4.5 V at 6.91 ns, so τ_{gc} is 4.91 ns. The output starts to fall from 12 ns and reaches 4.5 V at 13.45 ns, so τ_{gd} is 1.45 ns.

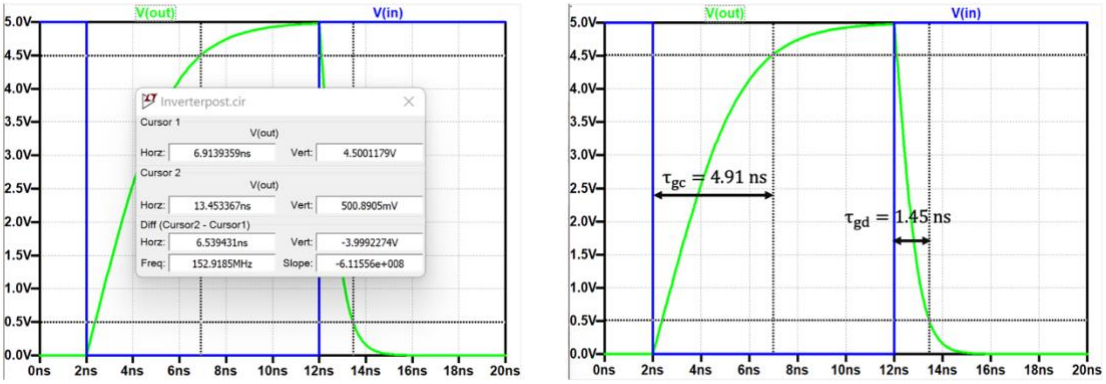

Figure 1.5: Transient plot of loaded "inverter.cir"

Task 8:

Here Eqn 1.2 and 1.3 are still used to calculate τ_{gc} and τ_{gd} in loaded and unloaded cases, with the difference that C_L is 19.6 fF in the loaded case and 150 fF in the unloaded case, the specific calculations are as follows:

$$\tau_{gc\_unloaded} = \frac{2\times 19.6\text{ fF}}{22.75\ \mu\text{A}\cdot\text{V}^{-2}\times(5\text{ V}-0.8\text{ V})} \times \left[\frac{0.8\text{ V}}{5\text{ V}-0.8\text{ V}} + \frac{1}{2}\ln\left(\frac{19\times 5\text{ V}-20\times 0.8\text{ V}}{5\text{ V}}\right)\right] = 0.64\text{ ns}$$

$$\tau_{gd\_unloaded} = \frac{2\times 19.6\text{ fF}}{77\ \mu\text{A}\cdot\text{V}^{-2}\times(5\text{ V}-0.8\text{ V})} \times \left[\frac{0.8\text{ V}}{5\text{ V}-0.8\text{ V}} + \frac{1}{2}\ln\left(\frac{19\times 5\text{ V}-20\times 0.8\text{ V}}{5\text{ V}}\right)\right] = 0.19\text{ ns}$$

$$\tau_{gc\_loaded} = \frac{2\times 150\text{ fF}}{22.75\ \mu\text{A}\cdot\text{V}^{-2}\times(5\text{ V}-0.8\text{ V})} \times \left[\frac{0.8\text{ V}}{5\text{ V}-0.8\text{ V}} + \frac{1}{2}\ln\left(\frac{19\times 5\text{ V}-20\times 0.8\text{ V}}{5\text{ V}}\right)\right] = 4.93\text{ ns}$$

$$\tau_{gd\_loaded} = \frac{2\times 150\text{ fF}}{77\ \mu\text{A}\cdot\text{V}^{-2}\times(5\text{ V}-0.8\text{ V})} \times \left[\frac{0.8\text{ V}}{5\text{ V}-0.8\text{ V}} + \frac{1}{2}\ln\left(\frac{19\times 5\text{ V}-20\times 0.8\text{ V}}{5\text{ V}}\right)\right] = 1.46\text{ ns}$$

Therefore, τ_{gc} is 0.64 ns, τ_{gd} is 0.19 ns under unloaded case and τ_{gc} is 4.93 ns, τ_{gd} is 1.46 ns under loaded case.

Task 9:

Table 2 records the calculated values, spice simulated values and their errors for τ_{gc} and τ_{gd} under different loaded cases. In the unloaded case, the calculated values are in full agreement with the simulated values. In the loaded case, the calculated values are close to the simulated values with only a small error of -4.05 and -6.85%, respectively.

Table 2: Comparison between the calculated and simulated values for τ_{gc} and τ_{gd} under unloaded/loaded case

Time Type	Calculated Result (ns)	Simulated Result (ns)	Error (%)
$\tau_{gc\_unloaded}$	0.64	0.64	0
$\tau_{gd\_unloaded}$	0.19	0.19	0
τ_{gc_loaded}	4.93	4.91	-4.05
τ_{gd_loaded}	1.46	1.45	-6.85

There are several reasons why these values are not exactly agreed:

1) **For calculation:** The calculated τ_{gc} and τ_{gd} may be inaccurate since the simulated output V_{out} does not fully reach V_{dd} (5 V) and 0.

2) **For simulation:** The base MOS model used here usually ignores or simplifies many advanced effects leading to inaccurate results, which are very important in modern fine

channel transistors. Examples include short-channel effects, velocity saturation, etc. For transistors with very small dimensions, the base model may not be able to accurately predict their behaviour as quantum and other nanoscale effects become important at such dimensions.

3) **Improvement**: It can be the use of advanced models such as the BSIM model, which are capable of more accurately describing the behaviour of the transistor under real operating conditions. Multi-scale modelling techniques can also be used to consider quantum and atomic level effects.

Task 10:

Eqn 1.16 and 1.17 can be used to calculate τ_{LD} under low to high charging procedure ($\tau_{LD}{}'_{L\to H}$) and high to low charging procedure ($\tau_{LD}{}'_{H\to L}$). C_{LD} is the input capacitance of next stage and it is 130.08 fF (8× 16.26 fF). The calculation process is as follows:

$$\tau_{LD}{}'_{L\to H} = \frac{\tau_{LD}}{C_{LD}} = \frac{\frac{2C_{LD}}{K_P(V_{dd}-|V_{TP}|)}\left[\frac{|V_{TP}|}{V_{dd}-|V_{TP}|}+\frac{1}{2}\ln\left(\frac{19V_{dd}-20|V_{TP}|}{V_{dd}}\right)\right]}{C_{LD}} \qquad \textbf{Eqn 1.16}$$

$$\tau_{LD}{}'_{L\to H} = \frac{2}{K_P(V_{dd}-|V_{TP}|)}\left[\frac{|V_{TP}|}{V_{dd}-|V_{TP}|}+\frac{1}{2}\ln\left(\frac{19V_{dd}-20|V_{TP}|}{V_{dd}}\right)\right]$$

$$\tau_{LD}{}'_{L\to H} = \frac{2}{22.75\ \mu A\cdot V^{-2}\times(5\ V-0.8\ V)}\times\left[\frac{0.8\ V}{5\ V-0.8\ V}+\frac{1}{2}\ln\left(\frac{19\times5\ V-20\times0.8\ V}{5\ V}\right)\right] = 32.87\ ns/pF$$

$$\tau_{LD}{}'_{H\to L} = \frac{\tau_{LD}}{C_{LD}} = \frac{\frac{2C_{LD}}{K_N(V_{dd}-V_{TN})}\left[\frac{V_{TN}}{V_{dd}-V_{TN}}+\frac{1}{2}\ln\left(\frac{19V_{dd}-20V_{TN}}{V_{dd}}\right)\right]}{C_{LD}} \qquad \textbf{Eqn 1.17}$$

$$\tau_{LD}{}'_{H\to L} = \frac{\tau_{LD}}{C_{LD}} = \frac{2}{K_N(V_{dd}-V_{TN})}\left[\frac{V_{TN}}{V_{dd}-V_{TN}}+\frac{1}{2}\ln\left(\frac{19V_{dd}-20V_{TN}}{V_{dd}}\right)\right]$$

$$\tau_{LD}{}'_{H\to L} = \frac{2}{77\ \mu A\cdot V^{-2}\times(5\ V-0.8\ V)}\times\left[\frac{0.8\ V}{5\ V-0.8\ V}+\frac{1}{2}\ln\left(\frac{19\times5\ V-20\times0.8\ V}{5\ V}\right)\right] = 9.71\ ns/pF$$

Therefore, τ_{LD} is 32.87 ns/pF for L→H and 9.71 ns/pF for H→L.

Task 11:

Eqn 1.18 and 1.19 are used to calculate propagation delay H→L (τ_{PHL}) and propagation delay L→H (τ_{PLH}). Eqn 1.20 is a comparison of the two equations and as a result it can be found that the result of comparing τ_{PHL} and τ_{PLH} at the same size is determined by $K_p{}'$and $K_N{}'$. Since $K_p{}'$ is larger than $K_N{}'$, τ_{PLH} is larger than τ_{PHL}.

$$\tau_{PHL} = \frac{\tau_{gc}}{2} = \frac{C_L}{K_P(V_{dd}-|V_{TP}|)}\left[\frac{|V_{TP}|}{V_{dd}-|V_{TP}|}+\frac{1}{2}\ln\left(\frac{19V_{dd}-20|V_{TP}|}{V_{dd}}\right)\right] \qquad \textbf{Eqn 1.18}$$

$$\tau_{PLH} = \frac{\tau_{gd}}{2} = \frac{C_L}{K_N(V_{dd}-V_{TN})}\left[\frac{V_{TN}}{V_{dd}-V_{TN}}+\frac{1}{2}\ln\left(\frac{19V_{dd}-20V_{TN}}{V_{dd}}\right)\right] \qquad \textbf{Eqn 1.19}$$

$$\frac{\tau_{PHL}}{\tau_{PLH}} = \frac{\frac{C_L}{K_P(V_{dd}-|V_{TP}|)}\left[\frac{|V_{TP}|}{V_{dd}-|V_{TP}|}+\frac{1}{2}\ln\left(\frac{19V_{dd}-20|V_{TP}|}{V_{dd}}\right)\right]}{\frac{C_L}{K_N(V_{dd}-V_{TN})}\left[\frac{V_{TN}}{V_{dd}-V_{TN}}+\frac{1}{2}\ln\left(\frac{19V_{dd}-20V_{TN}}{V_{dd}}\right)\right]} = \frac{K_P}{K_N} = \frac{K_P{}'\frac{W_p}{L_p}}{K_N{}'\frac{W_n}{L_n}} = \frac{K_P{}'}{K_N{}'} \qquad \textbf{Eqn 1.20}$$

$$\frac{\tau_{PHL}}{\tau_{PLH}} = \frac{K_p{}'}{K_N{}'} = \frac{13\ \mu A\cdot V^{-2}}{44\ \mu A\cdot V^{-2}} = 0.295 \approx \frac{1}{3} \rightarrow\ \tau_{PLH} > \tau_{PHL}$$

Part 2 – NAND3 Design and Layout:

Task 12:

Figure 2.1 shows the circuit diagram of NAND3. For this circuit, there are three PMOS in parallel and three NMOS in series. There are three inputs (A, B and C) and their output $f = \overline{A \cdot B \cdot C}$.

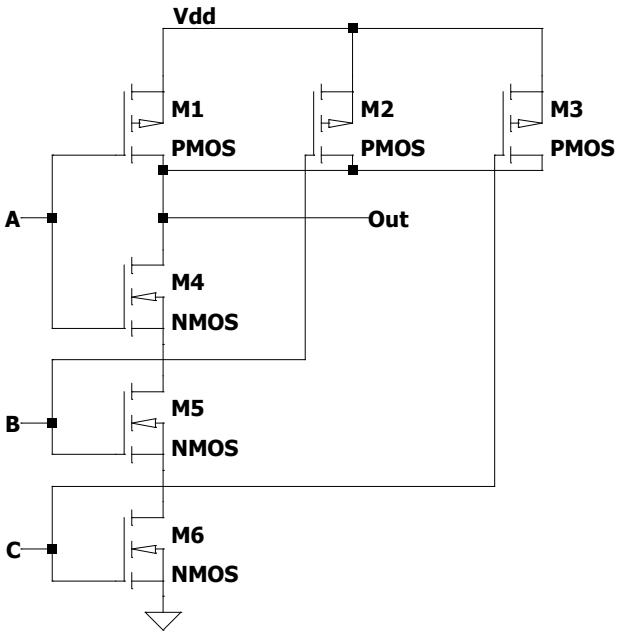

Figure 2.1: NAND3 schematic circuit diagram

Task 13:

According to the mentioned design, τ_{gc} and τ_{gd} must meet the time requirements of Eqn 2.1 and 2.2. Eqn 2.3 and 2.4 are the formulas to calculate τ_{gc} and τ_{gd} respectively. The reason why more simplified equations are used here compared to part 1 is that here $|V_{TP}|$ and V_{TN} can be designed to be 1 V, equal to 0.2 V_{dd}. These formulas are mainly based on the worst-case switching delay when driving a load of 100fF. For the NAND3 designed in Figure 2.1, there are three PMOS transistors in parallel and three NMOS transistors in series. The worst case rise time is when only one PMOS is on, which means the overall width to length ratio of three PMOS can equal to one PMOS ($(\frac{W_P}{L_P})_{equal} = \frac{W_P}{L_P}$), this shows in Eqn 2.3. The worst fall time should be both NMOS on, which means the overall width to length ratio of three NMOS can equal one PMOS divide by 3 ($(\frac{W_N}{L_N})_{equal} = \frac{W_N}{3L_N}$), this shows in Eqn 2.4. Based on the above design, $\frac{W_p}{L_p}$ and $\frac{W_n}{L_n}$ were calculated respectively:

$$1.6\ \text{ns} < \tau_{gc} < 2\ \text{ns} \qquad \textbf{Eqn 2.1}$$

$$1.6\ \text{ns} < \tau_{gd} < 2\ \text{ns} \qquad \textbf{Eqn 2.2}$$

$$\tau_{gc} = \frac{4C_L}{K_{total}V_{dd}} = \frac{4C_L}{K_P{}'(\frac{W_P}{L_P})_{equal}V_{dd}} = \frac{4C_L}{K_P{}'\frac{W_P}{L_P}V_{dd}} \qquad \textbf{Eqn 2.3}$$

$$1.6\text{ ns} < \tau_{gc} = \frac{4\times100\text{ fF}}{13\ \mu\text{A}\cdot\text{V}^{-2}\times\frac{W_p}{L_p}\times5\text{ V}} < 2\text{ ns}$$

$$3.08 < \frac{W_p}{L_p} < 3.85 \rightarrow \frac{W_p}{L_p} = 3.5$$

$$\tau_{gd} = \frac{4C_L}{K_{total}V_{dd}} = \frac{4C_L}{K_N{}'(\frac{W_n}{L_n})_{equal}V_{dd}} = \frac{4C_L}{K_N{}'\frac{W_n}{3L_n}V_{dd}} \qquad \textbf{Eqn 2.4}$$

$$1.6\text{ ns} < \tau_{gd} = \frac{4\times100\text{ fF}}{44\ \mu\text{A}\cdot\text{V}^{-2}\times\frac{W_n}{3L_n}\times5\text{ V}} < 2\text{ ns } 7$$

$$0.91 < \frac{W_n}{3L_n} < 1.14 \rightarrow 2.73 < \frac{W_n}{L_n} < 3.41 \rightarrow \frac{W_n}{L_n} = 3$$

Depending on the range obtained, $\frac{W_p}{L_p}$ is set as 3.5 and $\frac{W_n}{L_n}$ is set as 3. According to the title setting L is 2µm, so W_p is 7 µm and W_n is 6 µm.

Task 14:

Based on the design above, Figure 2.2 shows the layout of the NAND3.

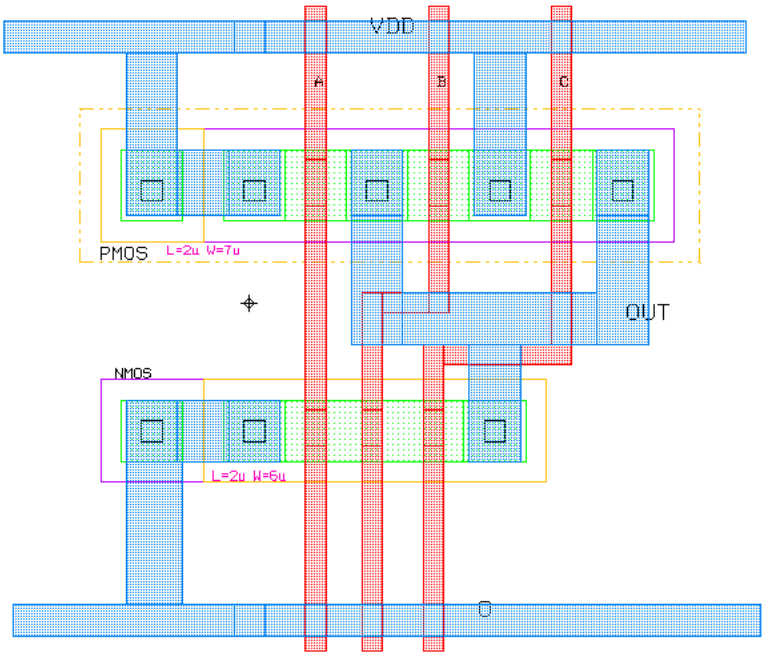

Figure 2.2: NAND3 layout

Eqn 2.5 is used to calculate the output capacitance, which only includes the calculation of the junction capacitance. The size of the junction area can be estimated from Fig. 2.2. Eqn 2.6 and 2.7 are used to calculate τ_{gc} and τ_{gd} at this stage of the design as follows:

$$C_{out} = C_{diffarea} = C_{jap}A_{jap} + C_{jan}A_{jan} \qquad \textbf{Eqn 2.5}$$

$$C_{out} = 2 \times 10^{-4}\ \text{pF} \cdot \mu\text{m}^{-2} \times (7\ \mu\text{m} \times 8\ \mu\text{m} + 7\ \mu\text{m} \times 10\ \mu\text{m}) + 2 \times 10^{-4}\ \text{pF} \cdot \mu\text{m}^{-2} \times (6\ \mu\text{m} \times 6\ \mu\text{m} + 2\ \mu\text{m} \times 6\ \mu\text{m}) = 34.8\ \text{fF}$$

$$\tau_{gc} = \frac{4C_L{}'}{K_{total}V_{dd}} = \frac{4(C_L+C_{out})}{K_P{}'(\frac{W_P}{L_P})_{equal}V_{dd}} = \frac{4\times(100\ \text{fF}+34.8\text{fF})}{13\ \mu\text{A}\cdot\text{V}^{-2}\times 3.5\times 5\ \text{V}} = 2.37\ \text{ns} \qquad \textbf{Eqn 2.6}$$

$$\tau_{gd} = \frac{4C_L{}'}{K_{total}V_{dd}} = \frac{4(C_L+C_{out})}{K_N{}'(\frac{W_n}{L_n})_{equal}V_{dd}} = \frac{4\times(100\ \text{fF}+34.8\text{fF})}{44\ \mu\text{A}\cdot\text{V}^{-2}\times\frac{3}{3}\times 5\ \text{V}} = 2.45\ \text{ns} \qquad \textbf{Eqn 2.7}$$

However, it can be noticed that both τ_{gc} and τ_{gd} exceed 2 ns, which does not meet the requirements. From the above calculations, the area of the diffusion part is too large, resulting in the calculated C_{out} being too large and the τ_{gc} /τ_{gd} not meeting the criteria, so the area of the diffusion part was reduced in the modified design. The modified layout is shown in Figure 2.3, which has $\frac{W_p}{L_p}$ of 3.75 and $\frac{W_n}{L_n}$ of 3.25. W_p is 7.5 and W_n is 6.5.

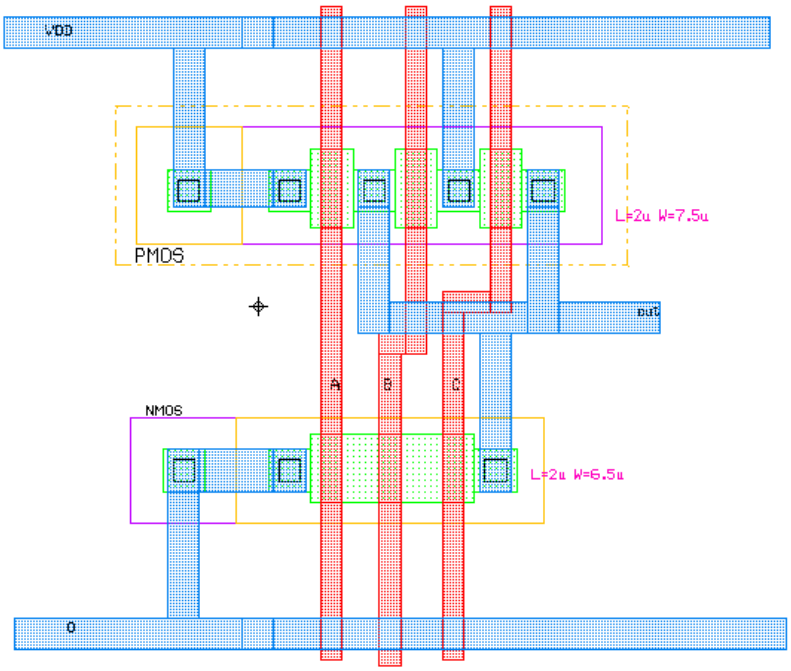

Figure 2.3: Modified NAND3 layout

Modified output capacitance, τ_{gc} and τ_{gd} are calculated as follows:

$$C_{out\_modified} = 2 \times 10^{-4}\ \text{pF} \cdot \mu\text{m}^{-2} \times (4\ \mu\text{m} \times 4\ \mu\text{m} \times 2 + 1\ \mu\text{m} \times 7.5\ \mu\text{m} \times 3) + 2 \times 10^{-4}\ \text{pF} \cdot \mu\text{m}^{-2} \times (4\ \mu\text{m} \times 4\ \mu\text{m} + 6.5\ \mu\text{m} \times 1\ \mu\text{m}) = 15.4\ \text{fF}$$

$$\tau_{gc} = \frac{4C_L{}'}{K_{total}V_{dd}} = \frac{4(C_L+C_{out})}{K_P{}'(\frac{W_P}{L_P})_{equal}V_{dd}} = \frac{4\times(100\ \text{fF}+15.4\ \text{fF})}{13\ \mu\text{A}\cdot\text{V}^{-2}\times 3.75\times 5\ \text{V}} = 1.89\ \text{ns} \qquad \textbf{Eqn 2.6}$$

$$\tau_{gd} = \frac{4C_L{}'}{K_{total}V_{dd}} = \frac{4(C_L+C_{out})}{K_N{}'(\frac{W_n}{L_n})_{equal}V_{dd}} = \frac{4\times(100\ \text{fF}+21.2\ \text{fF})}{44\ \mu\text{A}\cdot\text{V}^{-2}\times\frac{3.25}{3}\times 5\ \text{V}} = 1.94\ \text{ns} \qquad \textbf{Eqn 2.7}$$

In the changed design, τ_{gc} and τ_{gd} meet the requirements. They are both less than 2 ns and larger than 1.6 ns.

Part 3 - Discussion:

Task 15:

1) **Drive capability tuning:** Increase the drive strength of a NAND gate by using larger transistors. This can be achieved by increasing the width of the PMOS and NMOS transistors within the gate, thereby reducing the output resistance and allowing the gate to drive larger capacitive loads with less delay.
2) **Buffering:** A buffer or series of buffers is implemented behind the NAND gate. Buffers can be specifically designed to drive large capacitive loads, helping to maintain the speed of signal transitions by providing higher current drive capability.
3) **Rise/fall time symmetry:** Ensure that rise and fall times are symmetrical. Asymmetry in rise and fall times can result in different delays for logic '0' to '1' and '1' to '0' transitions, which can cause timing problems in digital circuits.
4) **Parasitic parameter reduction:** Minimise parasitic parameters such as parasitic capacitance and resistance, which increase the total load that the gate must drive.
5) **Optimised layout:** Optimise the layout of NAND gates to reduce parasitic capacitance, especially between the gate and the load. Keep interconnects as short as possible and use wider traces to reduce resistance.
6) **Multi-stage design:** Use a multi-stage gate design where the first stage drives a smaller load and each subsequent stage is designed to drive progressively larger loads. This helps keep switching speeds fast without the need for excessive transistors in a single stage.
7) **Impedance matching:** The output stage of a NAND gate is designed to match the impedance of the load. This minimises signal reflection and ensures that the maximum amount of power is transferred to the load.

Task 16:

Reasons for delay, power consumption, and area importance in terms of environmental impact and commercial market:

1) Delay:

Environmental Impact: Lower delay typically requires higher computing speeds and faster switching frequencies, which can lead to increased energy consumption, thereby increasing the environmental burden of electricity production, especially in areas dependent on fossil fuels.

Commercial Impact: In areas such as data centres, cloud computing and high-frequency trading, low delay is key to improving performance and responsiveness, which directly impacts quality of service and customer satisfaction. In consumer electronics, such as smartphones and gaming devices, low delay means a better user experience and can be used as a selling point for products to compete in the market.

2) Power consumption:

Environmental Impact: Power consumption is directly related to the energy efficiency of electronic devices. Not only does high power consumption mean higher power requirements, it also leads to more heat generation, requiring additional cooling, which in turn may increase the environmental impact. As the number of electronic devices increases globally, the rise in overall energy consumption is putting pressure on the environment.

Commercial Impact: Power consumption has a significant impact on the battery life of mobile devices, and low power consumption improves the endurance of devices and is an important consideration for consumers. In servers and data centres, power consumption is directly related to cooling costs, affecting operating costs and profits.

3) Area:

Environmental Impact: Reduced area reduces the environmental burden by allowing more chips to be made on the same size silicon, improving material utilisation and reducing waste.

Commercial Impact: A smaller area allows to produce more chips, which reduces the cost per unit of product and improves productivity. For consumer electronics products such as wearables and smartphones, miniaturisation helps to improve portability and meet consumer demand.

Relationship between them in terms of design considerations:

Delay and Power Consumption: Reducing delay requires an increase in switching speed, which can lead to an increase in power consumption.

Power Consumption and Area: When reducing power consumption there may be an option to use more efficient transistors, which are typically larger in size, which increases the area of the IC. Also, to manage the heat due to increased power consumption, a larger area may be needed for better thermal solutions.

Delay and Area: Smaller area designs may limit component placement and interconnect layout, which may increase the path length for signal transmission and thus increase delay.

Task 17:

To reduce the risk of layout design, the following measures can be taken:

1. Employ design automation tools to check design rule compliance, such as DRC (Design Rule Check).
2. Perform rigorous design verification processes, including LVS (Layout versus Schematic) checks to ensure that the layout matches the schematic.
3. Use EDA (Electronic Design Automation) tools to perform front-end and back-end simulations, such as timing analysis and power analysis, to ensure that the design is feasible in both theory and practice.

Task 18:

The following are the advantages and disadvantages of FinFETs:

Advantage:

1) **Lower Power Consumption:** FinFETs provide better control over the channel in the off state, resulting in lower leakage current. This translates into lower standby power consumption, which is critical for battery-powered devices.
2) **Higher performance:** Due to the 3D structure, current flows on three sides of the fins, providing better drive strength. This means FinFETs can run at higher speeds and provide better performance compared to planar transistors.
3) **Scalability:** FinFETs permit continued device size reduction, following Moore's Law. They can operate efficiently at lower voltages, which is vital when transistors become smaller.
4) **Reduced short-channel effects:** The 3D design of FinFETs helps mitigate short-channel effects such as drain-induced barrier lowering (DIBL) and threshold voltage variation, which are common problems with small transistors.
5) **Better device matching and variability:** The fabrication process for FinFETs results in

better performance in terms of device uniformity and matching, which is important for analogue circuit design and multi-core processors.

Disadvantage:

1) **Complex manufacturing process:** The 3D structure of FinFETs makes the manufacturing process more complex and expensive, which can increase the total cost of chip production.
2) **Heat dissipation issues:** Although FinFETs are more power efficient, the 3D structure may pose challenges in heat dissipation as transistor density increases on the chip.
3) **Design complexity:** Transitioning from planar FETs to FinFETs requires changes to the design process and tools, which can be complex and resource intensive.
4) **Parasitic Capacitance:** The 3D structure may result in increased parasitic capacitance, which may affect the switching characteristics and performance of the transistor.
5) **Self-heating:** FinFET devices can experience self-heating issues due to the fin structure that may impede the flow of heat away from the channel, which can impact performance.
6) **Fin Width Quantisation:** Fin widths cannot be scaled continuously but in discrete steps, which may limit the granularity of channel width adjustment for threshold voltage control.