1. GENERAL DESCRIPTION

iCatch's V57A SoC integrates advanced image signal processing (ISP), 8Mp video recording, computer vision (CV) and deep neural network processing, USB3.2 Gen1 connectivity, and security functions in a low power signle chip design. The embedded neural processing unit (NPU) with CV processing engine can enhance the object detection accuracy and reduce the false alarm rate to save the overall system power while meeting the next generation of intelligent computation need. The V57A SoC is designed for battery-powered applications, such as smart home camera, video doorbell, outdoor camera, portable and wearable cameras. It is also very suitable for power-limited automotive applications, such as single- or multi-channel dashboard camera recorders, driver and in-cabin monitoring system, electronic mirror, and more.

The V57A SoC includes iCatch's 8th generation ISP engine that can provide high dynamic range (HDR) video processing to reveal vivid details in high contrast regions under backlight conditions and deliver excellent image quality during the night or low-light environment. The chip can also compensate fisheye lens distortion in high degree and stabilize the image electronically. It supports both H.264/AVC and H.265/HEVC efficient video encoding up to 4K resolution in 30 frames per second. The flexible architecture can encode multiple bit-streams based on the bandwidth allocation for storage and for streaming.

A group of CV engines which comprise of an optical flow processing (OPF) accelerator, matrix arithmetic engine (MAE) with DSP functions and high-performance NPU engine, can manipulate the image and video data in real-time to support edge computing and intelligent processing, such as pedestrian detection, vehicle detection, distance extraction, behavior recognition, gesture recognition, or even action recognition, and much more. The embedded USB3.2 Gen1 device interface and support ultra high-speed and high-resolution video data transfer.

The V57A SoC also adds a series of security features, including security boot, hardware programmable security level for peripheral interfaces, data encryption and protection with a complete set of cypher coding engines, true random number generations (TRNG), and one-time programmable (OTP) memory. The user's data can be protected safely through the combination of these security functions.

The chip's software development kit can support not only the development of customer's solutions on the chip, but also a complete set of tools to port the customer's neural networks on to the V57A SoC.

2. FEATURES

2.1. Image Sensor Interface

- SubLVDS with 4/8/10-lanes or HiSPI and MIPI-CSI2 serial interfaces with 2/4 lanes
- Up to four sensor inputs

2.2. Advanced Image Signal Processing (ISP)

- Motion compensated temporal noise filtering for video
- Real-time multi-frame HDR video
- Advanced high-ISO noise reduction technology
- Multi-channel lens color shading correction with noise reduction
- On-the-fly and location-based bad pixel correction
- Superior interpolation (de-mosaic) with cross-talk and color aliasing suppression
- HDR Local tone mapping
- 180-axis hue and saturation adjustment
- 4X4 Pattern RGB-IR sensor support
- Real-time performance up to 240MPixel/Sec

2.3. Image process acceleration engine

- Matrix operation engines
- Scaling up/down engine
- De-warping engine for lens distortion correction (LDC) and multi-view affine transformation
- Motion detection engine
- HW accelerated optical flow engine for DVS sensor applications
- Pre/Post processing for NPU acceleration

2.4. Processor Cores

- Dual Arm Cortex-A7 CPU with NEON, frequency up to 720MHz
- Integrated 32KB I-cache, 32KB D-cache
- Always-on Controller Sub-system for ultra-low power applications

2.5. Neural network accelerator

- High performance 1.2 TOPS NPU engine
- Supports weight/bias quantization using UINT8, INT8, INT16, Float16, BFloat16 and Post-training quantization
- MAE engine – pre/post DSP accelerator

2.6. Audio

- Built in internal CODEC with mono input and mono line output
- A bidirectional I2S/PCM Interfaces to external codec for audio recording and playback
- One digital PDM signal input (digital stereo microphone) that support Wake On Sound (WOS) function
- Digital adaptive equalizers
- Support band-pass filter and notch filter
- Support audio sampling rate scale up for audio playback
- Built-in audio DSP for audio applications, like AEC, ALC, ANR, etc.

2.7. H.264/H.265

- Support H.264 BP/MP/HP and H.265 MP up to level 5
- Support H.264 and H.265 CABAC
- Real-time performance up to 280MPixel/Sec
- Up to 8 simultaneous encoding streams
- Advanced bitrate control

2.8. JPEG

- Built-in JPEG encode engine up to 480M pixels/s
- Built-in JPEG decode engine up to 240M pixels/s
- Support Motion-JPEG up to 4K2K resolution

2.9. Security

- Support secure boot
- Support AES/DES/3DES encryption and decryption
- Support ECC-256, ECC-384
- Support SHA-224, SHA-256, SHA-384, SHA-512, SHA-512/224, SHA-512/256
- True Random Number Generators
- Support 4k-bit OTP memory

2.10. Video output Capability

- Alpha blending OSD for user interface
- Support 4 lanes MIPI-DSI for panel display
- Support 4 lanes MIPI-CSI 2 for video output
- BT.601/656/1120 digital interface
- Support UPS051/UPS052/LCM interface

2.11. DRAM

- Programmable DRAM speed up to 1 GHz
- Support DDR3 and DDR3L

2.12. Peripherals

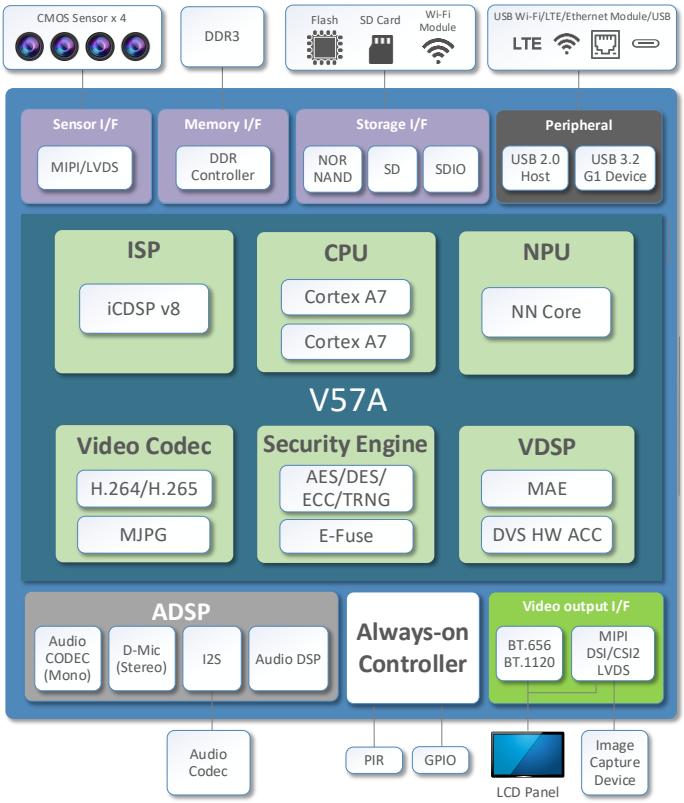
- Support NAND and SPI-XIP flash memory
- SD/SDHC/SDXC, MMC, and eMMC4.5/5.0 interfaces
- USB 3.2 Gen1 device or USB2.0 host interfaces
- Many GPIO, PWM, UART, SPI, and I2C ports
- Real-time clock and watchdog timer
- Multiple channels of 10-bits SAR ADC
- Stand-alone SDIO controller for Wi-Fi and UART for BT
- Support PIR decoder function

2.13. Package

- LFBGA-305 13x13x1.5 mm

3. BLOCK DIAGRAM

3.1. Block Diagram



4. DEVELOPMENT PLATFORM

The V57A Camera Development Platform includes evaluation board, software development kits and documentation. Users can develop their advanced imaging and video solutions with various networking capabilities.

4.1. Hardware

- V57A evaluation board
- Sensor board with OmniVision, Sony, or On Semi CMOS sensor
- IOT Wi-Fi module, Audio module with Echo Cancellation

4.2. Software Development Kit

- Libraries for ISP, 3A, NDK, RTOS, and Linux
- IOT Wi-Fi connected camera application source code of reference design
- PC tool chain of programmer, and font and string generator
- Android/iOS APP SDK for mobile phone connection

4.3. Documentation

- User's manual for SBC board, application notes, and API documents
- Data sheet, schematics and layout files