Yixiao Du

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EDUCATION

08/2020 - 08/2027 (expected) **Cornell University** — Ithaca, NY
- School of Electrical and Computer Engineering
- MS/Ph.D. in Electrical and Computer Engineering

08/2019 - 08/2020 **Cornell University** — Ithaca, NY
- School of Electrical and Computer Engineering
- M.Eng. in Electrical and Computer Engineering
- Overall GPA: 4.038/4.25
- Converted to MS/Ph.D. track in 08/2020

09/2015 - 06/2019 **University of Electronics Science and Technology of China (UESTC)** — Chengdu, China
- School of Electronic Science and Engineering (National Exemplary School of Microelectronics)
- Bachelor of Engineering in Microelectronics Science and Engineering
- Overall GPA: 3.91/4.00

RESEARCH EXPERIENCE

06/2020 - now **Computer Systems Lab, Cornell University** — Ithaca, NY
Graduate Research Assistant

- **High-Performance Sparse Linear Algebra on HBM-FPGAs (First Author)**
  Identified major challenges of accelerating sparse linear algebra on HBM-equipped FPGAs using high-level synthesis. Explored various solutions to tackle the aforementioned challenges. Built a high-performance accelerator prototype on FPGA.
- **GraphLily: Graph Linear Algebra Overlay on FPGA (Co-author)**
  Use high-level synthesis to build kernels that perform graph algorithms on graphs stored as sparse matrices. Use high-bandwidth memory to improve the performance. Fuse different kernels into one system which is capable of running multiple graph applications.

PUBLICATIONS

[1] **Y. Du**, Y. Hu, and Z. Zhang, High-Performance Sparse Linear Algebra on HBM-Equipped FPGAs Using HLS: A Case Study on SpMV, *International Symposium on Field-Programmable Gate Arrays (FPGA)*, Feb./Mar. 2022.

[2] Y. Hu, **Y. Du**, E. Ustun, and Z. Zhang, GraphLily: Accelerating Graph Linear Algebra on HBM-Equipped FPGAs, *International Conference On Computer Aided Design (ICCAD)*, Nov. 2021.

TEACHING EXPERIENCE

01/2022 – 05/2022 | **ECE/ENGRD 2300: Digital Logic and Computer Organization, Cornell University** | Ithaca, NY

Head Teaching Assistant

- **Design lab assignments and exam questions**
- **Hold office hours and lab sessions**
- **Lead tutorial sessions and exam review sessions**
- **Organize the TA team of this course**

SELECTED PROJECTS

10/2019 – 05/2020 | **FPGA acceleration of CNN-based power estimation** | Ithaca, NY

Cornell ECE M.Eng. Design Project

- Individual project.
- Created a workflow which integrates RTL hardware emulator, HLS machine learning accelerator and C++ software.
- Built a converter that converts a neural network into the format that the machine learning accelerator accepts.

11/2018 - 05/2019 | **Design of speech recognition system based on FPGA** | Chengdu, China

Undergraduate Final Design Project

- Individual project.
- Designed a voice recording and filtering system. Analyze the voice with MFCC and compare with pre-analyzed voice syllables.
- Achieved an accuracy of 90% in Chinese in simulation.

SKILLS

- Designing advanced hardware systems using high-level synthesis.
- Mastery of Digital Logic and Computer Architecture, rich experience on FPGAs.
- Building and testing digital hardware systems using Verilog.
- Building software programs using C, C++, or Python.
- Familiar with Linux command-line prompt.