CHAPTER 2

2.1

(a) $Y = \overline{A}\,\overline{B} + A\overline{B} + AB$

(b) $Y = \overline{A}\,\overline{B}\,\overline{C} + ABC$

(c) $Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + A\overline{B}C + ABC$

(d)

$$Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}B\overline{C}\,\overline{D} + \overline{A}BCD + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}C\overline{D} + ABC\overline{D}$$

(e)

$$Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}B\overline{C}D + \overline{A}BC\overline{D} + A\overline{B}\,\overline{C}D + A\overline{B}C\overline{D} + AB\overline{C}\,\overline{D} + ABCD$$

2.3

(a) $Y = A + \overline{B}$

(b) $Y = \overline{A}\,\overline{B}\,\overline{C} + ABC$

(c) $Y = \overline{A}\,\overline{C} + A\overline{B} + AC$

(d) $Y = \overline{A}\,\overline{B} + \overline{B}\,\overline{D} + AC\overline{D}$

(e)

$$Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}B\overline{C}D + \overline{A}BC\overline{D} + A\overline{B}\,\overline{C}D + A\overline{B}C\overline{D} + AB\overline{C}\,\overline{D} + ABCD$$

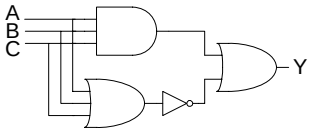
This can also be expressed as:

$$Y = \overline{(A \oplus B)}\,\overline{(C \oplus D)} + (A \oplus B)(C \oplus D)$$

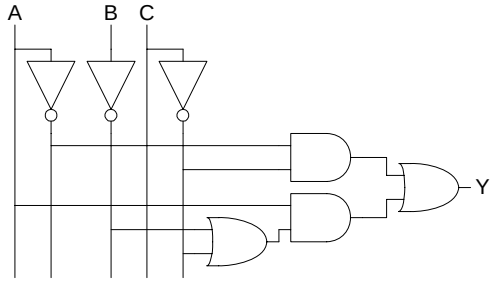
2.5

(a) Same as 2.4(a).

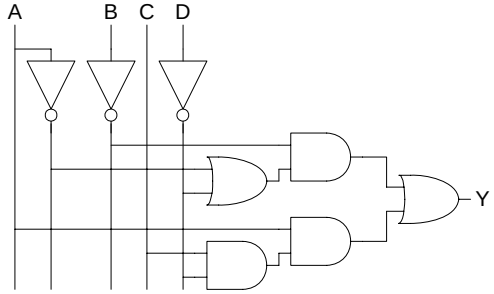
2.4 (b)



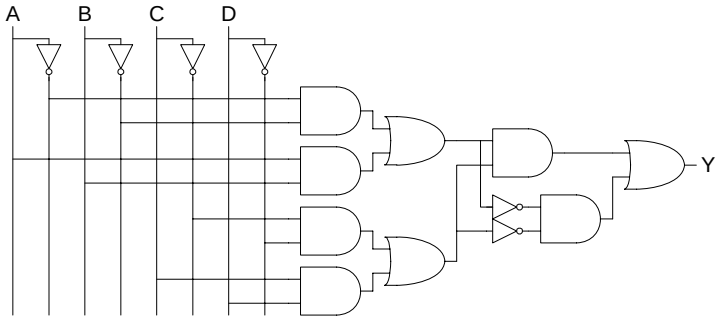
(c)



(d)



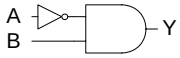
(e)



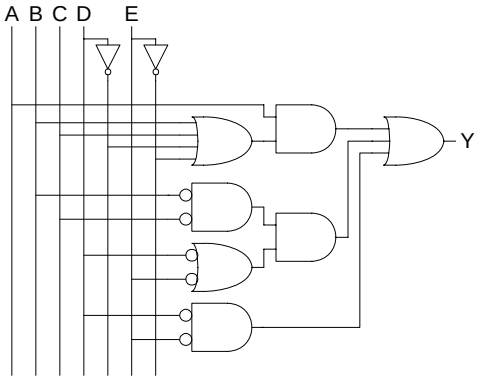
2.7
(a) $Y = AC + \overline{B}C$
(b) $Y = \overline{A}$
(c) $Y = \overline{A} + \overline{B}\,\overline{C} + \overline{B}\,\overline{D} + BD$

2.9
(a) $Y = B + \overline{A}\,\overline{C}$

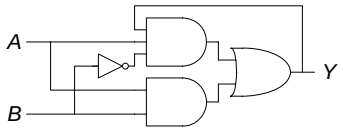
(b) $Y = \overline{A}B$



(c) $Y = AB + AC + A\overline{D} + A\overline{E} + \overline{B}\,\overline{C}\,\overline{D} + \overline{B}\,\overline{C}\,\overline{E} + \overline{D}\,\overline{E}$



2.11



$Y = A$

2.13
(a)

B	$B \bullet B$
0	0
1	1

(b)

B	C	D	$(B \bullet C) + (B \bullet D)$	$B \bullet (C + D)$
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

(c)

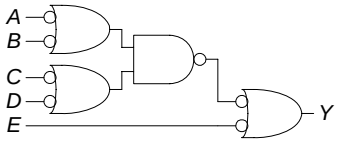
B	C	$(B \bullet C) + (B \bullet \overline{C})$
0	0	0
0	1	0
1	0	1
1	1	1

2.15

$$Y = \overline{A}D + A\overline{B}C + A\overline{C}D + ABCD$$

$$Z = A\overline{C}D + BD$$

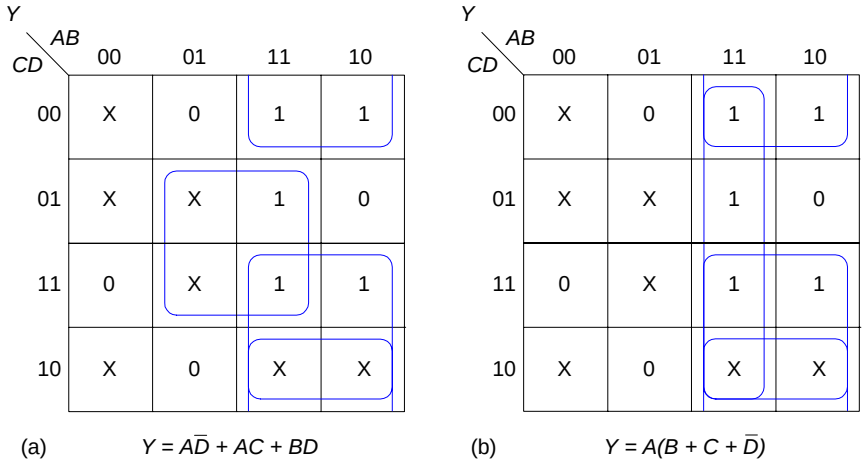
2.17



$Y = (\overline{A} + \overline{B})(\overline{C} + \overline{D}) + \overline{E}$

2.19

Two possible options are shown below:

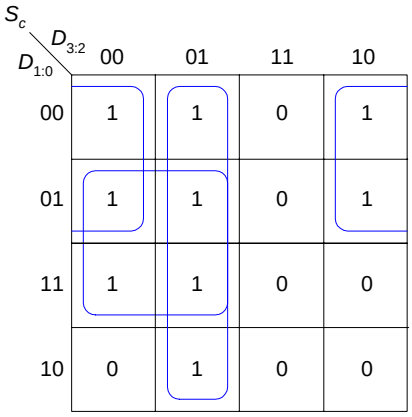


2.21

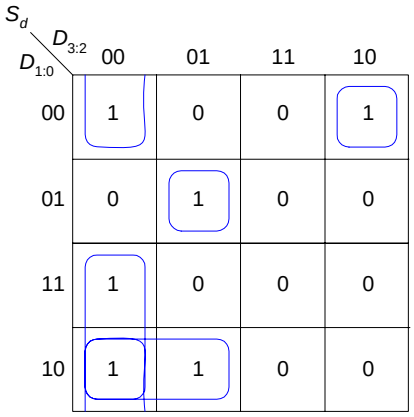
Option (a) could have a glitch when A=1, B=1, C=0, and D transitions from 1 to 0. The glitch could be removed by instead using the circuit in option (b).

Option (b) does not have a glitch. Only one path exists from any given input to the output.

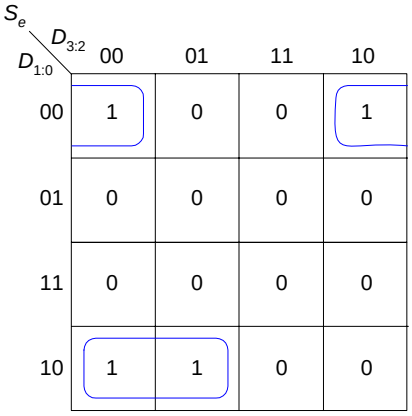
2.23 (a)



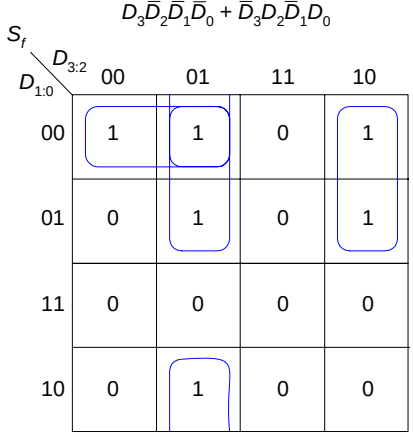
$S_c = \bar{D}_3 D_0 + \bar{D}_3 D_2 + \bar{D}_2 \bar{D}_1$



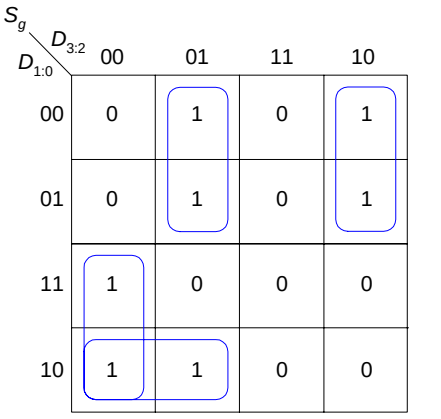
$S_d = \bar{D}_3 D_1 \bar{D}_0 + \bar{D}_3 \bar{D}_2 D_0 + \bar{D}_3 \bar{D}_2 D_1 + D_3 \bar{D}_2 \bar{D}_1 \bar{D}_0 + \bar{D}_3 D_2 \bar{D}_1 D_0$



$S_e = \bar{D}_2 \bar{D}_1 \bar{D}_0 + \bar{D}_3 D_1 \bar{D}_0$

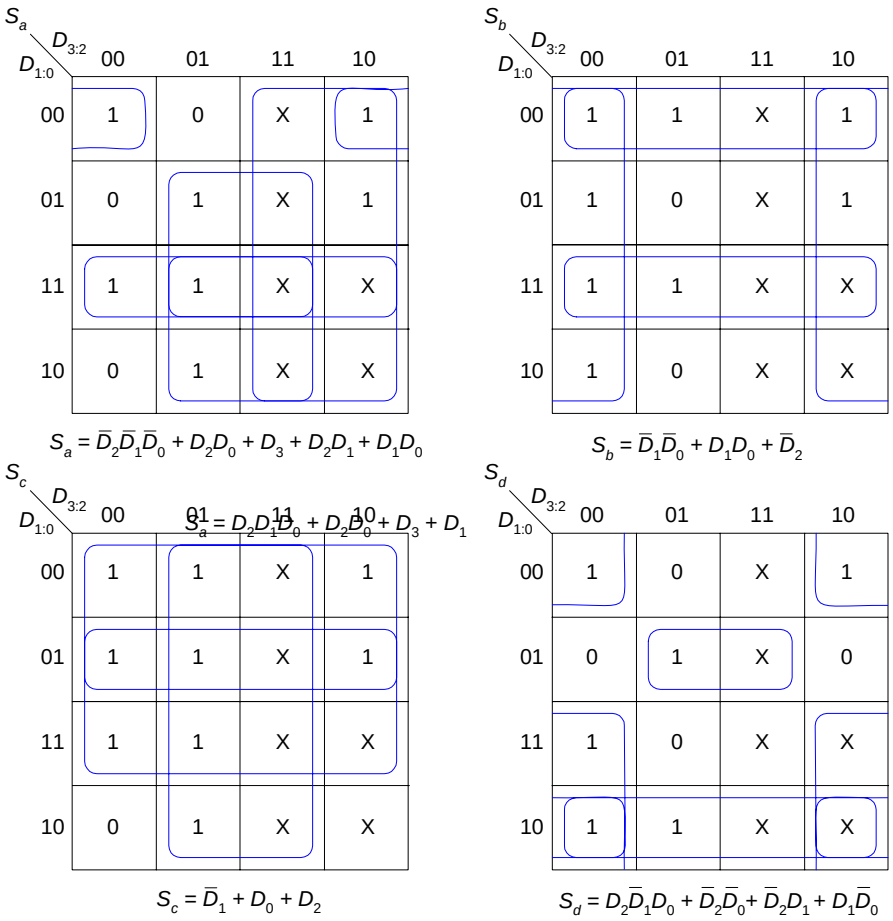


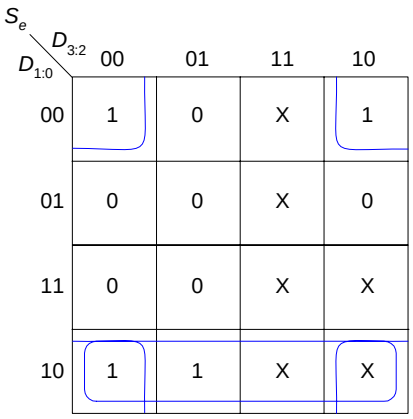
$S_f = \bar{D}_3 \bar{D}_1 \bar{D}_0 + \bar{D}_3 D_2 \bar{D}_1 + \bar{D}_3 D_2 \bar{D}_0 + D_3 \bar{D}_2 \bar{D}_1$



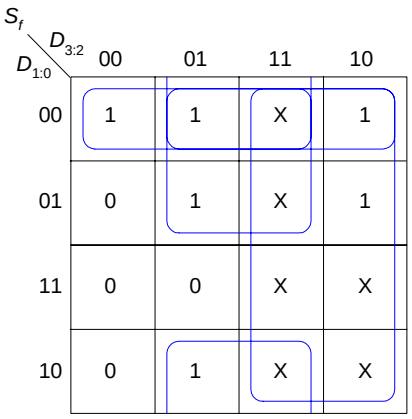
$$S_g = \bar{D}_3\bar{D}_2D_1 + \bar{D}_3D_1\bar{D}_0 + \bar{D}_3D_2\bar{D}_1 + D_3\bar{D}_2\bar{D}_1$$

(b)

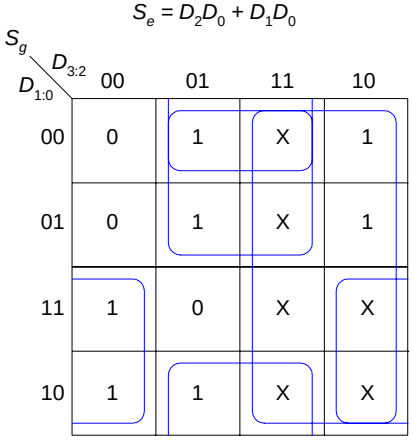

S_a
$D_{3:2}$
$D_{1:0}$
00 01 11 10
00 1 0 X 1
01 0 1 X 1
11 1 1 X X
10 0 1 X X
$S_a = \bar{D}_2\bar{D}_1\bar{D}_0 + D_2D_0 + D_3 + D_2D_1 + D_1D_0$
S_b
$D_{3:2}$
$D_{1:0}$
00 01 11 10
00 1 1 X 1
01 1 0 X 1
11 1 1 X X
10 1 0 X X
$S_b = \bar{D}_1\bar{D}_0 + D_1D_0 + \bar{D}_2$
S_c
$D_{3:2}$
$D_{1:0}$
00 01 11 10
00 1 1 X 1
01 1 1 X 1
11 1 1 X X
10 0 1 X X
$S_c = \bar{D}_1 + D_0 + D_2$
S_d
$D_{3:2}$
$D_{1:0}$
00 01 11 10
00 1 0 X 1
01 0 1 X 0
11 1 0 X X
10 1 1 X X
$S_d = D_2\bar{D}_1D_0 + \bar{D}_2\bar{D}_0 + \bar{D}_2D_1 + D_1\bar{D}_0$



$S_e = \bar{D}_2\bar{D}_0 + D_1\bar{D}_0$

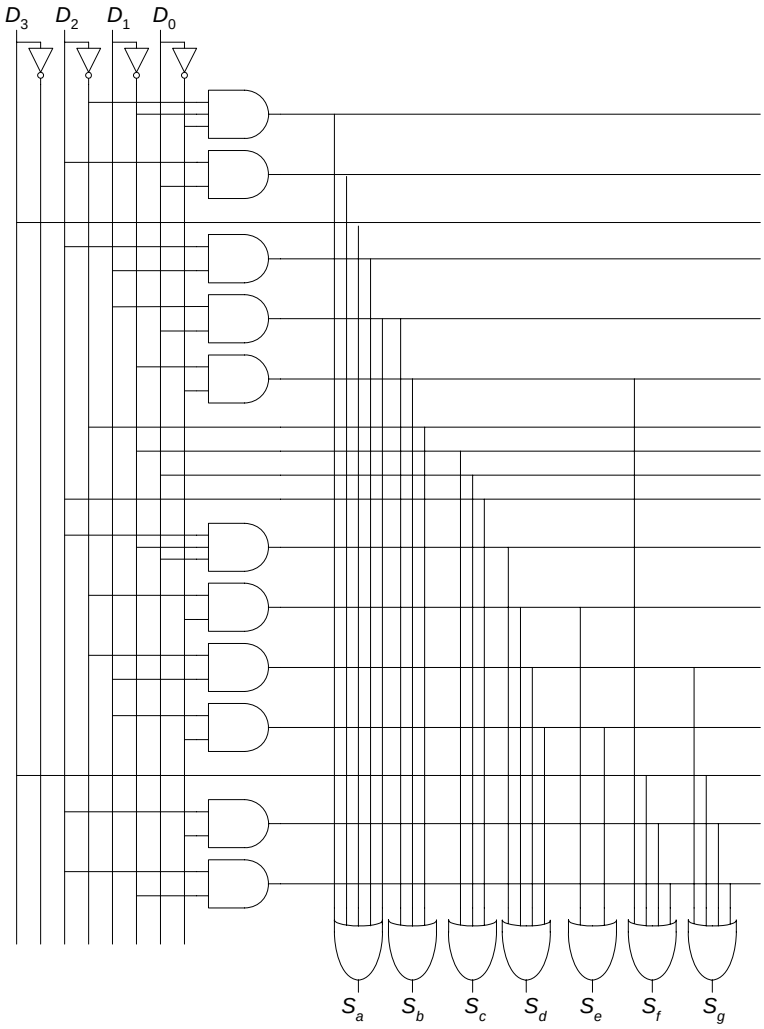


$S_f = \bar{D}_1\bar{D}_0 + D_2\bar{D}_1 + D_2\bar{D}_0 + D_3$



$S_g = \bar{D}_2D_1 + D_2\bar{D}_0 + D_2\bar{D}_1 + D_3$

(c)



2.25

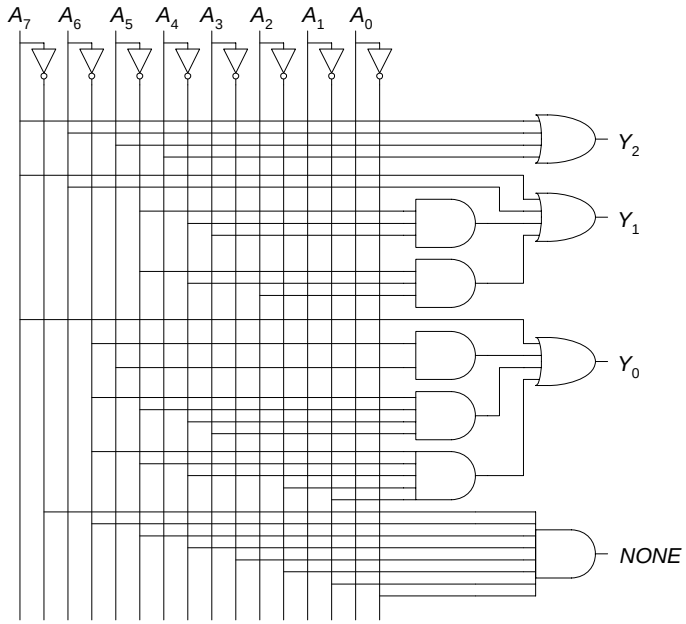
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Y_2	Y_1	Y_0	*NONE*
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	1	X	0	0	1	0
0	0	0	0	0	1	X	X	0	1	0	0
0	0	0	0	1	X	X	X	0	1	1	0
0	0	0	1	X	X	X	X	1	0	0	0
0	0	1	X	X	X	X	X	1	0	1	0
0	1	X	X	X	X	X	X	1	1	0	0
1	X	X	X	X	X	X	X	1	1	1	0

$$Y_2 = A_7 + A_6 + A_5 + A_4$$

$$Y_1 = A_7 + A_6 + \overline{A}_5\overline{A}_4A_3 + \overline{A}_5\overline{A}_4A_2$$

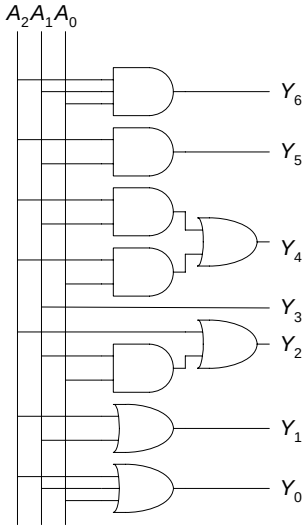
$$Y_0 = A_7 + \overline{A}_6A_5 + \overline{A}_6\overline{A}_5\overline{A}_4A_3 + \overline{A}_6\overline{A}_5\overline{A}_4\overline{A}_2A_1$$

$$NONE = \overline{A}_7\overline{A}_6\overline{A}_5\overline{A}_4\overline{A}_3\overline{A}_2\overline{A}_1\overline{A}_0$$



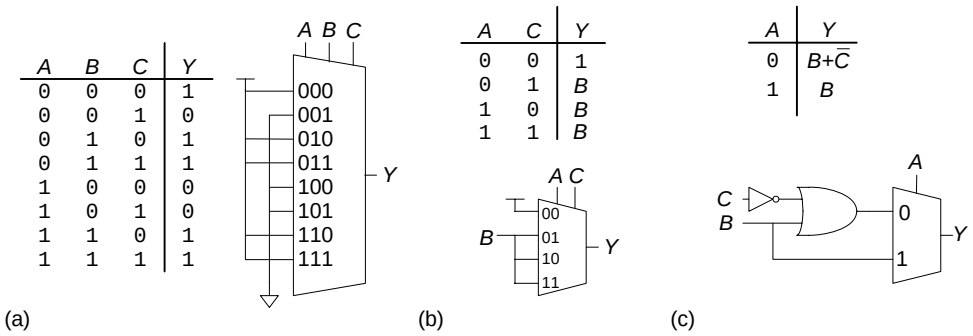
2.27

$$Y_6 = A_2A_1A_0$$
$$Y_5 = A_2A_1$$
$$Y_4 = A_2A_1 + A_2A_0$$
$$Y_3 = A_2$$
$$Y_2 = A_2 + A_1A_0$$
$$Y_1 = A_2 + A_1$$
$$Y_0 = A_2 + A_1 + A_0$$



2.29 $Y = \overline{C}\,\overline{D}(A \oplus B) + \overline{A}\,\overline{B} = \overline{A}\,\overline{C}\,\overline{D} + \overline{B}\,\overline{C}\,\overline{D} + \overline{A}B$

2.31



A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

(a)

A	C	Y
0	0	1
0	1	B
1	0	B
1	1	B

(b)

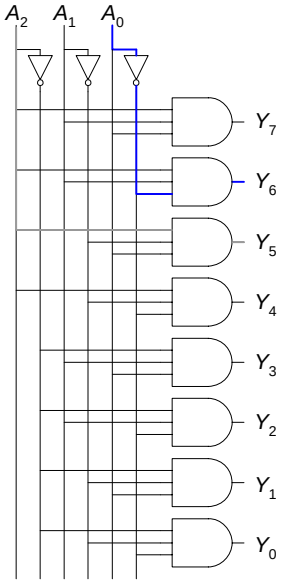
A	Y
0	$B+\overline{C}$
1	B

(c)

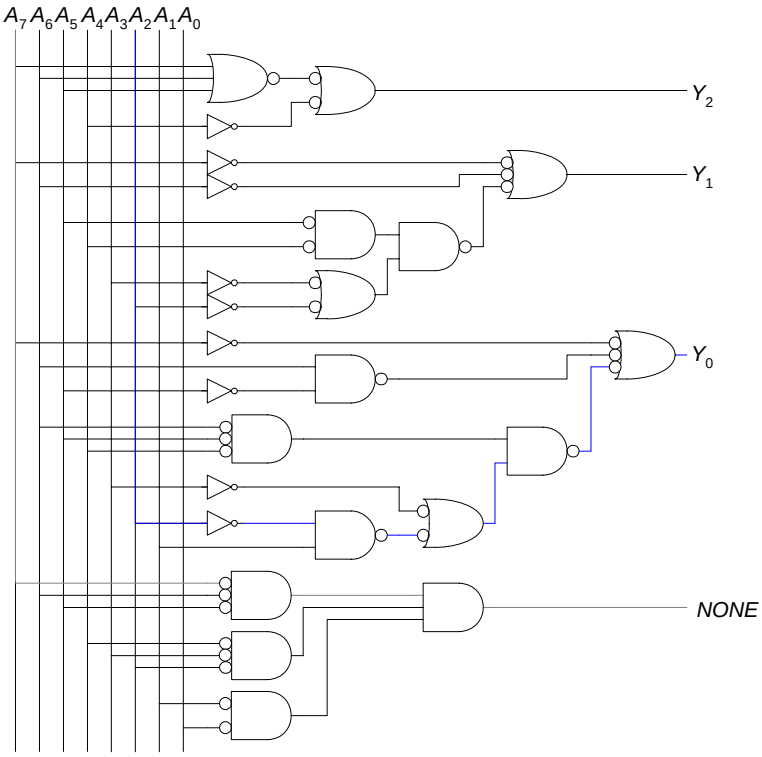
2.33

$t_{pd} = t_{pd\_NOT} + t_{pd\_AND3}$
$= 15 \text{ ps} + 40 \text{ ps}$
$= \mathbf{55 \text{ ps}}$

$t_{cd} = t_{cd\_AND3}$
$= \mathbf{30 \text{ ps}}$

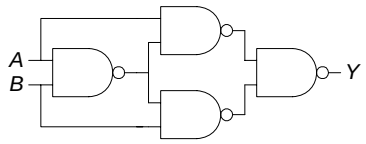


2.35



$t_{pd} = t_{pd\_INV} + 3t_{pd\_NAND2} + t_{pd\_NAND3}$
$= [15 + 3\ (20) + 30]$ ps
$=$ **105 ps**
$t_{cd} = 2t_{cd\_NOR3} + t_{cd\_AND3}$
$= [35 + 30]$ ps
$=$ **65 ps**

Question 2.1



Question 2.3

A tristate buffer has two inputs and three possible outputs: 0, 1, and Z. One of the inputs is the data input and the other input is a control input, often called the *enable* input. When the enable input is 1, the tristate buffer transfers the data input to the output; otherwise, the output is high impedance, Z. Tristate buffers are used when multiple sources drive a single output at different times. One and only one tristate buffer is enabled at any given time.

Question 2.5

A circuit's contamination delay might be less than its propagation delay because the circuit may operate over a range of temperatures and supply voltages, for example, 3-3.6 V for LVCMOS (low voltage CMOS) chips. As temperature increases and voltage decreases, circuit delay increases. Also, the circuit may have different paths (critical and short paths) from the input to the output. A gate itself may have varying delays between different inputs and the output, affecting the gate's critical and short paths. For example, for a two-input NAND gate, a HIGH to LOW transition requires two nMOS transistor delays, whereas a LOW to HIGH transition requires a single pMOS transistor delay.