# EE2026 (Part 1)
Tutorial 4 - Questions

Boolean Algebra and Minimization

1. A switching circuit has four inputs as shown. A and B represent the MSB and LSB bits of a binary number N_1. C and D represent the MSB and LSB bits of a binary number N_2. The output is to be 1 only if the product $N_1 \times N_2$ is less than or equal to 2.
   (a) Write the truth table for the system.
   (b) Write the canonical SOP and POS expressions for F.
   (c) Draw a Karnaugh-map (K-map) for the function F.
   (d) From the K-map, derive the MSOP expression for F.
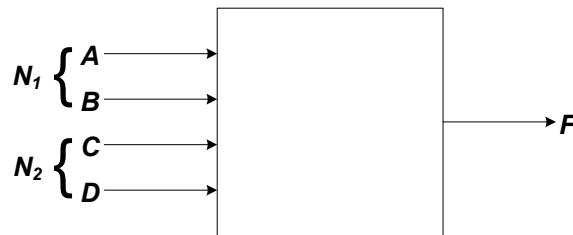
2. A bank vault has three locks with a different key for each lock. Each key is owned by a different person. To open the door, at least two people must insert their keys into the assigned locks. The signal lines A, B and C are 1 if there is a key inserted into lock 1, 2 or 3, respectively. Write an equation for the variable Z which is 1 if and only if the door should open.
   (a) Write the truth table for the system.
   (b) Write the canonical SOP and POS expressions for Z.
   (c) Draw a Karnaugh-map (K-map) for the function Z.
   (d) From the K-map, derive the MSOP expression for Z.

3. Use K-maps to obtain an MSOP and an MPOS for each of the following functions:
   (a) $Z = \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}B\overline{C}D + AB\overline{C}D + A\overline{B}\,\overline{C}D + AB\overline{C}\,\overline{D}$ with don't care for $ABCD = 1010$
   (b) $Z = \left(\overline{A} + B + \overline{C}\right)\left(A + B + \overline{C}\right)$ with don't cares for ABC = 111 and 110
   (c) $f(x_1, \ldots, x_4) = \sum m(0, 4, 5, 6, 7) + D(1, 12, 13, 14, 15)$, where $m(\,)$ is the set of minterms for which $f = 1$ and $D(\,)$ is the set of don't cares. For example, $m(2)$ is the minterm corresponding to $x_1 x_2 x_3 x_4 = 0010$ (this alternate shorthand notation is often used to express SOPs).

4. A combinational circuit has four inputs A, B, C and D and one output Z. The output is asserted whenever three or more of the inputs are asserted, otherwise the output is de-asserted. Find an MSOP expression for Z. Design the combinational circuit using only inverters, 2-input NAND gates and 3-input NAND gates. Assume that A, B and Z are active high signals, while C and D are active low signals. Use alternate gate representations for clarity of circuit diagrams. Calculate the critical path delay.

Gate	t_{pd}
NOT	0.3ns
2-input NAND	0.5ns
3-input NAND	0.8ns