EE2026: DIGITAL DESIGN

Academic Year 2025-2026, Semester 1

LAB 2: Combinational Circuits in Verilog

OVERVIEW:

A combinational circuit is one where the outputs depend only on the current inputs. In this lab, we will be designing some combinational circuits that are able to perform addition.

The pre-requisite for this lab requires one to be able to:

- Create a Verilog project and design source in Vivado.
- Create a testbench to simulate the design source.
- Generate the RTL schematic and the synthesised circuit schematic of the design source.
- Map and implement a design on the Basys 3 development board.

This lab will cover the following:

- Designing a one-bit full adder circuit using the dataflow modelling method.
- Designing a two-bit parallel adder circuit using the structural modelling method.

Tasks for this lab include:

- Designing the Verilog code of a one-bit full adder.
- Designing, simulating and implementing a four-bit parallel adder on the FPGA.
- Understanding a 1-bit two-to-one multiplexer.

GRADED ASSIGNMENT [CANVAS SUBMISSION: THURSDAY 11th SEPTEMBER 2025, 6:00 A.M.]:

Details are available at the end of this lab manual.

ONE-BIT-FULL ADDER:

Consider the binary addition shown in ***Figure 2.1***. To design a circuit that would perform the addition of two one-bit values, the circuit would need to have three input bits and two output bits.

Figure 2.1: *Binary Addition and functional block diagram of the one-bit full adder*

Such a circuit is called a one-bit full adder. It adds two bits (**A**, **B**) and the carry ($\mathbf{C_{in}}$) from a previous stage of addition, and produces a sum (**S**) and a carry ($\mathbf{C_{out}}$), as illustrated through a truth table in ***Figure 2.2***. By simplifying the truth table, the Boolean expressions for **S** and $\mathbf{C_{out}}$ can be obtained.

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + C_{in}\,(A \oplus B)$$

Figure 2.2: *Truth table and boolean expressions of the one-bit full adder*

Note: A half adder, in contrast to a full adder, does not involve a carry input. Thus, for a half adder, $S = A \oplus B$, and $C_{out} = AB$

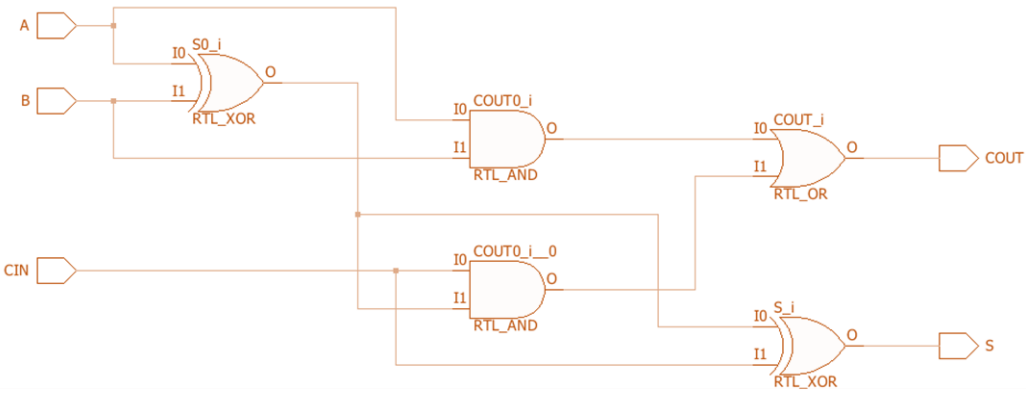
UNDERSTANDING | TASK 1

Using the dataflow method, complete the Verilog code for the one-bit full adder. Verify that the RTL schematic is as shown.

Verilog skeleton code for the one-bit-full adder:

```
module my_full_adder(input A, B, CIN, output S, COUT);

    assign S =
    assign COUT =

endmodule
```

RTL schematic for the one-bit full adder:



TWO-BIT FULL ADDER:

By cascading one-bit full adder blocks, the one-bit adder can be reused and parallel adders that add multiple bits can be created through the structural modelling method. A two-bit ripple-carry adder is illustrated in ***Figure 2.3***.

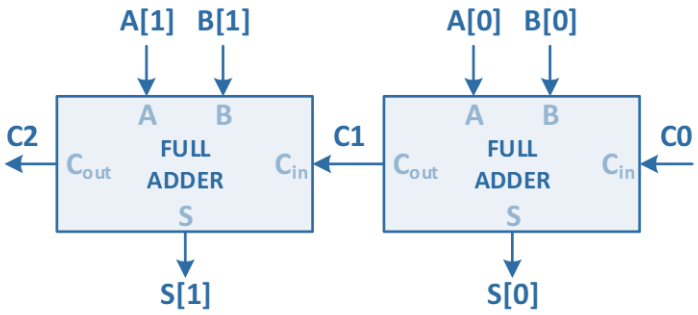


Figure 2.3: *Functional block diagram of the two-bit ripple-carry adder*

With the code for a one-bit full adder, a new module is created and two full adder blocks (fa0, fa1) are instantiated. By specifying the inputs and outputs to these blocks, the connection **C1** between them is made. Note that the order of signals during instantiation should respect the order in which they were declared in the one-bit full adder module **my_full_adder**.

This approach to hardware description is called structural modelling, whereby a more abstract module (for example, **my_2_bit_adder**) is built from simpler components describing gate-level hardware (such as **my_full_adder**).

Verilog code for two-bit ripple-carry adder, using structural modelling:

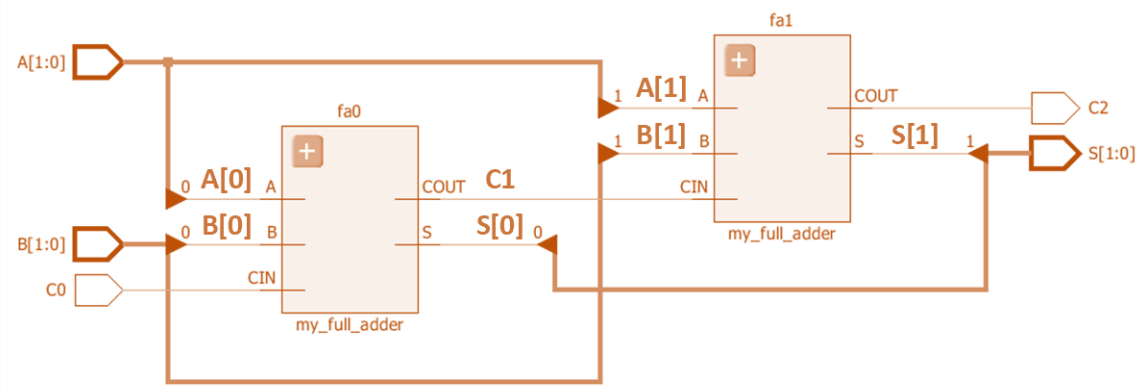
```
module my_2_bit_adder(input [1:0] A, input [1:0] B, input C0,
                      output [1:0] S, output C2);

    wire C1;

    my_full_adder fa0 (A[0], B[0], C0, S[0], C1);
    my_full_adder fa1 (A[1], B[1], C1, S[1], C2);

endmodule
```

[Note] Two-bit port declaration for A, B, S:

Instead of having multiple input and output ports (A1, A0, B1, B0, S1, S0), multi-bit vector ports are defined.

Example: `input [5:0] room`
Input port name is **room**, with size of 6 bits.
room[5] refers to the MSB.
room[0] refers to the LSB.

RTL schematic for the two-bit ripple-carry adder:



FOUR-BIT FULL ADDER:

The functional block diagram of a four-bit ripple-carry adder is shown in ***Figure 2.4***.

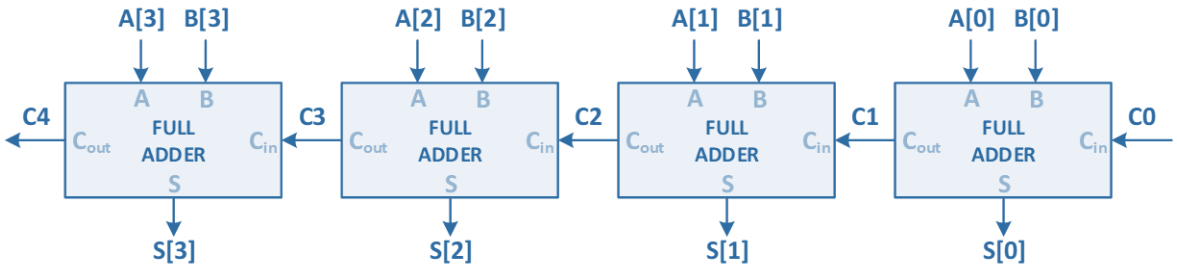


Figure 2.4: *Functional block diagram of a four-bit ripple-carry adder*

UNDERSTANDING | TASK 2

Start by adding a new design source for the four-bit full adder.

1. By using the structural modelling method, design a four-bit ripple-carry adder.
2. Generate the RTL schematic and check that connections between the blocks are correct.
3. Simulate your code with the following three sets of input values, and check that the simulation outputs are correct:

A:		0	0	1	1	A:		1	0	1	1	A:		1	1	1	1
B:	+	0	0	1	1	B:	+	0	1	1	1	B:	+	1	1	1	1
		□	□	□	□			□	□	□	□			□	□	□	□

[Note] Brief guidelines for multi-bit vector ports in the testbench:

- The port size should be indicated when declaring the signals. Inputs to the module being tested are declared using **reg**, whereas outputs from the module being tested are declared using **wire**:
  `reg [3:0] A; wire [3:0] S;`
- The parameters for the module being tested do not need the port size of the signals:
  `my_4_bit_adder module_alias (A, B, CARRY_IN, S, CARRY_OUT);`
- The testbench stimuli for multi-bit vector ports can be written as:
  `A = 4'b0011; B = 4'b0011; CARRY_IN = 1'b0;`

4. Synthesise and implement your code on the FPGA, using appropriate switches and LEDs on the Basys 3 development board to represent the inputs and outputs.

This task is considered completed and understood if you have the following items related to the four-bit full adder:

- The RTL schematic of your design (item 2 of this task)
- The simulation waveform results of the three testbench stimuli (item 3 of this task)
- The four-bit ripple-carry adder on the Basys 3 development board (item 4 of this task)

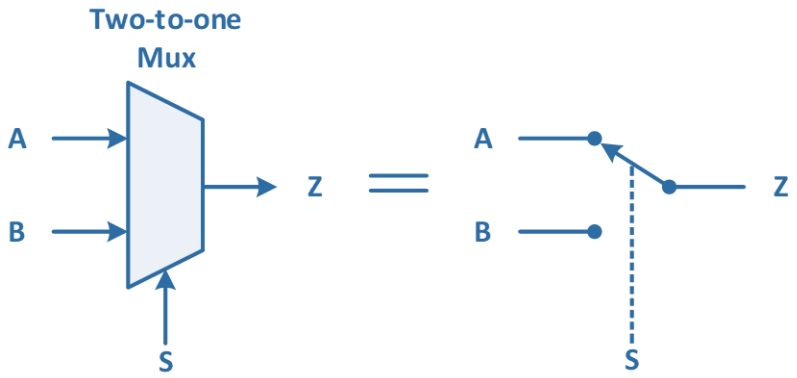
UNDERSTANDING | TASK 3

Instead of using four one-bit adder blocks, make a two-bit adder first. Then instantiate 2 sets of the two-bit adder to create a four-bit adder. Complete this practice task before working on the graded assignment.

1-BIT TWO-TO-ONE MULTIPLEXER (POST-LAB NON-GRADED – NO SUBMISSION REQUIRED):

Complete this practice task before working on the graded post-lab assignment!

A multiplexer (MUX) is a combinational circuit that connects one of its input signals to the output, based on the control signal. A simple 1-bit two-to-one mux, with inputs **A**, **B**, control signal **S**, and output **Z**, is illustrated as a functional block diagram, together with its simplified truth table, in **Figure 2.5.**



S	Z
0	A
1	B

Figure 2.5: *Functional block diagram and truth table of a 1-bit two-to-one multiplexer*

UNDERSTANDING | TASK 4

A quick way to implement the Verilog code for a 1-bit two-to-one multiplexer is using the conditional syntax:

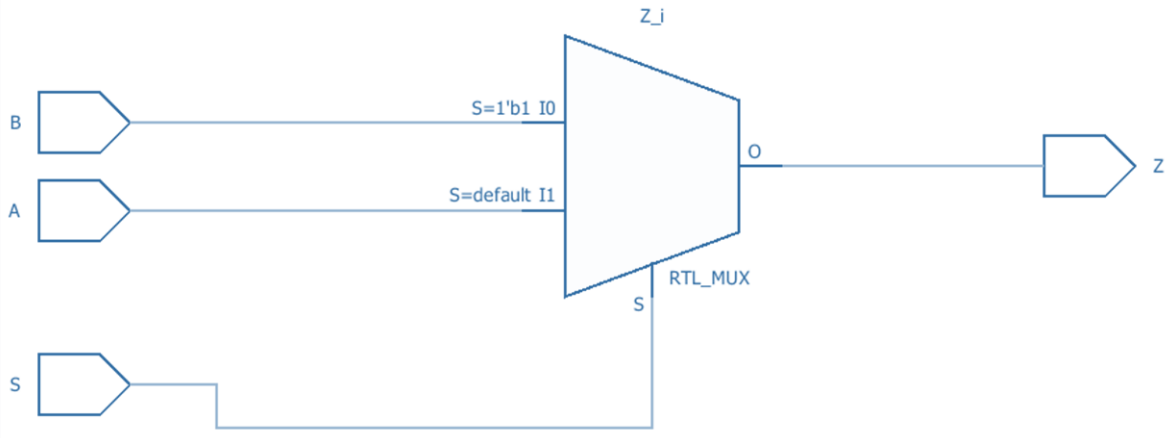
condition ? expression1 : expression2;

Notice in the schematic, how the code is automatically recognised as a MUX.

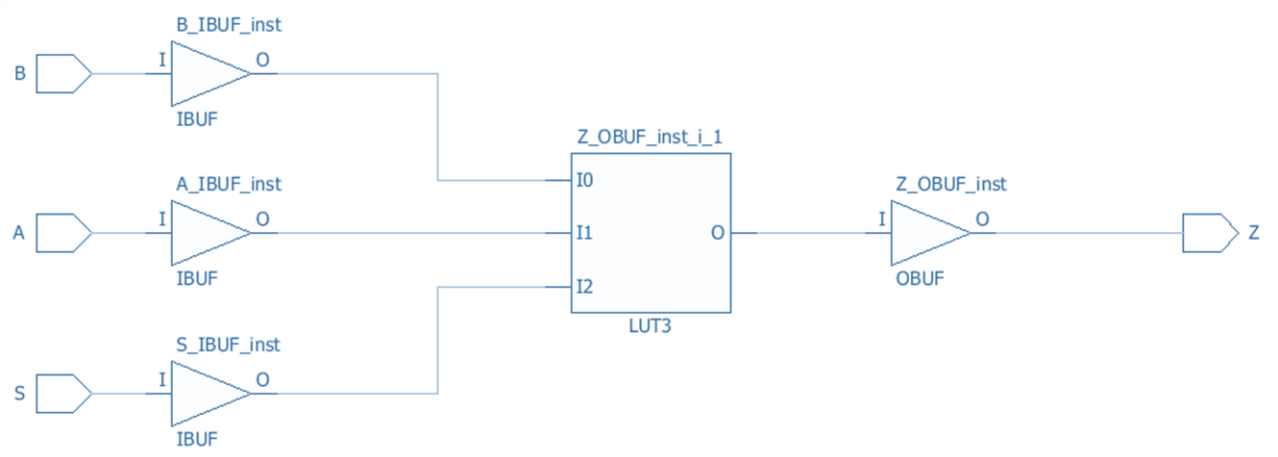
Verilog code for 1-bit two-to-one mux, using the dataflow method

```
module my_2_to_1_mux (input A, B, S, output Z);
    assign Z = S ? B : A; // assign B to Z if S = 1 or assign A to Z if S = 0;
endmodule
```

RTL schematic for the 1-bit two-to-one mux



Synthesised design schematic for the 1-bit two-to-one mux



Fill in the truth table for the **LUT3**, as extracted from the synthesised design schematic (click on LUT3 in Vivado, and look for the truth table) for the 1-bit two-to-one mux:

Explain how the truth table for the **LUT3** matches that of the truth table indicated in **Figure 2.5**:

BEFORE STARTING ON THE GRADED ASSIGNMENT:

Each student has a personalised requirement based on student matriculation number. Carefully write down your number, as mistakes in the student matriculation number are not accepted:

	7th Rightmost Number	6th Rightmost Number	5th Rightmost Number	4th Rightmost Number	3rd Rightmost Number	2nd Rightmost Number	1st Rightmost Number	Rightmost Alphabet
A	**0**							

Students are required to carefully read all the assignment requirements, and to enhance their understanding by looking at the example.

Marks are given for using your correct student matriculation number, and grading is done only once. Re-submissions, late submissions, or updates, even if very simple or minor, are **not accepted** after the grading.

Apply the switch and LED constraint requirements in SUBTASK C carefully. Marks will not be given if the wrong switches or LEDs are used.

GRADED POST-LAB ASSIGNMENT

Complete as much as possible, in **ONE working bitstream for this whole assignment**. It is much better to have a working program with some completed functionalities, instead of submitting a program without a working bitstream (No marks given).

IMPORTANT CHARACTERS

In this assignment, these are the important characters to note from your student matriculation number:

- The 2nd rightmost numerical value of your student matriculation number (Initialisation, subtask B)
- The 3rd rightmost numerical value of your student matriculation number (Subtask A)

INITIALISATION

When the program starts, the seven segment displays must show the following patterns **exactly**, based on the **2nd rightmost numerical value of your student matriculation number**:

2nd Rightmost Numerical Value	0	1	2	3	4
Required 7-Segments Displays					

2nd Rightmost Numerical Value	5	6	7	8	9
Required 7-Segments Displays					

In the previous lab, we had use one bit signal to control each LED / segment / anode. From this lab onwards:

It is **compulsory to use multi-bits vectors** to give values to the segments and anodes. For example:

- A value of **8'b00000000** to the segments turns on all 8 segments (7 segments + decimal point).
- A value of **4'b0000** to the anodes turns on all 4 anodes.

SUBTASK A (Structural modelling)

Based on the **3rd rightmost numerical value of your student matriculation number**, create two separate parallel adders as indicated in the table below:

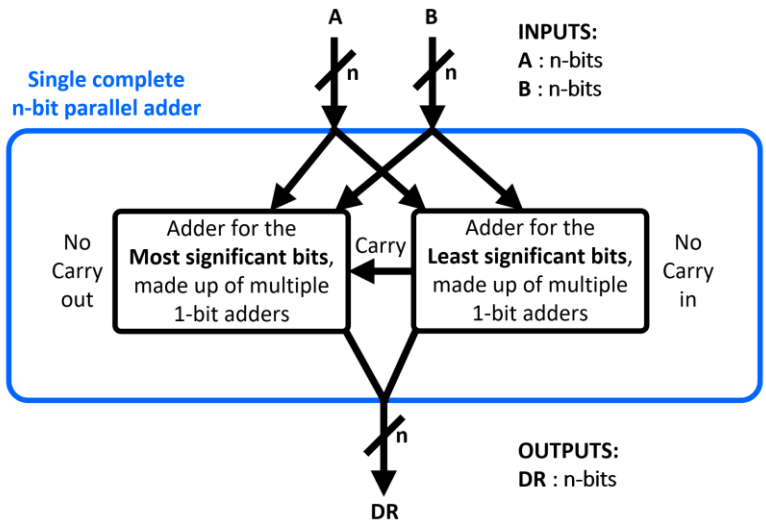
3rd Rightmost Numerical Value	Required parallel adders. Each one of these parallel adders must be made up of multiple 1-bit adders	
0	2-bit parallel adder	3-bit parallel adder
1	3-bit parallel adder	2-bit parallel adder
2	2-bit parallel adder	4-bit parallel adder
3	4-bit parallel adder	2-bit parallel adder
4	3-bit parallel adder	4-bit parallel adder
5	4-bit parallel adder	3-bit parallel adder
6	3-bit parallel adder	5-bit parallel adder
7	5-bit parallel adder	3-bit parallel adder
8	2-bit parallel adder	5-bit parallel adder
9	5-bit parallel adder	2-bit parallel adder

Following that, make use of both parallel adders to create a "single complete n-bit parallel adder" with inputs A and B, and output DR. The bits given to the "single complete n-bit parallel adder" must be divided between the two parallel adders as follows:

3rd Rightmost Numerical Value	**Most significant bits** of the complete adder must use the following adder	**Least significant bits** of the complete adder must use the following adder	n-bit input A, or Input B, of the complete adder	n-bit output DR of the complete adder
0	2-bit parallel adder	3-bit parallel adder	5 bits	5 bits
1	3-bit parallel adder	2-bit parallel adder	5 bits	5 bits
2	2-bit parallel adder	4-bit parallel adder	6 bits	6 bits
3	4-bit parallel adder	2-bit parallel adder	6 bits	6 bits
4	3-bit parallel adder	4-bit parallel adder	7 bits	7 bits
5	4-bit parallel adder	3-bit parallel adder	7 bits	7 bits
6	3-bit parallel adder	5-bit parallel adder	8 bits	8 bits
7	5-bit parallel adder	3-bit parallel adder	8 bits	8 bits
8	2-bit parallel adder	5-bit parallel adder	7 bits	7 bits
9	5-bit parallel adder	2-bit parallel adder	7 bits	7 bits

For the module dealing with the Least significant bits: There is no carry in, but there is a carry out.
For the module dealing with the Most significant bits: There is a carry in, but there is no carry out.

The block diagram for "single complete n-bit parallel adder" is as illustrated below:

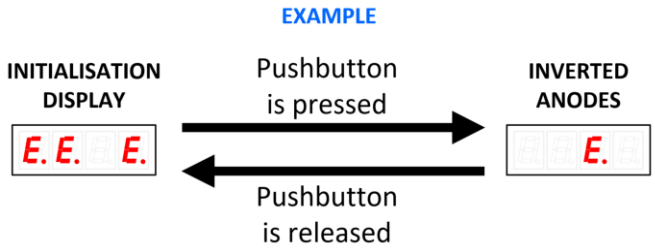


SUBTASK B (Manipulation and usage of multi-bits vectors)

When a certain pushbutton is pressed, the anodes of seven segment displays from the INITIALISATION part must be inverted. When that same pushbutton is released, the anodes of the seven displays must revert to how they were in the INITILISATION part.

The pushbutton to use is dependent on the **2nd rightmost numerical value of your student matriculation number**, as indicated in the table below:

2nd Rightmost Numerical Value	Pushbutton to use
0 , 5	BTNU (Up)
1 , 6	BTNR (Right)
2 , 7	BTND (Down)
3 , 8	BTNL (Left)
4 , 9	BTNC (Centre)



The result from the "single complete n-bit parallel adder" of SUBTASK A is called the default result (**DR**) and is to be shown by default on the LEDs of the Basys 3 development board. However, when the user presses and hold the pushbutton indicated at the start of this SUBTASK B, it is required to have another alternate n-bit result (**AR**) shown on the LEDs of the Basys 3 development board, instead of the n-bit default result (**DR**). That alternate n-bit result is dependent on the **2nd rightmost numerical value of your student matriculation number**, as shown in the table below:

2nd Rightmost Numerical Value	Alternate result (AR)	Further details
0	3 least significant bits of DR inverted	The other bits are not inverted
1	DR divided by 2	Ignore the decimal point of S (Round down)
2	DR multiplied by 8	Ignore bits that exceed the size of S
3	2 most significant bits of DR inverted	The other bits are not inverted
4	DR divided by 4	Ignore the decimal point of S (Round down)
5	DR multiplied by 2	Ignore bits that exceed the size of S
6	4 least significant bits of DR inverted	The other bits are not inverted
7	DR divided by 8	Ignore the decimal point of S (Round down)
8	DR multiplied by 4	Ignore bits that exceed the size of S
9	3 most significant bits of DR inverted	The other bits are not inverted

Avoid the usage of shift operators while trying to complete this subtask B.

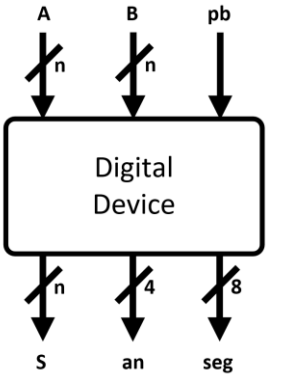
Hints:

- *To get the AR, consider: The usage of specific bits from the output DR of SUBTASK A / filling with zeros / concatenation.*
- *Use a multiplexor to determine whether DR or AR goes to the output S of the digital device*

Arithmetic operators for addition, subtraction, multiplication, and division are **NOT ALLOWED** anywhere inside this whole graded assignment. No marks will be given if arithmetic operators (**+** , **-** , ***** , **/**) are used

SUBTASK C (Implementation / Bitstream)

Combine the INITIALISATION, SUBTASK A, and SUBTASK B together, such that the digital device implemented on the Basys3 development board **only have these 6 ports** (In other words, only these 6 ports will be present in simulation also):



INPUTS:
A : n number of switches
B : n number of switches
pb : one pushbutton

OUTPUTS:
S : n number of LEDs
an : 4-bits anode
seg : 8-bits segment

It is COMPULSORY TO USE THE FOLLOWING SWITCHES to represent inputs A and B of the Digital Device:

- The input A must use consecutive switches on the Basys 3 development board, with the **least significant bit A[0] linked to SW0**. Similarly, A[1] should be linked to SW1, A[2] to SW2, and so on.

- The input B must use consecutive switches on the Basys 3 Development board, with the **least significant bit B[0] linked to SW8**. Similarly, B[1] should be linked to SW9, B[2] to SW10, and so on.

- **Switches not used by A or B must NOT be used or linked to any other signals under any circumstances.** For example, in a 4-bit Digital Device, SW4 to SW7, and SW12 and SW15, should not be linked to any signals, nor used in any circumstances.

It is COMPULSORY TO USE THE FOLLOWING LEDS to represent the output S of the Digital Device:

- The output S must use consecutive LEDs on the Basys 3 development board, with the **least significant bit S[0] linked to LD0**. Similarly, S[1] should be linked to LD1, S[2] should be linked to LD2, and so on.

- **LEDs not used by S must NOT be used or linked to any other signals under any circumstances.** For example, in a 4-bit Digital Device, with the 2nd rightmost numerical value of the student matriculation number being 3, LD4 to LD15, should not be linked to any signals, nor used in any circumstances (They must remain OFF).

SUBTASK D (Simulation)

You are also required to simulate and verify any **six unique** test cases in **one single simulation** for the digital device (Inputs A, B, pb, and outputs S, an, seg) created in SUBTASK C, and which meets the following conditions:

- Three out of the six test cases must have the pushbutton (pb) to be OFF
- Three out of the six test cases must have the pushbutton (pb) to be ON (A and B can be same as above, when pb is OFF)

A screenshot (PrintScreen) of the simulation waveform pattern from the Vivado simulation window must be obtained, and then pasted on a 1-page landscape page. Marks are only given if the simulation **waveforms and values** for **all six test cases** and are **clear and meet these number formats / representations**:

- Input A, input B, input pb, output S, output an, output seg are all in **binary or hexadecimal representation**
- **No 'X' or 'Z' values in any of the waveforms** (These indicate unknown or high impedance values)
- Inputs A, B and outputs S, an, seg must each be declared as multi-bits vectors (not as individual 1-bit) and must **not** be expanded in the simulation waveform window (In other words, there are 5 rows representing those 5 signals).

DOCUMENT UPLOAD REQUIREMENTS:

(1) Your name and matriculation number on the top of the document.
(2) The screenshot (PrintScreen) of the simulation waveform pattern from the Vivado simulation window on the document.

Print the **landscape** document as a **single PDF** for CANVAS upload. The PDF file **must follow the naming template** indicated in the CANVAS submission instruction at the end of this lab manual.

SUGGESTIONS

- Complete the MUX task and understand the purpose of MUX before working on the assignment.
- Assume the pushbutton works like a switch when it is pressed and held.
- The following will be taught in subsequent labs, and are thus not necessary in lab 2:
    - if-else functions (Instead, use something similar to the MUX task)
    - always blocks (Instead, use dataflow and structural modelling)
    - shift operators (Instead, make clever use of the multi-bits vector manipulation)

EXAMPLE:

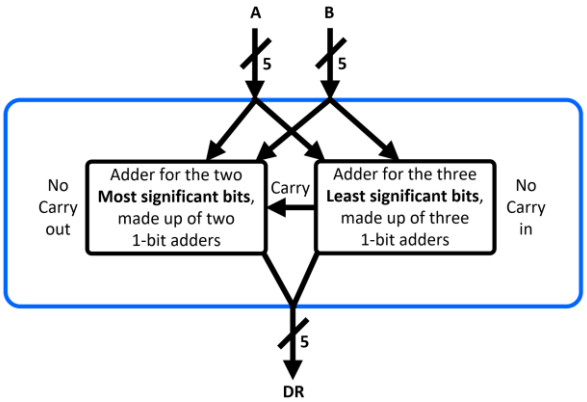
If your student matriculation number is A0159089Y, then:

2^{nd} rightmost numerical value: **8** (Initialisation and subtask B depends on this number)
3^{rd} rightmost numerical value: **0** (Subtask A depends on this number)

INITIALISATION

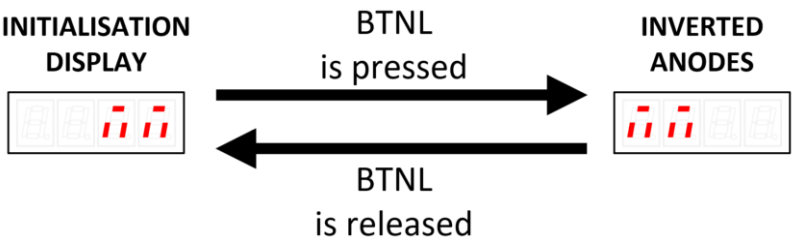
SUBTASK A

Matric. Value = 0	2-bit parallel adder	3-bit parallel adder	5 bits	5 bits



SUBTASK B

Matric. Value = 8	BTNL (Left)



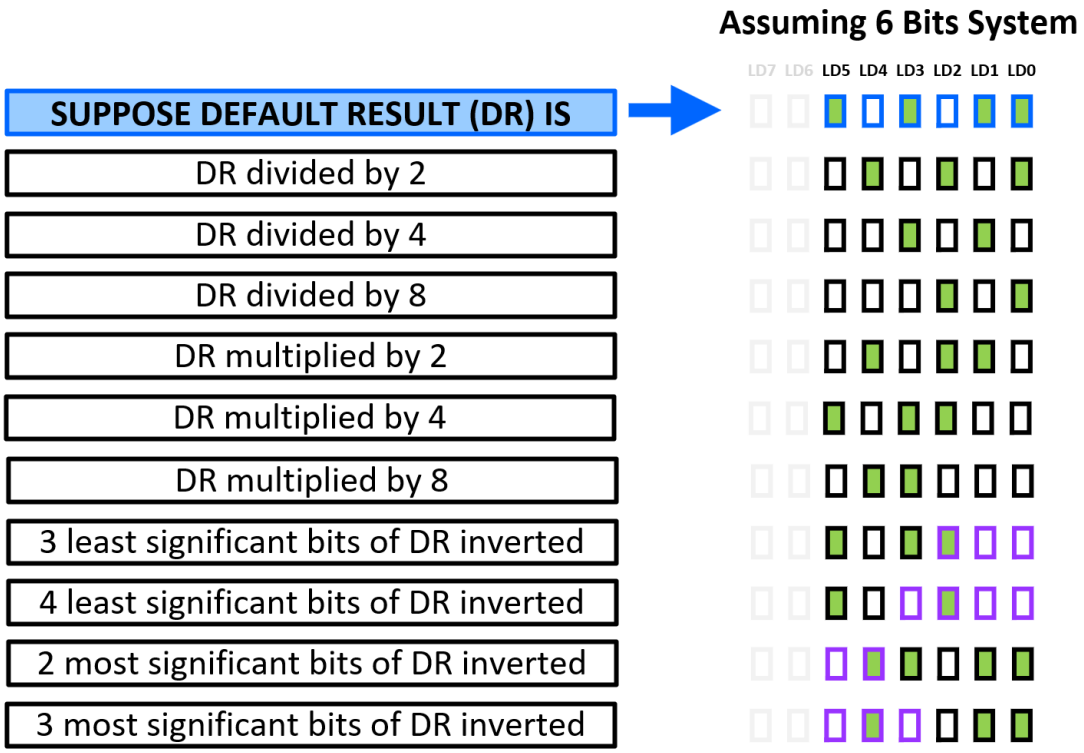
Matric. Value = 8	DR multiplied by 4	Ignore bits that exceed the size of S

SUBTASK C

A[0] linked to **SW0**, **A[1]** linked to SW1, **A[2]** linked to SW2, **A[3]** linked to SW3, **A[4]** linked to SW4
B[0] linked to **SW8**, **B[1]** linked to SW9, **B[2]** linked to SW10, **B[3]** linked to SW11, **B[4]** linked to SW12
pb linked to **BTNL**

S[0] linked to LD0, **S[1]** linked to LD1, **S[2]** linked to LD2, **S[3]** linked to LD3, **S[4]** linked to LD4
an[0] linked to AN0, **an[1]** linked to AN1, **an[2]** linked to AN2, **an[3]** linked to AN3
seg[0] linked to seg[0], **seg[1]** linked to seg[1], … **seg[5]** linked to seg[5], **seg[6]** linked to seg[6], **seg[7]** linked to dp

ADDITIONAL EXAMPLES FOR SUBTASK B



CANVAS SUBMISSION INSTRUCTIONS

- Ensure that your bitstream has been successfully generated and tested on your Basys 3 development board **BEFORE** archiving your Vivado workspace for CANVAS upload.

- It is compulsory to archive your project in a compressed form without any saved simulation waveforms. Follow the instructions given in the pdf: "Archive Project in Vivado 2018.02". **The archive size should not exceed 5 MB in size for any lab assignments.** If the archive size exceeds, ensure that there is no ".sim" folder in your Vivado project folder before archiving.

- **After** following the instructions in "**Archive Project in Vivado 2018.02**", rename your project archive as indicated in the appendix of this lab manual.

- **Separately** from the project archive, **the single PDF document** (Contains the simulation waveform) is to be named as indicated in the appendix of this lab manual.

- Upload to CANVAS EE2026 -> Assignments -> Lab 2 Graded Assignment -> Lab 2 Submission (On-Time).

- Download your CANVAS archive after uploading. **Click and drag the single folder within that archive to desktop**, and then open the Vivado project (.xpr) in that **extracted folder** to see if it can be opened. You can ignore "out-of-date" warnings. **Check if you can also run your bitstream correctly.** No project files and no working bitstream is equivalent to losing all marks.

- The CANVAS upload must be completed by **Thursday 11th September 2025, 6:00 A.M. (Morning)**. Avoid planning your upload during the grace period of 2 hours. (Grace period is for unexpected cases, such as slow internet)

- A penalty of 10% on the assignment 2 weight applies for **late submissions of up to 1 week**. Submissions after that 1 week may not be accepted. (Delaying the assignment will make all subsequent labs exponentially more difficult to manage)

- The late submission folder closes 1 week after the original deadline. **Late submissions are not graded if submissions are found in the on-time folder. Do not submit in the late submission folder if you have already submitted in the on-time folder. Inform your lab instructor if you have uploaded in both the on-time folder and late submission folder.** The late submission folder will be located at: CANVAS EE2026 -> Assignments -> Lab 2 Graded Assignment -> Lab 2 Submission (Late).

- Re-submissions, late submissions, or updates, even if very simple or minor, are **not accepted** after your original submission has been graded.

- Submissions through emails, file sharing programs, or links, are **not accepted**. Submissions must be officially submitted to, and downloadable from, Canvas in the correct on-time or late folder.

Plagiarism is penalised with a 100% penalty for all SOURCES and RECIPIENTS

All past and future submissions, and marks, will be reviewed in greater detail, for any person found to have plagiarised

ALL THE SUBMISSION INSTRUCTIONS LISTED ABOVE WILL AFFECT YOUR GRADES!

GRADING PROCESS

- During subsequent lab sessions, our graders will be providing you updates on the grading of your submission.

- Submissions not following all the ***CANVAS SUBMISSION INSTRUCTIONS*** (listed above) will not be graded immediately, and they will instead be reviewed towards the end of the semester. **You will not be able to see your submission results during the lab sessions in such situations**.

APPENDIX (COMPULSORY renaming just before CANVAS upload):

It is **compulsory to rename your project archive and PDF report**, just before the CANVAS upload, as listed in the table below.

Do not change any other part of the naming. Simply **copy** the naming from the table below and **paste** it while renaming your project archive and PDF report. Then upload these 2 items to CANVAS after the renaming. Penalties will be incurred if your submission cannot be found according to the exact naming template below.

CANVAS may automatically add a suffix (Example. "-1", "-2", "-3" etc.) at the end of the filename if you submit multiple files. That is acceptable and we will grade the latest file submitted within that on-time folder.

Archive Naming (.xpr.zip and .zip accepted)	PDF Report Naming
Lab2_Mon_AM_AARAV RAJESH_165_Archive	Lab2_Mon_AM_AARAV RAJESH_165_Report
Lab2_Mon_AM_ABE FOO QIAN YIN_426_Archive	Lab2_Mon_AM_ABE FOO QIAN YIN_426_Report
Lab2_Mon_PM_ABHIJIT BALAJEE_045_Archive	Lab2_Mon_PM_ABHIJIT BALAJEE_045_Report
Lab2_Mon_PM_ABIRAMI BASKARAN_550_Archive	Lab2_Mon_PM_ABIRAMI BASKARAN_550_Report
Lab2_Mon_AM_ABUDAHEER MOHAMMED IBRAHI_637_Archive	Lab2_Mon_AM_ABUDAHEER MOHAMMED IBRAHI_637_Report
Lab2_Fri_AM_ADIT BISWAS_789_Archive	Lab2_Fri_AM_ADIT BISWAS_789_Report
Lab2_Mon_PM_AFSHAL GULAM_376_Archive	Lab2_Mon_PM_AFSHAL GULAM_376_Report
Lab2_Mon_PM_AHMAD TIRMIZI BIN ADAM_523_Archive	Lab2_Mon_PM_AHMAD TIRMIZI BIN ADAM_523_Report
Lab2_Mon_PM_AIDAN CHIA TONG_306_Archive	Lab2_Mon_PM_AIDAN CHIA TONG_306_Report
Lab2_Mon_PM_ALEXANDER YAW KAI MUN_328_Archive	Lab2_Mon_PM_ALEXANDER YAW KAI MUN_328_Report
Lab2_Mon_PM_ALIYEV ESHGIN_149_Archive	Lab2_Mon_PM_ALIYEV ESHGIN_149_Report
Lab2_Mon_PM_ARIFF MUHAMMED AHSAN HUSA_407_Archive	Lab2_Mon_PM_ARIFF MUHAMMED AHSAN HUSA_407_Report
Lab2_Fri_AM_AW SHUO JIE_803_Archive	Lab2_Fri_AM_AW SHUO JIE_803_Report
Lab2_Mon_PM_AYDEN VAN ETTEN_971_Archive	Lab2_Mon_PM_AYDEN VAN ETTEN_971_Report
Lab2_Fri_AM_BADRINATH SANDHYA_704_Archive	Lab2_Fri_AM_BADRINATH SANDHYA_704_Report
Lab2_Mon_AM_BAE SOOHUN_652_Archive	Lab2_Mon_AM_BAE SOOHUN_652_Report
Lab2_Mon_PM_BAJAJ KRISHNA_769_Archive	Lab2_Mon_PM_BAJAJ KRISHNA_769_Report
Lab2_Mon_AM_BENJAMIN CHEK JUN KIET_381_Archive	Lab2_Mon_AM_BENJAMIN CHEK JUN KIET_381_Report
Lab2_Mon_PM_BENJAMIN LOH JIAN WEI_455_Archive	Lab2_Mon_PM_BENJAMIN LOH JIAN WEI_455_Report
Lab2_Mon_PM_BHADRA PARV_813_Archive	Lab2_Mon_PM_BHADRA PARV_813_Report
Lab2_Fri_AM_BINDAWALA AARAV_779_Archive	Lab2_Fri_AM_BINDAWALA AARAV_779_Report
Lab2_Mon_AM_BRENDAN TEY SHI HAN_957_Archive	Lab2_Mon_AM_BRENDAN TEY SHI HAN_957_Report
Lab2_Fri_AM_BRIEN LIM CHONG_162_Archive	Lab2_Fri_AM_BRIEN LIM CHONG_162_Report
Lab2_Mon_AM_CEDRIC TAN SI YU_331_Archive	Lab2_Mon_AM_CEDRIC TAN SI YU_331_Report
Lab2_Mon_PM_CHAKRABORTY SHRABASTI_685_Archive	Lab2_Mon_PM_CHAKRABORTY SHRABASTI_685_Report
Lab2_Mon_PM_CHAN YI FENG_824_Archive	Lab2_Mon_PM_CHAN YI FENG_824_Report
Lab2_Mon_AM_CHANG YI HERNG_612_Archive	Lab2_Mon_AM_CHANG YI HERNG_612_Report
Lab2_Mon_AM_CHARNG HE_580_Archive	Lab2_Mon_AM_CHARNG HE_580_Report
Lab2_Fri_AM_CHEN GUANWEN_978_Archive	Lab2_Fri_AM_CHEN GUANWEN_978_Report
Lab2_Fri_AM_CHEN HONGYU_122_Archive	Lab2_Fri_AM_CHEN HONGYU_122_Report
Lab2_Mon_PM_CHEN XINGTONG_961_Archive	Lab2_Mon_PM_CHEN XINGTONG_961_Report
Lab2_Mon_PM_CHEN YU HSIN_432_Archive	Lab2_Mon_PM_CHEN YU HSIN_432_Report
Lab2_Fri_AM_CHEO ZHI XIAN MATHEU_851_Archive	Lab2_Fri_AM_CHEO ZHI XIAN MATHEU_851_Report
Lab2_Mon_PM_CHEONG JIAN HAO_240_Archive	Lab2_Mon_PM_CHEONG JIAN HAO_240_Report
Lab2_Fri_AM_CHEW EN WEI_658_Archive	Lab2_Fri_AM_CHEW EN WEI_658_Report
Lab2_Mon_AM_CHIA HAO JUN_207_Archive	Lab2_Mon_AM_CHIA HAO JUN_207_Report
Lab2_Fri_AM_CHIA LE ISAAC_940_Archive	Lab2_Fri_AM_CHIA LE ISAAC_940_Report
Lab2_Mon_PM_CHNG RUI YONG SEAN_435_Archive	Lab2_Mon_PM_CHNG RUI YONG SEAN_435_Report
Lab2_Mon_PM_CHONG KAI JIE_314_Archive	Lab2_Mon_PM_CHONG KAI JIE_314_Report
Lab2_Mon_AM_CHONG WEIXUAN CYDRIC_871_Archive	Lab2_Mon_AM_CHONG WEIXUAN CYDRIC_871_Report

Lab2_Mon_PM_CHOY ZHAN HONG_444_Archive	Lab2_Mon_PM_CHOY ZHAN HONG_444_Report
Lab2_Mon_AM_CHUA YONG LIANG_014_Archive	Lab2_Mon_AM_CHUA YONG LIANG_014_Report
Lab2_Fri_AM_CUI JIAHAO_085_Archive	Lab2_Fri_AM_CUI JIAHAO_085_Report
Lab2_Mon_PM_DANIEL CHUA ZHENG JIE_443_Archive	Lab2_Mon_PM_DANIEL CHUA ZHENG JIE_443_Report
Lab2_Mon_PM_DENG HAOFU_338_Archive	Lab2_Mon_PM_DENG HAOFU_338_Report
Lab2_Mon_PM_DENY HAANS HAZRIEL BIN AR_153_Archive	Lab2_Mon_PM_DENY HAANS HAZRIEL BIN AR_153_Report
Lab2_Mon_PM_DIWAKAR VIDYA ADHAVAN_335_Archive	Lab2_Mon_PM_DIWAKAR VIDYA ADHAVAN_335_Report
Lab2_Mon_PM_DYLAN LIM_821_Archive	Lab2_Mon_PM_DYLAN LIM_821_Report
Lab2_Mon_AM_EMRY DANIEL BIN ABDUL LAT_550_Archive	Lab2_Mon_AM_EMRY DANIEL BIN ABDUL LAT_550_Report
Lab2_Fri_AM_FOO KANG_353_Archive	Lab2_Fri_AM_FOO KANG_353_Report
Lab2_Mon_AM_GABRA SHUBHAN_258_Archive	Lab2_Mon_AM_GABRA SHUBHAN_258_Report
Lab2_Mon_PM_GABRIEL LEE JING YI_006_Archive	Lab2_Mon_PM_GABRIEL LEE JING YI_006_Report
Lab2_Fri_AM_GAN ANDREW HOA THIEN_281_Archive	Lab2_Fri_AM_GAN ANDREW HOA THIEN_281_Report
Lab2_Fri_AM_GOH ANG LEE_598_Archive	Lab2_Fri_AM_GOH ANG LEE_598_Report
Lab2_Fri_AM_GOH SHAO ANN_219_Archive	Lab2_Fri_AM_GOH SHAO ANN_219_Report
Lab2_Mon_AM_GOH SZE ANH_325_Archive	Lab2_Mon_AM_GOH SZE ANH_325_Report
Lab2_Fri_AM_GOH YOU YI_326_Archive	Lab2_Fri_AM_GOH YOU YI_326_Report
Lab2_Mon_PM_GORDON HONG JIA JIE_465_Archive	Lab2_Mon_PM_GORDON HONG JIA JIE_465_Report
Lab2_Mon_PM_GU MINGYOUJIA_260_Archive	Lab2_Mon_PM_GU MINGYOUJIA_260_Report
Lab2_Mon_AM_GUO ZICHENG_823_Archive	Lab2_Mon_AM_GUO ZICHENG_823_Report
Lab2_Mon_AM_HANNAH WESTERHOUT HASAN_413_Archive	Lab2_Mon_AM_HANNAH WESTERHOUT HASAN_413_Report
Lab2_Mon_PM_HAO YIAN_006_Archive	Lab2_Mon_PM_HAO YIAN_006_Report
Lab2_Fri_AM_HIEW T G_306_Archive	Lab2_Fri_AM_HIEW T G_306_Report
Lab2_Fri_AM_HOWIE YEO HAO YU_345_Archive	Lab2_Fri_AM_HOWIE YEO HAO YU_345_Report
Lab2_Fri_AM_HU LIFAN_030_Archive	Lab2_Fri_AM_HU LIFAN_030_Report
Lab2_Fri_AM_HU XIRAN_503_Archive	Lab2_Fri_AM_HU XIRAN_503_Report
Lab2_Mon_AM_HUANG HAU SHUAN_356_Archive	Lab2_Mon_AM_HUANG HAU SHUAN_356_Report
Lab2_Mon_AM_HUANG YUANJIN_080_Archive	Lab2_Mon_AM_HUANG YUANJIN_080_Report
Lab2_Mon_AM_IRWAN AHMED NOOR_184_Archive	Lab2_Mon_AM_IRWAN AHMED NOOR_184_Report
Lab2_Fri_AM_JAIRUS LEUNG JIE RUI_337_Archive	Lab2_Fri_AM_JAIRUS LEUNG JIE RUI_337_Report
Lab2_Mon_AM_JANSEN KEN PEGRASIO_566_Archive	Lab2_Mon_AM_JANSEN KEN PEGRASIO_566_Report
Lab2_Fri_AM_JAVIER YEOH ZHI JI_430_Archive	Lab2_Fri_AM_JAVIER YEOH ZHI JI_430_Report
Lab2_Fri_AM_JOEL KU_232_Archive	Lab2_Fri_AM_JOEL KU_232_Report
Lab2_Fri_AM_JOEL LIM JUN YI_423_Archive	Lab2_Fri_AM_JOEL LIM JUN YI_423_Report
Lab2_Fri_AM_JOHN KENNETH LAYBA AGPAOA_489_Archive	Lab2_Fri_AM_JOHN KENNETH LAYBA AGPAOA_489_Report
Lab2_Fri_AM_JOSHUA TAM KA YUI_315_Archive	Lab2_Fri_AM_JOSHUA TAM KA YUI_315_Report
Lab2_Fri_AM_JOSHUA YEO WEE TZE_878_Archive	Lab2_Fri_AM_JOSHUA YEO WEE TZE_878_Report
Lab2_Mon_AM_JOVIAN JOSH_585_Archive	Lab2_Mon_AM_JOVIAN JOSH_585_Report
Lab2_Mon_AM_KARTHIK KATHIRESH_122_Archive	Lab2_Mon_AM_KARTHIK KATHIRESH_122_Report
Lab2_Mon_PM_KARTHIKEYAN VETRIVEL_899_Archive	Lab2_Mon_PM_KARTHIKEYAN VETRIVEL_899_Report
Lab2_Fri_AM_KENNETH WONG CUN WI_742_Archive	Lab2_Fri_AM_KENNETH WONG CUN WI_742_Report
Lab2_Mon_AM_KEVIN LOKE WEI YI_957_Archive	Lab2_Mon_AM_KEVIN LOKE WEI YI_957_Report
Lab2_Fri_AM_KHOO JUNHAO_052_Archive	Lab2_Fri_AM_KHOO JUNHAO_052_Report
Lab2_Mon_AM_KOH LI TIAN_429_Archive	Lab2_Mon_AM_KOH LI TIAN_429_Report
Lab2_Fri_AM_KOTHARI SMEET RONAK_661_Archive	Lab2_Fri_AM_KOTHARI SMEET RONAK_661_Report
Lab2_Fri_AM_KUAH JUN HONG BRYAN_384_Archive	Lab2_Fri_AM_KUAH JUN HONG BRYAN_384_Report
Lab2_Mon_AM_LABELLE LEE_619_Archive	Lab2_Mon_AM_LABELLE LEE_619_Report
Lab2_Fri_AM_LAM ZHEN LEI ETHAN_558_Archive	Lab2_Fri_AM_LAM ZHEN LEI ETHAN_558_Report
Lab2_Mon_PM_LAU EN XIN GRACE_497_Archive	Lab2_Mon_PM_LAU EN XIN GRACE_497_Report
Lab2_Fri_AM_LEE KAH HOE BRIAN_300_Archive	Lab2_Fri_AM_LEE KAH HOE BRIAN_300_Report
Lab2_Mon_PM_LEE KUAN YI_201_Archive	Lab2_Mon_PM_LEE KUAN YI_201_Report
Lab2_Mon_PM_LEONARD LIM TZE YANG_460_Archive	Lab2_Mon_PM_LEONARD LIM TZE YANG_460_Report
Lab2_Mon_PM_LI LINYING_166_Archive	Lab2_Mon_PM_LI LINYING_166_Report

Lab2_Fri_AM_LI XIAOYANG_853_Archive	Lab2_Fri_AM_LI XIAOYANG_853_Report
Lab2_Fri_AM_LIM KAI LER ETHAN_939_Archive	Lab2_Fri_AM_LIM KAI LER ETHAN_939_Report
Lab2_Mon_PM_LIM SWEE HOW GABRIEL_173_Archive	Lab2_Mon_PM_LIM SWEE HOW GABRIEL_173_Report
Lab2_Mon_AM_LIM ZE EN MATTHIAS_943_Archive	Lab2_Mon_AM_LIM ZE EN MATTHIAS_943_Report
Lab2_Mon_PM_LIU LEKUAN_703_Archive	Lab2_Mon_PM_LIU LEKUAN_703_Report
Lab2_Fri_AM_LIU YIHAN_493_Archive	Lab2_Fri_AM_LIU YIHAN_493_Report
Lab2_Mon_AM_LOH HAN XIANG_229_Archive	Lab2_Mon_AM_LOH HAN XIANG_229_Report
Lab2_Fri_AM_LOU YU_962_Archive	Lab2_Fri_AM_LOU YU_962_Report
Lab2_Mon_AM_LOUIS AGARA PERIN_320_Archive	Lab2_Mon_AM_LOUIS AGARA PERIN_320_Report
Lab2_Mon_AM_LOW ZEN WEI_635_Archive	Lab2_Mon_AM_LOW ZEN WEI_635_Report
Lab2_Mon_AM_LU QIANXI_033_Archive	Lab2_Mon_AM_LU QIANXI_033_Report
Lab2_Mon_PM_LUO HONGXUN_391_Archive	Lab2_Mon_PM_LUO HONGXUN_391_Report
Lab2_Fri_AM_MAHESH PURAV_679_Archive	Lab2_Fri_AM_MAHESH PURAV_679_Report
Lab2_Mon_PM_MANU DAGUR_861_Archive	Lab2_Mon_PM_MANU DAGUR_861_Report
Lab2_Mon_PM_MAO XIAOHAN_110_Archive	Lab2_Mon_PM_MAO XIAOHAN_110_Report
Lab2_Fri_AM_MARK NG JIAN XIONG_883_Archive	Lab2_Fri_AM_MARK NG JIAN XIONG_883_Report
Lab2_Mon_AM_MATHEW SAAYUJ ION_282_Archive	Lab2_Mon_AM_MATHEW SAAYUJ ION_282_Report
Lab2_Fri_AM_MICHAEL SHYAM WILFRED DAV_218_Archive	Lab2_Fri_AM_MICHAEL SHYAM WILFRED DAV_218_Report
Lab2_Mon_AM_MO HANQI_531_Archive	Lab2_Mon_AM_MO HANQI_531_Report
Lab2_Mon_AM_MOHAMED FARAS SO FARIDUL_806_Archive	Lab2_Mon_AM_MOHAMED FARAS SO FARIDUL_806_Report
Lab2_Fri_AM_MUHAMMAD AKMAL HANIS BIN _123_Archive	Lab2_Fri_AM_MUHAMMAD AKMAL HANIS BIN _123_Report
Lab2_Mon_PM_NAILA FAIQAH BINTE MUHAMM_406_Archive	Lab2_Mon_PM_NAILA FAIQAH BINTE MUHAMM_406_Report
Lab2_Mon_AM_NAVANEETHAN SANJAI_231_Archive	Lab2_Mon_AM_NAVANEETHAN SANJAI_231_Report
Lab2_Mon_AM_NEERAJ VENGADESSAN_959_Archive	Lab2_Mon_AM_NEERAJ VENGADESSAN_959_Report
Lab2_Mon_AM_NI SHI YONG_596_Archive	Lab2_Mon_AM_NI SHI YONG_596_Report
Lab2_Mon_PM_NICHOLAS LAU HONGYI_324_Archive	Lab2_Mon_PM_NICHOLAS LAU HONGYI_324_Report
Lab2_Mon_PM_NOCHUR SIVANSH_332_Archive	Lab2_Mon_PM_NOCHUR SIVANSH_332_Report
Lab2_Mon_PM_ONG CHONG YAO_901_Archive	Lab2_Mon_PM_ONG CHONG YAO_901_Report
Lab2_Mon_AM_ONG XIANG KAI_232_Archive	Lab2_Mon_AM_ONG XIANG KAI_232_Report
Lab2_Fri_AM_PANG ANG SHENG ASHER_237_Archive	Lab2_Fri_AM_PANG ANG SHENG ASHER_237_Report
Lab2_Mon_PM_PRANAV JANAKIRAMAN_346_Archive	Lab2_Mon_PM_PRANAV JANAKIRAMAN_346_Report
Lab2_Mon_AM_PREMIL ROSHAN_805_Archive	Lab2_Mon_AM_PREMIL ROSHAN_805_Report
Lab2_Fri_AM_PRERANA RAVI SHANKAR_092_Archive	Lab2_Fri_AM_PRERANA RAVI SHANKAR_092_Report
Lab2_Mon_PM_RAJAN PRAVEEN_146_Archive	Lab2_Mon_PM_RAJAN PRAVEEN_146_Report
Lab2_Mon_PM_RAJARAM SUSHMIITHAA_309_Archive	Lab2_Mon_PM_RAJARAM SUSHMIITHAA_309_Report
Lab2_Mon_PM_RAJESH KUMAR ASWIN_713_Archive	Lab2_Mon_PM_RAJESH KUMAR ASWIN_713_Report
Lab2_Mon_PM_REHAAN MAHMOOD_719_Archive	Lab2_Mon_PM_REHAAN MAHMOOD_719_Report
Lab2_Fri_AM_RISHABH RAMPRASAD SHENOY_597_Archive	Lab2_Fri_AM_RISHABH RAMPRASAD SHENOY_597_Report
Lab2_Mon_AM_ROHAN H_155_Archive	Lab2_Mon_AM_ROHAN H_155_Report
Lab2_Mon_AM_ROSHAN ALAGAR PREMKUMAR_245_Archive	Lab2_Mon_AM_ROSHAN ALAGAR PREMKUMAR_245_Report
Lab2_Fri_AM_RUSSELL NG JUN HENG_204_Archive	Lab2_Fri_AM_RUSSELL NG JUN HENG_204_Report
Lab2_Mon_PM_RYAN KOH JUN HAO_601_Archive	Lab2_Mon_PM_RYAN KOH JUN HAO_601_Report
Lab2_Mon_PM_RYAN PANG ZE XI_453_Archive	Lab2_Mon_PM_RYAN PANG ZE XI_453_Report
Lab2_Mon_PM_RYAN TAN RONG CHANG_406_Archive	Lab2_Mon_PM_RYAN TAN RONG CHANG_406_Report
Lab2_Mon_AM_SAMUEL LEE WEN JIN_232_Archive	Lab2_Mon_AM_SAMUEL LEE WEN JIN_232_Report
Lab2_Mon_PM_SANGHI NISHCHAY_666_Archive	Lab2_Mon_PM_SANGHI NISHCHAY_666_Report
Lab2_Mon_AM_SARAVANAN RAJESHWARI AKSH_513_Archive	Lab2_Mon_AM_SARAVANAN RAJESHWARI AKSH_513_Report
Lab2_Mon_PM_SEAN LEE WEI SHU_252_Archive	Lab2_Mon_PM_SEAN LEE WEI SHU_252_Report
Lab2_Fri_AM_SEAN TAN KAI JIE_767_Archive	Lab2_Fri_AM_SEAN TAN KAI JIE_767_Report
Lab2_Fri_AM_SEAN TAN LIYU_776_Archive	Lab2_Fri_AM_SEAN TAN LIYU_776_Report
Lab2_Mon_PM_SEOW JACKIE JAVIER_092_Archive	Lab2_Mon_PM_SEOW JACKIE JAVIER_092_Report
Lab2_Mon_PM_SHAH JAINAM AMIT_339_Archive	Lab2_Mon_PM_SHAH JAINAM AMIT_339_Report
Lab2_Fri_AM_SHAH KUSHAL HITESH_473_Archive	Lab2_Fri_AM_SHAH KUSHAL HITESH_473_Report

Lab2_Mon_PM_SHAUN TAN SHU REN_075_Archive	Lab2_Mon_PM_SHAUN TAN SHU REN_075_Report
Lab2_Fri_AM_SHENNON TAY_016_Archive	Lab2_Fri_AM_SHENNON TAY_016_Report
Lab2_Mon_AM_SHYAMAL VARNAN VENKATARAM_949_Archive	Lab2_Mon_AM_SHYAMAL VARNAN VENKATARAM_949_Report
Lab2_Mon_PM_SIM MENG TECK_476_Archive	Lab2_Mon_PM_SIM MENG TECK_476_Report
Lab2_Mon_PM_SINGH SIDDHANT NARAYAN_752_Archive	Lab2_Mon_PM_SINGH SIDDHANT NARAYAN_752_Report
Lab2_Mon_AM_SRINIVASAN RANGANATHAN_330_Archive	Lab2_Mon_AM_SRINIVASAN RANGANATHAN_330_Report
Lab2_Mon_AM_SRIVASTAVA HARSHIT_749_Archive	Lab2_Mon_AM_SRIVASTAVA HARSHIT_749_Report
Lab2_Mon_PM_SUWEI SHRESTHA_946_Archive	Lab2_Mon_PM_SUWEI SHRESTHA_946_Report
Lab2_Mon_PM_TAN CHUN LIANG_676_Archive	Lab2_Mon_PM_TAN CHUN LIANG_676_Report
Lab2_Fri_AM_TAN KAI CONG_476_Archive	Lab2_Fri_AM_TAN KAI CONG_476_Report
Lab2_Mon_AM_TAN PANG_905_Archive	Lab2_Mon_AM_TAN PANG_905_Report
Lab2_Mon_AM_TAN WEI HENG_981_Archive	Lab2_Mon_AM_TAN WEI HENG_981_Report
Lab2_Mon_AM_TAN YAN HAO MALCOLM_363_Archive	Lab2_Mon_AM_TAN YAN HAO MALCOLM_363_Report
Lab2_Mon_PM_TAN YUE YANG_427_Archive	Lab2_Mon_PM_TAN YUE YANG_427_Report
Lab2_Fri_AM_TANPRASERTKUL PRAN_173_Archive	Lab2_Fri_AM_TANPRASERTKUL PRAN_173_Report
Lab2_Mon_PM_TAO ENZE_746_Archive	Lab2_Mon_PM_TAO ENZE_746_Report
Lab2_Fri_AM_TEO YU XIANG ALOYSIUS_442_Archive	Lab2_Fri_AM_TEO YU XIANG ALOYSIUS_442_Report
Lab2_Mon_PM_THEN CHIN KIAT_534_Archive	Lab2_Mon_PM_THEN CHIN KIAT_534_Report
Lab2_Fri_AM_THIA YANG HAN_615_Archive	Lab2_Fri_AM_THIA YANG HAN_615_Report
Lab2_Mon_AM_TIRODKAR OM MILIND_212_Archive	Lab2_Mon_AM_TIRODKAR OM MILIND_212_Report
Lab2_Fri_AM_TJHIN BRIAN_808_Archive	Lab2_Fri_AM_TJHIN BRIAN_808_Report
Lab2_Fri_AM_TOH EE SEN IZEN_600_Archive	Lab2_Fri_AM_TOH EE SEN IZEN_600_Report
Lab2_Mon_PM_TOH YI WEI_295_Archive	Lab2_Mon_PM_TOH YI WEI_295_Report
Lab2_Mon_AM_TONG KAR YUE ABIGAIL_126_Archive	Lab2_Mon_AM_TONG KAR YUE ABIGAIL_126_Report
Lab2_Mon_PM_VANSH PURI_003_Archive	Lab2_Mon_PM_VANSH PURI_003_Report
Lab2_Mon_AM_VENKATESH KSHEERABTHI NAT_380_Archive	Lab2_Mon_AM_VENKATESH KSHEERABTHI NAT_380_Report
Lab2_Mon_AM_VIHAAN_665_Archive	Lab2_Mon_AM_VIHAAN_665_Report
Lab2_Fri_AM_VINAY VANJRE RAVI_336_Archive	Lab2_Fri_AM_VINAY VANJRE RAVI_336_Report
Lab2_Fri_AM_WAI YAN_450_Archive	Lab2_Fri_AM_WAI YAN_450_Report
Lab2_Fri_AM_WANG CHUHAO_566_Archive	Lab2_Fri_AM_WANG CHUHAO_566_Report
Lab2_Mon_AM_WANG JIAWEI_498_Archive	Lab2_Mon_AM_WANG JIAWEI_498_Report
Lab2_Fri_AM_WANG PENGJIN_104_Archive	Lab2_Fri_AM_WANG PENGJIN_104_Report
Lab2_Mon_PM_WANG ZAIXI_940_Archive	Lab2_Mon_PM_WANG ZAIXI_940_Report
Lab2_Mon_PM_WEN JUN YU_517_Archive	Lab2_Mon_PM_WEN JUN YU_517_Report
Lab2_Fri_AM_WENG XIAN YANG_191_Archive	Lab2_Fri_AM_WENG XIAN YANG_191_Report
Lab2_Mon_PM_WESLEY LOW_090_Archive	Lab2_Mon_PM_WESLEY LOW_090_Report
Lab2_Mon_PM_WONG EE SHAWN_244_Archive	Lab2_Mon_PM_WONG EE SHAWN_244_Report
Lab2_Mon_AM_WU ZI EN ELLIOT JOHN_902_Archive	Lab2_Mon_AM_WU ZI EN ELLIOT JOHN_902_Report
Lab2_Mon_PM_XU HUANGHAO_370_Archive	Lab2_Mon_PM_XU HUANGHAO_370_Report
Lab2_Fri_AM_XU ZIHAO_485_Archive	Lab2_Fri_AM_XU ZIHAO_485_Report
Lab2_Fri_AM_XYLON CHAN YI CHONG_514_Archive	Lab2_Fri_AM_XYLON CHAN YI CHONG_514_Report
Lab2_Mon_PM_YADAV ARYAN SUNILKUMAR_694_Archive	Lab2_Mon_PM_YADAV ARYAN SUNILKUMAR_694_Report
Lab2_Mon_PM_YAN XIANGYU_416_Archive	Lab2_Mon_PM_YAN XIANGYU_416_Report
Lab2_Mon_PM_YAO XIANG_192_Archive	Lab2_Mon_PM_YAO XIANG_192_Report
Lab2_Mon_PM_YAP JIT EN FAITH_368_Archive	Lab2_Mon_PM_YAP JIT EN FAITH_368_Report
Lab2_Mon_AM_YEE JIA JIE_896_Archive	Lab2_Mon_AM_YEE JIA JIE_896_Report
Lab2_Mon_PM_YEO CHEN XIAN_213_Archive	Lab2_Mon_PM_YEO CHEN XIAN_213_Report
Lab2_Fri_AM_YEO SI ZHAO_884_Archive	Lab2_Fri_AM_YEO SI ZHAO_884_Report
Lab2_Fri_AM_YEO TECK IAN BRYAN_832_Archive	Lab2_Fri_AM_YEO TECK IAN BRYAN_832_Report
Lab2_Mon_AM_YEO YEE CHING_332_Archive	Lab2_Mon_AM_YEO YEE CHING_332_Report
Lab2_Mon_PM_YEOH SOO LEONG_125_Archive	Lab2_Mon_PM_YEOH SOO LEONG_125_Report
Lab2_Mon_AM_YEUNG KEITH_484_Archive	Lab2_Mon_AM_YEUNG KEITH_484_Report
Lab2_Mon_PM_YI YANG_914_Archive	Lab2_Mon_PM_YI YANG_914_Report

Lab2_Fri_AM_ZHANG YIZE_948_Archive	Lab2_Fri_AM_ZHANG YIZE_948_Report
Lab2_Mon_AM_ZHAO ZEYU_093_Archive	Lab2_Mon_AM_ZHAO ZEYU_093_Report
Lab2_Fri_AM_ZHENG HUIJIE_077_Archive	Lab2_Fri_AM_ZHENG HUIJIE_077_Report
Lab2_Fri_AM_ZHENG KAIWEN_674_Archive	Lab2_Fri_AM_ZHENG KAIWEN_674_Report
Lab2_Fri_AM_ZHU YICHENG_485_Archive	Lab2_Fri_AM_ZHU YICHENG_485_Report

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FINAL CHECKLIST FOR ASSIGNMENT 2:

Grading is done only once. Re-grading due to not meeting the checklist below are not accepted.

- ☐ I have used the **exact and correct numbers** from my student matriculation number for the assignment.
- ☐ I have named the submitted archive, and pdf report, **according to the given template**.
- ☐ The submitted archive is **less than 5 MB** (Delete ".sim" folder if more than 5 MB. Penalty of up to 10% apply if ≥5 MB).
- ☐ I confirm that the two uploaded **submissions (archive, and report) are the correct / latest versions**.
- ☐ I have **downloaded both (archive, and report) submissions** and confirmed that they were properly uploaded to canvas.
- ☐ I confirm that the **grader need not "Generate bitstream"**, as the bitstream is already there during "Program Device".
- ☐ I have carefully verified the bitstream in my **CANVAS submission**, and it works exactly as I expected.