RAS IP Block Generation and Integration Guide

IP Generation

The RAS IP block generation is integrated in HRDA.

Step 1, generate a SystemRDL file for RAS using hrda template.

```
# generate a SystemRDL template for RAS,
# you just need to specify the record number of each node
# e.g. --ras_record_list 1 2 3 for 3 nodes with 1, 2, 3 records respectively
hrda template -rdl --ras_template --ras_record_list <record-number-list> -n
<template-name>
```

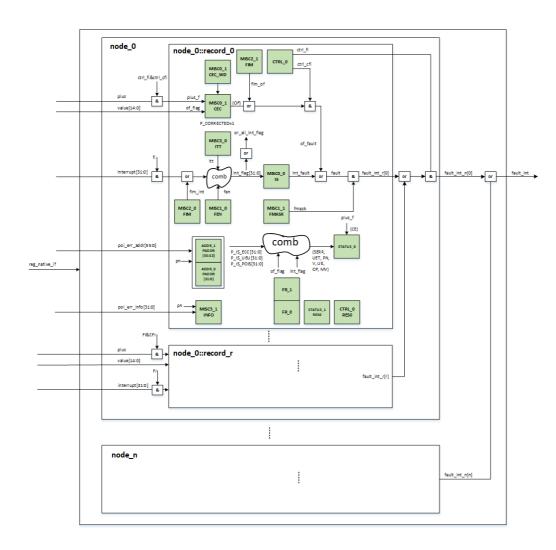
In the generated template SystemRDL file, you can add implementation-specified description to nodes, records and registers based on your own usage.

Step 2, generate Verilog RTL using hrda generate.

```
# generate RTL using the template
hrda generate -f <template-name>.rdl -grtl -gdir <output-directory>
```

Architecture

All nodes and records are in one regslv module as shown below.



- Description:

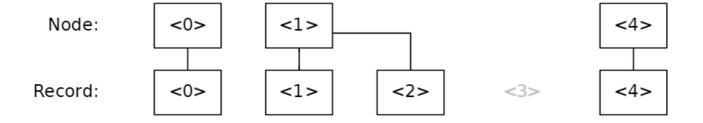
 P_ED[1:0]: if this record is the first record of a node, then set P_ED[1:0] = 2'b10; otherwise set P_ED[1:0] = 2'b00; CTRL is exist only in the first record owned by
- the node; otherwise CTRL is RESO;

 P_IS_ECC[31:0]: 1 means it is ecc error;

 P_IS_UEU[31:0]: 1 means it is unrecover
- error; P_IS_POIS[31:0]: 1 means it is poison error
- P_B_POIS[31:0]: In means it is positive which comes from external; in one record, there are 32 input errors and 1 corrected error with a counter; SERR: the priority of errors are ECC>Implementation_defined_error>poison>corrected_error; SERR will be overwrited by higher priority. higher priority.
- UET: only support UEU and UER, the priority of UEU is higher than UER, so UEU could overwrite UER.

- when poison error happen, set PN=1
 when uncorrected error happen, set UE=1
 when overflow error happen, set OF=1
 SERR, UET, PN, V, UE, OF, MV can be update by hardware when fault=1
- set CE=1 when plus f=1
- set Ct=1 when plus]=1
 the priority of software is higher than
 hardware
 STATUS_0, MISCO_0, MISCO_1, ADDR_0,
 ADDR_1 and MISC3_1 form a snapshot group.
 Accessing STATUS_0 will trigger a snapshot.

Additionally, the record ID does not start from 0 in a new node but is given a global ID in the RAS IP block as shown below.



There are 1 corrected error counter and 32 uncorrected error interrupt for each record. See RAS IP block specification for more details.

Port Definition

reg_native_if

register native interface connecting to the upstream regdisp module.

<node_name>_<record_name>__plus

input, 1 bit to indicate that the corrected error counter should be incremented in a record.

<node_name>_<record_name>__plus_value

input, 15 bits to indicate the value to be added to the corrected error counter in a record.

• <node_name>_<record_name>__interrupt

input, 32-bit input uncorrected error interrupt signals for each record.

fault_int

output, 1-bit fault interrupt signal for the whole RAS IP block.

Parameterization

Each record has a set of parameters to be configured by user.

<node_name>_<record_name>_P_IS_ECC

32 bit, with each bit indicating whether the corresponding <node_name>_<record_name>__interrupt signal is 2-bit uncorrected ECC error or not.

• <node_name>_<record_name>_P_IS_UEU

32 bit, with each bit indicating whether the corresponding <node_name>_<record_name>__interrupt signal is unrecoverable error or not.

<node_name>_<record_name>_P_IS_POIS

32 bit, with each bit indicating whether the corresponding <node_name>_<record_name>__interrupt signal is poison error or not.

Users can only set one of the three parameters to 1 in the same bit position for each record.

If neither of P_IS_ECC, P_IS_UEU and P_IS_POIS is set in the same bit position in a record, the corresponding <node_name>_<record_name>__interrupt signal is treated as IMPLEMENTATION DEFINED.

Note:

- 1. IMPLEMENTATION DEFINED error will be treated as uncorrected and recoverable error (UER).
- 2. Poison error is a special type of uncorrected error.