200 LEVEL PAST QUES

DEPARTMENT OF COMPUTER SCIENCE

AHMADU BELLO UNIVERSITY, ZARIA, NIGERIA

FIRST SEMESTER EXAMINATION FOR 2016/2017 SESSION

COURSE CODE: COSC303 COURSE TITLE: COMPUTER ARCHITECTURE

INSTRUCTION: ATTEMPT ANY FOUR QUESTIONS. TIME ALLOWED: 2HOURS

1.

a. Explain radix conversion algorithm and use it to convert the number 67.575 into binary

b. Provide a brief discussion on each of the following:

i. Historical background for the development of computer systems, starting from the first recorded attempt to build a computer, the Z1, in 1938, ending up with the IBM701.

ii. The technological development of computers.

2.

a.

i. Briefly discuss simple execution cycle of a CPU

ii. Give a brief explanation of the sections of CPU

b. Consider a machine A with the execution of 100 percent instructions for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200MHz.

MHz Instruction category	Percentage of occurrence	No. of cycles per instruction	No of instructions in millions
ALU	38	1	8
Load & store	15	3	4
Branch	42	4	2
Others	5	5	4

i. Compute the overall CPI
ii. What is the MPIS rating?
iii. Calculate the CPU time.

3.

a.

i. With the aid of suitable diagram explain Booth's Algorithm

ii. Give the steps required to represent a number in 2's complement and represent the number (-22) in 2's complement

b. With the aid of Booth algorithm multiply 6 by 2

4.

a. Give detail explanations of the main different organizations use in cache memory.

b. Consider the case of a main memory consisting of 4K blocks, a cache memory consisting of 128 blocks, and a block size of 16 words dividing the main memory and the cache according to the direct-mapped cache technique. There are a total of 32 main memory blocks that map to a given cache block. For example, main memory blocks 0, 128, 256, 384 . . . 3968 map to cache block 0. We therefore call the direct-mapping technique a many-to-one mapping technique. According to the direct-mapping technique the MMU interprets the address issued by the processor by dividing the address into three fields namely: word field, Block field and tag field. Compute the:

i. Word field
ii. Block field
iii. Tag field
iv. The total number of fields in the main address

5.

a.

i. Briefly explain shared I/O arrangement and give it's advantage and disadvantage

ii. Discuss the protocol steps in programmed I/O.

b.

i. Give summarized steps of DMA operation and write short note on bus arbitration

ii. Explain synchronous and asynchronous bus

6.

a.

i. Discuss the term pipelining.

ii. What are the 4 steps in pipelining?

iii. Explain pipeline stall.

iv. List and explain 4 methods used to reduce pipeline stall do to instruction dependency.

b.

i. Explain ways by which the length of the microinstruction could be determine in a microprogrammed control.

ii. Write short note on Horizontal Versus Vertical Microinstructions.