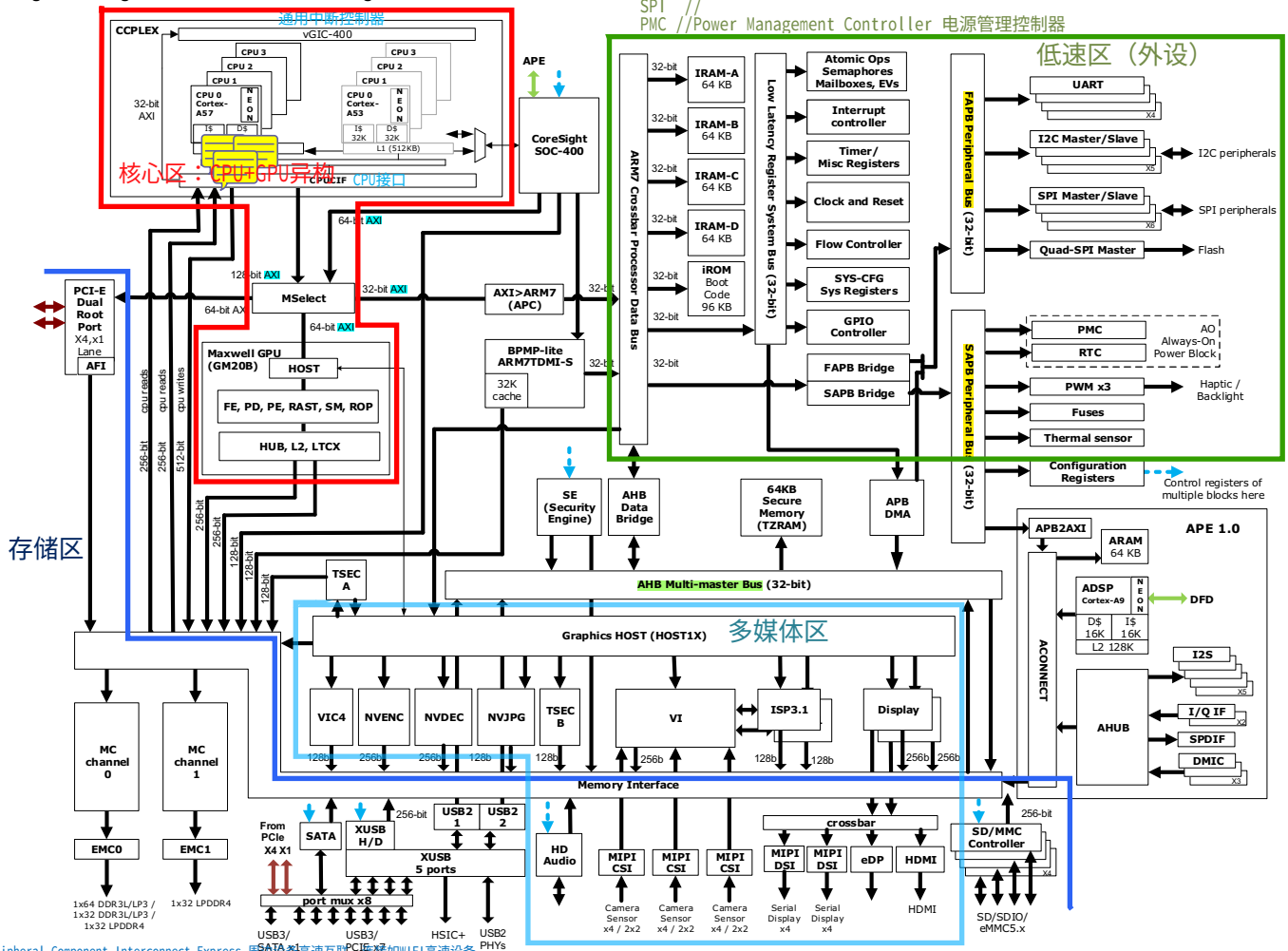
关于总线：AXI(Advanced eXtensible Interface)最快
AHB(Advanced High-performance Bus)次之
APB(Advanced Peripheral Bus)最慢
从下图不难看出，AXI用于与CPU的数据/指令传输
APB用于与外设通信

IRAM //片内存储器
IROM //片内只读存器
Semaphore //信号量 -> 多核互斥
ATOMIC //原子操作 -> 同步
Clock //时钟
Flow Control //流控 -> 多核流程排序
GPIO //General Purpose Input/Output 通用输入输出
RTC //Real Time Clock 实时时钟
PWM //Pulse Width Modulation 脉冲宽度调制
UART //Universal Asynchronous Receiver/Transmitter 通用异步收发传输器 -> 串口调试
I2C //
SPI //
PMC //Power Management Controller 电源管理控制器

Figure 1: Tegra X1 Processor Block Diagram



PCIE //Peripheral Component Interconnect Express 局部设备高速互联，连接如WIFI高速设备
EMC //External Memory Controller 接外部存储器（如内存）的接口
MC //Memory Controller 内存控制器模块，处理来自内部客户端的请求并，进行仲裁其中分配内存带宽。
DDR //Double Data Rate SDRAM 双倍速率同步动态随机存储器，即内存
LPDDR // Low Power Double Data Rate SDRAM，低功耗双倍数据速率内存
SATA //Serial Advanced Technology Attachment 接硬盘的常用接口

1.3 Memory Controller and Internal Bus Architecture

The Tegra X1 mobile processor has a highly optimized 64-bit memory controller, supporting low latency access for the CPU, optimized high bandwidth access for the graphics and video devices, and controlled latency for real time devices such as display.

There is a three-level hierarchy of memory clients:

1. Memory controller clients: The memory controller directly arbitrates between various requesters using a complex algorithm optimizing DRAM efficiency. The highest bandwidth clients all fall into this class, and they communicate directly with the memory controller using a proprietary high-speed bus.
2. AHB devices: These generally have a built-in DMA engine, and share a single memory client using the AHB bus protocol.
3. APB devices: All APB devices are slaves, and are serviced by a shared multi-channel APB DMA controller which is also an APB device.

Special provisions are made for the CPU to bypass parts of the memory controller arbitration to help achieve a lower latency.

1.4 Reading Register Tables

Every register table has an address line followed by a table containing the bit descriptions for that register. The address line contains: