

RK818

Power Management System Specifications

PRELIMINARY CONFIDENTIAL

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Revision History

Date	Version	Remarks
2013-11-19	0.1	Initial Specifications
2014-03-15	0.2	Register map added
2014-07-18	0.3	 Added ordering information Added Operational Description







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1 DESCRIPTION

The RK818 is a complex power-management integrated circuit (PMIC) for multi-core system applications powered by a Li-ion or a Li-ion polymer battery cell, or by a 5V input either from an USB port or from an adaptor. The RK818 can provide a complete power management solution with very few external components.

The RK818 provides four configurable synchronous step-down converters and one synchronous step-up converter with current capability up to 4A and 2.5A, respectively. The device also contains 9 LDO regulators, one linear switch, one switch-mode charger, a battery fuel gauge, and the power path management function. Power-up/power-down controller is configurable and can support any customized power-up/power-down sequences (OTP based). A real-time clock (RTC) is also integrated to provide a 32-kHz output buffer, and real time function. The RK818 supports 32-kHz clock generation based on a crystal oscillator.

The switch-mode charger, together with the power path controller integrated in the RK818, allows supplying power to the loads while it is charging the battery. The charger provides functions such as input current limiting, trickle current charging, constant current (CC)/constant voltage (CV) charging, charging termination, charging over time protection, etc. All these functions can be conveniently configured through the I²C digital interface. The input current limit can be set to maximum 3A to accommodate a power adaptor as the input supply. When an input current limiting is triggered, the power path controller will distribute the input power in a way that the loads have the higher priority than the battery to take the input power. The difference between the input and output power will be used to charge the battery. In a case that the output power required by the loads exceeds the input power, the power path controller will automatically turn on the battery switch so that the battery can supply extra power to the loads together with the input supply. A "battery fuel gauge" is also integrated in the RK818. Using the proprietary algorithms and the sensed battery current and voltage, the gauge can accurately calculate the battery capacity based on the charging/discharging characteristics of the battery preloaded in the system. The gauge then sends the battery capacity information to the processor through the I²C interface. Other functions that the charger provides includes tiny current charging for an over discharged battery, or so called "dead battery", battery temperature monitoring, safe charging timer and



over temperature shut down.

The RK818 can dynamically adjust the output voltage of each DC-DC converter, as required by the processor based on the processor's operation status so as to maximize the system efficiency. The output voltages of most channels can be configured through the I²C interface. The inputs of all channels have soft start function, which greatly reduces the inrush current at the startup. The frequency compensations of all the control loops are implemented internally to eliminate external compensation components.

The 2MHz switching frequency allows small size inductors to be used for both buck and boost converters. Also, as all the power switches are integrated on chip, no external power switches and Schottky diodes are needed, which reduces the system cost significantly.

The RK818 is available in a QFN68 7.0 mm x 7.0 mm package, with a 0.35-mm pin pitch.





2 FEATURES

- Input range: 3.8V 6V for USB input; 2.7V 4.5V for BAT input
- Switch mode Li-ion battery charger providing charging current up to 3A.
- Power path controller with 5A current path.
- Accurate battery fuel gauge.
- Real time clock (RTC)
- Low standby current of less than 40uA (at 32KHz clock frequency)
- 2MHz switching frequency for the buck converters
- 1MHz switching frequency for the boost converter
- Fast transient response due to the current mode architecture
- Internal frequency compensation and soft start
- Programmable output voltage and power up/down sequence through I2C interface
- Proprietary circuit architecture achieving high efficiency
- Internal discharge path in off state for BUCs and LDOs
- Power channels:
 - Ch1: Synchronous buck converter, 4A max
 - Ch 2: Synchronous buck converter, 4A max
 - Ch 3: Synchronous buck converter, 2.5A max
 - Ch 4: Synchronous buck converter, 2.5A max
 - Ch5: Synchronous boost converter, 2.5A max
 - Ch6-7, Ch9 and Ch11: LDOs, 150mA max
 - Ch8: Low noise, high PSRR LDO ,100mA max
 - Ch10, 12,14: LDOs, 300mA max
 - Ch13: LDO, 400mA max
 - Ch15: Low R_{dson} switch,0.15ohm (Vgs=3V)
 - Ch16: HDMI5V switch, 80mA max
 - Ch17: OTG switch, 800mA max
- Fixed and programmable power up/down sequences
- Package: 7mmx7mm QFN68



3 BLOCK DIAGRAM

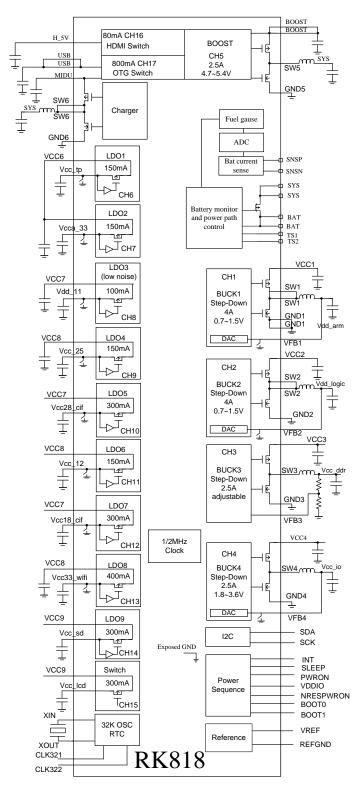


Figure 3-1 System Block Diagram



4 TYPICAL APPLICATION

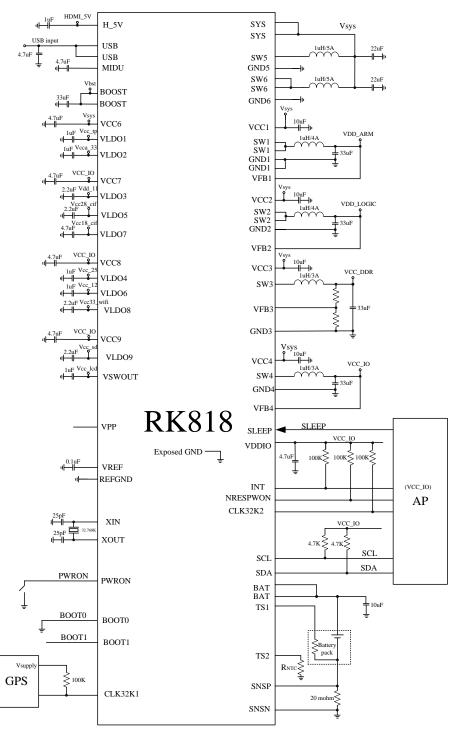


Figure 4-1 RK818 Typical Application Diagram



5 PIN DESCRIPTION

QFN68 7mm x 7mm, pitch0.35mm

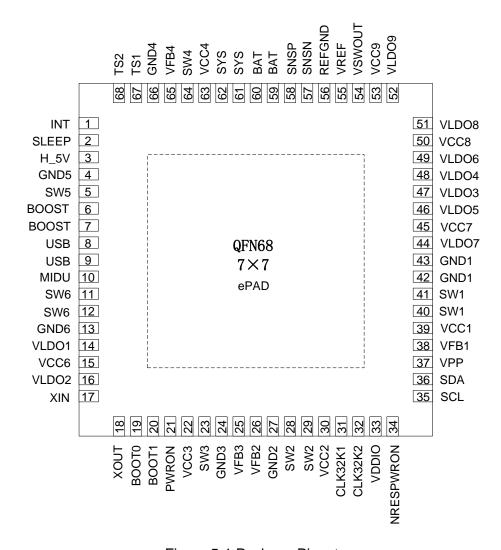


Figure 5-1 Package Pinout

6 PINOUT DEFINITION

Pin No	Pin Name	Pin Description
1	INT	Interrupt request pin. Active low.
2	SLEEP	Input pin for switching state between sleep and non-sleep state.
3	H_5V	5v supply output for HDMI
4	GND5	Power ground

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5	SW5	Switch output
6,7	BOOST	BOOST output
8,9	USB	Power input from USB
10	MIDU	Middle point of USB power supply
11:12	SW6	Switch output
13	GND6	Power ground
14	VLDO1	LDO1 output
15	VCC6	Power supply for LDO
16	VLDO2	LDO2 output
17	XIN	32.768KHz crystal oscillator input
18	XOUT	32.768KHz crystal oscillator output
19	воото	Boot sequence selection, low bit
20	BOOT1	Boot sequence selection, high bit
21	PWRON	Power on or power off enable pin, active low, internal 100K pull high
		to power supply
22	VCC3	Power supply for DCDC3
23	SW3	Switch output of DCDC3
24	GND3	Power ground for DCDC3
25	VFB3	feedback voltage for DCDC3
26	VFB2	DCDC2 output voltage feedback input
27	GND2	Power ground for DCDC2
28,29	SW2	Switch output of DCDC2
30	VCC2	Power supply for DCDC2
31	CLK32K1	32.768K clock1 output, open drain,
32	CLK32K2	32.768K clock2 output, open drain,
33	VDDIO	Power supply for IO
34	NRESPWON	Reset pin after power on, active low
35	SCL	Clock input of I2C
36	SDA	Data input/output of I2C
37	VPP	Power supply for testing, floating in the application
38	VFB1	DCDC1 output voltage feedback input
39	VCC1	Power supply for DCDC1
40:41	SW1	Switch output of DCDC1
42,43	GND1	Power ground for DCDC1
44	VLD07	LDO7 output
45	VCC7	Power supply for LDO
46	VLDO5	LDO5 output



		8 0					
47	VLDO3	LDO3 output					
48	VLDO4	LDO4 output					
49	VLDO6	LDO6 output					
50	VCC8	Power supply for switch					
51	VLDO8	LDO8 output					
52	VLDO9	LDO9 output					
53	VCC9	Power supply for LDO					
54	VSWOUT	Switch output					
55	VREF	Internal reference voltage					
56	REFGND	Reference ground					
57	SNSN	Bat charging and discharging sense current negative pin					
58	SNSP	Bat charging and discharging sense current positive pin					
59,60	BAT	Positive battery terminal					
61:62	SYS	DC-DC regulator output to power the system load and charge the					
		battery					
63	VCC4	Power supply for DCDC4					
64	SW4	Switch output of DCDC4					
65	VFB4	DCDC4 output voltage feedback input					
66	GND4	Power ground for DCDC4					
67	TS1	Thermistor1 input. Connect a thermistor from this pin to ground. The					
		thermistor is usually inside the battery pack.					
68	TS2	Thermistor2 input. Connect a thermistor from this pin to ground.					
		Or it can be used as analog input pin of internal ADC if the control b					
	_	is set to ADC function.					
Exposed	Exposed ground	It must be connected to ground for thermal and electrical					
pad		enhancement.					

Table 1 Pin Descriptions





7 ORDERING INFORMATION

Orderable Device	RoHS status	Package	Package Qty	Device special feature
RK818	RoHS pass	QFN68(7X7)	2600ea/inner box* 6 inner boxes/outer box	NA

8 ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Voltage range on pins USB , MIDU , BOOST , SWx/H_5V	-0.3	6.5	V
Voltage range on pins VCCx, VFBx, VLDOx, VSWOUT, VREF	-0.3	6.5	V
Voltage range on pin CLK32K1:CLK32K2, SLEEP	-0.3	6.5	V
Voltage range on pins XIN,XOUT, BOOT0:BOOT1: PWRON	-0.3	VSYS _{MAX} +0.3	
Voltage range on pins NRESPWRON, INT, SDA, SCL	-0.3	4	V
Storage temperature range, T _S	-40	150	$^{\circ}\mathbb{C}$
Operating temperature range, T _J	-40	125	$^{\circ}\mathbb{C}$
Maximum Soldering Temperature, T _{SOLDER}		300	$^{\circ}\mathbb{C}$

Table 2 Absolute Maximum Ratings

Note 1. Exposure to the conditions exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

9 RECOMMENDED OPERATING CONDITIONS

Parameter	Min	TYP	Max	Units
Voltage range on pins USB	4	5	5.5	V
Voltage range on other pins			5.5	V
Power Dissipation			2.7	W

Table 3 Recommended Operating Conditions



10ELECTRICAL CHARACTERISTICS

Test conditions: V_{USB} =5.0V, T_A = 25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
USBIN						
USB Operating Range	V_{USB}		4	5	6	V
USB Under Voltage Lockout		Rising	3.65	3.8	3.95	V
Threshold		Falling		3.6		V
LIOD DATE TO A LI		Rising		70		mV
USB vs BATT Threshold		Falling		30		mV
		Min Current	60	80	100	mA
11001		Default	400	450	500	mA
USB Input Current Limit	l _{USB}	Max current	2.7	3	3.3	А
		step (from 1A to 3A)		200		mA
Maximum USB and BATT Power on Reset Threshold (Rising)	V _{PORH}				2.2	V
Maximum USB and BATT	V _{PORL}		1.2			V
Power on Reset Threshold (Falling)						
Over Voltage Lock Out Threshold (USB Rising)	V _{TH(OVLO)}		5.7	6.0	6.3	V
Over Voltage Lock Out Hysteresis	V _{HYS}			0.2		V
High-Side PMOS Peak Current Limit		0.5A step, Default=4.5A	4		5.5	А
USB Input Quiescent Current	lUSBquie t	Charger Enable mode			10	mA
		Disabled		3	5	uA
SYS to USB Reverse Current		VSYS=4.2V,USB			2	uA
Blocking		floating			2	uA
CHARGING CONTROLLER						
				4.05		V
				4.1		V
	V	VBAT>VRECH, ICHG ≤		4.15		V
Terminal Battery Voltage	V_{BAT}	IBF		4.2		V
				4.3		V
				4.35		V
	accuracy		-1		1	%



					<u> </u>	
PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Recharge Threshold at V _{BATT}	V_{RECH}			V_{BAT}		V
Troonargo Tinoonola at VBAIT	▼ RECH			-0.15		
Recharge Hysteresis				75		mV
Trickle Charge Threshold	V _{TRICKLE}		2.85	3.0	3.15	V
Trickle Charge Hysteresis				200		mV
Trickle Charge Current	I _{TRICKLE}			10%		Icc
Dead bat Charge Threshold	V_{DEAD}		1.8	2	2.2	V
Dead bat Charge Hysteresis				200		mV
Dead bat Charge Current	I _{DEAD}			40		mA
Termination Charger Current	I _{BF}	50mA Step, default=150mA	100		250	mA
BAT Leakage Current	I _{BATT}	VBAT=4.2V, SYS float, USB float		20	30	uA
Charge current	Icc	0.2A step, default=2A	1		3	Α
Trickle Charge Time		30 minutes step, default=60 minutes	30		210	Min
Total Charge Time		2 hours step,default=6	4		16	Hour
Conversion Efficiency, Constant				84		
voltage stage (Vin=5V,Vbat=4.2V)				04		
Ibat=3A				87		
lbat=2.5A				89		
lbat=2A						
Ibat=1.5A				91		%
lbat=1A				94		
lbat=500mA				93		
lbat=200mA				95		
Conversion Efficiency, Constant				86		
current stage (Vin=5V,Ibat=2A) Vbat=3.6V				87		
Vbat=3.8V				01		%
Vbat=4.0V				88		
Vbat=4.2V				89		
A/D CONVERTER				l	l	<u> </u>
Resolution				12		bits
Input voltage range		Battery voltage	0		4.4	V
input voltage ratige		Current channel	-64		64	mV



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
		TS1/TS2	0		2.2	V
Supply current	Active			0.6		mA
SYS INPUT						
0)/0 D	Vava	A		3.6		V
SYS Regulation Voltage	Vsys	Auto setting		4.4		V
BAT to SYS Resistance		ISYS=200mA, VBAT=4.2V		0.05	0.08	Ω
BAT to SYS Current Limit	IBATLIM	0.5A step,default=5A	3		5	Α
BATT TO GITO GUITOIR EITIIR	·BATEIM	SYS short		200		mA
BAT to SYS Current Limit accuracy		O TO OHOIC	-10	200	10	%
SYS voltage range	V _{SYSINPUT}		2.7		5.45	V
SYS low alarm voltage, if 3.3V	- STORNEUT				0.10	
(2.8V~3.5V programmable, step=100mV)	V_{BLO}		3.25	3.3	3.35	V
SYS under voltage threshold (vin	V _{BUVL}			2.7		V
falling)						
SYS under voltage threshold (vin rising)	V _{BUVH}		2.8	2.9	3.0	V
SYS OK voltage threshold (3.3V~3.6V OTP programmable,	V _{вок}			3.4		V
step=100mV) Stand-by current, V _{DD} =3.6V, device	1			40		^
OFF state 32KHz clock running	I _{Q(STNBY)}			40		uA
THERMAL PROTECTION						
THERMAL TROTEOTION		10 °C step,	85			
Thermal Limit Temperature		default=85 °C			115	°C
Thermal Shutdown		20 °C step, default=140 °C	140		160	°C
OSCILLATOR	L	I	L			
Switching Frequency	f_{SW}		1.8	2	2.2	MHz
CH1:2,3,4(Tj=25℃)						
Switching Frequency,	f _{SW}		0.9	1	1.1	MHz
CH5(Tj=25℃)						
LOGIC INPUT			<u>'</u>		•	
Input LOW-Level Voltage (V _{DDIO})	V _{IL}				0.3xV _{DDIO}	V
Input HIGH-Level Voltage (V _{DDIO})	V _{IH}		0.7xV _{DDIO}			V
LOGIC OUTPUT	•		<u> </u>		-	
LOW-Level Output Voltage, 3.0	V _{OL}				0.4	V



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
mA sink current						
HIGH-Level Output Voltage, 3.0	V _{OH}		V _{DDIO} -0.4			V
mA source current						
NRESPWON pin LOW-Level	V _{OL(NRES)}				0.4	V
Output Voltage, 3.0mA sink current	0=(:::=0)					
CLK32KOUT1 pin LOW-Level	V _{OL(CLKO1)}				0.4	V
Output Voltage, 3.0mA sink current						
CLK32KOUT2 pin LOW-Level	V _{OL(CLKO2)}				0.4	
Output Voltage, 3.0mA sink current						
CLK32KOUT2 pin HIGH-Level	V _{OH(CLKO2)}		V _{DDIO} -0.4			V
Output Voltage, 3.0mA source	,					
current						
Ch1: BUCK DC-DC CONVERTER	R (VDD_ARM)				1
Input supply voltage range	V _{INPUT1}		2.7		5.5	V
Voltage Adjustable Range, 6bit	V _{FB1}	Step=12.5mV	0.7125		1.500	V
Output voltage transition rate						
BUCK1_RATE=00				2		
BUCK1_RATE=01				4		mV/us
BUCK1_RATE=10				6		
BUCK1_RATE=11				10		
Power Good threshold (Vout rising)	V_{PG1}			93		%
Output under voltage lockout(Vout	V_{UV1}			85		%
falling)						
Output over voltage lockout (Vout	V _{OV1}			117		%
rising)						
Preset Voltage, Default(Tj=25℃)	V _{FB1(Default}		1.078	1.100	1.122	V
)					
Preset Voltage,	V _{FB1(Default}		1.067	1.100	1.133	V
Default(-10°C≦T _j ≦+85°C))					
Load Regulation, I _{OUT1} = 200mA to				0.1		%/A
4A						
Line Regulation, VCC1 = 3 to 5.5V,				0.1		%/V
I _{OUT1} = 2A						
Rated output current	I _{MAX1}	Reg90H<1:0>=<11>		4		Α
Switch Current Limit	I _{CL1}	0.4A step, default=3.6A	3.2		4.4	А
Operating Quiescent Current, No	I _{Q1}			70		uA
load, V _{DD} =3.8V						
Minimum Switch Current Limit	I _{CLMIN1}	50mA step,	50		400	mA
		default=150mA				



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PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Minimum ON Time	T _{on1(min)}			45		ns
Soft-start Time	t _{SS1}	Step=400us,	400		800	us
		default=400us				
C _{OUT} Discharge Switch ON	R _{DIS2}			050		- 1
Resistance				250		ohm
Conversion Efficiency						
(Vin=3.8V,Vout=1.1V)						
lout=4A				65		
lout=3.5A				68		
lout=3A				71		
lout=2.5A				75		
lout=2A				79		%
lout=1.5A				83		
lout=1.3A				86		
iout=1 A						
lout=500mA				89		
lout=100 mA				80		
lout=10 mA				81		
Ch2: BUCK DC-DC CONVERTE	ER (VDD_LO	G)				
Input supply voltage range	V _{INPUT2}		2.7		5.5	V
Voltage Adjustable Range, 6bit	V_{FB2}	Step=12.5mV	0.7125		1.500	V
Output voltage transition rate						
BUCK2_RATE=00				2		
BUCK2_RATE=01				4		mV/us
BUCK2_RATE=10				6		
BUCK2_RATE=11				10		
Power Good threshold (Vout rising)	V_{PG2}			93		%
Output under voltage lockout (Vout	V_{UV2}			85		%
falling)						
Output over voltage lockout (Vout	V_{OV2}			117		%
rising)						
Preset Voltage, Default(Tj=25℃)	V _{FB2(Default}		1.078	1.100	1.122	V
Droopt V. II)		4.007	4.400	4.400	
Preset Voltage,	V _{FB2(Default}		1.067	1.100	1.133	V
Default(-10°C \leq T _j \leq +85°C) Load Regulation, I _{OUT2} = 200 mA to)			0.1		%/A
Load Regulation, IOUT2 = 200 IIIA to				0.1	<u> </u>	/o/A



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
4A						
Line Regulation, VCC2 = 3 to 5.5V,				0.1		%/V
$I_{OUT2} = 2A$						
Rated output current	I _{MAX2}	Reg90H<3:2>=<11>		4		А
Switch Current Limit	I _{CL2}	0.4A step, default=3.6A	3.2		4.4	А
Operating Quiescent Current, No load, V _{DD} =3.8V	I _{Q2}			70		uA
Minimun Switch Current Limit	I _{CLMIN2}	50mA step, default=150mA	50		400	mA
Minimum ON Time	T _{on2(min)}			45		ns
Soft-start Time	t _{SS2}	Step=400us, default=400us	400		800	us
C _{OUT} Discharge Switch ON Resistance	R _{DIS2}			250		ohm
Conversion Efficiency						
(Vin=3.8V,Vout=1.1V)						
Iout=4A				62		
lout=3.5A				65		
lout=3A				69		
lout=2.5A				73		
lout=2A				76		%
lout=1.5A				81		
lout=1 A				85		
lout=500mA				89		
lout=100 mA				85		
lout=10 mA				83		
Ch3: BUCK DC-DC CONVERTI	ER (VDD_D	DR)				ı
Input supply voltage range	V _{INPUT3}		2.7		5.5	V
Feedback Voltage, Default($Tj=25^{\circ}C$)	V _{FB3(Default}		0.98	1.00	1.02	V
Feedback Voltage,	V _{FB3(Default}		0.97	1.00	1.03	V
Default(-10°C \leq T _j \leq +85°C))					
Power Good threshold (Vout rising)	V _{PG3}			93		%
Output under voltage lockout (Vout	V _{UV3}			85		%



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
falling)						
Output over voltage lockout (Vout	V _{OV3}			117		%
rising)						
Load Regulation, $I_{OUT3} = 100mA$ to				0.1		%/A
2.5A						
Line Regulation, VCC3 = 3 to 5.5V,				0.1		%/V
$I_{OUT3} = 2A$						
Rated output current	I _{MAX3}	Reg90H<5:4>=<11>		2.5		Α
Switch Current Limit	I _{CL3}	0.5A step, default=2.5A	2		3.5	Α
Operating Quiescent Current, No	I_{Q3}			70		uA
load, V _{DD} =3.8V						
Minimun Switch Current Limit	I _{CLMIN3}	50mA step,	50		400	mA
		default=150mA				
Minimum ON Time	T _{on3(min)}			45		ns
Soft-start Time	t _{SS3}	Step=400us,	400		800	us
		default=400us				
C _{OUT} Discharge Switch ON	R _{DIS3}			250		ohm
Resistance	5.00					
Conversion Efficiency						
(Vin=3.8V,Vout=1.5V)						
lout=2.5A				70		
lout=2A				75		
				00		
lout=1.5A				80		%
lout=1 A				84		
				88		
Iout=500mA				00		
lout=100 mA				84		
				83		
lout=10 mA				00		
Ch4: BUCK DC-DC CONVERTE	R (VDD_10)			1	1
Input supply voltage range	V _{INPUT4}		2.7		5.5	V
Voltage Adjustable Range, 4bit	V_{FB4}	Step=100mV	1.8		3.6	V
Feedback Voltage,	V _{FB4(Default}		2.94	3.00	3.06	V
Default(Tj=25°C))					
Feedback Voltage,	V _{FB4(Default}		-2.91	3.00	3.09	V
Default(-10°C \leq T _j \leq +85°C))					
Power Good threshold (Vout rising)	V_{PG4}			93		%
Output under voltage lockout (Vout	V_{UV4}			85		%



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
falling)						
Output over voltage lockout (Vout	V _{OV4}			117		%
rising)						
Load Regulation, $I_{OUT4} = 100mA$ to				0.1		%/A
2.5A						
Line Regulation, VCC4 = 3 to 5.5V,				0.1		%/V
$I_{OUT4} = 2A$						
Rated output current	I _{MAX4}	Reg90H<7:6>=<11>		2.5		Α
Switch Current Limit	I _{CL4}	0.5A step, default=3A	2.5		4	Α
Operating Quiescent Current, No	I_{Q4}			70		uA
load, V _{DD} =3.8V						
Minimun Switch Current Limit	I _{CLMIN4}	50mA step,	50		400	mA
		default=150mA				
Minimum ON Time	T _{on4(min)}			45		ns
Soft-start Time	t _{SS4}	Step=400us,		400		us
		default=400us				
C _{OUT} Discharge Switch ON	R _{DIS4}			250		Ohm
Resistance	TVDI54			200		Omm
Conversion Efficiency,						
(DCR<50mohm) Vin=3.8V,Vout=3V						%
lout=2.5A				81		
lout=2A				84		
lout=1.5A				87		
lout=1 A				91		
lout=500mA				94		
lout=100mA				94		
				88		
lout=10mA				75		
Ch5: BOOST DC-DC CONVERT	TER (VCC_5	iV)	<u> </u>	l	1	
Input supply voltage range	V _{INPUT5}		2.7		4.4	V
Output Voltage	V_{FB5}	Step=0.1v,default=5v	4.7		5.4	V
Voltage, Default(Tj=25°C)	V _{FB5(Default}		4.90	5.0	5.10	V
)					
Voltage, Default(-10°C \leq T _j \leq +85°C)	V _{FB5(Default}		4.75	5.0	5.25	V
)					
Power Good threshold (Vout rising)	V_{PG5}			90		%
Output under voltage lockout (Vout	V_{UV5}			85		%
falling)						



			1 Wia		1	1
PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Load Regulation, $I_{OUT5} = 100mA$ to				0.2		%/A
2.5A						
Line Regulation, $Vin = 3$ to 4.2V,				0.1		%/V
$I_{OUT5} = 1.5A$						
Rated output current	I _{MAX5}	Reg3A<4:3>=11		2.5		Α
Switch Current Limit	I _{CL5}	0.5A step, default=4.5A	4		5.5	Α
Minimum ON Time	T _{on5(min)}			70		ns
Soft-start Time	t _{SS5}			400		us
C _{OUT} Discharge Switch ON Resistance	R _{DIS5}			250		ohm
Operating Quiescent Current, No load, V _{DD} =3.8V	I_{Q5}			250		uA
Auto switch load current between PWM and PFM	I _{PWM/PFM5}			50		mA
Conversion Efficiency,				80		
(DCR<50mohm) Vin=3.8V,Vout=5V						
lout=2.5A				85		
lout=2A				89		
lout=1.5A						
lout=800mA				93		0/
lout=500mA				94		%
lout=100mA				90		
lout=10mA				71		
Ch6 : LD01 (VCC_TP)						
Input supply voltage range	V _{INPUT6}		2.7	-	5.5	V
V _{OUT} Output Voltage Adjustable	V _{OUT6}		1.8		3.4	V
Range, 4bit(step=100mv)						
V _{OUT} Output Voltage,	V _{OUT6(Defa}		3.234	3.300	3.366	V
Default(Tj=25°C)	ult)					
V _{OUT} Output Voltage, Default(Tj=	V _{OUT6(Defa}		3.201	3.300	3.399	V
-10~85℃)	ult)					
Power Good threshold (Vout rising)	V_{PG6}			93		%
Output under voltage lockout (Vout falling)	V_{UV6}			85		%
V_{OUT} Load Regulation, $I_{OUT} = 1$ mA to 150mA				0.005		%/mA



PARAMETERS							
	PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Power Supply Reject Ratio (f = 10kHz, Voure=3.3V)	V_{OUT} Line Regulation, $V_{IN6} = 3$ to 5V,				0.03		%/V
10kHz, Voure=3.3V)	$I_{OUT6} = 0.1A$						
Output noise (10Hz to 100kHz, Voune=3.3V) OUTNOISE 6 300 uVrms Propout voltage @ 150mA (Voune=3.3V) VbRore 200 mV Rated output current Invasco 150 mA Operating Quiescent Current, No load, Vone=3.8V Icue 250 300 mA Current Limit, VOUT6 = Vourie x 0.95 Icue 250 300 mA O.95 Soft-start Time 400 us Cour Discharge Switch ON Resistance Roise 400 us Ch7: LD02 (VCCA_33) Vour Output Voltage ange Vour Vour Output Voltage Adjustable Range, 4bit(step=100mv) 2.7 5.5 V Vour Output Voltage Adjustable Pelault (Tj=25°C) Vourroutput Voltage, Vourroute Unit Voltage, Vourroute Unit Voltage, Vourroute Unit Voltage, Vourroute Unit Voltage, Unit Voltage Icabout (Vout Tising) 3.234 3.300 3.399 V Power Good threshold (Vout rising) Vnc2 93 % % Output over voltage lockout (Vout failing) Vnc2 93 % Vour Laa Regulation, Vnc7 = 3 to 5V, Iourre = 0.1A	Power Supply Reject Ratio (f =	PSRR6			50		dB
Vourse=3.3V) 6 200 mV Dropout voltage	10kHz, V _{OUT6} =3.3V)						
Dropout voltage @ 150mA Vorone	Output noise (10Hz to 100kHz,	OUT _{NOISE}			300		uVrms
(Vours=3.3V) Rated output current I _{MAXB} 150 mA Operating Quiescent Current, No Iog 28 uA Iogad, Vop=3.8V 250 300 mA Oss 250 300 mA Oss 3	V _{OUT6} =3.3V)	6					
Rated output current	Dropout voltage @ 150mA	V _{DROP6}			200		mV
Operating Quiescent Current, No Ioa	(V _{OUT6} =3.3V)						
Ioad, Vbo=3.8V	Rated output current	I _{MAX6}			150		mA
Current Limit, VOUT6 = VouT6 x Icle 250 300 mA	Operating Quiescent Current, No	I _{Q6}			28		uA
Soft-start Time	load, V _{DD} =3.8V						
Soft-start Time	Current Limit, VOUT6 = V _{OUT6} x	I _{CL6}		250	300		mA
Cour	0.95						
Resistance Roise 400 ohm	Soft-start Time	t _{SS6}			400		us
Resistance Ch7: LD02 (VCCA_33)	C _{OUT} Discharge Switch ON	Б			400		- 1
Input supply voltage range	Resistance	K _{DIS6}			400		onm
Vout	Ch7: LD02(VCCA_33)			•	•		•
Range, 4bit(step=100mv) Vout Output Voltage, output Vout Output Voltage, output Vout Output Voltage, output Default(Tj=-10~85°C) output Power Good threshold (Vout rising) VPG7 Output under voltage lockout (Vout falling) VVV7 Output over voltage lockout (Vout rising) Vov7 Vout Load Regulation, lout = 1mA to 150mA 0.005 Vout Line Regulation, Viny= 3 to 5V, lout7 = 0.1A 0.03 Power Supply Reject Ratio (f = PSRR7 10kHz, Vout7=3.3V) 50 Output noise (10Hz to 100kHz, Vout7=3.3V) OutNoise 7	Input supply voltage range	V _{INPUT7}		2.7		5.5	V
4bit(step=100mv) VouT Output Voltage, VouT7(Defa uit) 3.234 3.300 3.366 V	V _{OUT} Output Voltage Adjustable	V _{OUT7}		1.8		3.4	V
Vout	Range,						
Default(Tj=25°C)	4bit(step=100mv)						
Vout Output Voltage, Default (Tj=-10~85°C) Voltage, uit) 3.201 3.300 3.399 V Power Good threshold (Vout rising) VPG7 93 % Output under voltage lockout (Vout falling) VUV7 85 % Output over voltage lockout (Vout rising) VOV7 125 % Vout Load Regulation, Iout = 1mA to 150mA 0.005 %/mA Vout Line Regulation, VIN7= 3 to 5V, Iout7 = 0.1A 0.03 %/V Power Supply Reject Ratio (f = PSRR7 50 dB 10kHz, VOUT7=3.3V) OUTNOISE 300 uVrms Vout7=3.3V) 7 UVrms 300 UVrms	V _{OUT} Output Voltage,	V _{OUT7(Defa}		3.234	3.300	3.366	V
Default(Tj=-10~85°C) ult) Power Good threshold (Vout rising) V _{PG7} 93 % Output under voltage lockout (Vout falling) V _{UV7} 85 % Output over voltage lockout (Vout rising) V _{OV7} 125 % VouT Load Regulation, I _{OUT} = 1mA to 150mA 0.005 %/mA VouT Line Regulation, V _{IN7} = 3 to 5V, I _{OUT7} = 0.1A 0.03 %/V Power Supply Reject Ratio (f = PSRR7 to 10kHz, V _{OUT7} =3.3V) 50 dB Output noise (10Hz to 100kHz, V _{OUT7} =3.3V) OUT _{NOISE} to 100kHz, V _{OUT7} =3.3V) 300 uVrms	Default(Tj=25℃)	ult)					
Power Good threshold (Vout rising) V _{PG7} 93 %	V _{OUT} Output Voltage,	V _{OUT7(Defa}		3.201	3.300	3.399	V
Output under voltage lockout (Vout falling) Output over voltage lockout (Vout rising) Vout Load Regulation, Iout = 1mA to 150mA Vout Line Regulation, Vint = 3 to 5V, Iout = 0.1A Power Supply Reject Ratio (f = PSRR7	Default(Tj=-10~85°C)	ult)					
falling) Output over voltage lockout (Vout rising) Vov7 125 % Vout Load Regulation, Iout = 1mA to 150mA 0.005 %/mA Vout Line Regulation, VIN7= 3 to 5V, Iout7 = 0.1A 0.03 %/V Power Supply Reject Ratio (f = 10kHz, Vout7=3.3V) PSRR7 50 dB Output noise (10Hz to 100kHz, Vout7=3.3V) OUTNOISE Vout7=3.3V) 300 uVrms	Power Good threshold (Vout rising)	V_{PG7}			93		%
Output over voltage lockout (Vout rising) Vout Load Regulation, Iout = 1mA to 150mA 0.005 %/mA Vout Line Regulation, Vinter = 0.1A 0.003 %/V Power Supply Reject Ratio (f = 10kHz, Voute=3.3V) PSRR7 50 dB Output noise (10Hz to 100kHz, Voute=3.3V) OUTNOISE 300 uVrms	Output under voltage lockout (Vout	V_{UV7}			85		%
rising) Vout Load Regulation, Iout = 1mA to 150mA Vout Line Regulation, Vint = 3 to 5V, Iout = 0.1A Power Supply Reject Ratio (f = PSRR7	falling)						
VOUT Load Regulation, IOUT = 1mA to 150mA 0.005 %/mA VOUT Line Regulation, VINT = 3 to 5V, IOUTT = 0.1A 0.03 %/V Power Supply Reject Ratio (f = PSRR7 10kHz, VOUTT = 3.3V) 50 dB Output noise (10Hz to 100kHz, VOUTT = 3.3V) 0UTNOISE 100kHz, VOUTT = 3.3V) 300 uVrms	Output over voltage lockout (Vout	V _{OV7}			125		%
to 150mA $V_{\text{OUT}} \text{ Line Regulation, } V_{\text{INT}} = 3 \text{ to 5V,} \\ I_{\text{OUT7}} = 0.1A \\ Power Supply Reject Ratio (f = PSRR7) $	rising)						
$V_{\text{OUT}} \text{ Line Regulation, } V_{\text{IN7}} = 3 \text{ to 5V,} \\ I_{\text{OUT7}} = 0.1A \\ \\ \text{Power Supply Reject Ratio (f = PSRR7 } 50 \\ I_{\text{OkHz, }} V_{\text{OUT7}} = 3.3V) \\ \\ \text{Output noise (10Hz to 100kHz, } OUT_{\text{NOISE}} \\ V_{\text{OUT7}} = 3.3V) \\ \\ \text{7} \\ \\ \text{300} \text{uVrms} \\ \\ \text{V}_{\text{OUT7}} = 3.3V) \\ \\ \text{7} \\ \\ \text{10} \text{ and } V_{\text{IN0}} = 0.03 \\ \\ \text{10} \text{ both } V_{\text{IN0}} = 0.03 \\ \\ \text{10} \text{ both } V_{\text{IN0}} = 0.03 \\ \\ \text{10} \text{ both } V_{\text{OUT7}} = 0.03 \\ \\ \text{10} \text{ both } V_{O$	V_{OUT} Load Regulation, $I_{OUT} = 1mA$				0.005		%/mA
Doutroise Dout	to 150mA						
Power Supply Reject Ratio (f = PSRR7 50 dB 10kHz, V _{OUT7} =3.3V) Output noise (10Hz to 100kHz, OUT _{NOISE} 300 uVrms V _{OUT7} =3.3V)	V_{OUT} Line Regulation, V_{IN7} = 3 to 5V,				0.03		%/V
10kHz, V _{OUT7} =3.3V) Output noise (10Hz to 100kHz, V _{OUT7} =3.3V) OUT _{NOISE} 300 uVrms	I _{OUT7} = 0.1A						<u> </u>
Output noise (10Hz to 100kHz, OUT _{NOISE} 300 uVrms V _{OUT7} =3.3V)	Power Supply Reject Ratio (f =	PSRR7			50		dB
V _{OUT7} =3.3V) 7	10kHz, V _{OUT7} =3.3V)						
	Output noise (10Hz to 100kHz,	OUT _{NOISE}			300		uVrms
Dropout voltage @ 150mA V _{DROP7} 200 mV	V _{OUT7} =3.3V)	7					
	Dropout voltage @ 150mA	V _{DROP7}			200		mV



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
(V _{OUT7} =3.3V)						
Operating Quiescent Current, No	I _{Q7}			28		uA
load, V _{DD} =3.8V						
Rated output current	I _{MAX7}			150		mA
Current Limit, VOUT7 = V _{OUT7} x	I _{CL7}		250	300		mA
0.95						
Soft-start Time	t _{SS7}			400		us
C _{OUT} Discharge Switch ON	_					
Resistance	R _{DIS7}			400		Ohm
Ch8 : LD03(VDD_11)	<u> </u>		l .	l	l .	l
Input supply voltage range	V _{INPUT7}		2.7		5.5	V
V _{OUT} Output Voltage Adjustable	V _{OUT8}		0.8		2.5	V
Range,						
4bit (0.8V~2V, step=100mV, 2V~						
2.5V step=500mV)						
V _{OUT} Output Voltage,	V _{OUT8(Defa}		1.078	1.100	1.122	V
Default(Tj=25°C)	ult)					
V _{OUT} Output Voltage,	V _{OUT8}		1.067	1.100	1.133	V
Default(Tj=-10~85℃)	(Default)					
Power Good threshold (Vout rising)	V_{PG8}			93		%
Output under voltage lockout (Vout	V_{UV8}			85		%
falling)						
V_{OUT} Load Regulation, $I_{OUT} = 1mA$				0.006		%/mA
to 150mA						
V_{OUT} Line Regulation, $V_{IN8} = 3$ to 5V,				0.015		%/V
$I_{OUT8} = 0.05A$						
Power Supply Reject Ratio (f =	PSRR8			70		dB
10kHz, V _{OUT8} =1.1V)						
Output noise (10Hz to 100kHz,	OUT _{NOISE}			30		uVrms
V _{OUT8} =1.1V)	8					
Dropout voltage @ 100mA	V_{DROP8}			200		mV
(V _{OUT8} =2.5V)						
Rated output current	I _{MAX8}			100		mA
Operating Quiescent Current, No	I_{Q8}			52		uA
load, V _{DD} =3.8V						
Current Limit, VOUT8 = V _{OUT8} x	I _{CL8}		150	200		mA
0.95						
Soft-start Time	t _{SS8}			400		us
C _{OUT} Discharge Switch ON	R _{DIS8}			400		Ohm



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Resistance						
Ch9: LD04(VCC_25)			•			
Input supply voltage range	V _{INPUT9}		2.7		5.5	V
V _{OUT} Output Voltage Adjustable	V _{ОUТ9}		1.8		3.4	V
Range,						
4bit(step=100mv)						
V _{OUT} Output Voltage,	V _{OUT9(Defa}		2.450	2.500	2.550	V
Default(Tj=25°C)	ult)					
V _{OUT} Output Voltage,	V _{OUT9(Defa}		2.425	2.500	2.575	V
Default(Tj=-10~85℃)	ult)					
Power Good threshold (Vout rising)	V_{PG9}			93		%
Output under voltage lockout (Vout	V _{UV9}			85		%
falling)						
V_{OUT} Load Regulation, $I_{OUT} = 1mA$				0.005		%/mA
to 150mA						
V_{OUT} Line Regulation, $V_{IN9} = 3$ to 5V,				0.03		%/V
I _{OUT9} = 0.15A						
Power Supply Reject Ratio (f =	PSRR9			50		dB
10kHz, V _{OUT9} =3.3V)						
Output noise (10Hz to 100kHz,	OUT _{NOISE}			300		uVrms
V _{OUT9} =3.3V)	9					
Dropout voltage @ 150mA	V_{DROP9}			200		mV
(V _{OUT9} =3.3V)						
Operating Quiescent Current, No	I _{Q9}			28		uA
load, V _{DD} =3.8V						
Rated output current	I _{MAX9}			150		mA
Current Limit, VOUT9 = V_{OUT9} x	I _{CL9}		250	300		mA
0.95						
Soft-start Time	t _{SS9}			400		us
C _{OUT} Discharge Switch ON	R _{DIS9}			400		Ohm
Resistance						
Ch10 : LD05 (VCC28_CIF)	1 .,		<u> </u>	I	T	
Input supply voltage range	V _{INPUT10}		2.7		5.5	V
V _{OUT} Output Voltage Adjustable	V _{OUT10}		1.8		3.4	V
Range,						
4bit(step=100mv)						
V _{OUT} Output Voltage,	V _{OUT10(Def}		2.744	2.800	2.856	V
Default(Tj=25℃)	ault)			_		_
V _{OUT} Output Voltage,	V _{OUT10(Def}		2.716	2.800	2.884	V



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Default(Tj=-10~85°C)	ault)					
Power Good threshold (Vout rising)	V _{PG10}			93		%
Output under voltage lockout (Vout	V _{UV10}			85		%
falling)						
V_{OUT} Load Regulation, $I_{OUT} = 1mA$				0.003		%/mA
to 300mA						
V_{OUT} Line Regulation, $V_{IN10} = 3$ to				0.01		%/V
$5V$, $I_{OUT10} = 0.3A$						
Power Supply Reject Ratio (f =	PSRR10			52		dB
10kHz, V _{OUT10} =3.3V)						
Output noise (10Hz to 100kHz,	OUT _{NOISE}			300		uVrms
V _{OUT10} =3.3V)	10					
Dropout voltage @ 300mA	V _{DROP10}			200		mV
(V _{OUT10} =2.8V)						
Operating Quiescent Current, No	I _{Q10}			28		uA
load, V _{DD} =3.8V						
Rated output current	I _{MAX10}			300		mA
Current Limit, VOUT10 = $V_{OUT10} x$	I _{CL10}		350	500		mA
0.95						
Soft-start Time	t _{SS10}			400		us
C _{OUT} Discharge Switch ON	R _{DIS10}			400		Ohm
Resistance	T CDISTO			100		011111
Ch11: LD06(VCC_12)						
Input supply voltage range	V _{INPUT11}		2.7		5.5	V
V _{OUT} Output Voltage Adjustable	V _{OUT11}		0.8		2.5	V
Range,						
5bit(step=100mv)						
V _{OUT} Output Voltage,	V _{OUT11(Def}		1.176	1.200	1.224	V
Default(Tj=25℃)	ault)					
V _{OUT} Output Voltage,	V _{OUT11(Def}		1.164	1.200	1.236	V
Default(Tj=-10~85℃)	ault)					
Power Good threshold (Vout rising)	V _{PG11}			93		%
Output under voltage lockout (Vout	V _{UV11}			85		%
falling)						
V_{OUT} Load Regulation, $I_{OUT} = 1mA$				0.005		%/mA
to 150mA						
V_{OUT} Line Regulation, $V_{IN11} = 3$ to				0.015		%/V
5V, I _{OUT11} = 0.1A						
Power Supply Reject Ratio (f =	PSRR11			70		dB



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
10kHz, V _{OUT11} =3.3V)						
Output noise (10Hz to 100kHz,	OUT _{NOISE}			30		uVrms
V _{OUT11} =3.3V)	11					
Dropout voltage @ 150mA	V _{DROP11}			200		mV
(V _{OUT11} =2.5V)						
Operating Quiescent Current, No	I _{Q11}			52		uA
load, V _{DD} =3.8V						
Rated output current	I _{MAX11}			150		mA
Current Limit, VOUT11 = V _{OUT11} x	I _{CL11}		200	300		mA
0.95						
Soft-start Time	t _{SS11}			400		us
C _{OUT} Discharge Switch ON	_					-
Resistance	R _{DIS11}			400		Ohm
Ch12: LD07(VCC18_CIF)			<u>I</u>			
Input supply voltage rangef	V _{INPUT12}		2.7		5.5	V
V _{OUT} Output Voltage Adjustable	V _{OUT12}		0.8		2.5	V
Range,						
5bit(step=100mv)						
V _{OUT} Output Voltage,	V _{OUT12(Def}		1.764	1.800	1.836	V
Default(Tj=25℃)	ault)					
V _{OUT} Output Voltage,	V _{OUT12(Def}		-1.736	1.800	1.854	V
Default(Tj=-10~85℃)	ault)					
Power Good threshold (Vout rising)	V_{PG12}			93		%
Output under voltage lockout (Vout	V_{UV12}			85		%
falling)						
V _{OUT} Load Regulation, I _{OUT} = 1mA				0.005		%/mA
to 300mA						
V_{OUT} Line Regulation, $V_{IN12} = 3$ to				0.015		%/V
5V, I _{OUT12} = 0.3A						
Power Supply Reject Ratio (f =	PSRR12			65		dB
10kHz, V _{OUT12} =3.3V)						
Output noise (10Hz to 100kHz,	OUT _{NOISE}			50		uVrms
V _{OUT12} =3.3V)	12					
Dropout voltage @ 300mA	V _{DROP12}			200		mV
(V _{OUT12} =2.5V)						
Operating Quiescent Current, No	I _{Q12}			48		uA
load, V _{DD} =3.8V						
Rated output current	I _{MAX12}			300		mA
Current Limit, VOUT12 = V _{OUT12} x	I _{CL12}		400	400		mA



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
0.95						
Soft-start Time	t _{SS12}			400		us
C _{OUT} Discharge Switch ON	_			050		01
Resistance	R _{DIS12}			250		Ohm
Ch13 : LD08 (VCC33_WIFI)						
Input supply voltage range	V _{INPUT13}		2.7		5.5	V
V _{OUT} Output Voltage Adjustable	V _{OUT13}		1.8		3.4	V
Range,						
4bit(step=100mv)						
V _{OUT} Output Voltage,	V _{OUT13(Def}		3.234	3.300	3.366	V
Default(Tj=25°C)	ault)					
V _{OUT} Output Voltage,	V _{OUT13(Def}		3.201	3.300	3.399	V
Default(Tj=-10~85°C)	ault)					
Power Good threshold (Vout rising)	V _{PG13}			93		%
Output under voltage lockout (Vout	V _{UV13}			85		%
falling)						
V_{OUT} Load Regulation, $I_{OUT} = 1mA$				0.003		%/mA
to 150mA						
V_{OUT} Line Regulation, $V_{IN13} = 3$ to				0.01		%/V
5V, I _{OUT6} = 0.15A						
Power Supply Reject Ratio (f =	PSRR13			50		dB
10kHz, V _{OUT13} =3.3V)						
Output noise (10Hz to 100kHz,	OUT _{NOISE}			300		uVrms
V _{OUT13} =3.3V)	13					
Dropout voltage @ 300mA	V _{DROP13}			200		mV
(V _{OUT13} =2.8V)						
Operating Quiescent Current, No	I _{Q13}			30		uA
load, V _{DD} =3.8V				400		1
Rated output current	I _{MAX13}		500	400		mA
Current Limit, VOUT13 = $V_{OUT13} x$ 0.95	I _{CL13}		500	600		mA
Soft-start Time	toous			400		HE
C _{OUT} Discharge Switch ON	t _{SS13}			400		us
Resistance	R _{DIS13}			400		Ohm
Ch14 : LD09 (VCC_SD)				<u> </u>		
	\ \		2.7		<i>E E</i>	1/
Input supply voltage range	V _{INPUT14}		2.7		5.5	V
V _{OUT} Output Voltage Adjustable	V _{OUT14}		1.8		3.4	V
Range, 4bit(step=100mv)	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		0.004	0.000	0.000	
V _{OUT} Output Voltage,	V _{OUT14(Def}		3.234	3.300	3.366	V



PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Default(Tj=25℃)	ault)					
V _{OUT} Output Voltage, Default	V _{OUT14Defa}		3.201	3.300	3.399	V
(Tj=-10~85℃)	ult)					
Power Good threshold (Vout rising)	V _{PG14}			93		%
Output under voltage lockout (Vout	V _{UV14}			85		%
falling)						
V_{OUT} Load Regulation, $I_{OUT} = 1mA$				0.003		%/mA
to 150mA						
V_{OUT} Line Regulation, $V_{IN14} = 3$ to				0.01		%/V
5V, I _{OUT14} = 0.15A						
Power Supply Reject Ratio (f =	PSRR14			50		dB
10kHz, V _{OUT14} =3.3V)						
Output noise (10Hz to 100kHz,	OUT _{NOISE}			300		uVrms
V _{OUT13} =3.3V)	14					
Dropout voltage @ 300mA	V _{DROP14}			200		mV
(V _{OUT13} =2.8V)						
Operating Quiescent Current, No	I _{Q14}			30		uA
load, V_{DD} =3.8 V						
Rated output current	I _{MAX14}			300		mA
Current Limit, VOUT14 = $V_{OUT14} x$	I _{CL14}		400	500		mA
0.95						
Soft-start Time	t _{SS14}			400		us
C _{OUT} Discharge Switch ON	R _{DIS14}			400		Ohm
Resistance	TVDIS14			400		Onn
Ch15 :SWITCH (VCC_LCD)						
Input supply voltage range	V _{INPUT15}		2.7		5.5	V
Rated output current	I _{MAX15}			300		mA
On resistance(Vgs=3V)				150		mohm
Current Limit	I _{CL15}		400	500		mA
C _{OUT} Discharge Switch ON	R _{DIS15}			400		Ohm
Resistance	21010					
Ch16: H_5V (HDMI_5V)	<u> </u>		<u> </u>		Τ	1
Input supply voltage range	V _{INPUT16}		4.7		5.4	V
Rated output current	I _{MAX16}			80		mA
OL47 OTO CWITOU						
Ch17: OTG SWITCH Input supply voltage range	V _{INPUT17}		4.7		5.4	V
			4.1	000	J. 4	<u> </u>
Rated output current	I _{MAX17}			800		mA



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PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
output current limit	I _{CL17}	0.1A step, default=0.8A	0.7		1	А
RTC						
RTC Operating Voltage Range	V _{IN}		2.5		5.5	V
RTC Supply Current	ΙQ			5	10	uA
CLK32OUT1 jitter (open drain)				100		ns
(always on)						
CLK32OUT1 duty cycle			40		60	%
CLK32OUT2 jitter (open drain)				100		ns
CLK32OUT2 duty cycle			40		60	%
12C INTERFACE TIMING						
SCL clock frequency	f _{SCL}				400	kHz
SCL high time	t _{HIGH}		0.6			us
SCL low time	t _{LOW}		1.3			us
Data setup time	t _{SU,DAT}		0.1			us
Data hold time	t _{HD,DAT1}		0		0.1	us
Setup time for repeated start	t _{SU,STA}		0.1			us
HOLD time for start/repeated start	t _{HD,STA}		0.1			us
Bus free time between a stop and condition	t _{BUF}		1.3			us
Rise time of SCL/SDA	tr		20 +		300	ns
			0.1C _B			
Fall width of SCL/SDA	t _f		20 +		300	ns
			0.1C _B			
Pulse width of suppressed spike	t _{SP}		0		50	ns
Capacitive load for each of bus line	C _{B2}				400	pF

11 FUNCTIONAL DESCRIPTION

11.1 POWER UP/POWER DOWN

The RK818 can be powered by either a battery, or an external power supply through the USB port. When the PMIC is powered by a battery only, pressing the PWRON key powers up the PMIC. All the power channels start up at the default output voltages with a preset power up sequence, which has 2mS intervals between the channels. When the power up process is done, the NRESPWRON turns to high logic level to inform the processor that all the power rails are up and stable. And now the processor can communicate with the PMIC to

re-configure the output voltage of each power channel if needed.

To power down the PMIC, the processor needs to issue a "power down" signal through the I²C interface. Upon receiving the power down signal, the PMIC first saves all the information on the existing states, and then switches the NRESPWRON to low logic level. At this point, the power channels start to be turned off one after another with the power down sequence. If for any reason the processor fails to issue the power down signal, the PMIC can be powered off by "pressing and holding" the PWRON key.

In a case where a battery is the sole power supply and the PMIC is in off state, when an external power supply is plugged into the USB, the PMIC will first check to see if this is a valid power supply. If the power supply from the USB is valid, then the power channels are turned on and the battery is charged.

11.2 SWITCHING CHARGER

The RK818 has integrated a switch mode charger, which provides the functions like trickle current charging, constant current charging, constant voltage charging, charging termination, automatic recharging, battery temperature monitoring, charging timer and thermal feedback protection. The values of constant current and constant voltage charging can be set through I²C interface.

The input average current limit function allows as large as possible a charging current to be used without having to worry about the input current exceeding the maximum current allowed by the USB port. The input current limits can be configured through I²C interface. For example, when an USB port is used as the input, the input current limit can be configured to either 450mA, or 820mA, to meet the requirements of USB2.0 and USB3.0: respectively.

The charger also has a timer function which sets the maximum charging time for trickle, constant current and constant voltage charging, respectively. If the charging does not complete when a preset maximum charging time is reached, the charging is terminated.

The battery temperature can be monitored through the TS1 pin. A battery typically has a thermistor inside. The RK818 sinks a constant current into the thermistor and senses the voltage across the thermistor through an internal ADC. A safe charging temperature range is preset in the PMIC. The charging can proceed normally if the battery temperature falls within the preset range. If, however, the battery temperature goes either above the upper limit or below the lower limit of the preset range, the charging will pause until the battery temperature goes back in the preset range. If the value of the available thermistor is either too large or too small, a normal resistor can be connected in series or in parallel with the thermistor so that the sensed voltage fits the ADC's input range.

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During Charging, Vsys will be set to 3.6V when the battery voltage is below 3.6V. This design is to guarantee that when an external power supply is plugged into the USB port to charge the battery while the battery voltage is low, the Vsys is already at 3.6V, which allows the PMIC to start up quickly without having to wait for the Vsys ramping up.

11.3 POWER PATH MANAGEMENT

A power path management function is integrated in the RK818, which, together with the accurate input current limit function, can provide intelligent power path control. In a power path control process, the PMIC gives the outputs, or the system loads, the highest priority of using the input power. The battery is getting charged only if the input power is greater than the output power required by the system loads. The intelligent power path control function automatically reduces the charging current when the output power required by the loads increases. In an extreme case where the required output power is greater than the input power, the charging current will be cut off and the battery will join the input power supply to provide power to the load. This is how the intelligent power path control works: As the system power loading increases, the PMIC will draw more input current from the power supply to meet the output power requirement while keep the charging current unchanged. If the system power loading continues to increase to the point where the input current limit is reached, then the PMIC will lower the charging current so that enough power still goes to the load. If the system power loading further increases and due to the input current limit, the input power can not meet the output power requirement, then the battery will start to discharge to supply power to the load together with the USB power supply. If for some reason the USB is unplugged, the battery will automatically switched in to take over the USB power supply and provide full power to the load. The wide power path loop bandwidth allows all the above mentioned power path switching transient to be quick and seamless and therefore no overshoot and notch occur at the system and output voltages.

To minimize the loss from the voltage drop along the current path when the battery is charged or discharged, a $50m\Omega$ MOSFET is integrated in the RK818 to serve as a control switch as well as the power switch of the switching mode battery charger.

11.4 THERMAL FOLDBACK

Generally speaking, the higher the operating junction temperature is, the shorter the chip's life time. Therefore, keeping the operating junction temperature as low as possible is one of the keys in reliability design. The RK818 provides a thermal feedback protection function for



charging process. When the die temperature reaches a preset value, the PMIC will lower the charging current so as to keep the die temperature within an appropriate range. The life time of the PMIC equipped with this function can be reliably prolonged and no over-heat damage will occur.

11.5 BATTERY FUEL GAUGE

The RK818 provides an accurate battery fuel gauge. A 12-bit ADC is integrated in the RK818 to collect the information on the battery, such as battery voltage, charging/discharging status, battery temperature, etc. Using the proprietary algorithms and the information collected by the ADC, the battery fuel gauge can accurately calculate the battery capacity based on the charging/discharging characteristics of the battery preloaded in the system. The gauge then sends the battery capacity information to the processor through the I²C interface.

11.6 BUCK CONVERTERS

The RK818 provides four high current synchronous buck converters, which deliver up to 4A, 4A, 2.5A and 2.5A, respectively. An enhanced current mode architecture is used, which improves the transient response significantly. All output voltages can be adjusted dynamically during operation through DVS (Dynamic Voltage Scaling), which guarantees a linear and gradual voltage ramping up and down. A complete set of protection functions, such as short circuit protection, is implemented in the buck converters too.

The key parameters such as operating mode, output voltage, DVS change rate, and output current limit can be configured through the I²C interface.

11.7 BOOST CONVERTER

The synchronous boost converter has 2.5A current capability and is used to power the OTG and the HTMI5V. The OTG has a built-in current limiting switch, which can effectively protect the boost converter from being damaged if a short circuit occurs at the OTG port.

As the USB input port and the OTG output port share a same pin, when the USB port is being used as a power supply and charging the battery, the OTG switch is forbidden to be turned on. Only when there is no external power supply plugged into the USB port, can the OTG be turned on and serve as a power supply.

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The key parameters such as operating mode, output voltage, and output current limit can be configured through the I²C interface.

11.8 LOW DROPOUT REGULATORS (LDOS)

The RK818 also integrates nine LDOs and one low R_{dson} switch, with four LDOs (Ch6, Ch7, Ch9 and Ch11) capable of providing up to 150mA and three LDOs (CH10, CH12 and CH14) providing maximum 300mA. The LDO on Ch8 is a low noise, high PSRR LDO which delivers up to 100mA current and the LDO on Ch14 has 400mA current capability. The parameters such as output voltage in the different operating modes can be adjusted through the I^2C interface.

11.9 **REAL TIME CLOCK (RTC)**

The RK818 integrates a crystal oscillator buffer and a real time clock (RTC). The buffer works with an external 32.768kHz crystal oscillator. With the RTC function, the PMIC provides second/minute/hour/day/month/year information, alarm wake up as well as time calibration. The RK818 provides two channels of 32.768kHz clocks with open drain outputs, where one channel is constantly on and the other is enabled through I²C interface.



12 STATE MACHINE DESCRIPTION

12.1 STATE DIAGRAM

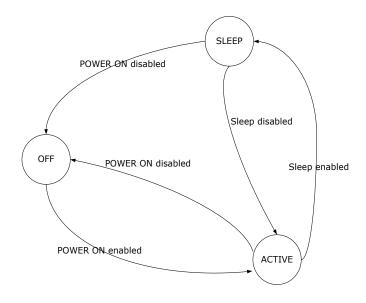


Figure 12-1 PMU State Diagram

OFF state: the PMIC is off. All channels are shut down.

ACTIVE state: the PMIC is on. All channels are on and operates as required by the system.

SLEEP state: the PMIC is in low power standby.

12.2 POWER ON ENABLE CONDITIONS

If none of the device power-on disable conditions is met, the following conditions are available to turn on and/or maintain the ON state of the device:

- PWRON signal is low for a period of time
- USB is plugged in. (PLUG_IN_INT goes to high level)
- RTC set time power on

12.3 POWER-ON DISABLE CONDITIONS

The PMIC will be powered off, or can not be powered on under the following conditions:

 PWRON signal keeps at low lever longer than the long-press delay T_{DPWRONLP} and PWRON_LP_ACT is set to "0" (If it is set to "1", the PMIC will restart automatically after the it is shut down) The interrupt corresponding to this condition is



PWRON_LP_INT in the INT_STS_REG register.

- The die temperature reaches the TSD threshold, in which case the TSD_STS bit in the register THERMAL_REG is set to "1".
- Vsys is lower than UVLO threshold, in which case the VB_UV_STS bit in the registerVB_MON_REG is set to "1".
- Vsys is lower than the low voltage warning threshold which can be set with the VB_LO_SEL bit in the register VB_MON_REG, and the VB_LO_ACT bit is set to "0".
- Vsys is higher than the over voltage protection threshold.
- The DEV_OFF control bit is set to "1". (DEV_OFF is reset when the system is powered off).
- The temperature sensed at TS2 is either too high or too low. (To use TS2, a thermistor on a device to be monitored should be connected between TS2 and GND, and the ADC_TS2_EN bit in the register ADC_CTRL_REG must be set to "enable". When the sensed voltage at TS2, which is saved in the register TS2_ADC_REG, is greater than the value in BAT_LTS_TS2_REG or smaller than the value in BAT_HTS_TS2_REG, the PMIC will be powered off.

12.4 SLEEP ENABLE CONDITIONS

- SLEEP signal is at high level
- Or DEV SLP control bit is set to "1".
- And interrupt flag inactive (INT high): No non-masked interrupt pending

The SLEEP state can be controlled by programming DEV_SLP and keeping the SLEEP state.

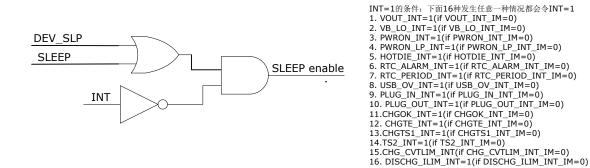


Figure 12-2 SLEEP enable control

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13 POWER UP SEQUENCE

	PROCESSOR TYPE		/RK2928		Partial Customized BUCK1-4,LDO3-LDO5, LDO7		RK3066 01			ıstomized
	ВООТ	Г		11		0		 I		00
		Maximum	Typical	Power Up	Typical	Power Up	Typical	Power Up	Typical	Power Up
	Output Voltage Range	l _{out}	Vout	Sequence	Vout	Sequence	Vout	Sequence	Vout	Sequence
BUCK1	0.7V-1.5V (step 25mV)	2A	1.1V	3	ОТР	ОТР	1.2V	3	ОТР	ОТР
BUCK2	0.7V-1.5V (step 25mV)	2A	1.1V	1	ОТР	ОТР	1.2V	1	ОТР	ОТР
виск3	setting by external resistors	1.0A	1.2V	4	1.2V	ОТР	1.2V	4	1.2V	ОТР
BUCK4	1.8V-3.6V(step 0.1V)	1.5A	3.0V	1	ОТР	OTP	3.0V	1	OTP	OTP
LDO1	1.8V-3.4V	150mA	3.3V	Х	3.3V	Х	3.3V	Х	OTP	OTP
LDO2	1.8V-3.4V	150mA	3.0V	х	3	х	3.0V	X	ОТР	ОТР
LDO3	0.8V-2.5V	100mA	1.1V	1	ОТР	ОТР	1.1V	1	ОТР	ОТР

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LDO4	1.8V-3.4V	100mA	2.5V	x	OTP	OTP	2.5V	2	OTP	OTP
LDO5	1.8V-3.4V	300mA	3V	1	OTP	OTP	3.0V	2	OTP	OTP
LDO6	0.8V-2.5V	150mA	1.2V	х	1.2V	Х	1.1V	Х	OTP	ОТР
LDO7	0.8V-2.5V	300mA	1.8V	2	OTP	OTP	1.8	2	OTP	OTP
LDO8	1.8V-3.4V	400mA	1.8V	х	1.8V	Х	1.8V	Х	OTP	ОТР
LDO9	1.8V-3.4V	300mA	3.0V	4	3.0V	5	3.0V	4	OTP	ОТР
SWITCH	3V	300mA	3.0V	х	3.0V	Х	3.0V	Х	Х	OTP
oTG	4.7V-5.4V(step 0.1V)	800mA	5V	Х	5V	Х	5V	Х	х	Х
HDMI_5V	4.7V-5.4V(step 0.1V)	80mA	5V	Х	5V	Х	5V	х	х	Х

Table 4 Power up/down Sequence



13.1 **BOOT1=1: BOOT0 = 1**

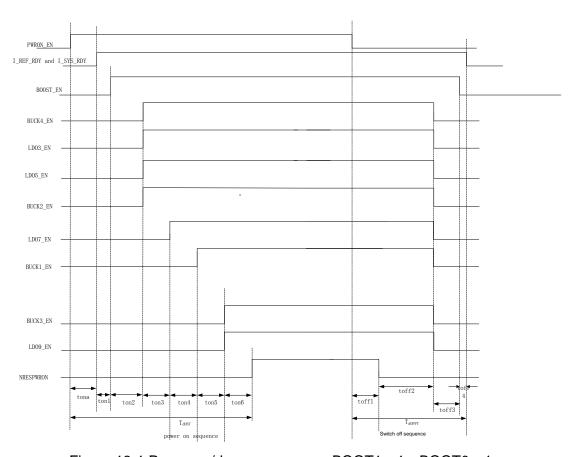


Figure 13-1 Power up/down sequence: BOOT1=1, BOOT0=1

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13.2 **BOOT1=0: BOOT0 = 1**

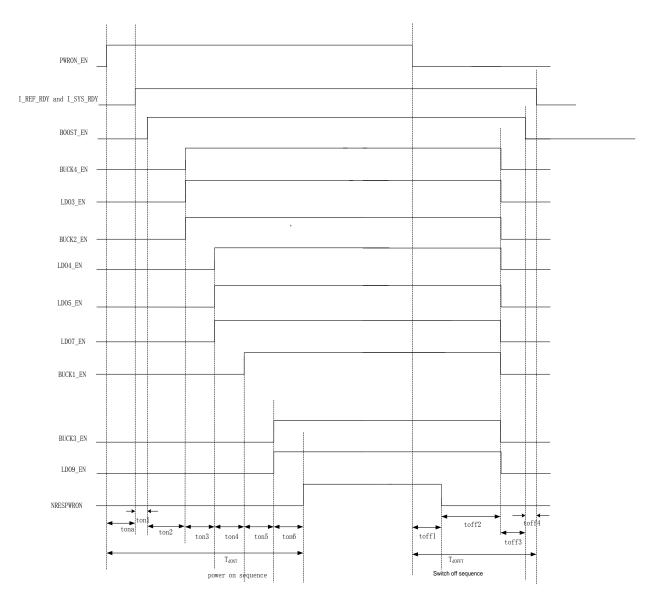


Figure 13-2 Power up/down sequence, BOOT1=0: BOOT0=1

13.3 **BOOT1=1: BOOT0 = 0**

In the "10" mode, 9 power channels are powered up, which are BUCK1- BUCK4, LDO3-LDO5 and LDO7. The power up sequence and the default output voltage of these 9 channels can be configured through OTP. The default output voltage of the BUCK3 can also be set by the external resistors. The default output voltage of the LDO9 is 3V.



13.4 **BOOT1=0: BOOT0 = 0**

In the mode of "00", 14 power channels are powered up, among which, the power up sequence and the default voltage of the BUCK1-4, LDO1-9 and the SWITCH can be configured through OTP. Again, The default output voltage of the BUCK3 can also be set by the external resistors. The voltage of the SWITCH is the same as the input supply.

13.5 **BOOT TIMING CHARACTERISTICS**

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNIT
T _{ona}	power on enable to system ready and reference ready delay				us
Ton1	Reference and system ready to boost enable delay		66×t _{CK32K}		us
Ton2	Boost enable delay to 1st channel enable delay		66×t _{CK32K}		us
Ton3	1st channel enable to 2st channel enable delay		66×t _{CK32K}		us
Ton4	2nd channel enable to 3rd channel enable delay		66×t _{CK32K}		us
Ton5	3rd channel enable to 4th channel enable delay		66×t _{CK32K}		us
Ton6	4th channel enable to NRESPWRON rising edge delay		50		ms
toff1	PWRON disable to NRESPWRON falling delay		1×t _{CK32K}		us
Toff2	NRESPWRON falling delay to supplies disable delay		2		ms
Toff3	Other supplies disable to boost disable		2		ms
Toff4	Supplies disable to house-keeping disable delay		1×t _{CK32K}		us

Table 5 BOOT Timing Characteristics



14 POWER CONTROL TIMING

14.1 DEVICE TURN-ON WITH USB PLUG_IN

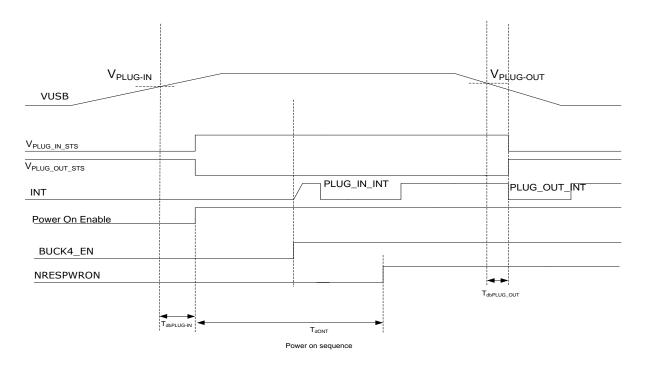


Figure 14-1 Turn on sequence when USB is plugged in (PLUP_IN_INT triggered power on enable)

14.2 POWER CONTROL TIMING WHEN POWERED BY BAT

Vbat=Vsys, as shown in the Figure 14-2

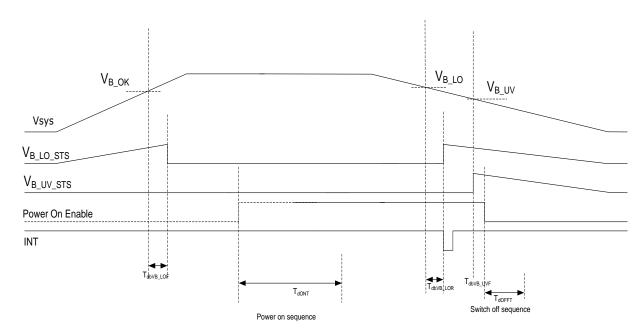


Figure 14-2 Power Control Timing with VIN Falling

14.3 TIMING CHARACTERISTICS

(USB or Vsys rising, falling and plug-in)

Parameter	Description	Min	Тур	Max	Unit
T_{dbVB_LOF}	VB_LO falling-edge debouncing delay		2		ms
T _{dONT}	Total power on delay time(ton1~ton6)		62		ms
T_{dbVB_LOR}	VB_LO rising-edge debouncing delay		2		ms
T _{dVB_UVF}	VB_UV falling-edge debouncing delay		2		ms
T_{dOFFT}	Total power off delay time		2		ms
T _{dbPLUG_IN}	USB plug-in debouncing delay		100		ms
T_{dbPLUG_OUT}	USB plug-out debouncing delay		100		ms

Table 6 Timing characteristics of USB and VSYS voltages



14.4 DEVICE STATE CONTROL THROUGH PWRON SIGNAL

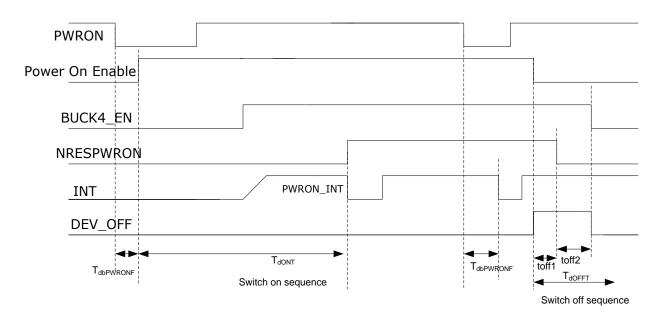


Figure 14-3 PWRON turn on/DEV_OFF turn off (DEV_OFF software power off signal comes before t_{off1})

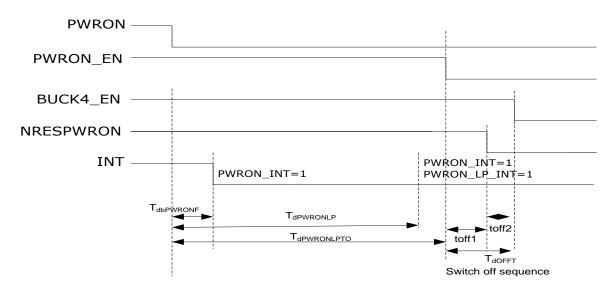


Figure 14-4 PWRON long press turn off (Register setting Reg4B<6>=0: Long press turning off Reg4B<5:4>=0: Long press time set to 6S)

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14.5 TIMING CHARACTERISTICS (PWRON, DEV_OFF)

Parameter	Description	Min	Тур	Max	Unit
T _{dbPWRONF}	PWRON falling-edge debouncing delay		500		ms
T _{dONT}	Total power on delay time(ton1~ton6)		62		ms
T _{dPWRONLP}	PWRON long press delay to interrupt (PWRON falling edge to PWRON_LP_INT=1)		4		S
T _{dPWRONLPTO}	PWRON long press delay to turn off (PWRON falling edge to NRESPWRON falling edge)		6		S
toff1	POWER ON disable to NRESPWRON falling delay		1×t _{CK32K}		us
Toff2	NRESPWRON falling delay to supplies disable delay		2		ms
T_{dOFFT}	total power off delay time		2		ms

Table 7 PWRON/DEV_OFF timing characteristics

14.6 SLEEP STATE CONTROL

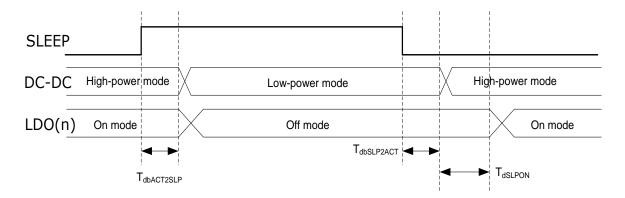


Table 14-5 SLEEP/ACTIVE Transition Timing



14.7 TIMING CHARACTERISTICS (SLEEP)

Parameter	Description	Min	Тур	Max	Unit
T _{dbACT2SLP}	SLEEP falling-edge debouncing delay		3×t _{ck32k}		us
T _{dbSLP2ACT}	SLEEP rising-edge debouncing delay		3×t _{ck32k}		us
T _{dSLPON}	Delay to turn on enable after SLEEP		1×t _{ck32k}		us
GSLPON	rising-edge debouncing				

Table 8 SLEEP Timing Characteristics

15 REGISTER DEFINITION

15.1 **REGISTER MAP**

HEX	FUNCTION DESCRIPTION	R/W	DEFAULT/
ADDRESS			RESET
	RTC REGISTERS		
00	SECONDS REG	RW	00
01	MINUTES REG	RW	5 0
02	HOURS REG	RW	0 8
03	DAYS_REG	RW	21
04	MONTHS_REG	RW	01
05	YEARS_REG	RW	13
06	WEEKS_REG	RW	01
08	ALARM_SECONDS_REG	RW	00
09	ALARM_MINUTES REG	RW	00
0A	ALARM_HOURS REG	RW	00
0B	ALARM_DAYS_REG	RW	01
0C	ALARM_MONTHS_REG	RW	01
0D	ALARM_YEARS_REG	RW	00
10	RTC_CTRL_REG	RW	00
11	RTC_STATUS_REG	RW	8 2
12	RTC_INT_REG	RW	00
13	RTC_COMP_LSB_REG	RW	00
14	RTC_COMP_MSB_REG	RW	00
	RESERVED REGISTERS		
0E	RESERVED	RW	00



		anagement	J
0F	RESERVED	RW	00
15	RESERVED	RW	00
16	RESERVED	RW	00
17	RESERVED	RW	00
18	RESERVED	RW	00
	MISC REGISTERS		
20	CLK32KOUT_REG	RW	00
21	VB_MON_REG	RW	06
22	THERMAL_REG	RW	00
	POWER CHANNEL CONTROL/MONITOR REGIS	TERS	
23	DCDC_EN_REG	RW	boot
24	LDO_EN_REG	RW	boot
25	SLEEP_SET_OFF_REG1	RW	00
26	SLEEP_SET_OFF_REG2	RW	00
27	DCDC_UV_STS_REG	RO	00
28	DCDC_UV_ACT_REG	RW	1F
29	LDO_UV_STS_REG	RO	00
2A	LDO_UV_ACT_REG	RW	FF
2B	DCDC_PG_REG	RO	00
2C	LDO_PG_REG	RO	00
2D	VOUT_MON_TDB_REG	RW	02
	POWER CHANNEL CONFIGIGRATION REGIST	ERS	
2E	BUCK1_CONFIG_REG	RW	01
2F	BUCK1_ON_VSEL	RW	boot
30	BUCK1_SLP_VSEL	RW	00
31	BUCK1_DVS_VSEL	RW	00
32	BUCK2_CONFIG_REG	RW	01
33	BUCK2_ON_VSEL	RW	boot
34	BUCK2_SLP_VSEL	RW	00
35	BUCK2_DVS_VSEL	RW	00
36	BUCK3_CONFIG_REG	RW	01
37	BUCK4_CONFIG_REG	RW	00
38	BUCK4_ON_VSEL	RW	boot
39	BUCK4_SLP_VSEL_REG	RW	00
3A	BOOST_CONFIG_REG	RW	09
3B	LDO1_ON_VSEL_REG	RW	boot
3C	LDO1_SLP_VSEL_REG	RW	00
3D	LDO2_ON_VSEL_REG	RW	boot
3E	LDO2_SLP_VSEL_REG	RW	00



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			System
3F	LDO3_ON_VSEL_REG	RW	boot
40	LDO3_SLP_VSEL_REG	RW	00
41	LDO4_ON_VSEL_REG	RW	boot
42	LDO4_SLP_VSEL_REG	RW	00
43	LDO5_ON_VSEL_REG	RW	boot
44	LDO5_SLP_VSEL_REG	RW	00
45	LDO6_ON_VSEL_REG	RW	boot
46	LDO6_SLP_VSEL_REG	RW	00
47	LDO7_ON_VSEL_REG	RW	boot
48	LDO7_SLP_VSEL_REG	RW	00
49	LDO8_ON_VSEL_REG	RW	boot
4A	LDO8_SLP_VSEL_REG	RW	00
4B	DEVCTRL_REG	RW	00
	INTERRUPT REGISTERS		
4C	INT_STS_REG1	RW	00
4D	INT_STS_MSK_REG1	RW	00
4E	INT_STS_REG2	RW	00
4F	INT_STS_MSK_REG2	RW	00
50	IO_POL_REG	RW	06
	BOOST/OTG/DCDC CURRENT LIMIT REGISTERS	3	
52	H5V_EN_REG	RW	00
53	SLEEP_SET_OFF_REG3	RW	00
54	BOOST_LDO9_ON_VSEL_REG	RW	
55	BOOST_LDO9_SLP_VSEL_REG	RW	60
56	BOOST_CTRL_REG	RW	00
90	DCDC ILMAX	RW	55
	CHARGING CONTROL REGISTERS		
9A	CHRG_COMP_REG	RW	00
AO	SUP_STS_REG	RW	0C
A1	USB_CTRL_REG	RW	
A3	CHRG_CTRL_REG1	RW	B5
	CHRG_CTRL_REG1 CHRG CTRL REG2		
A4		RW	4A
A5	CHRG_CTRL_REG3	RW	02
A6	OTG_ILIM_REG	RW	8C
A 0	BAT_CTRL_REG	DW	00
A8	BAT_HTS_TS1_REG	RW	00
A9	BAT_LTS_TS1_REG	RW	FF
AA	BAT_HTS_TS2_REG	RW	00



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			Javv
AB	BAT_LTS_TS2_REG	RW	FF
AC	TS_CTRL_REG	RW	8F
AD	ADC_CTRL_REG	RW	00
AE	ON_SOURCE	RO	00
AF	OFF_SOURCE	RO	00
	BATTERY FUEL GAUGE REGISTER		
В0	GGCON	RW	4A
B1	GGSTS	RW	40
B2	FRAME_SMP_INTERV_REG	RW	01
В3	AUTO_SLP_CUR_THR_REG	RW	40
B4	GASCNT_CAL_REG3	RW	00
B5	GASCNT_CAL_REG2	RW	00
B6	GASCNT_CAL_REG1	RW	00
B7	GASCNT_CAL_REG0	RW	00
B8	GASCNT3	R	00
B9	GASCNT2	R	00
BA	GASCNT1	R	00
BB	GASCNT0	R	00
ВС	BAT_CUR_AVG_REGH	R	00
BD	BAT_CUR_AVG_REGL	R	00
BE	TS1_ADC_REGH	R	00
BF	TS1_ADC_REGL	R	00
C0	TS2_ADC_REGH	R	00
C1	TS2_ADC_REGL	R	00
C2	BAT_OCV_REGH	R	00
C3	BAT_OCV_REGL	R	00
C4	BAT_VOL_REGH	R	00
C5	BAT_VOL_REGL	R	00
C6	RELAX_ENTRY_THRES_REGH	RW	00
C7	RELAX_ENTRY_THRES_REGL	RW	60
C8	RELAX_EXIT_THRES_REGH	RW	00
C9	RELAX_EXIT_THRES_REGL	RW	60
CA	RELAX_VOL1_REGH	R	00
СВ	RELAX_VOL1_REGL	R	00
CC	RELAX_VOL2_REGH	R	00
CD	RELAX_VOL2_REGL	R	00
			·



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CE	BAT_CUR_R_CALC_REGH	R	00
CF	BAT_CUR_R_CALC_REGL	R	00
D0	BAT_VOL_R_CALC_REGH	R	00
D1	BAT_VOL_R_CALC_REGL	R	00
D2	CAL_OFFSET_REGH	RW	7F
D3	CAL_OFFSET_REGL	RW	FF
D4	NON_ACT_TIMER_CNT_REGL	R	00
D5	VCALIB0_REGH	R	00
D6	VCALIB0_REGL	R	00
D7	VCALIB1_REGH	R	00
D8	VCALIB1_REGL	R	00
DD	IOFFSET_REGH	R	00
DE	IOFFSET_REGL	R	00
	DATA REGISTERS	•	
DF	DATA0	RW	00
E0	DATA1	RW	00
E1	DATA2	RW	00
E2	DATA3	RW	00
E3	DATA4	RW	00
E4	DATA5	RW	00
E5	DATA6	RW	00
E6	DATA7	RW	00
E7	DATA8	RW	00
E8	DATA9	RW	00
E9	DATA10	RW	00
EA	DATA11	RW	00
EB	DATA12	RW	00
EC	DATA13	RW	00
ED	DATA14	RW	00
EE	DATA15	RW	00
EF	DATA16	RW	00
F0	DATA17	RW	00
F1	DATA18	RW	00
F2	DATA19	RW	00
	I	l	1

NOTE: Addresses of 60h through 9Fh (except for 9Ah) are for OTP. F3h through FFhare for OTP registers, read/write on these registers is forbidden.



15.2 REGISTER DESCRIPTION

15.2.1 RTC REGISTER

15.2.1.1 SECONDS_REG: RTC SECOND REGISTER

ADDRESS: 00	Н			TYPE: F	RW			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV		SEC1			SE	C0	
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7 Reserved

Bit 6-4 Set the second digit of the RTC seconds (0-5) Bit 3-0 Set the first digit of the RTC seconds (0-9)

Note BCD coding from 00 to 59

15.2.1.2 MINUTES_REG: RTC MINUTE REGISTER

ADDRESS: 01H			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV		MIN1			MIN	V 0	
DEFAULT	0	1	0	1	0	0	0	0

DESCRIPTION

Bit 7 Reserved

Bit 6-4 Set the second digit of the RTC minutes (0-5) Bit 3-0 Set the first digit of the RTC minutes (0-9)

Note BCD coding from 00 to 59

15.2.1.3 HOURS_REG: RTC HOUR REGISTER

ADDRESS: 02H				TYPE: R	W			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	PM/AM	RESV	НО	UR1		HOL	JR0	
DEFAULT	0	0	0	0	1	0	0	0

DESCRIPTION

Power Management System

Bit 7 Set PM or AM: Only used in PM-AM mode, 1: PM. 0:AM.

Bit 6 Reserved

Bit 5-4 Set the second digit of the RTC hours
Bit 3-0 Set the first digit of the RTC hours
Note HOUR1/0 BCD coding from 0 to11/23

15.2.1.4 DAYS_REG: RTC DAY REGISTER

ADDRESS: 03H				TYPE: RV	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	DA	.Y1		DA'	Y0	
DEFAULT	0	0	1	0	0	0	0	1

DESCRIPTION

Bit 7-6 Reserved

Bit 5-4 Set the second digit of the RTC days
Bit 3-0 Set the first digit of the RTC days
Note BCD coding from 0 to 28/29/30/31

15.2.1.5 MONTHS_REG: RTC MONTH REGISTER

ADDRESS: 04H				TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	MONTH1		MONT	ГН0	
DEFAULT	0	0	0	0	0	0	0	1

DESCRIPTION

Bit 7-5 Reserved

Bit 4 Set the second digit of the RTC months
Bit 3-0 Set the first digit of the RTC months

Note BCD coding from 01 to 12

15.2.1.6 YEARS_REG: RTC YEAR REGISTER

ADDRESS: 05H				TYPE: R\	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL		YEA	AR1			YEA	R0	
DEFAULT	0	0	0	1	0	0	1	1

Power Management System

DESCRIPTION

Bit 7-5 Set the second digit of the RTC years

Bit 3-0 Set the first digit of the RTC years

Note BCD coding from 00 to 99

15.2.1.7 WEEKS_REG: RTC WEEK REGISTER

ADDRESS: 06H				TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RESV		WEEK	
DEFAULT	0	0	0	0	0	0	0	1

DESCRIPTION

Bit 7-3 Reserved

Bit 3-0 Set the second digit of the RTC weeks

Note BCD coding from 1 to 7

ALARM SECONDS REG: RTC ALARM SECOND REGISTER

ADDRESS: 08H				TYPE: R\	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	Al	_ARM_SE	C1		ALARM	_SEC0	
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7 Reserved

Bit 6-4 Set the second digit of the RTC alarm seconds

Bit 3-0 Set the first digit of the RTC alarm seconds

Note BCD coding from 00 to 59

15.2.1.8 ALARM_MINUTES_REG: RTC ALARM MINUTE REGISTER

ADDRESS: 09H				TYPE: R\	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	Al	ALARM_MIN1 ALARM_MIN0					
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Power Management System

Bit 7 Reserved

Bit 6-4 Set the second digit of the RTC alarm minutes
Bit 3-0 Set the first digit of the RTC alarm minutes

Note BCD coding from 00 to 59

15.2.1.9 ALARM_HOURS_REG: RTC ALARM HOUR REGISTER

ADDRESS: 0AH			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	ALARM_PM_AM	RESV	ALARM_	_HOUR1		ALARM_	HOUR0	
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7	Set PM) or	AM: only u	ised in PM-AM	l mode,	1: PM. 0:AM.

Bit 6 Reserved

Bit 5-4 Set the second digit of the RTC alarm hours
Bit 3-0 Set the first digit of the RTC alarm hours
Note HOUR1/0 BCD coding from 0 to 11/23

15.2.1.10 ALARM_DAYS_REG: RTC ALAR DAY REGISTER

ADDRESS: 0BH				TYPE: R\	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	ALARM	I_DAY1		ALARM_	DAY0	
DEFAULT	0	0	0	0	0	0	0	1

DESCRIPTION

	110001100
Bit 5-4	Set the second digit of the RTC alarm days
Bit 3-0	Set the first digit of the RTC alarm days
Note	BCD coding from 0 to 28/29/30/31

15.2.1.11 ALARM_MONTHS_REG: RTC ALARM MONTH REGISTER

ADDRESS: 0CH				TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	ALARM_ MONTH1	ALARM_MONTH0			
DEFAULT	0	0	0	0	0	0	0	1

Bit 7-6

Reserved





DESCRIPTION

Bit 4 Set the second digit of the RTC alarm months
Bit 3-0 Set the first digit of the RTC alarm months

Note BCD coding from 01 to 12

15.2.1.12 ALARM YEARS REG: RTC ALARM YEAR REGISTER

ADDRESS: 0DH	ADDRESS: 0DH					RW				
Bit	Bit7	Bit6	Bit5 Bit4 Bit3 Bit2 Bit1 Bi					Bit0		
SYMBOL		ALARM.	_YEAR1		ALARM_YEAR0					
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-5 Set the second digit of the RTC alarm years

Bit 3-0 Set the first digit of the RTC alarm years

Note BCD coding from 00 to 99

15.2.1.13 RTC_CTRL_REG: RTC CONTROL REGISTER

ADDRES	S: 10H		TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RTC_READ	GET_TI	SET_32_	TEST_M	AMPM_	AUTO_	ROUND_30S	STOP_
	SEL	ME	COUNTER	ODE	MODE	COMP	(Auto Clr)	RTC
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7	RTC_READ_SEL:	0: Read access directl	y to d	ynamic registers.
-------	---------------	------------------------	--------	-------------------

1: Read access to static shadowed registers.

Bit 6 GET_TIME: Rising transition of this register transfers dynamic registers into static shadowed registers..

Bit 5 SET_32_COUNTER: 1: Set the 32Khz counter with COMP_REG value. It must only be used when the RTC is frozen.

Bit 4 TEST_MODE: 1: Test mode (Auto compensation is enabled when the 32kHz counter reaches at its end)

Bit 3 AMPM MODE: 0: 24 hours mode.

1: 12 hours mode (PM-AM mode)

Bit 2 AUTO_COMP: 0: No auto compensation RW0.

1: Auto compensation enabled

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Bit 1 ROUND_30S: 1: When "1" is written, the time is rounded to the closest minute

in the next second, and is self-cleared after rounding.

Bit 0 STOP_RTC: 0: RTC is running.

1: RTC is frozen.

RTC_time can only be changed during RTC frozen.

15.2.1.14 RTC_STATUS_REG: RTC STATUS REGISTER

ADDR	RESS: 11H			TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	POWER_UP (Write 1 Clr)	ALARM (Write 1 Clr)	EVENT_1D (Write 1 Clr)	EVENT_1H (Write 1 Clr)	EVENT_1M (Write 1 Clr)	EVENT_1S (Write 1 Clr)	RUN (RO)	RESV
DEFAU	1	0	0	0	0	0	1	0
LT								

DESCRIPTION

Bit 7	POWER_UP: POWER_UP is set by a reset, is cleared by writing one in
	this hit

- Bit 6 ALARM: Indicates that an alarm interrupt has been generated (bit clear by writing 1) The alarm interrupt keeps its low level, until the micro-controller writes 1 in the ALARM bit of the RTC_STATUS register. The timer interrupt is a low-level pulse (15 µs duration).
- Bit 5 EVENT 1D: One day has occurred
- Bit 4 EVENT 1H: One hour has occurred
- Bit 3 EVENT 1M: One minute has occurred
- Bit 2 EVENT 1S: One secondr has occurred
- Bit 1 RUN: 0: RTC is frozen. 1: RTC is running. This bit shows the real state of the RTC
- Bit 0 RESEVERED

15.2.1.15 RTC_INT_REG: RTC INTERRUPT REGISTER

ADDRESS: 12H				TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	INT_SLEEP_	INT_ALARM	INT_TIMER	EVE	RY
	KESV	KESV	KESV	MASK_EN	_EN	_EN		
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-5 RESEVERED

Bit 4 INT_SLEEP_MASK_EN:

1: Mask periodic interrupt while the device is in SLEEP mode

0: Normal mode, no interrupt masked.

Bit 3 INT_ALARM_EN: Enable one interrupt when the alarm value is reached

1: Enable

0: Disable

Bit 2 INT_TIMER_EN:Enable periodic interrupt

Bit 1-0 EVERY: 00: every second 01: every minute 10: every hour 11:

every day

15.2.1.16 RTC_COMP_LSB_REG: RTC COMPENSATION LSB REGISTER

ADDRESS: 13H				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL		RTC_COMP_LSB							
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit7-0 This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [LSB]

15.2.1.17 RTC_COMP_MSB_REG: RTC COMPENSATION MSB REGISTER

ADDRESS: 14H				TYPE: RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		RTC_COMP_MSB								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit7-0 This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [MSB]

15.2.2 MISC REGISTERS

15.2.2.1 CLK32KOUT_REG: RTC 32KHz CLOCK OUTPUT REGISTER

ADDRESS: 20H				TYPE:	RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0			
SYMBOL			CLK32KO	CLK32KO							
		RESERVED UT2_FUN UT2_EN									
DEFAULT	0	0	0	0	0	0	0	0			

DESCRIPTION

Bit 7-2 RESERVED

Bit 1 CLK32KOUT2_FUN: CLK32KOUT2 pin functional definition

0: 32.768K clock output

1: Recovery function

Bit 0 CLK32KOUT2_EN: If CLK32KOUT2_FUN=0, then

1: CLK32KOUT2 is enabled 0: CLK32KOUT2 is disabled

15.2.2.2 VB_MON_REG: BATTERY VOLTAGE MONITOR REGISTER

ADDRESS	S: 21H	TYPE: RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	PLUG_IN _STS (RO)	VB_UV_ STS (RO)	VB_LO_ ACT	VB_LO_ STS (RO)	VB_LO_SEL		L
DEFAULT	0	0	0	1	0	1	0	0

DESCRIPTION

D:4 7	DECEDVED
RIT /	RESERVED

Bit 6 PLUG_IN_STS: charger plug-in event occurs(DC PIN voltage >3.8V)

0: no charger plug in1: charger pluged inThis bit is read only

Bit 5 VB_UV_STS: Battery under voltage lockout status(shut down system if the

bit=1)

This bit is read only

Bit 4 VB LO ACT: VBAT low action

0: shut down system1: insert interrupt

Bit 3 VB_LO_STS: Battery low voltage status





0: VBAT>VB_LO_SEL 1: VBAT<VB_LO_SEL This bit is used and a

This bit is read only

Bit 2-0 VB_LO_SEL: Battery low voltage threshold

000~111: 2.8V~ 3.5V, step=100mV

15.2.2.3 THERMAL REG: THERMAL CONTROL REGISTER

ADDRESS		TYPE: F	RW.					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	TSD_T EMP	HOTDIE_TEMP		HOTDIE_STS (RO)	TSD_STS (RO)
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-5 Reserved

Bit 4 TSD_TEMP: Thermal shutdown temperture threshold

0: 140°C; 1: 160°C

Bit 3-2 HOTDIE_TEMP: Hot-die temperature threshold

00: 85°C; **01**: 95°C; **10**: 105°C; **11**: 115°C;

Bit 1 HOTDIE STS: Hot-die warning

This bit is read only bit.

Bit 0 TSD-STS: Thermal shut down

15.2.3 POWER CHANNEL CONTROL/MONITOR REGISTERS 15.2.3.1 DCDC_EN_REG : DC-DC CONVERTER ENABLE REGISTER

ADDRESS: 23	TYPE: F	RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	OTG_E	SWITC	LDO9_	BOOST	BUCK4	BUCK3	BUCK2	BUCK1
	N	H_EN	EN	_EN	_EN	_EN	_EN	_EN
DEFAULT				Во	oot			

DESCRIPTION

Bit 7 OTG_EN, OTG enable

Enable
 Disable



DEFAULT value is set by boot.

Bit 6 SWITCH_EN: SWITCH enable

1: Enable 0: Disable

DEFAULT 由 bootSet.

Bit 5 LDO9_EN: LDO9 enable

1: Enable 0: Disable

DEFAULT value is set by boot.

Bit 4 BOOST EN: BOOST enable

1: Enable 0: Disable

The default value is set by boot.

Bit 3-0 BUCK(n)_EN: BUCKn enable

1: Enable 0: Disable

The default value is set by boot.

15.2.3.2 LDO_EN_REG: LDO ENABLE REGISTER

ADDRESS: 24	TYPE: F	RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	LDO8_	LDO7_	LDO6_	LDO5_	LDO4_	LDO3_	LDO2_	LDO1_
	EN	EN	EN	EN	EN	EN	EN	EN
DEFAULT				Во	oot			

DESCRIPTION

Bit 7-0 LDOn: LDO(n) enable

1: Enable0: Disable

The default value is set by boot.

15.2.3.3 SLEEP_SET_OFF_REG1 : SLEEP SET OFF REGISTER #1

ADDRES	SS: 25H			TYPE: R\	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0



	OTG_S	SWITCH_	1 DO0 CLD	BOOST_S	BUCK4_S	BUCK3_S	BUCK2_S	BUCK1_
SYMBOL	LP_SE	SLP_SET_	LDO9_SLP SET OFF	LP_SET_O	LP_SET_O	LP_SET_O	LP_SET_O	SLP_SE
	T_OFF	OFF	_561_0FF	FF	FF	FF	FF	T_OFF
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7 1: OTG is set off in sleep mode

0: No effect.

Bit 6 1: Switch is set off in sleep mode

0: No effect.

Bit 5 1: LDO9 is set off in sleep mode

0: No effect.

Bit 4 1: The boost converter is set off in sleep mode

0: No effect.

Bit 3 1: Buck4 is set off in sleep mode

0: No effect.

Bit 2 1: Buck3 is set off in sleep mode

0: No effect.

Bit 1 1: Buck2 is set off in sleep mode

0: No effect.

Bit 0 1: Buck1 is set off in sleep mode

0: No effect.

15.2.3.4 SLEEP_SET_OFF_REG2: SLEEP SET OFF REGISTER #2

ADDRESS: 26	TYPE: F	RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	LDO8_S	LDO7_S	LDO6_S	LDO5_S	LDO4_S	LDO3_S	LDO2_S	LDO1_S
	LP_SET_							
	OFF							
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7 1: LDO8 is set off in sleep mode

0: No effect.

Bit 6 1: LDO7 is set off in sleep mode

0: No effect.

Bit 5 1: LDO6 is set off in sleep mode



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0: No effect.

Bit 4 1: LDO5 is set off in sleep mode

0: No effect.

Bit 3 1: LDO4 is set off in sleep mode

0: No effect.

Bit 2 1: LDO3 is set off in sleep mode

0: No effect.

Bit 1 1: LDO2 is set off in sleep mode

0: No effect.

Bit 0 1: LDO1 is set off in sleep mode

0: No effect.

15.2.3.5 DCDC UV STS REG: DC-DC UNDER VOLTAGE STATUS REGISTER

ADDRE	ESS: 27H			TYPE: RO						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL	OTG_U	H5V_U	LDO9_UV	BOOST_	BUCK4_	BUCK3_	BUCK2_	BUCK1_		
	V_STS	V_STS	_STS	UV_STS	UV_STS	UV_STS	UV_STS	UV_STS		
DEFAUL	0	0	0	0	0	0	0	0		
Т										

DESCRIPTION

Bit 7 OTG_UV_STS: OTG under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 6 H5V_UV_STS: H5V under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 5 LDO9 UV STS: LDO9 under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 4 BOOST_UV_STS: BOOST under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 3 BUCK4_UV_STS: BUCK4 under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 2 BUCK3 UV STS: BUCK3 under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal



Bit 1 BUCK2_UV_STS: BUCK2 under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 0 BUCK1_UV_STS: BUCK1 under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

15.2.3.6 DCDC_UV_ACT_REG: DC-DC UNDER VOLTAGE ACTION REGISTER

ADDRE	ESS: 28H			TYPE: R\	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	OTG_U	H5V_U	LDO9_UV	BOOST_	BUCK4_	BUCK3_	BUCK2_	BUCK1_
	V_ACT	V_ACT	_ACT	UV_ACT	UV_ACT	UV_ACT	UV_ACT	UV_ACT
DEFAUL	0	0	0	0	0	0	0	0
Т								

DESCRIPTION

Bit 7 OTG_UV_ACT: OTG under voltage action.

1: Restart OTG

0: No effect

Bit 6 H5V_UV_ACT: H5V under voltage action.

1: Restart H5V

0: No effect

Bit 5 LDO9_UV_ACT: LDO9 under voltage action.

1: Restart LDO9

0: No effect

Bit 4 BOOST UV ACT: BOOST under voltage action.

1: shut down converter(this shut down action will also reset the BOOST EN bit to 0)

0: No effect

Bit 3 BUCK4_UV_ACT: BUCK4 under voltage action.

1: Restart BUCK4

0: No effect

Bit 2 BUCK3 UV ACT: BUCK3 under voltage action.

1: Restart BUCK3

0: No effect

Bit 1 BUCK2_UV_ACT: BUCK2 under voltage action.

1: Restart BUCK2

0: No effect





Bit 0

BUCK1 UV ACT: BUCK1 under voltage action. 1: Restart BUCK1

0: No effect

15.2.3.7 LDO UV STS REG: LDO UNDER VOLTAGE S TATUS REGISTER

ADDRES	SS: 29H		TYPE: RO)				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	LDO8_UV	LDO7_UV	LDO6_UV	LDO5_UV	LDO4_UV	LDO3_U	LDO2_U	LDO1_U
	_STS	_STS	_STS	_STS	_STS	V_STS	V_STS	V_STS
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Di+ 7	1DO0	1 11 /	ctc.	$I \cup O$	under veltage	\ flaa
Bit 7	LDUO	$\mathbf{U}\mathbf{v}$	DID.	LUUO	under voltage	: IIau.

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 6 LDO7_UV_STS: LDO7 under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

LDO6_UV_STS: LDO6 under voltage flag. Bit 5

1: Output voltage drop below 85% of nominal voltage

0: Normal

LDO5 UV STS: LDO5 under voltage flag. Bit 4

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 3 LDO4 UV STS: LDO4 under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 2 LDO3_UV_STS: LDO3 under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 1 LDO2 UV STS: LDO2 under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

Bit 0 LDO1 UV STS: LDO1 under voltage flag.

1: Output voltage drop below 85% of nominal voltage

0: Normal

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15.2.3.8 LDO UV ACT REG: LDO UNVER VOLTAGE ACTION REGISTER

ADDRESS: 2A	TYPE: RW							
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	LDO8_U	LDO7_U	LDO6_U	LDO5_U	LDO4_U	LDO3_U	LDO2_U	LDO1_U
	V_ACT	V_ACT	V_ACT	V_ACT	V_ACT	V_ACT	V_ACT	V_ACT
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7 LDO8_UV_ACT: LDO8 under voltage action

1: Restart LDO8

0: No effect

Bit 6 LDO7_UV_ACT: LDO7 under voltage action

1: Restart LDO7

0: No effect

Bit 5 LDO6_UV_ACT: LDO6 under voltage action

1: Restart LDO6

0: No effect

Bit 4 LDO5_UV_ACT: LDO5 under voltage action

1: Restart LDO5

0: No effect

Bit 3 LDO4_UV_ACT: LDO4 under voltage action

1: Restart LDO4

0: No effect

Bit 2 LDO3_UV_ACT: LDO3 under voltage action

1: Restart LDO3

0: No effect

Bit 1 LDO2_UV_ACT: LDO2 under voltage action

1: Restart LDO2

0: No effect

Bit 0 LDO1_UV_ACT: LDO1 under voltage action

1: Restart LDO1

0: No effect

15.2.3.9 DCDC_PG_REG: DC-DC POWER GOOD STATUS REGISTER

ADDRES	ADDRESS: 2BH			TYPE: RO						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		



SYMBOL	OTG_ PG_S TS	H5V_P G_STS	LDO9_P G_STS	BOOST_ PG_STS	BUCK4_P G_STS	BUCK3_P G_STS	BUCK2_P G_STS	BUCK1_P G_STS
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

	DESCRIPTION
Bit 7	OTG_PG_STS: OTG power good flag.
	1: Power good, Vout>90% of setting voltage
	0: Power not good, Vout<90% of setting voltage
Bit 6	H5V_PG_STS: H5V power good flag.
	 Power good, Vout>90% of setting voltage
	0: Power not good, Vout<90% of setting voltage
Bit 5	LDO9_PG_STS: LDO9 power good flag.
	 Power good, Vout>90% of setting voltage
	0: Power not good, Vout<90% of setting voltage
Bit 4	BOOST_PG_STS: BOOST power good flag.
	 Power good, Vout>90% of setting voltage
	0: Power not good, Vout<90% of setting voltage
Bit 3	BUCK4_PG_STS : BUCK4 power good flag.
	 Power good, Vout>90% of setting voltage
	0: Power not good, Vout<90% of setting voltage
Bit 2	BUCK3_PG_STS : BUCK3 power good flag.
	 Power good, Vout>90% of setting voltage
	0: Power not good, Vout<90% of setting voltage
Bit 1	BUCK2_PG_STS : BUCK2 power good flag.
	 Power good, Vout>90% of setting voltage
	0: Power not good, Vout<90% of setting voltage
Bit 0	BUCK1_PG_STS : BUCK1 power good flag.
	1: Power good, Vout>90% of setting voltage
	0: Power not good, Vout<90% of setting voltage

15.2.3.10 LDO_PG_REG : LDO POWER GOOD STATUS REGISTER

ADDRES	SS: 2CH	TYPE: RO)					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	LDO8_PG	LDO7_PG	LDO6_PG	LDO5_PG	LDO4_PG	LDO3_P	LDO2_P	LDO1_P
	_STS	_STS	_STS	_STS	_STS	G_STS	G_STS	G_STS



DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

- Bit 7 LDO8 PG STS: LDO8 power good flag.
 - 1: Power good, Vout>90% of setting voltage
 - 0: Power not good, Vout<90% of setting voltage
- Bit 6 LDO7_PG_STS: LDO7 power good flag.
 - 1: Power good, Vout>90% of setting voltage
 - 0: Power not good, Vout<90% of setting voltage
- Bit 5 LDO6_PG_STS: LDO6 power good flag.
 - 1: Power good, Vout>90% of setting voltage
 - 0: Power not good, Vout<90% of setting voltage
- Bit 4 LDO5 PG STS: LDO5 power good flag.
 - 1: Power good, Vout>90% of setting voltage
 - 0: Power not good, Vout<90% of setting voltage
- Bit 3 LDO4_PG_STS: LDO4 power good flag.
 - 1: Power good, Vout>90% of setting voltage
 - 0: Power not good, Vout<90% of setting voltage
- Bit 2 LDO3 PG STS: LDO3 power good flag.
 - 1: Power good, Vout>90% of setting voltage
 - 0: Power not good, Vout<90% of setting voltage
- Bit 1 LDO2_PG_STS: LDO2 power good flag.
 - 1: Power good, Vout>90% of setting voltage
 - 0: Power not good, Vout<90% of setting voltage
- Bit 0 LDO1 PG STS: LDO1 power good flag.
 - 1: Power good, Vout>90% of setting voltage
 - 0: Power not good, Vout<90% of setting voltage

15.2.3.11 VOUT MON TDB REG: VOUT DEBOUNCE MONITOR REGISTER

ADDRES	SS: 2DH	TYPE: RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RESV	RESV	VOUT_M	ON_TDB
DEFAULT	0	0	0	0	0	0	1	0



DESCRIPTION

Bit 7-2 Reserved

Bit 1-0 VOUT_MON_TDB: Vout monitor debouncing time(UV_STS rising edge and PG_STS rising edge debounce time)

00: 62us

01: 124us(default)

10: 186us 11: 248us

15.2.4 POWER CHANNEL CONFIGURATION REGISTER 15.2.4.1 BUCK1_CONFIG_REG : BUCK1 CONFIGURATION REGISTER

ADDRES	SS: 2EH			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	RESV	BUCK1_ PHASE	RESV	BUCK1	_RATE	BU	CK1_ILMIN		
DEFAULT	0	0	0	1	1	0	1	0	

DESCRIPTION

Bit 7 Reserved

Bit 6 BUCK1 PHASE,

0: Normal,

1: Inverted

Bit 5 Reserved

Bit 4-3 BUCK1_RATE: Voltage change rate after DVS

00: 2mv/us01: 4mv/us10: 6mv/us11: 10mv/us

Bit 2-0 BUCK1_ILMIN:

000: 50mA, 001: 100mA, 010: 150mA, 011: 200mA 100: 250mA, 101: 300mA, 110: 350mA, 111: 400mA

15.2.4.2 BUCK1_ON_VSEL : BUCK1 ACTIVE MODE REGISTER

ADDRES	SS: 2FH	TYPE: RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	BUCK1_O N_FPWM	RESV			BUCK1_C	N_VSEL		



DEFAULT	0	0	Boot

DESCRIPTION

Bit 7 BUCK1 ON FPWM:

1: Forced PWM mode in active mode.

0: PWM/PFM auto change mode.(default)

Bit 6 Reserved

Bit 5-0 BUCK1_ON_VSEL: BUCK1 active mode voltage selection,

 $0.7125V \sim 1.5V$, step=12.5mV

000 000: 0.7125V 000 001: 0.725V

••••

111 111: 1.5V

The default value is set by boot.

15.2.4.3 BUCK1_SLP_VSEL: BUCK1 SLEEP MODE REGISTER

ADDRES	SS: 30H		TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	BUCK1_S LP_FPWM	RESV			BUCK1_SI	LP_VSEL		
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7 BUCK1_SLP_FPWM:

1: Forced PWM mode in sleep mode.

0: PWM/PFM auto change mode.(default)

Bit 6 Reserved

Bit 5-0 BUCK1_SLP_VSEL: BUCK1 sleep mode voltage selection, 0.7125V~1.5V,

step=12.5mV

000 000: 0.7125V 000 001: 0.725V

.

111 111: 1.5V

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15.2.4.4 BUCK2 CONFIG REG: BUCK2 CONFIGURATION REGISTER

ADDRESS: 32H				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	RESV	BUCK2_ PHASE	RESV	BUCK2	ВІ	JCK2_ILM	IN		
DEFAULT	0	0	0	1	1	0	1	0	

DESCRIPTION

Bit 7 Reserved

Bit 6 BUCK2_PHASE,

0: Normal,

1: Inverted

Bit 5 Reserved

Bit 4-3 BUCK2_RATE: Voltage change rate after DVS.

00: 2mv/us

01: 4mv/us

10: 6mv/us

11: 10mv/us

Bit 2-0 BUCK2 ILMIN:

000: 50mA, 001: 100mA, 010: 150mA, 011: 200mA 100: 250mA, 101: 300mA, 110: 350mA, 111: 400mA

15.2.4.5 BUCK2_ON_VSEL : BUCK2 ACTIVE MODE REGISTER

ADDRESS: 33H				TYPE: R	W				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	BUCK2_O N_FPWM	RESV	BUCK2_ON_VSEL						
DEFAULT	0	0	Boot						

DESCRIPTION

Bit 7 BUCK2_ON_FPWM

1: Forced PWM mode in active mode.

0: PWM/PFM auto change mode.(default)

Bit 6 Reserved

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Bit 5-0 BUCK2_ON_VSEL: BUCK2 active mode voltage selection, 0.7125V~1.5V ,

step=12.5mV

000 000: 0.7125V 000 001: 0.725V

.

111 111: 1.5V

The default value is set by boot.

15.2.4.6 BUCK2_SLP_VSEL: BUCK2 SLEEP MODE REGISTER

ADDRESS: 34H				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	BUCK2_S LP_FPWM	RESV	BUCK2_SLP_VSEL						
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7 BUCK2 SLP FPWM:

1: Forced PWM mode in sleep mode.

0: PWM/PFM auto change mode.(default)

Bit 6 Reserved

Bit 5-0 BUCK2_SLP_VSEL: BUCK1 sleep mode voltage selection, 0.7125V~1.5V,

step=12.5mV

000 000: 0.7125V 000 001: 0.725V

.

111 111: 1.5V

15.2.4.7 BUCK3_CONFIG_REG: BUCK3 CONFIGURATION REGISTER

ADDRESS: 36H				TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	BUCK3_O N_FPWM	BUCK3_ PHASE	RESV	RESV	RESV	BUCK3_ILMIN		N
DEFAULT	0	0	0	0	0	0	1	0

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DESCRIPTION

Bit 7 BUCK3 ON FPWM:

1: Forced PWM mode in active mode.

0: PWM/PFM auto change mode.(default)

Bit 6 BUCK3_PHASE,

0: Normal,

1: Inverted

Bit 5-3 Reserved

Bit 2-0 BUCK3_ILMIN:

000: 50mA, 001: 100mA, 010: 150mA, 011: 200mA 100: 250mA, 101: 300mA, 110: 350mA, 111: 400mA

15.2.4.8 BUCK4_CONFIG_REG: BUCK4 CONFIGURATION REGISTER

ADDRESS: 37H				TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	BUCK4_ PHASE	RESV	RESV	RESV	BUCK4_ILMIN		
DEFAULT	0	0	0	0	0	0	1	0

DESCRIPTION

Bit 7 RESERVED

Bit 6 BUCK4_PHASE,

0: Normal,

1: Inverted

Bit 2-0 BUCK4_ILMIN:

000: 50mA, 001: 100mA, 010: 150mA, 011: 200mA 100: 250mA, 101: 300mA, 110: 350mA, 111: 400mA

15.2.4.9 BUCK4 ON VSEL: BUCK4 ACTIVE MODE REGISTER

ADDRESS: 38H				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	BUCK4_O N_FPWM	RESV	RESV	BUCK4_ON_VSEL					
DEFAULT	0	0	0			Boot			





DESCRIPTION

Bit 7 BUCK4_ON_FPWM:

1: Forced PWM mode in active mode.

0: PWM/PFM auto change mode.(default)

Bit 6-4 **RESERVED**

Bit 3-0 BUCK4_ON_VSEL: BUCK4 active mode voltage selection, 1.8V~3.3V,

step=100Mv

00000: 1.8V 00001: 1.9V

01110: 3.2V 01111: 3.3V 10000: 3.4V 10001: 3.5V 10010: 3.6V

The default value is set by boot.

BUCK4_SLP_VSEL: BUCK4 SLEEP MODE REGISTER 15.2.4.10

ADDRES	SS: 39H			TYPE: R\	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	BUCK4_S LP_FPWM	RESV	RESV		BUC	K4_SLP_VS	SEL	
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

BUCK4_SLP_FPWM: Bit 7

1: Forced PWM mode in sleep mode.

0: PWM/PFM auto change mode.(default)

Bit 6-5 Reserved

Bit 4-0 BUCK4_SLP_VSEL: BUCK4 sleep mode voltage selection, 1.8V~3.3V ,

step=100Mv

00000: 1.8V 00001: 1.9V

01110: 3.2V 01111: 3.3V



10000: 3.4V 10001: 3.5V 10010: 3.6V

15.2.4.11 BOOST_CONFIG_REG: BOOST CONFIGURATIN REGISTER

ADDRES	ADDRESS: 3AH				1			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	BOOST_A NTI_RING	BOOST_ PHASE	BOOST_	ILMAX	ВС	OST_ILMI	N
DEFAULT	0	0	0	0	1	0	1	0

DESCRIPTION

Bit 7 RESERVED

Bit 6 BOOST_ANTI_RING: BOOST anti-ring enable

0: Disable1: Enable

Bit 5 BOOST_PHASE,

0: Normal

1: Inverted

Bit 4-3 BOOST_ILMAX:

00: 4A,01: 4.5A,10: 5A,11: 5.5A

Bit 2-0 BOOST_ILMIN:

000: 75mA, 001: 100mA, 010: 125mA, 011: 150mA 100: 175mA, 101: 200mA, 110: 225mA, 111: 250mA

15.2.4.12 LDO1_ON_VSEL_REG: LDO1 ACTIVE MODE VOLTAGE REGISTER

ADDRES	SS: 3BH		TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV		LDO1_	ON_VSEL		
DEFAULT	0	0	0		E	3oot		

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DESCRIPTION

Bit 7-5 **RESERVED**

LDO1_ON_VSEL: LDO1 active mode voltage selection, 1.8V~3.4V, Bit 4-0

step=0.1V

00000: 1.8V 00001: 1.9V

01110: 3.2V 01111: 3.3V 10000: 3.4V

The default value is set by boot.

15.2.4.13 LDO1_SLP_VSEL_REG : LDO1 SLEEP MODE VOLTAGE SELECT **REGISTER**

ADDRES	ADDRESS: 3CH				N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV		LDO	1_SLP_VS	SEL	_
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-5 Reserved

Bit 4-0 LDO1_SLP_VSEL: LDO1 SLEEP mode voltage selection. 1.8V~3.4V,

step=0.1V

00000: 1.8V 00001: 1.9V

01110: 3.2V 01111: 3.3V

10000: 3.4V

15.2.4.14 LDO2_ON_VSEL_REG: LDO2 ACTIVE MODE VOLTAGE SELECT **REGISTER**

ADDRES	SS: 3DH		TYPE: R\	N				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV		LDC	02_ON_VSE	L	
DEFAULT	0	0	0			Boot		



DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO2_ON_VSEL: LDO2 active mode voltage selection. 1.8V~3.4V, step=0.1V

00000: 1.8V 00001: 1.9V

- - -

01110: 3.2V 01111: 3.3V 10000: 3.4V

DEFAULT value is set by boot.

15.2.4.15 LDO2_SLP_VSEL_REG : LDO2 SLEEP MODE VOLTAGE SELECT REGISTER

ADDRES	ADDRESS: 3EH				N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV		LDO2	_SLP_VSE	EL .	
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO2_SLP_VSEL: LDO2 sleep mode voltage selection.

1.8V~3.4V, step=0.1V

00000: 1.8V 00001: 1.9V

. . . .

01110: 3.2V 01111: 3.3V 10000: 3.4V

15.2.4.16 LDO3_ON_VSEL_REG : LDO3 ACTIVE MODE VOLTAGE SELECT REGISTER

ADDRES	SS: 3FH			TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV		LDO3_0	ON_VSEL	
DEFAULT	0	0	0	0		В	oot	



DESCRIPTION

Bit 7-4 RESERVED

Bit 4-3 LDO3_ON_VSEL: LDO3 active mode voltage selection.

0.8V~2.5V, step=0.1V

0000: 0.8V 0001: 0.9V

- - -

1100: 2.0V 1101: 2.2V 1111: 2.5V

DEFAULT value is set by boot.

15.2.4.17 LDO3_SLP_VSEL_REG : LDO3 SLEEP MODE VOLTAGE SELECT REGISTER

ADDRES	ADDRESS: 40H				TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	RESV	RESV	RESV	RESV		LDO3_SL	P_VSEL		
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 LDO3_SLP_VSEL: LDO3 sleep mode voltage selection.

0.8V~2.5V, step=0.1V

0000: 0.8V 0001: 0.9V

. . . .

1100: 2.0V 1101: 2.2V 1111: 2.5V

DEFAULT value is set by boot.

15.2.4.18 LDO4_ON_VSEL_REG: LDO4 ACTIVE MODE VOLTAGE SELECT

ADDRES	SS: 41H	TYPE: F	RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV		LDC	04_ON_VS	EL	
DEFAULT	0	0	0			Boot		

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO4_ON_VSEL: LDO4 active mode voltage selection.

1.8V~3.4V, step=0.1V

00000: 1.8V 00001: 1.9V

- - -

01110: 3.2V 01111: 3.3V 10000: 3.4V

DEFAULT value is set by boot.

15.2.4.19 LDO4_SLP_VSEL_REG : LDO4 SLEEP MODE VOLTAGE SELECT REGISTER

ADDRES	SS: 42H	TYPE: F	RW.					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV		LDO	4_SLP_VS	SEL	
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO2_SLP_VSEL: LDO2 sleep mode voltage selection.

1.8V~3.4V, step=0.1V

00000: 1.8V 00001: 1.9V

. . . .

01110: 3.2V 01111: 3.3V 10000: 3.4V

15.2.4.20 LDO5_ON_VSEL_REG : LDO5 ACTIVE MODE VOLTAGE SELECT REGISTER

ADDRES	ADDRESS: 43H				TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	



SYMBOL	RESV	RESV	RESV	LDO5_ON_VSEL
DEFAULT	0	0	0	Boot

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO5_ON_VSEL: LDO5 active mode voltage selection.

1.8V~3.4V, step=0.1V

00000: 1.8V 00001: 1.9V

. . . .

01110: 3.2V 01111: 3.3V 10000: 3.4V

DEFAULT is set by boot.

15.2.4.21 LDO5_SLP_VSEL_REG : LDO5 SLEEP MODE VOLTAGE SELECT REGISTER

ADDRESS: 44H				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	RESV	RESV	RESV	LDO5_SLP_VSEL					
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO5_SLP_VSEL: LDO5 sleep mode voltage selection.

1.8V~3.4V, step=0.1V

00000: 1.8V 00001: 1.9V

. . . .

01110: 3.2V 01111: 3.3V 10000: 3.4V

15.2.4.22 LDO6_ON_VSEL_REG : LDO6 ACTIVE MODE VOLTAGE SELECT REGISTER



Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	RESV	RESV	RESV	LDO6_ON_VSEL					
DEFAULT	0	0	0	Boot					

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO6_ON_VSEL: LDO6 active mode voltage selection.

0.8V~2.5V, step=0.1V

00000: 0.8V 00001: 0.9V

.

10000: 2.4V 10001: 2.5V

DEFAULT is set by boot.

15.2.4.23 LDO6_SLP_VSEL_REG : LDO6 SLEEP MODE VOLTAGE SELECT REGISTER

ADDRES	TYPE: F	RW							
Bit	Bit7	Bit6	Bit5	Bit4 Bit3 Bit2 Bit1 Bit0					
SYMBOL	RESV	RESV	RESV	LDO6_SLP_VSEL					
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO6_SLP_VSEL: LDO6 sleep mode voltage selection.

0.8V~2.5V, step=0.1V

00000: 0.8V 00001: 0.9V

.

10000: 2.4V 10001: 2.5V

15.2.4.24 LDO7_ON_VSEL_REG : LDO7 ACTIVE MODE VOLTAGE SELECT REGISTER

ADDRESS: 47H	TYPE: RW



Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	RESV	RESV	RESV	LDO7_ON_VSEL					
DEFAULT	0	0	0	Boot					

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO7_ON_VSEL: LDO7 active mode voltage selection.

0.8V~2.5V, step=0.1V

00000: 0.8V 00001: 0.9V

.

10000: 2.4V 10001: 2.5V

DEFAULT is set by boot.

15.2.4.25 LDO7_SLP_VSEL_REG : LDO7 SLEEP MODE VOLTAGE SELECT REGISTER

ADDRESS: 48H				TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	LDO7_SLP_VSEL				
DEFAUL T	0	0	0	0	0	0	0	0
T	-	-	-	_	_	-		

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO7_SLP_VSEL: LDO7 sleep mode voltage selection.

0.8V~2.5V, step=0.1V

00000: 0.8V 00001: 0.9V

.

10000: 2.4V 10001: 2.5V





15.2.4.26 LDO8_ON_VSEL_REG : LDO8 ACTIVE MODE VOLTAGE SELECT REGISTER

ADDRES	TYPE: RW								
Bit	Bit7	Bit6	Bit5	Bit4 Bit3 Bit2 Bit1 Bit0					
SYMBOL	RESV	RESV	RESV	LDO8_ON_VSEL					
DEFAULT	0	0	0	Boot					

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO8_ON_VSEL: LDO8 active mode voltage selection.

1.8V~3.4V, step=0.1V

00000: 1.8V 00001: 1.9V

. . . .

01110: 3.2V 01111: 3.3V 10000: 3.4V

DEFAULT is set by boot.

15.2.4.27 LDO8_SLP_VSEL_REG : LDO8 SLEEP MODE VOLTAGE SELECT REGISTER

ADDRESS: 4AH				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	RESV	RESV	RESV	LDO8_SLP_VSEL					
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-5 RESERVED

Bit 4-0 LDO8_SLP_VSEL: LDO8 sleep mode voltage selection.

1.8V~3.4V, step=0.1V

00000: 1.8V 00001: 1.9V

. . . .

01110: 3.2V 01111: 3.3V 10000: 3.4V



15.2.4.28 DEV CTRL_REG : DEVICE CONTROL REGISTER

ADDRESS: 4BH				TYPE: R\	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	PWRO N_LP_ ACT	PWRON_LP_OFF_TI ME		DEV_OFF _RST	RESV	DEV_SL P	DEV_O FF
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7 RESERVED

Bit 6 Long Press Action Selection

0: Power off

1: Power off and restart

Bit 5-4 PWRON_LP_OFF_TIME: PWRON long press turn off time:

00: 6s 01: 8s 10: 10s 11: 12s

Bit 3 DEV_OFF_RST: Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event) and activate reset of the digital core.

Bit 2 Reserved

Bit 1 DEV_SLP: Write 1 allows SLEEP device state (if DEV_OFF = 0 and DEV_OFF_RST = 0).

Write '0' will start a SLEEP to ACTIVE device state transition (wake-up event) (if DEV_OFF = 0 and DEV_OFF_RST = 0). This bit is cleared in OFF state.

Bit 0 DEV_OFF: Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event). This bit is cleared in OFF state.

15.2.5 **INTERRUPT REGISTER**

15.2.5.1 INT STS REG1: INTERRUPT STATUS REGISTER #1

ADDRESS: 4CH	TYPE: RW	



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Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMB OL	USB_OV_I NT(Write 1 clr or RegA3<7> =0 clr	RTC_PERI OD_INT (Write 1 clr)	RTC_ALA RM_INT (Write 1 clr)	HOTDI E_INT (Write 1 clr)	PWRON _LP_INT (Write 1 clr)	PWRO N_INT (Write 1 clr)	VB_LO _INT (Write 1 clr)	VOUT_L O_INT (Write 1 clr)
DEFA	0	0	0	0	0	0	0	0
ULT								

DESCRIPTION

	1100 01/100 1100
Bit 7	USB_OV_INT: USB over voltage event interrupt.
Bit 6	RTC_PERIOD_INT: RTC period event interrupt.
Bit 5	RTC_ALARM_INT: RTC alarm event interrupt.
Bit 4	HOTDIE_INT: Hot die event interrupt status.
Bit 3	PWRON_LP_INT: PWRON PIN long press event interrupt status.
Bit 2	PWRON_INT: PWRON event interrupt status.
Bit 1	VB_LO_INT: Battery under voltage alarm event interrupt status.
Bit 0	VOUT_LO_INT: VOUT under voltage alarm event interrupt status
Note:	1: Interrupt asserted, write "1" to clear
	0: No interrupt

15.2.5.2 INT_MSK_REG1: INTERRUPT MASK REGISTER #1

ADDF	RESS: 4DF	1		TYPE: R\	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBO	USB_OV	RTC_PE	RTC_AL	HOTDIE_	PWRON	PWRON	VB_LO_I	VOUT_
L	_INT_IM	RIOD_IM	ARM_IM	IM	_LP_IM	_IM	М	LO_IM
DEFAU	0	0	0	0	0	0	0	0
LT								

DESCRIPTION

Bit 7	USB_OV_INT_IM: USB over voltage event interrupt mask.							
Bit 6	RTC_PERIOD_INT: RTC period event interrupt mask.							
Bit 5	RTC_ALARM_INT: RTC alarm event interrupt mask.							
Bit 4	HOTDIE_INT: Hot die event interrupt status mask.							
Bit 3	PWRON_LP_INT: PWRON PIN long press event interrupt status mask.							
Bit 2	PWRON_INT: PWRON event interrupt status mask.							
Bit 1	VB_LO_INT: Battery under voltage alarm event interrupt status							





mask.

Bit 0 VOUT_LO_IM: Vout under voltage alarm event interrupt status mask

Note: 1: Mask the specified interrupt

0: Do not mask the specified interrupt

15.2.5.3 INT_STS_REG2: INTERRUPT STATUS REGISTER#2

AD	DRESS:	4EH		TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMB OL	DISCHG_ILI M_INT (Write 1 clr)	CHG_CVTLIM_I NT (Write 1 clr or RegA3<7>=0 clr)	TS2_IN T (Write 1 clr)	CHGTS1_INT (Write 1 clr or RegA3<7>=0 clr)	CHGTE_INT (Write 1 clr or RegA3<7>=0 clr)	CHGOK_INT (Write 1 clr or RegA3<7>=0 clr)	PLUG_OUT_IN T (Write 1 clr)	PLUG_IN_I NT (Write 1 clr)
DEFAU	0	0	0	0	0	0	0	0
LT								

DESCRIPTION

	DESCRIPTION
Bit 7	DISCHG_ILIM_INT: Discharging triggering current limit event interrupt.
Bit 6	CHG_CVTLIM_INT: Charging triggering input voltage limit, or current limit, or
	temperature protection event interrupt.
Bit 5	TS2_INT: TS2 value exceeding upper or lower limits event interrupt.
Bit 4	CHGTS1_INT: TS1 value exceeding upper or lower limits event interrupt.
Bit 3	CHGTE_INT: Charging overtime event interrupt.
Bit 2	CHGOK_INT: Charging termination event interrupt
Bit 1	PLUG_OUT_INT: charger plug out event interrupt(PLUG_IN_STS falling
	edge interrupt)
Bit 0	PLUG_IN_INT: charger plug in event interrupt(PLUG_IN_STS rising
	edge interrupt)

Note: Write "1" to clear.

15.2.5.4 INT_STS_MSK_REG2 : INTERRUPT MASK REGISTER#2

ADD	RESS: 4F	Ή		TYPE: F	RW			
Bit	Bit7 Bit6 Bit5			Bit4	Bit3	Bit2	Bit1	Bit0
SYMB	DISCHG_IL	CHG_CVTL	TS2_I	CHGTS1	CHGTE_I	CHGOK	PLUG_OU	PLUG_IN
OL	IM_INT_IM	IM_INT_IM	NT_IM	_INT_IM	NT_IM	_INT_IM	T_INT_IM	_INT_IM



DEFA	0	0	0	0	0	0	0	0
ULT								

DESCRIPTION

- Bit 7 DISCHG_ILIM_INT_IM: Discharging triggering current limit event interrupt mask
 - 1: Mask the interrupt
 - 0: Do not mask the interrupt
- Bit 6 CHG_CVTLIM_INT_IM: Charging triggering input voltage limit, or current limit, or temperature protection event interrupt mask.
 - 1: Mask the interrupt
 - 0: Do not mask the interrupt
- Bit 5 TS2_INT_IM: TS2 value exceeding upper or lower limits event interrupt mask
 - 1: Mask the interrupt
 - 0: Do not mask the interrupt
- Bit 4 CHGTS1_INT_IM:TS1 value exceeding upper or lower limits event interrupt mask.
 - 1: Mask the interrupt
 - 0: Do not mask the interrupt
- Bit 3 CHGTE_INT_IM: Charging overtime event interrupt mask
 - 1: Mask the interrupt
 - 0: Do not mask the interrupt
- Bit 2 CHGOK_INT_IM: Charging termination event interrupt mask.
 - 1: Mask the interrupt
 - 0: Do not mask the interrupt
- Bit 1 PLUG_OUT_INT_IM: Charger plug out event interrupt mask.
 - 1: Mask the interrupt
 - 0: Do not mask the interrupt
- Bit 0 PLUG IN INT IM: Charger plug in event interrupt mask
 - 1: Mask the interrupt
 - 0: Do not mask the interrupt

15.2.5.5 IO POL REG: IO POLARITY REGISTER

ADDRES	SS: 50H			TYPE: F	RW			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RESV	RESV	RESV	INT_POL
DEFAULT	0	0	0	0	0	0	0	0

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DESCRIPTION

Bit 7-1 RESERVED

Bit 0 INT POL: INT pin polarity

0: active low1: active high

15.2.6 **BOOST/OTG/DCDC REGISTER**

15.2.6.1 H5V_EN_REG:

ADDRES			TYPE: F	₹W				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RESV	BST_UHV_S T	REF_RDY_C TRL	H5V_EN
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-3 RESERVED

Bit 2 BST_UHV_ST: Boost over load enable

0: Enable1: Disable

Bit 1 REF_RDY_CTRL: ref_rdy control

0: After PMIC is powered up, if vref is lower than a preset value, then ref_rdy

can be switched to logic low level.

1: After PMIC is powered up, if vref is lower than a preset value, then RED_rdy

must be kept at logic high level.

Bit 0 H5V_EN: HDMI 5V enable control

1: Enable 0: Disable

15.2.6.2 SLEEP_SEL_OFF_REG3:

ADDRES	SS: 53H			TYPE: F	RW			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RESV	RESV	RESV	H5V_SLP_SET_ OFF
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION





Bit 7-1 RESERVED

Bit 0 1: HDMI 5V disabled in the SLEEP mode

0: HDMI 5V enabled in the SLEEP mode

15.2.6.3 BOOST_LDO9_ON_VSEL_REG:

ADDRESS: 54H				TYPE: F	RW			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	BOOST	_ON_VS	EL	LDO9_ON_VSEL				
DEFAULT					由 BOOT 🖟	分 定		

DESCRIPTION

Bit 7-5 BOOST_ON_VSEL<2:0>: BOOST active mode voltage selection

000: 4.7V 001: 4.8V 010: 4.9V 011: 5V 100: 5.1V 101: 5.2V 110: 5.3V 111: 5.4V

Bit 4-0 LDO9_ON_VSEL: LDO9 active mode voltage selection

1.8V~3.4V, step=0.1V

00000: 1.8V 00001: 1.9V

. . . .

01110: 3.2V 01111: 3.3V 10000: 3.4V

Default value is set by boot.

15.2.6.4 BOOST_LDO9_SLP_VSEL_REG:

ADDRES	SS: 55H			TYPE: F	RW			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	BOOST_SLP_VSEL			LDO9_SLP_VSEL				
DEFAULT	0	0 1 1			0	0	0	0

DESCRIPTION

Bit 7-5 BOOST_SLP_VSEL<2:0>: BOOST SLEEP mode voltage selection

000: 4.7V 001: 4.8V

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010: 4.9V 011: 5V 100: 5.1V 101: 5.2V 110: 5.3V 111: 5.4V

Bit 4-0 LDO9_SLP_VSEL: LDO9 SLEEP mode voltage selection

1.8V~3.4V, step=0.1V

00000: 1.8V 00001: 1.9V

. . .

01110: 3.2V 01111: 3.3V 10000: 3.4V

15.2.6.5 BOOST_CTRL_REG: BOOST 控制 REGISTER

ADDRES	ADDRESS: 56H				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL	RESV	BST_H V_ST	BST_SWI TCH_VT	BST_SWIT CH_VT_HY S	BST_SWI TCH_EN	RESV	RESV	RESV		
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7 RESERVED

Bit 6 BST_HV_ST: boost startup with heavy load

0: disable

1: enable

Bit 5 BST_SWITCH_VT: Switching threshold from Boost mode to Switch mode.

0: 3.8V

1: 3.9V

Bit 4 BST_SWITCH_VT_HYS: Hysteresis of switching threshold from Boost mode to

Switch mode.

0: 200mV 1: 300mV

Bit 3 BST_SWITCH_EN: Boost operating in the switch mode enable control.

0: Disable

1: Enable

Bit 2:0 RESERVED



15.2.6.6 DCDC_ILMAX: DCDC inductor peak current register

ADDRESS: 56H				TYPE: RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL	BUCK4_	ILMAX	BUCK3_IL	MAX	BUCK2_II	_MAX	BUCK1_ILMAX			
DEFAULT	0	1	0	1	0	1	0	1		

DESCRIPTION

Bit 7:6 BUCK4_ILMAX:BUCK4 inductor peak current bit

00: 2.5A 01:3A 10:3.5A 11:4A

Bit 5:4 BUCK3 ILMAX:BUCK3 inductor peak current bit

00: 2A 01:2.5A 10:3A 11:3.5A

Bit 3:2 BUCK2 ILMAX:BUCK2 inductor peak current bit

Bit 1:0 BUCK1 ILMAX:BUCK1 inductor peak current bit

15.2.7 CHARGER SET REGISTER 15.2.7.1 CHRG_COMP_REG:

ADDRESS: 9AH TYP			TYPE: R\	E: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RE	SV	BAT_SYS_CMP_DL Y		CHRG_	IRVS	CHRG_OUTC\	/_COMP
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-6 RESERVED

Bit 5-4 BAT_SYS_CMP_DLY: Delay time for the voltage comparator between BAT and

SYS.

00: 20uS 10: 10uS 01: 40uS 11: 20uS

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Bit 3-2 CHRG_IRVS: Setting the charger reverse current.

Bit 1-0 CHRG_OUTCV_COMP: Setting the charger output voltage loop compensation

15.2.7.2 SUP STS REG:

ADDRES	ADDRESS: A0H				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL	BAT_EXS	С	CHG_STS			USB_IL	USB_EXS	USB_EFF		
STIVIBOL	(Read only)	(Read only)			LIM_EN	IM_EN	(Read only)	(Read only)		
DEFAULT	0	0	0	0	1	1	0	0		

DESCRIPTION

Bit 7 BAT_EXS: Battery existence monitor

0: No battery

1: With battery

Bit 6-4 CHG_STS: Charging status

000: No Charging

001: Wakeup current charging010: Trickle current charging

011: Constant current or constant voltage charging

100: Charging termination101: USB over voltage

110: Battery temperature fault

111: Charging time fault

Bit 3 USB_VLIM_EN: USB input voltage limit enable control

0: Disable1: Enable

Bit 2 USB_ILIM_EN: USB input current limit enable control

0: Disable1: Enable

Bit 1 USB_EXS: USB plug-in monitor

0: No USB plugged in1: USB plugged in

Bit 0 USB EFF: USB fault monitor

0: USB fault 1: USB okay





15.2.7.3 USB CTRL REG:

ADDRES	SS: A1H			TYPE: I	RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL	CHRG_ CT_EN	USB_	USB_VLIM_SEL			USB_ILIM_SEL				
DEFAULT					OTP					

DESCRIPTION

Bit 7 CHRG_CT_EN: Charger Thermal foldback enable

0:disable

1:enable

Bit 6-4 USB_VLIM_SEL: USB input voltage selection

000: 4.0V, 001: 4.1V, 010: 4.2V, 011: 4.3V

100: 4.4V, 101: 4.5V, 110: 4.6V, 111: 4.7V

Bit 3-0 USB_ILIM_SEL: USB input current selection

0000: 0.45A, 0001: 0.08A, 0010: 0.85A, 0011: 1A,

0100: 1.25A, 0101: 1.5A, 0110: 1.75A, 0111: 2A,

1000: 2.25A, 1001: 2.5A, 1010: 2.75A, 1011: 3A,

11xx:3A

DEFAULT value is set by BOOT

15.2.7.4 CHRG_CTRL_REG1: CHARGE CONTROL REGISTER1

ADDRES	ADDRESS: A3H				RW.					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL	CHRG_ EN	CHRG	CHRG_VOL_SEL			_SEL CHRG_CUR_SEL				
DEFAULT	1	0	1	1	0	1	0	1		

DESCRIPTION

Bit 7 CHRG_EN: Charger enable

0: Disable

1: Enable

Bit 6-4 CHRG_VOL_SEL: Charging termination voltage selection

000: 4.05V, 001:4.1V, 010:4.15V, 011:4.2V

100: 4.3V, 101/110/111: 4.35V

Bit 3-0 CHRG_CUR_SEL: Charging current selection

0000:1A, 0001:1.2A, 0010:1.4A, 0011:1.6A

0100:1.8A, 0101:2A, 0110:2.2A, 0111:2.4A



1000:2.6A, 1001:2.8A, 1010--1111:3A

15.2.7.5 CHRG_CTRL_REG2: CHARGER CONTROL REGISTER2

ADDRESS: A4H			TYPE: RW					
Bit	Bit7	t7 Bit6 Bit5		Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	CHRG_T	ERM_SEL	CHI	RG_TIMER_	TRIKL	CHRG_	_TIMER_CC	CV
DEFAULT	0	1	0	0	1	0	1	0

DESCRIPTION

Bit 7-6	CHRG_TERM_SEL: Charging termination current selection
	00:100mA, 01:150mA, 10:200mA, 11:250mA
Bit 5-3	CHRG_TIMER_TRIKL: Trickle current charging time selection
	000:30min. 001:60min, 010:90min, 011:120min,
	100:150min, 101:180min, 110, 111:210min
Bit 2-0	CHRG_TIMER_CCCV: Constant current/voltage charging timeout threshold
	selection

000:4h, 001:5h, 010:6h, 011:8h, 100:10h 101:12h, 110:14h, 111:16h

15.2.7.6 CHRG_CTRL_REG3: CHARGING CONTROL REGISTER3

ADDRES	ADDRESS: A5H			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
	SYS_C	TS2_S	CHRG_TE	CHRG_	CHRG_TI	CHRG_TI	CHRC	<u>}_</u>	
SYMBOL	AN_S	D_EN	RM_ANA_	PHASE	MER_TRI	MER_CCC	FREG)	
	D		DIG		KL_EN	V_EN			
DEFAULT	0	0	0	0	0	0	1	0	

DESCRIPTION

	DECOMI TION
Bit 7	SYS_CAN_SD: Vsys shutdown control with battery as sole power supply
	0: Disable
	1: Enable
Bit 6	TS2_SD_EN: PMIC EN bit control when TS2 is over either upper or lower limit
	0: Disable the EN bit
	1: Enable the EN bit
Bit 5	CHRG_TERM_ANA_DIG: Charging termination flag bit source selection

0: Analog

1: Digital

Bit 4 CHRG_PHASE: Charger timer reverse mode control

0: Normal

1: Reverse

Bit 3 CHRG_TIMER_TRIKL_EN: Trickle current charging timer control

0: Enable

1: Disable

Bit 2 CHRG_TIMER_CCCV_EN: Constant current/constant voltage timer control

0: Disable

1: Enable

Bit 1-0 CHRG_FREQ: Charger switching frequency selection

00:1MHz, 01:1.33MHz, 1x:2MHz

15.2.7.7 OTG_ILIM_REG/BAT_CTRL_REG: OTG/BATTERY CURRENT LIMIT REGISTER

ADDRES	TYPE: RW							
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	BAT_DIS_IL	H5V_IPK	OTG_IPK	OTG_ILIN	/I_SEL	BAT_D	ISCHR(G_ILIM
STIVIBUL	IM_EN	LIM_SEL	LIM_SEL					
DEFAULT	1	0	0	0	1	1	0	0

DESCRIPTION

Bit 7	RAT DIS	II IM EN: I	Discharging cu	urrent limit function control

0: Disable

1: Enable

Bit 6 H5V_IPKLIM_SEL: HDMI 5V peak current limit selection

0: 100mA

1: 115mA

Bit 5 OTG_IPKLIM_SEL: OTG peak current limit selection

0:125%*OTG_ILIM_SEL

1:150%*OTG_ILIM_SEL

Bit 4-3 OTG_ILIM_SEL:OTG current limit selection

00:700mA, 01:800mA, 10:900mA, 11:1A

Bit 2-0 BAT_DISCHRG_ILIM: Discharging current limit selection

000:3A, 001:3.5A, 010:4A, 011 4.5A, 1xx:5A

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15.2.7.8 BAT_HTS_TS1_REG: TS1 HT PROTECTION THRESHOLD REGISTER

ADDRESS: A8H				TYPE: RW						
Bit	Bit7	Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0						Bit0		
SYMBOL		BAT_HTS_TS1								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 BAT_HTS_TS1: Battery over temperature protection threshold sensed at TS1.

15.2.7.9 BAT_LTS_TS1_REG: TS1 LT PROTECTION REGISTER

ADDRESS: A9H			TYPE: F	TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL		BAT_LTS_TS1							
DEFAULT	1	1	1	1	1	1	1	1	

DESCRIPTION

Bit 7-0 BAT_LTS_TS1: Battery low temperature protection threshold sensed at TS1.

15.2.7.10 BAT_HTS_TS2_REG: TS2 HT PROTECTION REGISTER

ADDRESS: AAH				TYPE: RW						
Bit	Bit7	Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0						Bit0		
SYMBOL		BAT_HTS_TS2								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 BAT_HTS_TS2: Battery over temperature protection threshold sensed at TS2



15.2.7.11 BAT_LTS_TS2_REG: TS2 LT PROTECTION REGISTER

ADDRESS: ABH				TYPE: RW						
Bit	Bit7	Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0						Bit0		
SYMBOL		BAT_LTS_TS2								
DEFAULT	1	1	1	1	1	1	1	1		

DESCRIPTION

Bit 7-0 BAT_LTS_TS2: Battery low temperature protection threshold sensed at TS2.

15.2.7.12 TS_CTRL_REG: TS PIN CONTROL REGISTER

ADDRES	TYPE: RW							
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	GG_E	TS2_TE	TS2 FUN	TS1 FUN	TS2_CUR		TS1_CUR	
STWIDOL	Ν	(Read only)	102_1011	101_101				
DEFAULT	1	0	0	0	1	1	1	1

DESCRIPTION

Bit 7 GG_EN: Battery fuel gauge enable control

0: Disable

1: Enable

Bit 6 TS2_TE: Flag for TS2 value out of higher or lower limit

0: Out of limit

1: In the limit

Bit 5 TS2_FUN: TS2 pin function selection

0: External temperature monitoring (NTC thermistor connected externally)

1: ADC input

Bit 4 TS1_FUN: TS1pin function selection

0: External temperature monitoring (NTC thermistor connected externally)

1:ADC input

Bit 3-2 TS2_CUR: TS2 pin output current selection in the temperature monitoring mode

00:20uA, 01:40uA, 10:60uA, 11:80uA

Bit 1-0 TS1_CUR: TS1 pin output current selection in the temperature monitoring mode

00:20uA, 01:40uA, 10:60uA, 11:80uA



15.2.7.13 ADC_CTRL_REG: ADC CONTROL REGISTER

ADDRESS	S: ADH	TYPE: RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	ADC_V	ADC_CU	ADC_TS	ADC_T	ADC_PH	ADC_CLK_SEL		L
STIVIBOL	OL_EN	R_EN	1_EN	S2_EN	ASE			
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7 ADC_VOL_EN: If GG_EN=0: Battery voltage ADC enable control

0: Disable

1: Enable

Bit 6 ADC_CUR_EN: If GG_EN=0: Battery current ADC enable control

0: Disable

1: Enable

Bit 5 ADC_TS1_EN: TS1 ADC enable control

0: Disable

1: Enable

Bit 4 ADC_TS2_EN: TS2 ADC enable control

0: Disable

1: Enable

Bit 3 ADC_PHASE: ADC's clock phase

0: Normal

1: Reverse

Bit 2-0 ADC_CLK_SEL: ADC clock frequency selection

000: 2Meg, 001: 1Meg, 010: 500K, 011: 250K, 100: 125K

101: 64K, 110: 32K, 111: 16K

15.2.7.14 ON_SOURCE_REG: POWER UP SOURCE REGISTER

ADDRES	SS: AEH			TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	ON_P WRON	ON_P LUG_I N	ON _RT C	RESTAR T_RESE TB	RESTART_ PWRON_L P	RESTART _RECOVE RY	RESV	RESV
DEFAULT	0	0	0	0	0	0	0	0



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	DESCRIPTION
Bit 7	ON_PWRON: PMIC power up by pressing PWRON
Bit 6	ON_PLUG_IN: PMIC power up by USB plugging in
Bit 5	ON_RTC: PMIC power up by RTC timer
Bit 4	RESTART_RESETB: PMIC restart by pulling down NRESPWRON pin
Bit 3	RESTART_PWRON_LP: PMIC restart by long pressing PWRON
Bit 2	RESTART_RECOVERY: PMIC restart by long pressing PWRON to trigger
	Recovery
Bit 1-0	RESERVED

15.2.7.15 OFF_SOURCE_REG: POWER OFF SOURCE REGISTER

ADDRESS:	AFH			TYPE: R					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
	OFF_R	OFF_S	OFF_T	OFF_S	OFF_D	OFF_P	OFF_	OFF_S	
SYMBOL	EF_DN	YS_O	SD	YS_U	EV_OF	WRON_	TS2	YS_LO	
		V		V	F	LP			
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7	OFF_REF_DN: PMIC power off due to Vref off the range during normal
	operation
Bit 6	OFF_SYS_OV: PMIC power off by Vsys over voltage protection
Bit 5	OFF_TSD: PMIC power off due to over temperature protection
Bit 4	OFF_SYS_UV: PMIC power off due to Vsys under voltage protection
Bit 3	OFF_DEV_OFF: PMIC power off due to DEV_OFF bit written
Bit 2	OFF_PWRON_LP: PMIC power off due to long pressing PWRON
Bit 1	OFF_TS2: PMIC power off due to TS2 value over the high or low limit
Bit 0	OFF_SYS_LO: PMIC power off due to Vsys low voltage set by software (If
	Reg21<4> vb_lo_act=0)

15.2.8 BATTERY FUEL GAUGE CONFIGURATION REGISTER 15.2.8.1 GGCON_REG: FUEL GAUGE CONFIGURATION REGISTER

ADDDECC. DOLL	7.05
ADDRESS: B0H	TYPE: RW



Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0)(145.0)	CUR_SAMPL_		ADC_OFF_CAL_		OCV_SAMPL_		ADC_CUR_	ADC_RE
SYMBOL	CON_TIMES		INTERV		INTERV		VOL_MODE	S_MODE
DEFAULT	0	1	0	0	1	0	1	0

DESCRIPTION

Bit 7-6	CUR_SAMPL_CON_TIMES: The number of continuous sampling on the battery
	current ADC

00:8 01:16 10:32 11:64

Bit 5-4 ADC_OFF_CAL_INTERV<1:0>: ADC's error calibration interval time 00:8min, 01:16min, 10:32min, 11:48min

Bit 3-2 OCV_SAMPL_INTERV<1:0>: OCV sampling interval time 00:8min, 01:16min, 10:32min, 11:48min

Bit 1 ADC_CUR_VOL_MODE: Fuel gauge operation mode selection

0: Voltage mode

1: Current mode

Bit 0 ADC_RES_MODE: Battery internal resistance calculation control

0: Disable 1: Enable

15.2.8.2 GGSTS_REG: FUEL GAUGE STATUS REGISTER

ADDRES	SS: B1H			TYPE: R\	N			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CVMPOL DECV	RES_CUR_AVG_		BAT_	RELAX_V	RELAX_V	RELAX_S	IV_AVG_U	
SYMBOL RESV		SEL<1:0>		CON	OL1_UPD	OL2_UPD	TS(RO)	PD_STS
DEFAULT	0	1	0	0	0	0	0	0

DESCRIPTION

Bit 6-5 RES_CUR_AVG_SEL<1:0>: The fraction of the current ripple for internal resistance calculation

00: 1/2, 01:1/4, 10:1/8, 11:1/16

Bit 4 BAT_CON: The rising edge detection when the battery is first connected

0: Not detected

1: Detected

Bit 3 RELAX_VOL1_UPD:Flag bit for battery voltage1 update in the relaxation state.

0:NOT

1:YES

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Bit 2 RELAX_VOL2_UPD: Flag bit for battery voltage1 update in the relaxation state

0:NOT

1:YES

Bit 1 RELAX_STS: Flag bit for battery turning to relaxation state

0: Not in relaxation

1: in relaxation

Bit 0 IV_AVG_UPD_STS: Flag bit for the internal resistance successfully sensed

0: Not sensed

1: Sensed

15.2.8.3 FRAME_SMP_INTERV_REG:

ADDRES	l		TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	AUTO_SLP_EN	FRAME_SMP_INTERV_REG<4:0>				
DEFAULT	0	0	0	0	0	0	0	1

DESCRIPTION

Bit 7-6 RESERVED

Bit 5 AUTO_SLP_EN: Automatically switching to SLEEP mode control

0: Disable

1: Enable

Bit4-Bit0 FRAME_SMP_INTERV_REG<4:0>: The interval of DATA frame acquisition in

the SLEEP mode

15.2.8.4 AUTO_SLP_CUR_THR_REG: CURRENT THRESHOLD REGISTER

ADDRESS: B3H				TYPE: F	TYPE: RW					
Bit	Bit7	Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0						Bit0		
SYMBOL		AUTO_SLP_CUR_THR_REG<7:0>								
DEFAULT	0	1	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 AUTO_SLP_CUR_THR_REG<7:0> : Current threshold for automatically switching to Sleep mode



15.2.8.5 GASCNT_CAL_REG3: BAT CAPACITY CALIBRATION REGISTER3

ADDRES			TYPE: RW							
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		GASCNT_CAL<31:24>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 GASCNT_CAL<31:24>: Calibrated battery capacity value bits <31:24>

15.2.8.6 GASCNT_CAL_REG2: BAT CAPACITY CALIBRATION REGISTER2

ADDRESS: B5H				TYPE: F	RW.					
Bit	Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1						Bit1	Bit0		
SYMBOL		GASCNT_CAL<23:16>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 GASCNT_CAL<23:16>: Calibrated battery capacity value bits <23:16>

15.2.8.7 GASCNT_CAL_REG1: BAT CAPACITY CALIBRATION REGISTER1

ADDRES			TYPE: F	TYPE: RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		GASCNT_CAL<15:8>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 GASCNT_CAL<15:8>: Calibrated battery capacity value bits <15:8>

15.2.8.8 GASCNT_CAL_REG0: BAT CAPACITY CALIBRATION REGISTER0

ADDRES			TYPE: F	TYPE: RW						
Bit	Bit7	Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit								
SYMBOL		GASCNT_CAL<7:0>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 GASCNT_CAL<7:0>: Calibrated battery capacity value bits <7:0>

15.2.8.9 GASCNT_REG3: BAT CAPACITY REGISTER3

ADDRESS: B8H				TYPE: F	₹					
Bit	Bit7	Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bi						Bit0		
SYMBOL		GASCNT <31:24>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 GASCNT<31:24>: Battery capacity value bits<31:24>

15.2.8.10 GASCNT_REG2: BAT CAPACITY REGISTER2

ADDRES			TYPE: F	TYPE: R						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		GASCNT <23:16>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 GASCNT<23:16>: Battery capacity value bits<23:16>

15.2.8.11 GASCNT_REG1: BAT CAPACITY REGISTER1

ADDRES			TYPE: R							
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		GASCNT <15:8>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 GASCNT<15:8>: Battery capacity value bits<15:8>



15.2.8.12 GASCNT REGO: BAT CAPACITY REGISTERO

ADDRESS: BBH				TYPE: R						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		GASCNT <7:0>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 GASCNT<7:0>: Battery capacity value bits<7:0>

15.2.8.13 BAT_CUR_REGH: BAT CURRENT HIGH BITS REGISTER

ADDRES	ADDRESS: BCH				TYPE: R					
Bit	Bit Bit7 Bit6 Bit5				Bit4 Bit3 Bit2 Bit1 Bit0					
SYMBOL	RESV	RESV	RESV	RESV	BAT_CUR_AVG<11:8>					
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 BAT_CUR_AVG<11:8>: Battery average current value bits<11:8>

15.2.8.14 BAT_CUR_AVG_REGL: BAT CURRENT LOW BITS REGISTER

ADDRES			TYPE: R							
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		BAT_CUR_AVG<7:0>								
DEFAULT	0 0 0 0 0 0 0 0							0		

DESCRIPTION

Bit 7-0 BAT_CUR_AVG<7:0>: Battery average current value bits<7:0>

15.2.8.15 TS1_ADC_REGH: TS1 ADC HIGH BITS REGISTER

ADDRES	SS: BEH			TYPE: F	₹			
Bit	Bit7 Bit6 Bit5			Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	SYMBOL RESV RESV RESV RESV					TS1_ADC<1	1:8>	



1									
	DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 TS1_ADC<11:8>: TS1 ADC value bits<11:8>

15.2.8.16 TS1_ADC_REGHL: TS1 ADC LOW BITS REGISTER

ADDRESS: BFH				TYPE: F	TYPE: R					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		TS1_ADC<7:0>								
DEFAULT	0	0 0 0 0 0 0								

DESCRIPTION

Bit 7-0 TS1_ADC<7:0>: TS1 ADC value bits<7:0>

15.2.8.17 TS2_ADC_REGH: TS2 ADC HIGH BITS REGISTER

ADDRES	ADDRESS: C0H				₹				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	RESV	RESV	RESV	RESV	TS2_ADC<11:8>				
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 TS2_ADC<11:8>: TS2 ADC value bits<15:8>.

15.2.8.18 TS2_ADC_REGHL: TS2 ADC LOW BITS REGISTER

ADDRESS: C1H				TYPE: R						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL			TS2_	_ADC<7:0>	•					



DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-0 TS2_ADC<7:0>: TS2 ADC value bits<7:0>

15.2.8.19 BAT_OCV_REGH: BAT OVER VOLTAGE HIGH BITS REGISTER

ADDRES	SS: C2H			TYPE: R					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	RESV	RESV	RESV	RESV	BAT_OCV<11:8>				
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 BAT_OCV<11:8>: Battery OCV value bits<11:8>

15.2.8.20 BAT_OCV_REGL: BAT OVER TEMP LOW BITS REGISTER

ADDRES	ADDRESS: C3H				TYPE: R					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL	· · · · · · · · · · · · · · · · · · ·	BAT_OCV<7:0>								
DEFAULT	0	0 0 0 0 0 0 0								

DESCRIPTION

Bit 7-0 BAT_OCV<7:0>: Battery OCV voltage value bits<7:0>.

15.2.8.21 BAT_VOL_REGH: BAT VOLTAGE HIGH BITS REGISTER

ADDRES	SS: C4H			TYPE: F	२			
Bit	Bit Bit7 Bit6 Bit5				Bit3	Bit2	Bit1	Bit0
SYMBOL	SYMBOL RESV RESV RESV RESV					BAT_VOL<1	1:8>	



1									
	DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 BAT_VOL<11:8>: Real time battery voltage value bits<11:8>.

15.2.8.22 BAT_VOL_REGL: BAT VOLTAGE LOW BITS REGISTER

ADDRESS: C5H				TYPE: F	TYPE: R					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		BAT_VOL<7:0>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 BAT_VOL<7:0>: Real time battery voltage value bits<7:0>.

15.2.8.23 RELAX_ENTRY_THRES_REGH

ADDRES	SS: C6H			TYPE: F	RW.				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	RESV	RESV	RESV	RESV	RELAX_ENTRY_THRES<11:8>				
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 RELAX_ENTRY_THRES<11:8>: The threshold value bits<15:8> for the battery going into relaxation state

15.2.8.24 RELAX_ENTRY_THRES_REGL

ADDRES	SS: C7H			TYPE: F	RW.			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0



SYMBOL		RELAX_ENTRY_THRES<7:0>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 RELAX_ENTRY_THRES<7:0>: The threshold value bits<7:0> for the battery going into relaxation state

15.2.8.25 RELAX_EXIT_THRES_REGH

ADDRES	SS: C8H			TYPE: F	RW.			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RELAX_EXIT_THRES<11:8>			
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 RELAX_EXIT_THRES<11:8>: The threshold value bits<15:8> for the battery out of relaxation state

15.2.8.26 RELAX_EXIT_THRES_REGL

ADDRES	ADDRESS: C9H				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		RELAX_EXIT_THRES<7:0>								
DEFAULT	0	1	1	0	0	0	0	0		

DESCRIPTION

Bit 7-0 RELAX_EXIT_THRES<7:0>: The threshold value bits<7:0> for the battery out of relaxation state

15.2.8.27 RELAX_VOL1_REGH

ADDRES	SS: CAH			TYPE: F	₹			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RELAX_VOL1<11:8>			
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 RELAX_VOL1<11:8>: Voltage1 value bits<11:8> in the relaxation state

15.2.8.28 RELAX_VOL1_REGL

ADDRES	SS: CBH			TYPE: R					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL		RELAX_VOL1<7:0>							
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-0 RELAX_VOL1<7:0>: Voltage1 value bits<7:0> in the relaxation state

15.2.8.29 RELAX_VOL2_REGH

ADDRES	SS: CCH			TYPE: F	२			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	RELAX_VOL2<11:8>			
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 RELAX_VOL2<11:8>: Voltage2 value bits<11:8> in the relaxation state

15.2.8.30 RELAX_VOL2_REGL

ADDRES	SS: CDH			TYPE: F	₹					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		RELAX_VOL2<7:0>								
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION



Bit 7-0 RELAX_VOL2<7:0>: Voltage2 value bits<7:0> in the relaxation state

15.2.8.31 BAT_CUR_R_CALC_REGH:BAT CURRENT HIGH BITS REGISTER

ADDRES	ADDRESS: CEH				२			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	BAT_CUR_R_CALC<11:8>			
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 BAT_CUR_R_CALC<11:8>: Battery stable current value bits<11:8> for the internal resistance calculation.

15.2.8.32 BAT_CUR_R_CALC_REGL: BAT CURRENT LOW BITS REGISTER

ADDRESS: CFH			TYPE: F	₹					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL		BAT_CUR_R_CALC<7:0>							
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-0 BAT_CUR_R_CALC<7:0>: Battery stable current value bits<7:0> for the internal resistance calculation.

15.2.8.33 BAT_VOL_R_CALC_REGH: BAT VOLTAGE HIGH BITS REGISTER

ADDRES	ADDRESS: D0H				₹			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	BAT_VOL_R_CALC<11:8>			
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION



Bit 7-4 RESERVED

Bit 3-0 BAT_VOL_R_CALC<11:8>: Battery stable voltage value bits<11:8> for the internal resistance calculation.

15.2.8.34 BAT_VOL_R_CALC_REGL: BAT VOLTAGE LOW BITS REGISTER

ADDRESS: D1H			TYPE: F	₹					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL				BAT_VO	L_R_CALC	C<7:0>			
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-0 BAT_VOL_R_CALC<7:0>: Battery stable voltage value bits<7:0> for the internal resistance calculation.

15.2.8.35 CAL_OFFSET_REGH: OFFSET HIGH BITS REGISTER

ADDRES	ADDRESS: D2H				RW			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	CAL	_OFFSET_RE	G<11:8>	
DEFAULT	0	1	1	1	1	1	1	1

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 CAL_OFFSET_REG<11:8>: PCB current offset value bits<11:8>.

15.2.8.36 CAL_OFFSET_REGL: OFFSET LOW BITS REGISTER

ADDRES	ADDRESS: D3H			TYPE: F	RW.					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL		CAL_OFFSET_REG<7:0>								
DEFAULT	1	1	1	1	1	1	1	1		

DESCRIPTION

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Bit 7-0 CAL_OFFSET_REG<7:0>: PCB current offset value bits<7:0>.

15.2.8.37 NON_ACT_TIMER_CNT_REGL:

ADDRES	ADDRESS: D4H			TYPE: F	₹			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL		NON_ACT_TIMER_CNT<7:0>						
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-0 NON_ACT_TIMER_CNT<7:0>: Timer for SLEEP or OFF state (Unit: minute)

15.2.8.38 VCALIBO_REGH: VOLTAGEO CALIBRATION HIGH BITS REGISTER

ADDRES	ADDRESS: D5H				₹			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	VCALIB0<11:8>			
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 Voltage0 calibration value bits<11:8> for calculating offset error and gain error.

15.2.8.39 VCALIBO_REGL: VOLTAGEO CALIBRATION LOW BITS REGISTER

ADDRESS: D6H			TYPE: F	₹					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL		VCALIB0<7:0>							
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-0 Voltage0 calibration value bits<7:0> for calculating offset error and gain error.

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15.2.8.40 VCALIB1_REGH: VOLTAGE1 CALIBRATION HIGH BITS REGISTER

ADDRES	ADDRESS: D7H				२			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	VCALIB1<11:8>			
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 Voltage1 calibration value bits<11:8> for calculating offset error and gain error.

15.2.8.41 VCALIB1_REGL: VOLTAGE1 CALIBRATION LOW BITS REGISTER

ADDRESS: D8H			TYPE: F	₹				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL		VCALIB1<7:0>						
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7- Voltage1 calibration value bits<7:0> for calculating offset error and gain error.

15.2.8.42 IOFFSET_REGH: CURRENT OFFSET HIGH BITS REGISTER

ADDRES	ADDRESS: DDH				२			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	RESV	RESV	RESV	RESV	IOFFSET<11:8>			
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-4 RESERVED

Bit 3-0 Calculated current offset value bits<11:8>



15.2.8.43 IOFFSET_REGL: CURRENT OFFSET LOW BITS REGISTER

ADDRES	SS: DEH			TYPE: F	₹				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL				IOFFSET	Γ<7:0>				
DEFAULT	0	0 0 0 0 0 0 0 0							

DESCRIPTION

Bit 7-0 Calculated current offset value bits<7:0>

15.2.9 **DATA REGISTER**

15.2.9.1 DATAO_REG: DATAO DATA REGISTER

ADDRESS: DFH				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	DATA0(7)	DATA0(6)	DATA0(5)	DATA0(4)	DATA0(3)	DATA0(2)	DATA0(1)	DATA0(0)	
DEFAUL	0	0	0	0	0	0	0	0	
Т									

DESCRIPTION

Bit 7-0 DATA0<7:0>

15.2.9.2 DATA1_REG: DATA1 DATA REGISTER

ADDRES	SS: E0H			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	DATA1(7)	DATA1(6)	DATA1(5)	DATA1(4)	DATA1(3)	DATA1(2)	DATA1(1)	DATA1(0)	
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-0 DATA1<7:0>

15.2.9.3 DATA2_REG: DATA2 DATA REGISTER

ADDRESS: E1H	TYPE: RW
--------------	----------



Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	DATA2(7)	DATA2(6)	DATA2(5)	DATA2(4)	DATA2(3)	DATA2(2)	DATA2(1)	DATA2(0)
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-0 DATA2<7:0>

15.2.9.4 DATA3_REG: DATA3 DATA REGISTER

ADDRES			TYPE: F	TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	DATA3(7)	DATA3(6)	DATA3(5)	DATA3(4)	DATA3(3)	DATA3(2)	DATA3(1)	DATA3(0)	
DEFAULT	0	0	0	0	0	0	0	0	

DESCRIPTION

Bit 7-0 DATA3<7:0>

15.2.9.5 DATA4_REG: DATA4 DATA REGISTER

ADDRES			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	DATA4(7)	DATA4(6)	DATA4(5)	DATA4(4)	DATA4(3)	DATA4(2)	DATA4(1)	DATA4(0)
DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-0 DATA4<7:0>

15.2.9.6 DATA5_REG: DATA5 DATA REGISTER

ADDRES	ADDRESS: E4H				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL	DATA5(7)	DATA5(6)	DATA5(5)	DATA5(4)	DATA5(3)	DATA5(2)	DATA5(1)	DATA5(0)		
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 DATA5<7:0>



15.2.9.7 DATA6_REG: DATA6 DATA REGISTER

ADDRES	ADDRESS: E5H					TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0			
SYMBOL	DATA6(7)	DATA6(6)	DATA6(5)	DATA6(4)	DATA6(3)	DATA6(2)	DATA6(1)	DATA6(0)			
DEFAULT	0	0	0	0	0	0	0	0			

DESCRIPTION

Bit 7-0 DATA6<7:0>

15.2.9.8 DATA7_REG: DATA7 DATA REGISTER

ADDRES	ADDRESS: E6H				TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL	DATA7(7)	DATA7(6)	DATA7(5)	DATA7(4)	DATA7(3)	DATA7(2)	DATA7(1)	DATA7(0)		
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 DATA7<7:0>

15.2.9.9 DATA8_REG: DATA8 DATA REGISTER

ADDRES			TYPE: F	TYPE: RW						
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
SYMBOL	DATA8(7)	DATA8(6)	DATA8(5)	DATA8(4)	DATA8(3)	DATA8(2)	DATA8(1)	DATA8(0)		
DEFAULT	0	0	0	0	0	0	0	0		

DESCRIPTION

Bit 7-0 DATA8<7:0>

15.2.9.10 DATA9_REG: DATA9 DATA REGISTER

ADDRES	SS: E8H			TYPE: F	RW.			
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	DATA9(7)	DATA9(6)	DATA9(5)	DATA9(4)	DATA9(3)	DATA9(2)	DATA9(1)	DATA9(0)



DEFAULT	0	0	0	0	0	0	0	0

DESCRIPTION

Bit 7-0 DATA9<7:0>

15.2.9.11 DATA10_REG: DATA10 DATA REGISTER

ADE	ADDRESS: E9H			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMB OL	DATA10(7)	DATA10(6)	DATA10(5)	DATA10(4)	DATA10(3)	DATA10(2)	DATA10(1)	DATA10(0)	
DEFA	0	0	0	0	0	0	0	0	
ULT									

DESCRIPTION

Bit 7-0 DATA10<7:0>

15.2.9.12 DATA11 REG: DATA11 DATA REGISTER

ADE	ADDRESS: EAH			TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMB OL	DATA11(7)	DATA11(6)	DATA11(5)	DATA11(4)	DATA11(3)	DATA11(2)	DATA11(1)	DATA11(0)
DEFA	0	0	0	0	0	0	0	0
ULT								

DESCRIPTION

Bit 7-0 DATA11<7:0>

15.2.9.13 DATA12_REG: DATA12 DATA REGISTER

ADD	ADDRESS: EBH			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMB OL	DATA12(7)	DATA12(6)	DATA12(5)	DATA12(4)	DATA12(3)	DATA12(2)	DATA12(1)	DATA12(0)	
DEFA	0	0	0	0	0	0	0	0	
ULT									

Version 0.3

DESCRIPTION

Bit 7-0 DATA12<7:0>

15.2.9.14 DATA13_REG: DATA13 DATA REGISTER

ADD	ADDRESS: ECH			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMB OL	DATA13(7)	DATA13(6)	DATA13(5)	DATA13(4)	DATA13(3)	DATA13(2)	DATA13(1)	DATA13(0)	
DEFA	0	0	0	0	0	0	0	0	
ULT									

DESCRIPTION

Bit 7-0 DATA13<7:0>

15.2.9.15 DATA14_REG: DATA14 DATA REGISTER

ADE	ADDRESS: EDH			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	DATA14(7)	DATA14(6)	DATA14(5)	DATA14(4)	DATA14(3)	DATA14(2)	DATA14(1)	DATA14(0)	
DEFAUL	0	0	0	0	0	0	0	0	
T									

DESCRIPTION

Bit 7-0 DATA14<7:0>

15.2.9.16 DATA15_REG: DATA15 DATA REGISTER

ADD	ADDRESS: EDH			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMBOL	DATA15(7)	DATA15(6)	DATA15(5)	DATA15(4)	DATA15(3)	DATA15(2)	DATA15(1)	DATA15(0)	
DEFAUL	0	0	0	0	0	0	0	0	
T									

DESCRIPTION



Bit 7-0 DATA15<7:0>

15.2.9.17 DATA16_REG: DATA16 DATA REGISTER

ADE	ADDRESS: EFH			TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMBOL	DATA16(7)	DATA16(6)	DATA16(5)	DATA16(4)	DATA16(3)	DATA16(2)	DATA16(1)	DATA16(0)
DEFAUL	0	0	0	0	0	0	0	0
T								

DESCRIPTION

Bit 7-0 DATA16<7:0>

15.2.9.18 DATA17_REG: DATA17 DATA REGISTER

ADD	ADDRESS: F0H			TYPE: RW					
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SYMB OL	DATA17(7)	DATA17(6)	DATA17(5)	DATA17(4)	DATA17(3)	DATA17(2)	DATA17(1)	DATA17(0)	
DEFA	0	0	0	0	0	0	0	0	
ULT									

DESCRIPTION

Bit 7-0 DATA17<7:0>

15.2.9.19 DATA18_REG: DATA18 DATA REGISTER

ADE	ADDRESS: F1H			TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMB OL	DATA18(7)	DATA18(6)	DATA18(5)	DATA18(4)	DATA18(3)	DATA18(2)	DATA18(1)	DATA18(0)
DEFA	0	0	0	0	0	0	0	0
ULT								

DESCRIPTION

Bit 7-0 DATA18<7:0>

15.2.9.20 DATA19_REG: DATA19 DATA REGISTER

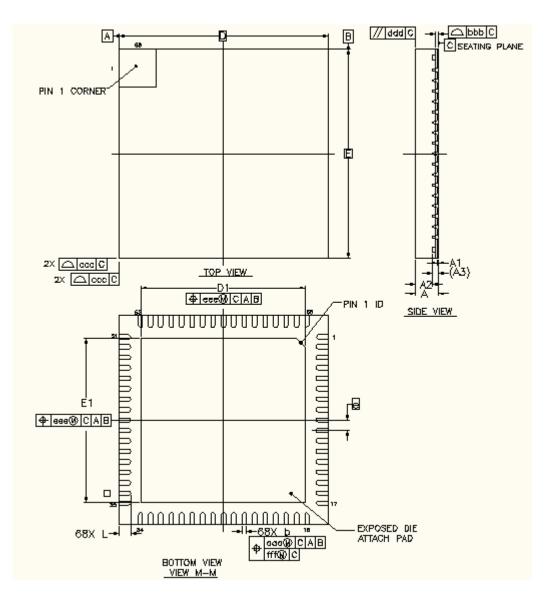
ADE	ADDRESS: F2H			TYPE: RW				
Bit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYMB OL	DATA19(7)	DATA19(6)	DATA19(5)	DATA19(4)	DATA19(3)	DATA19(2)	DATA19(1)	DATA19(0)
DEFA	0	0	0	0	0	0	0	0
ULT								

DESCRIPTION

Bit 7-0 DATA19<7:0>



16 PACKAGE INFORMATION



QFN68 7mm X 7mm



DESCRIPTION	CVMDOL		MILLIMETER	
DESCRIPTION	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	А	0.70	0.75	0.80
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	-	0.55	0.57
MATERIAL THICKNESS	А3	-	0.203 _{REF}	-
PACKAGE SIZE	D	-	7 _{BSC}	-
PACKAGE SIZE	Е	-	7 _{BSC}	-
EP SIZE	D1	5.39	5.49	5.59
EP SIZE	E1	5.39	5.49	5.59
LEAD LENGTH	L	0.30	0.4	0.50
LEAD PITCH	е		0.35_{BSC}	
LEAD WIDTH	b	3.402	0.15	0.164
LEAD OSITION OFFSET	aaa		0.07	
LEAD COPLANARITY	bbb		0.08	
PACKAGE EDGE PROFILE	ccc		0.10	
MOLD FLATNESS	ddd		0.10	
EP POSITION OFFSET	eee		0.10	
	fff		0.05	

Note:

- 1. Coplanarity applies to leads, corner leads and die attach pad.
- 2. Dimension b applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measure in that radius area.