CS 303 Logic and Digital System Design Assigned : 05/05/2024

Project Assignment Due : 31/05/2024

Digital Combination Lock with User ID

You are asked to design a digital combination lock. In addition to the ordinary version, this circuit is expected to have unique codes for up to 100 users, who are expected to identify themselves by the use of a 2-digit decimal number.

You are provided with a template design in *project template.zip* with the top level circuit in *project.dig*. The template contains a block labeled encoder in Verilog HDL, which, implied by the name, encodes the keypad. When any of the 10 keys is pressed, the DATA output shows the number by the respective button, while DA gets asserted for exactly one clock period.

The **mode selector** is to be used for setting the entry mode. Pressing ID should put the machine in user identification entry. Pressed keys should change the user ID shown in the seven-segment display; the last pressed key should make the units digit shift to the tens digit and replace the units digit. This action is to be handled by the **shifter** block.

Once PASSWD mode selected through the **mode selector**, keypad entries should flow into the **shifter pwd** block. Each time a code is entered, LEDs should get turned on incrementally from left to right. Once the 4th code is entered, the block is expected to compare this against the user's private code stored in the ROM.

User passwords are in the ROM block, whose content is determined by the *password.hex* file in raw hex format. Line 2 contains the code for user 00, line 3 is for user 01, and so on. Once a number (in the range 0-99) is applied to the A input, the corresponding user's pass code is returned though D as a 16-bit BCD number.

Upon code entry, the LED labeled GRANTED should be tuned on if the code matches, and DENIED, otherwise. Either LED is to remain on for approximately 3 seconds after which the machined is expected to return to its initial state. During this time period, the machine is to remian in PASSWD entry mode, and any additional code entry should be prohibited. The timing is to be handled by the **timer** block.

Requirements and notes:

- Full synchronous design: all FFs to be driven with a 100Hz clock, and no clock gating allowed.
- Schematic or HDL designs accepted.
- You mach change the inputs and outputs of the blocks, and add more blocks if necessary.
- All buttons, LEDs and displays to be kept intact, and expected to function as stated.
- You may work in groups of two (no more).