



Difference Between the Hi3518 and the Hi3516

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About This Document

Purpose

The Hi3518 is a high-performance system-on-chip (SoC) launched by HiSilicon for high definition Internet Protocol camera (HD-IPC) applications. The software development kit (SDK) of the Hi3518 is similar to that of the Hi3516. The Hi3518 SDK is optimized for better performance. This document describes the differences between the Hi3518 and the Hi3516 from the aspects of specifications, SDK components, and application programming interfaces (APIs).

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3516	V100
Hi3518	V100


Intended Audience

This document is intended for:





- Technical support engineers
- Software development engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 DANGER	Alerts you to a high risk hazard that could, if not avoided, result in serious injury or death.



Symbol	Description
 WARNING	Alerts you to a medium or low risk hazard that could, if not avoided, result in moderate or minor injury.
 CAUTION	Alerts you to a potentially hazardous situation that could, if not avoided, result in equipment damage, data loss, performance deterioration, or unanticipated results.
 TIP	Provides a tip that may help you solve a problem or save time.
 NOTE	Provides additional information to emphasize or supplement important points in the main text.

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

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This issue is the first draft release.



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1 Differences on Specifications

Table 1-1 describes the specifications differences between the Hi3518 and the Hi3516. For details on the specifications of the Hi3518, see the *Hi3518 HD IP Camera SoC Brief Data Sheet*.

Table 1-1 Specifications differences

Key Specifications	Hi3518	Hi3516
Processor	ARM 9@Max. 440 MHz	ARM Cortex A9@Max. 800 MHz
Image signal processor (ISP)	<ul style="list-style-type: none">• 17x15 zone weight• Antifog and anti-false color• 2-magapixel image inputs	<ul style="list-style-type: none">• 9x7 zone weight• 5-magapixel image inputs
Video input (VI)	<ul style="list-style-type: none">• One VI interface that provides the ISP function• 8-, 10-, or 12-bit RGB bayer inputs, a maximum of 74.25 MHz clock frequency• BT.601 or BT.656• 1080p@30 fps or 720p@30 fps• Lens distortion correction (LDC)• Image rotation by 90 ° or 270 °	<ul style="list-style-type: none">• Two VI interfaces and dual-sensor inputs. One interface provides the ISP function.• 8-, 10-, 12-, 14-, or 16-bit RGB bayer inputs, a maximum of 150 MHz clock frequency• BT.601, BT.656, or BT.1120• 1080p@30 fps, 720p@60 fps, or 16M@2 fps
Video output (VO)	<ul style="list-style-type: none">• One composite video broadcast signal (CVBS) output• One BT.1120 video output interface for connecting to the external high-definition multimedia interface (HDMI) or serial digital interface (SDI), maximum performance of 1080p@30 fps• CVBS output or BT.1120 output	<ul style="list-style-type: none">• One BT.656 output from the same source and one CVBS output• One BT.1120 video output interface for connecting to the external HDMI or SDI, maximum performance of 1080p@30 fps



Key Specifications	Hi3518	Hi3516
Video pre-processing (VPP)	<ul style="list-style-type: none">• One input and multiple outputs. That is, after an input image is processed, several images can be output for subsequent processing.• Scaling on images in channels	Image enhancement
Video encoding and decoding	<ul style="list-style-type: none">• H.264 BP/MP encoding• 720p@30 fps+VGA@30 fps+QVGA@30 fps+720p@1 fps JPEG snapshot	<ul style="list-style-type: none">• H.264 BP/MP/HP encoding• MPEG4 SP encoding• 1080p@30 fps+D1@30 fps+CIF@30 fps+QVGA@30 fps+1080p JPEG snapshot 1 fps
Audio	One integrated audio CODEC, supporting 16-bit voice inputs and outputs	Two inter-IC sound (I2S) interfaces and one integrated audio CODEC, supporting 16-bit voice inputs and outputs
Double-date rate (DDR)	DDR2/DDR3 synchronous dynamic random access memory (SDRAM) interfaces, 16-bit data width, 440 MHz, a maximum of 2 Gbits capacity for the Hi3518A or 1 Gbit for the Hi3518C	DDR2/DDR3 SDRAM interfaces, 32- or 16-bit data width, 500 MHz, a maximum of 1 Gbit capacity
Network	<ul style="list-style-type: none">• Media access control (MAC) interface• Reduced media independent interface (RMII) and media independent interface (MII) modes, 10/100 Mbit/s full-duplex or half-duplex mode, physical (PHY) clock output	<ul style="list-style-type: none">• Gigabit media access control (GMAC) interface• Reduced gigabit media independent interface (RGMI) and MII modes
Peripheral component interconnect express (PCIe)	None	One PCIe 1.1 interface
Secure digital input/output (SDIO)	One SDIO 2.0 interface, supporting a maximum of 32 GB secure digital high capacity (SDHC)	Two SDIO 2.0 interfaces, supporting a maximum of 32 GB capacity
Audio-to-digital converter (ADC)	One integrated low-speed ADC with dual channels	None



2 Differences on SDK Components

Table 2-1 describes the SDK component differences between the Hi3518 and the Hi3516.

Table 2-1 SDK component differences

Component	Hi3518	Hi3516
lib	uClibc-0.9.32.1	uClibc-0.9.30.2
Tool chain	arm-hisiv100nptl-linux-	arm-hisiv100-linux-
Linux kernel	linux-3.0.y, supporting ARM9	linux-2.6.35, supporting ARM Cortex A9
File system	squashfs file system, high compression ratio, and no 16 MB size limitation	cramfs file system



3 Differences on APIs

Table 3-1 describes the API differences between the Hi3518 and the Hi3516. For details, see the *HiMPP Media Processing Software Development Reference*.

Table 3-1 API differences

Module	Change Extent of the Hi3518 Compared with the Hi3516	Description
System control	Partially new	<ul style="list-style-type: none">• The operations of allocating, releasing, and refreshing the media memory zone (MMZ) are added.• The video buffer pools support multiple DDRs.
ISP	Partially new	The functions of antifog, anti-false color, and crosstalk removal are added.
VI	Modification	<ul style="list-style-type: none">• User images are supported.• The functions of controlling the camera flash, LDC, rotation, and luminance statistics are added.• The VPP operations are not supported.
VO	Modification	<ul style="list-style-type: none">• An API for controlling channel playing is added.• An API for controlling color space conversion (CSC) is added.
VPP	Completely new	The Hi3516 supports video pre-processing by using the VPP module, and the Hi3518 supports video pre-processing by using the video process subsystem (VPSS). The VPSS uses the scheme of one input and multiple outputs. That is, a group can output the images from multiple channels. The group and channels process images separately.
Video encoding (VENC)	Partially new	<ul style="list-style-type: none">• The frame skipping reference function is added.• The color-to-gray function is added.• The JPEG snapshot mode is added.
Motion detection (MD)	Partially new	The function of detecting input user images is added.



Module	Change Extent of the Hi3518 Compared with the Hi3516	Description
Frame buffer	Partially new	An API for refreshing displayed contents in extended mode is added.
Two-dimensional engine (TDE)	Partially new	The functions of LDC, rotation, and filling for images are added.