Hi3518E Hardware Design

User Guide

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About This Document

Purpose

This document describes the design recommendations for the hardware schematic diagrams, printed circuit board (PCB), board thermal dissipation, and hardware design methods of the Hi3518E.

Related Version

The following table lists the product versions related to this document.

Product Name	Version
Hi3518E	V100

Intended Audience

This document is intended for:

- Technical support engineers
- Hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B03 (2014-03-27)

This issue is the second draft release, which incorporates the following changes:

Chapter 3 Thermal Design Recommendations

Chapter 3 is added.

Issue 00B02 (2014-02-28)

This issue is the first draft release..

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1 Design Recommendations for Schematic Diagrams

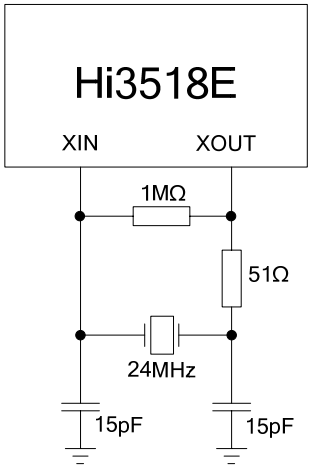
1.1 Design Recommendations for the Small System

1.1.1 Clocking Circuit

The system clock can be generated by combining the internal feedback circuit of the Hi3518E with an external 24 MHz crystal oscillator circuit.

Figure 1-1 shows the recommended connection mode and component specifications of the crystal oscillator circuit. The load capacitors and clocks must match, and the frequency deviation must be within 30 ppm.

Figure 1-1 Crystal oscillator circuit



Note: The capacitance of the capacitors in Figure 1-1 must match the load capacitance of the actual crystal oscillator. The inherent load capacitance varies according to the brand and model of the crystal oscillator. The clock frequency deviation must be within ±30 ppm.

1.1.2 Reset and Watchdog Circuits

The Hi3518E selects the internal or external reset mode by checking the status of the POR_SEL pin during power-on.

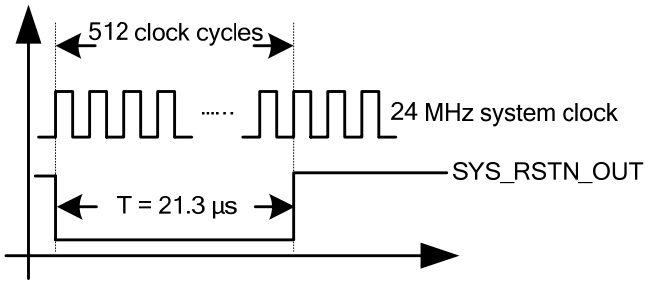
- When the POR_SEL level is low, internal reset is selected. After the master chip is powered on, the power-on-reset (POR) circuit resets the entire chip (the pulse width of the reset signal is about 140 ms), and the RSTN pin is invalid. In internal reset mode, the RSTN and WDG_RSTN pins can be floated.

  In internal reset mode, peripherals (such as the flash memory) must be reset before the system is reset or peripherals and the system are reset at the same time. Otherwise, exceptions such as boot failures of the system may occur. In addition, when internal reset is selected, the WDG_RSTN pin is floated. The integrated watchdog generates a reset signal to reset the chip if the system is abnormal, and the reset system outputs a reset signal through the SYS_RSTN_OUT pin to reset peripherals.

CAUTION

As shown in Figure 1-2, the duration of the reset signal from the SYS_RSTN_OUT pin when the system is abnormal is about 21.3 µs (512 x 24 MHz system clock cycle). Therefore, the SYS_RSTN_OUT pin cannot be used to reset the peripherals that require the reset duration be longer than 21.3 µs. In this case, an external reset signal is required to reset such peripherals.

Figure 1-2 Duration of the reset signal from the SYS_RSTN_OUT pin



- When the POR_SEL level is high, external reset is selected. In this case, the RSTN pin is a reset signal input pin. The valid reset signal must have low-level pulse, and the pulse width must be greater than 12 input clock cycles for the XIN pin. Typically, the pulse width of the reset signal is 100–300 ms.

  During board design, if external reset is selected, you are advised to use a dedicated reset chip to generate reset signals to ensure system stability.

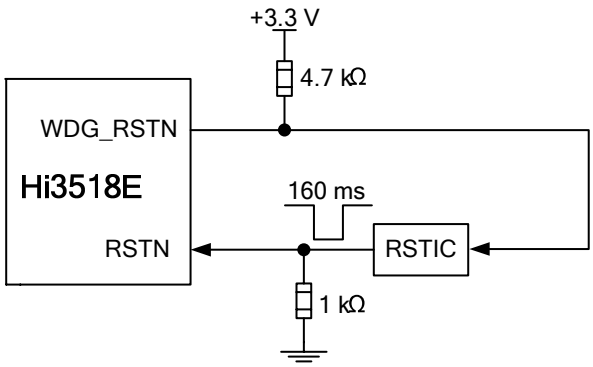
  When the system is abnormal, the WDG_RSTN pin can generate a low-level pulse. The pulse triggers an external reset chip to generate a reset signal. The WDG_RSTN pin cannot be directly connected to the RSTN pin.

CAUTION

Because the WDG_RSTN pin is an open drain (OD) output pin, it must be connected to an external pull-up resistor. A 1−4.7 kilohm resistor is recommended.

Figure 1-3 shows the typical external reset and watchdog circuit.

Figure 1-3 Typical external reset and watchdog circuit



1.1.3 JTAG Debug Interface

The Hi3518E Joint Test Action Group (JTAG) interface complies with the IEEE1149.1 standard. PCs can be connected to the Realview-ICE simulator over this interface for debugging the A9 CPU. Table 1-1 lists the signals of the JTAG debug interface.

Table 1-1 Signals of the JTAG debug interface

Signal	Description
TCK	JTAG clock input, internal pull-down. You are advised to connect this signal to a pull-down resistor on the board.
TDI	JTAG data input, internal pull-up. You are advised to connect this signal to a pull-up resistor on the board.
TMS	JTAG mode selection input, internal pull-up. You are advised to connect this signal to a pull-up resistor on the board.
TRSTN	JTAG reset input, internal pull-down. You are advised to connect this signal to a pull-down resistor on the board in normal cases. When a debugger such as Realview-ICE is connected over the JTAG interface, you are advised to connect this signal to a pull-up resistor on the board.
TDO	JTAG data output. You are advised to connect this signal to a pull-up resistor on the board.

For details about the impedance of pull-up and pull-down resistors described in Table 1-1, see Figure 1-4.

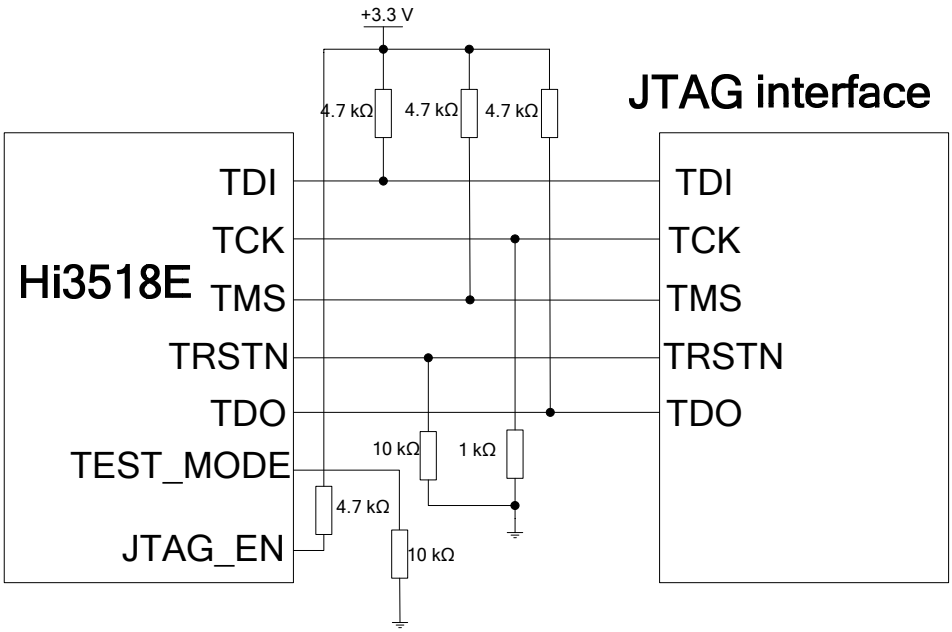
You can set the operating mode of the Hi3518E to normal mode or test mode by configuring the TEST_MODE pin. For details, see Table 1-2.

Table 1-2 TEST_MODE pin configuration

TEST_MODE	Description
0	The Hi3518E works in normal mode.
1	The Hi3518E works in test mode. In this case, the design for test (DFT) can be performed.

Figure 1-4 shows the JTAG connection mode and standard connector pins. If the JTAG function is used, connect the JTAG_EN pin to a 1−4.7 kilohm pull-up resistor.

Figure 1-4 JTAG connection mode and standard connector pins



1.1.4 System Configuration Circuit for Hardware Initialization

The Hi3518E can boot from the SPI flash in 3-byte or 4-byte address mode. Hardware needs to be configured as required for hardware initialization, which is implemented by connecting a pull-up or pull-down resistor on the board. Table 1-3 describes hardware configuration signals.

Table 1-3 Hardware configuration signals

Signal	Direction	Description
JTAG_EN	I	JTAG debug enable. 0: disabled 1: enabled
BOOT_SEL	I	Boot mode select. 0: SPI flash Note: BOOT_SEL must be set to **0**; otherwise, the system fails to boot.
SFC_ADDR_MODE	I	SPI flash controller (SFC) address length. 0: 3 bytes 1: 4 bytes

1.1.5 DDR Circuit

Because the Hi3518E has two embedded 64 MB DDR2 SDRAMs, you only need to pay attention to the DDR power design. For details, see the section 1.2 "Power Supply Design."

CAUTION

The DDRC ZQ pin of the Hi3518E is led out. Connect this pin to a 1% 240 OHM resistor and then to GND.

1.1.6 SPI Flash Circuit

1.1.6.1 Introduction

- When an SPI flash connects to the flash interface, the maximum capacity is 32 MB, and the clock frequency is 56 MHz.
- The 3-byte and 4-byte address modes are supported for the SPI flash.
- The Hi3518E does not support the NAND flash.

1.1.6.2 Signal Processing

Table 1-4 describes the recommended design when an external SPI flash is connected.

Table 1-4 Recommended design when an SPI flash is connected

Signal	Connection Mode (4-Layer PCB)	Connection Mode (6-Layer PCB)
SFC_CLK	A 33 Ω resistor is connected in series at the Hi3518E end.	A 33 Ω resistor is connected in series at the Hi3518E end.

Signal	Connection Mode (4-Layer PCB)	Connection Mode (6-Layer PCB)
SFC_DIO/SFC_DOI /SFC_WP/SFC_HOLD	The signals are connected directly. SFC_WP needs to be connected to a pull-down resistor. A 1−4.7 kilohm pull-down resistor is recommended.	The signals are connected directly. SFC_WP needs to be connected to a pull-down resistor. A 1−4.7 kilohm pull-down resistor is recommended.

CAUTION

If you want to use the reset signal from the SYS_RSTN_OUT pin to reset an SPI flash when internal POR reset is selected, ensure that the reset duration of the SPI flash is less than or equal to 21.3 μs.

1.2 Power Supply Design

For details about the system power supply design, see the schematic diagram of the Hi3518E demo board.

1.2.1 Core Power Supply

The core power pins DVDD12 are connected to the 1.2 V digital power. The capacity of the 1.2 V power chip must be greater than or equal to 1 A. Each DVDD12 pin connects to at least two 10 μF grounding filtering bypass capacitors. At least one 100 nF decoupling capacitor connects to each DVDD12 pin close to the power pin.

1.2.2 Power Supply of the Embedded DDRs

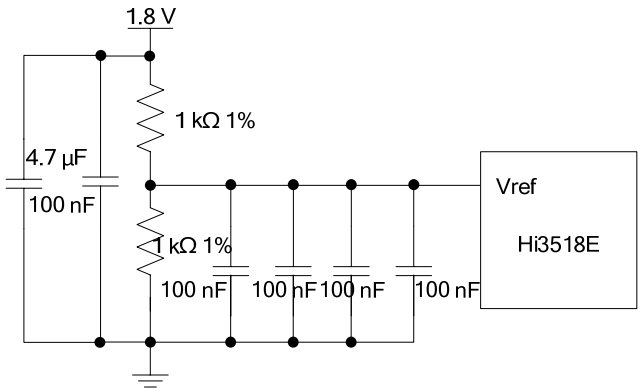
Because the Hi3518E has embedded DDR2 SDRAMs, the power supply design must comply with the SSTL-18 level standard, the power supply must be 1.8 V, and the reference voltage V_{ref} must be 0.9 V.

The DDR power pins DDR_VDDQ are connected to the 1.8 V digital power. A 100 nF ceramic filtering capacitor needs to be connected close to each power pin, and at least one 10 μF grounding filtering capacitor needs to be connected to the power supply of the DDRs.

You are advised to design an independent DC-DC circuit on the board to supply power to the 1.8 V power pins of the DDRs. The power is supplied to the DDRC reference power pin V_{ref} by using 1% voltage-divided resistors. The voltage-divided power is 0.9 V. A 0.1 μF decoupling capacitor is connected close to each power pin and reference power pin.

Figure 1-5 shows the reference design of the voltage-divided circuit.

Figure 1-5 Reference design of the voltage-dividing power supply network



1.2.3 I/O Power Supply

The I/O power pins DVDD33 are connected to the 3.3 V digital power. At least one 10 μF grounding filtering bypass capacitor is connected to the DVDD33 power supply, and each DVDD33 pin is connected to a 100 nF decoupling capacitor close to the power pin.

For the video input (VI) interface power (DVDD3318 pin), the I/O power supplies for the sensor CLK, VI, and SPI0 parts can be 1.8 V or 3.3 V, and the I/O level standards of various sensors are supported.

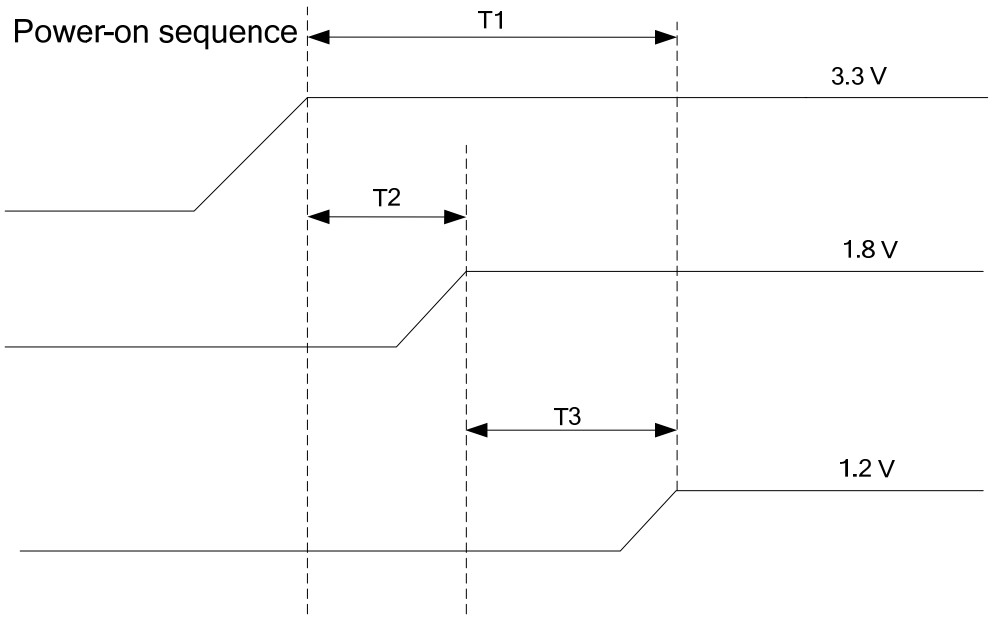
1.2.4 PLL Power Supply

It is recommended that the phase-locked loop (PLL) power supply be isolated by using 1 kilohm@100 MHz external memory interface (EMI) beads. For details, see the schematic diagram of the Hi3518E demo board.

1.2.5 Power-On Sequences

Figure 1-6 show the requirements on the power-on sequences of the core power supply, DDR power supply, and I/O power supply.

Figure 1-6 Power-on sequence



NOTE

- 0 < T1 ≤ 100 ms
- T2 > 0
- T3 > 0

1.2.6 Notes

Ensure that the output voltage of each power supply meets the requirements even when ripples and noises occur. For details about the power supply requirements of each module, see section the section "Electrical Specifications" in the *Hi3518E 720p IP Camera SoC Data Sheet*.

1.3 Design Recommendations for Peripheral Interfaces

1.3.1 USB Port

USB Power Supply

The analog power AVDD33_USB/AVDD33_USB25 must be isolated from the digital power. You are advised to use planes to reduce the parasitic effect, coupling noise, and power supply impedance. In addition, filtering capacitors are placed close to pins.

The digital power DVDD12_USB and digital GND DVSS_USB must not be interfered. Ensure that short and wide traces are used.

USB Protective Circuit

A protective circuit must be designed on the USB circuit to ensure electrostatic discharge (ESD) protection. To prevent USB traces from being affected by protective components, follow the following guidelines:

- Place the protective components close to the USB connector port.
- Use the TVS pipes with low parasitic capacitors as protective components, and ensure that the breakdown voltage is 8 kV, and the breakdown time is less than 1 ns.
- Ensure that the parasitic capacitors of the protective components connected to the high-speed USB 2.0 port are less than 1 pF.

1.3.2 MAC Interface

Interface Design

The MAC interface supports the reduced media-independent interface (RMII) and media independent interface (MII) modes. Figure 1-7 to Figure 1-10 show the signal connections in the two modes by using the RTL8201F as an example.

Figure 1-7 Signal connections in MII mode (clocks provided by the Hi3518E)

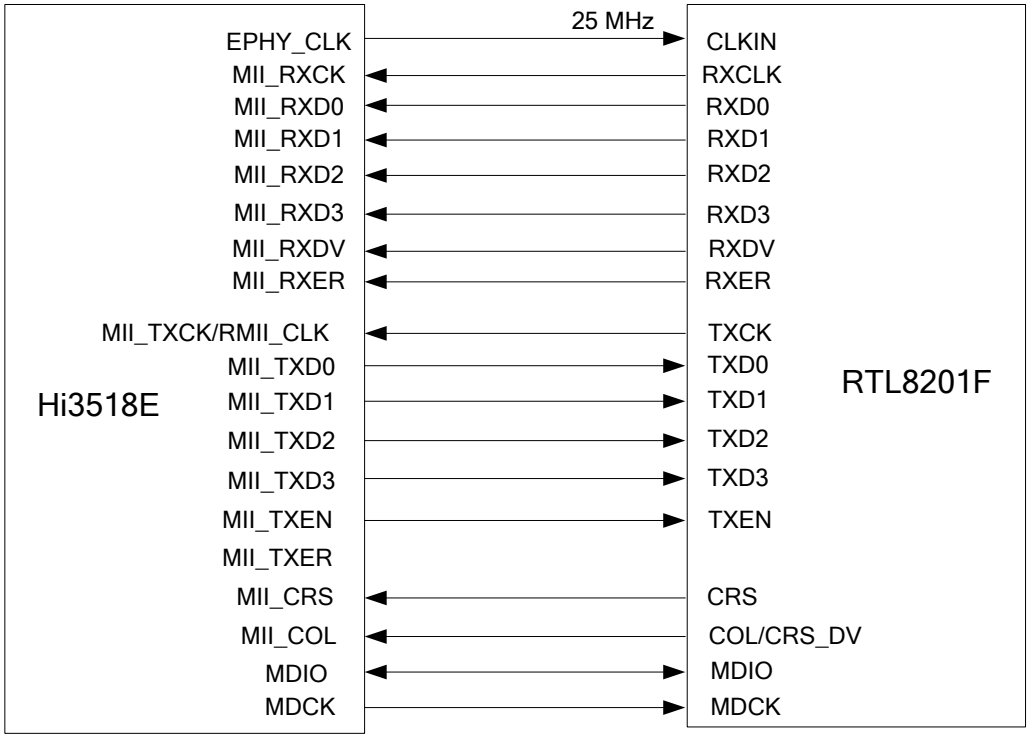


Figure 1-8 Signal connections in MII mode (clocks provided by external components)

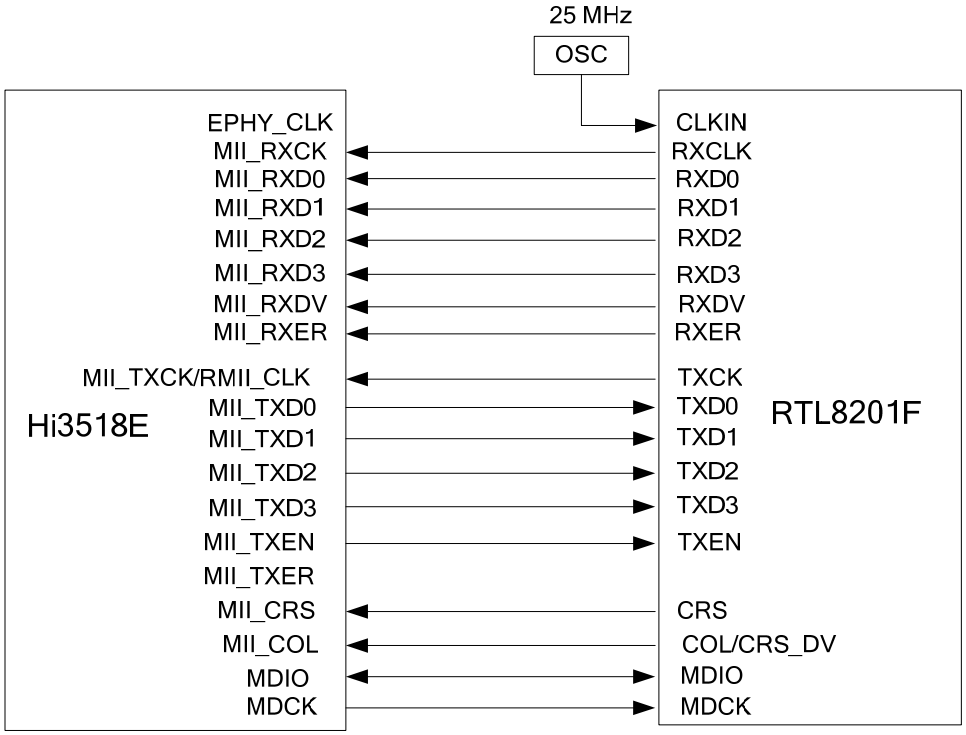


Figure 1-9 Signal connections in RMII mode (clocks provided by the Hi3518E)

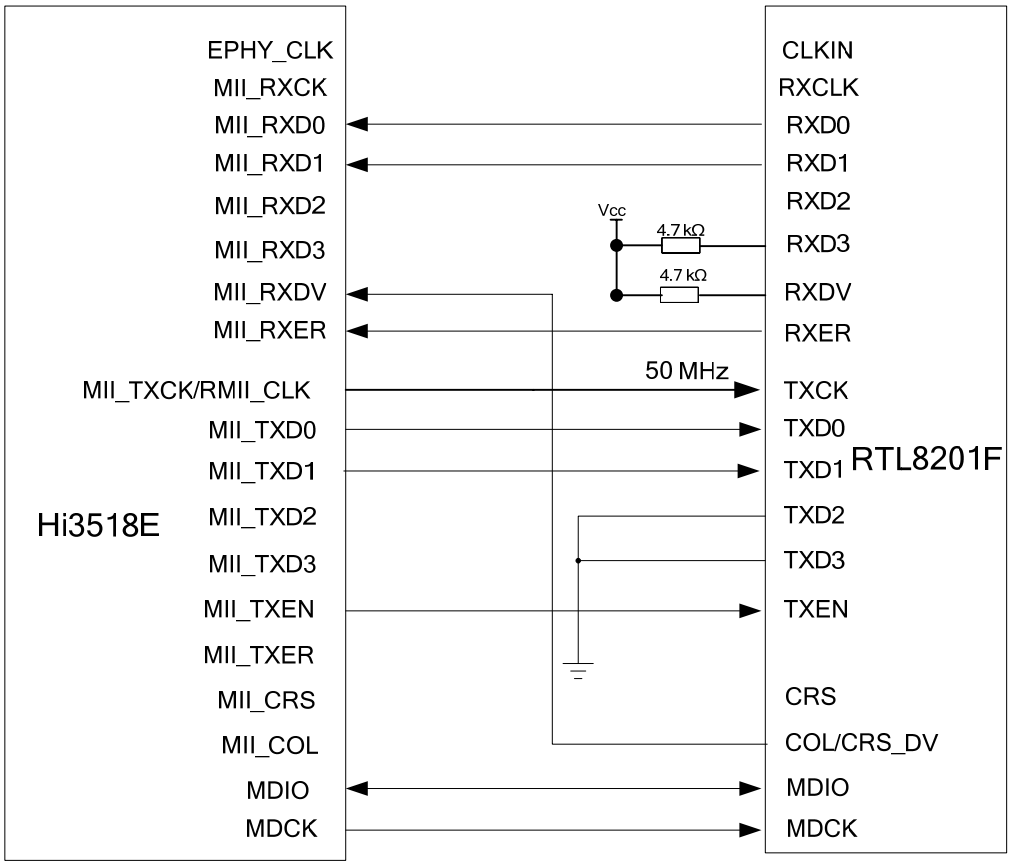
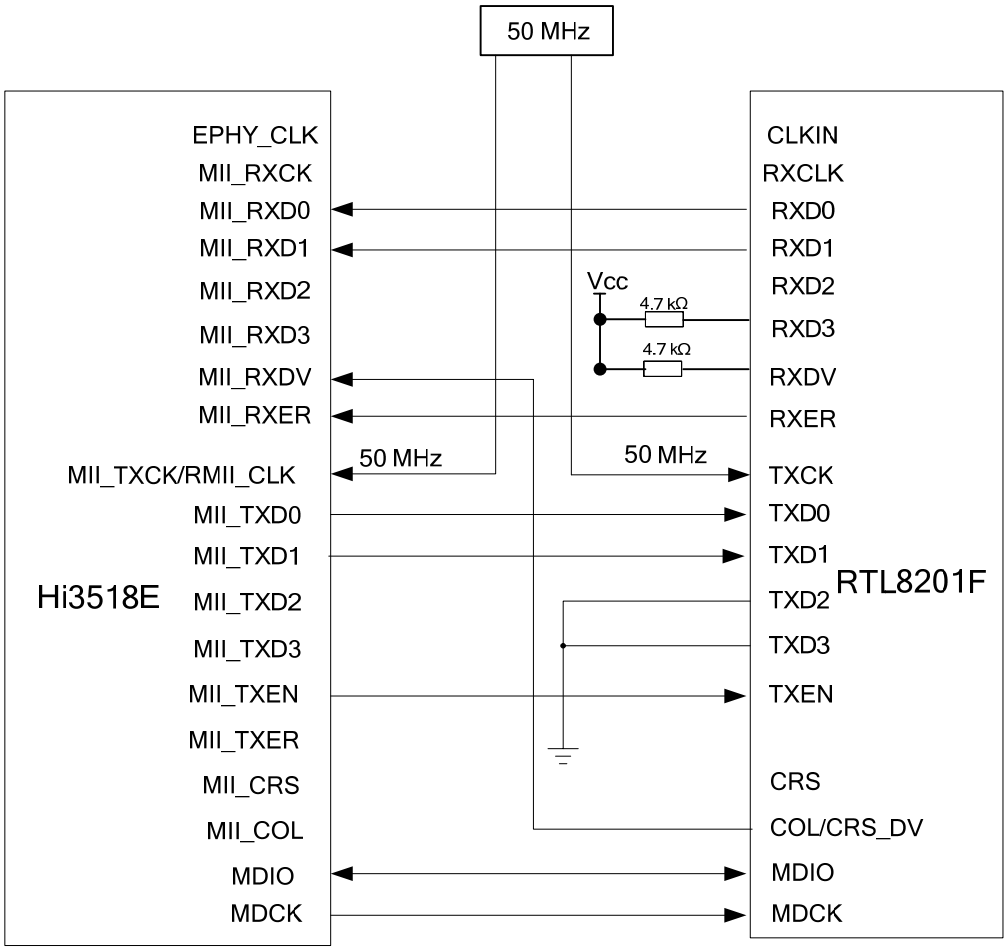


Figure 1-10 Signal connections in RMII mode (clocks provided by external components)



All MAC signals are connected in point-to-point topology. Each PCB trace must be less than or equal to 6 inches. The following are recommendations for designing matched resistors:

- Connect a 1−4.7 kΩ pull-up resistor to the MDIO signal.
- It is recommended that a 22-ohm resistor be connected to the MDCK signal in series close to the source end to ensure the signal quality.
- It is recommended that 33-ohm resistors are connected to the TXD0−TXD3 signals in series close to the source end to ensure the signal quality.
- In RMII mode, TXD2 and TXD3 can be floated on the Hi3518E end. For details about the configurations on the PHY end, see the user manuals provided by PHY vendors.
- In MII mode, it is recommended that a 33 Ω resistor be connected to the TXCK signal in series close to the interconnected PHY. In RMII mode, the TXCK pin of the Hi3518E is multiplexed as the RMII_CLK pin. If the RMII_CLK pin is used as the clock source, it is recommended that a 33-ohm resistor be connected in series on the Hi3518E end. In this case, the reference clock of the ETH PHY needs to set to input. For details about how to set the clock direction, see the user manuals provided by PHY vendors.
- It is recommended that 33-ohm resistors are connected to the RXD0−RXD3 signals in series close to the source end to ensure the signal quality.
- Connect a 33 Ω resistor to the RXCK signal in series close to the interconnected PHY.

- In RMII mode, the Hi3518E reference clock can be set to input or output based on the design requirements and ETH PHY features.

1.3.3 Audio Interfaces

Analog Audio Interface

The Hi3518E provides stereo input/output interfaces (AC_LINEL, AC_LINER, AC_OUTL, and AC_OUTR).

- The 3.3 V power of the audio digital-to-analog converter (ADAC) must be isolated from the 3.3 V system power. It is recommended that a 2.2 μF filtering capacitor be connected to the AC_VREF pin, and a 470-kilohm resistor be connected to the filtering capacitor in parallel to reduce the discharge time of the AC_VREF pin. For details, see the schematic diagram of the Hi3518E demo board.
- AC_LINEL and AC_LINER can act as the line or MIC input channels. If the input device is a passive MIC device, the MIC_BIAS must be added to the input signal. If the input device is an active line-in device (such as a PC), no bias is required.
- There are three series of sampling rates: 32 kHz, 44.1 kHz, and 48 kHz.
  - 32 kHz-series sampling rates: 8 kHz, 16 kHz, 32 kHz, 64 kHz, and 128 kHz
  - 44.1 kHz-series sampling rates: 11.025 kHz, 22.05 kHz, 44.1 kHz, 88.2 kHz, and 176.4 kHz
  - 48 kHz-series sampling rates: 12 kHz, 24 kHz, 48 kHz, 96 kHz, and 192 kHz
- The output amplitude of the ADAC at full scale is 0.875 Vrms.
- You are advised to connect an audio amplifier and filtering circuit to the audio output pins AC_OUTL and AC_OUTR. For details, see the schematic diagram of the Hi3518 peripheral board.
- The following are the overall design recommendations (including but not limited to) for the intercom application scenario:
  - Ensure that the MIC and speaker are as far as possible to minimize coupling between them.
  - The MIC must be sealed to prevent sound passing from the mechanical part to the MIC. The speaker should also be sealed.
  - Ensure that the size of the speaker cavity opening is more than 15% of the sectional area of the cavity. Typically, a larger sound cavity indicates better low-frequency audio quality but poorer echo cancellation effect.
  - The MIC opening is typically a round hole with 0.8−1.2 mm diameter. No sound cavity is designed for the MIC, that is, the MIC opening is a straight hole.
  - The MIC is sealed with rubber or foam to prevent the crosstalk of the speaker in the IP camera or crosstalk to the MIC due to the sound vibration of the IP camera. Ensure that there is no crosstalk and resonance in the IP camera.

1.3.4 Video Interfaces

VI Interface

The Hi3518E has only one physical VI interface.

- The VI interface supports the raw data input, a maximum of 12-bit width, and a maximum of 74.25 MHz frequency.
- For a 12-bit sensor, the raw data pins connect to D0−D11 of the VI interface in sequence.
- For a 10-bit sensor, the raw data pins connect to any 10-bit pins of the VI interface in sequence. The pins D2 to D11 are recommended. It is recommended that any unused pin be connected to a 4.7 kΩ resistor and then to GND.

VO Interface

The Hi3518E has only one physical video output (VO) interface. This interface is called VOU interface.

- The VOU interface signal is multiplexed with the Ethernet (ETH) interface signal. If the ETH interface is used, the VOU interface is unavailable.
- If the VOU interface acts as the BT.1120 output, the bit width is 16 bits, and the maximum interface frequency is 74.25 MHz.
- The VOU interface does not provide external row sync and field sync signals and supports only internal sync.
- For a BT.1120 signal, the upper eight bits are the Y (luminance) signal, and the lower eight bits are the C (chrominance) signal.

1.3.5 RTC Interface

The timing accuracy of the embedded RTC is affected by the manufacturing accuracy and temperature offset of the external crystal oscillator. For details about correction schemes, see the *RTC Correction Scheme Application Notes*.

If high timing accuracy is required, you are advised to select the external RTC with an embedded crystal oscillator or a crystal oscillator with the temperature compensation function.

1.4 Unused Pins

Process unused pins as follows:

- If the JTAG function is not used, connect the JTAG_EN pin to a pull-down resistor (the 1−4.7 kilohm resistor is recommended), configure the JTAG_TCK, JTAG_TMS, JTAG_TRSTN, JTAG_TDO, and JTAG_TDI pins as GPIO pins, and set these pins to output pins. In this case, the JTAG_TCK, JTAG_TMS, JTAG_TRSTN, JTAG_TDO, and JTAG_TDI pins can be floated.
- If internal POR is selected to reset the master chip, connect the POR_SEL pin to a pull-down resistor. In this case, the RSTN pin can be floated.
- If SPI0 and SPI1 are not used, configure the corresponding pins as GPIO pins, and set these pins to output pins. In this case, the pins can be floated.
- The power supplies of the SAR_ADC, audio CODEC, and USB module must be retained even they are not used.
- If the over-current protection function is not used for the USB module, configure the USB_OVRCUR pin as a GPIO pin, and set this pin to output pin. In this case, this pin can be floated.

1.5 Sensor Board

- To ensure picture quality, you are advised to use a low dropout (LDO) regulator to supply power to the sensor. Pay attention to the analog power and PLL power of the sensor. Typically, the core units of the sensor require a larger current. The efficiency and thermal dissipation of the LDO regulator need to be considered.
- The analog part and digital part of the sensor are separated. To be specific, the analog GND and digital GND are separated and connected by using 0 Ω resistors in single-point mode. The analog power branch has an independent LDO regulator and does not share the power branch with the digital power. During the design of PCB layout and stacked architecture, ensure that the digital part and analog part do not intersect, avoiding interference and coupling.
- If the sensor board is connected to the main board by using a connector, ensure that current return paths are provided for the data signals from the connector when specifying signals for connector pins. This avoids signal crosstalk. That is, each data signal trace or clock signal trace is connected to an independent GND trace to form a current return path. Note that a clock signal trace is designed between two GND traces, and two data signal traces are designed between two GND traces. For details, see the Hi3518E schematic diagram.

2 PCB Design Recommendations

2.1 PCB Design Recommendations for the Small System

2.1.1 Power Supplies for the Small System

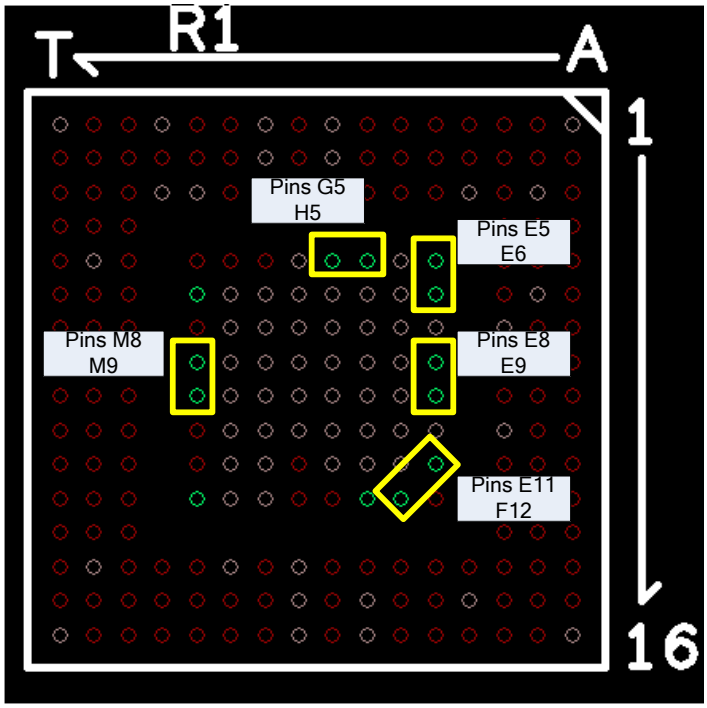
Core Power Supply

Note that the current of the core power plane must be at least 1 A.

If the core power plane is used, each 100 nF filtering capacitor must be placed close to the power pin to reduce the parasitic inductance. Figure 2-1 shows the core power pins on the Hi3518E. Connect decoupling capacitors to these pins as follows:

- Connect at least one 2.2 μF capacitor to the pins E5 and E6 each.
- Connect at least one 2.2 μF capacitor to the pins G5 and H5 each.
- Connect at least one 2.2 μF capacitor to the pins E8 and E9 each.
- Connect at least one 2.2 μF capacitor to the pins M8 and M9 each.
- Connect at least one 2.2 μF capacitor to the pins E11 and M12 each.
- Connect at least one 100 nF capacitor to other pins each.
- Place at least one 10 μF capacitor on the core power plane.

Figure 2-1 Core power pins on the Hi3518E



DDR Power Supply

Decoupling capacitor are placed close to each 1.8 V power pin of the Hi3518E. At least one 10 μF grounding filtering capacitor is placed on the 1.8 V power plane.

The 0.9 V reference power for the embedded DDRs of the Hi3518E must be isolated from other power supplies. You can connect the Hi3518E and the DDRs by using wide traces. Ensure that decoupling capacitors are placed close to each power pin and the V_{REF} is masked by surrounding GND traces.

The design recommendations for the V_{REF} are as follows:

- Pay attention to the V_{REF} routing when designing the V_{REF}. According to the SSTL-18 standard, the noise of the V_{REF} cannot be greater than ±1% of the V_{REF} level. To reduce the noise, ensure that the V_{REF} traces are as wide as possible. In addition, you are advised to route the V_{REF} traces at the power layer over a copper plane. This copper plane cannot be used as the reference plane for routing signal traces.
- A decoupling capacitor needs to be connected to each V_{REF} pin. The trace of each V_{REF} pin must be as wide as possible, and the spacing between the trace and other signal traces must be 20–25 mils.

I/O Power Supply

At least one 10 μF grounding filtering bypass capacitor is connected to the DVDD33 power supply, and a 100 nF decoupling capacitor is connected to each DVDD33 power pin close to the power pin.

2.1.2 Clock and Reset Circuits

Clock

The power and GND pins of the Hi3518E PLL unit include AVDD12_PLL, AVDD33_PLL, and AVSS_PLL. Design the PCB based on the following guidelines:

- AVDD12_PLL is the 1.2 V PLL power. You are advised to isolate it from the 1.2 V board digital power by using EMI beads. The level deviation of the 1.2 V power must be within ±5%.
- AVDD33_PLL is the 3.3 V PLL power. You are advised to isolate it from the 3.3 V digital power by using EMI beads. The level deviation of the 3.3 V power must be within ±5%.
- AVSS_PLL is the PLL reference GND. It is recommended that the decoupling capacitors of the AVDD12_PLL and AVDD33_PLL power supplies form a π-shaped circuit with EMI beads, and the capacitors be connected to the GND plane through separate vias.
- The system clock traces of the crystal oscillator circuit must be as short as possible, and be surrounded by GND traces.

Reset

The Hi3518E can be reset internally or externally by configuring the POR_SEL pin. During power-on, if POR_SEL is **0**, internal reset is enabled; if POR_SEL is **1**, internal reset is disabled, and the chip is reset externally. For details about the circuit design, see the schematic diagram of the Hi3518E demo board.

2.1.3 SPI Flash Signals

Route SPI flash signal traces on a PCB based on the following guidelines:

- The spacing between adjacent traces complies with the 3W rule. The 3W rule indicates that the trace spacing is three times the trace width.
- It is recommended that a 33-ohm resistor be connected to the clock signal in series close to the Hi3518E to ensure the signal quality.

2.1.4 ETH Signals

Route ETH signal traces on a PCB based on the following guidelines

- The spacing between adjacent traces complies with the 3W rule.
- It is recommended that a 33-ohm resistor be connected to the clock signal in series close to the source end to ensure the signal quality.

2.2 PCB Design Recommendations for Typical Peripheral Interfaces

2.2.1 USB Port

PCB Design Recommendations

To ensure good signal quality, route the data lines of the USB 2.0 host port in differential mode. You are advised to design the PCB routing based on the following guidelines to meet the 480 MHz/s requirement for the USB 2.0 port:

- The differential data traces must be short and straight, and the internal differential traces must have the same length. It is recommended that the length deviation be within 5 mils.
- Ensure that the impedance of each differential data trace is 90 ohm±10%.
- Route differential data traces on the plane that is close to the GND plane and never change the routing plane.
- Route differential data traces by referencing a complete GND plane, and do not cross the plane splits.
- Minimize the use of vias and corners when routing differential data traces. When corners are required, use arcs or 135° turns rather than a 90° turn. This reduces the signal reflection and impedance variance.
- Keep the differential data traces more than 50 mils away from other high-speed cyclic signals and strong current signals to reduce crosstalk. Keep the differential data traces at least 20 mils away from low-speed noncyclic signals.
- Place the REXT resistor close to the Hi3518E.

USB Power Supply

The Hi3518E has one USB 2.0 host port. The power pins and GND pins of the USB unit are AVDD33_USB/AVDD33_USB25, AVSS_USB, DVDD12_USB, and AVSS_USB that correspond to the 3.3 V power, 3.3 V GND, 3.3 V core power, and 3.3 V core GND respectively. AVDD33_USB/AVDD33_USB25 are analog 3.3 V power pins, and AVSS_USB is the 3.3 V analog GND pin. The level deviation of AVDD33_USB/AVDD33_USB25 must be within ±7%. You are advised to isolate the 3.3 V analog USB power from the 3.3 V digital board power by using EMI beads, and place filtering capacitors close to AVDD33_USB/AVDD33_USB25 and AVSS_USB pins.

USB Protective Circuit

A USB protective circuit is required to implement ESD protection. To prevent signals along USB traces from being attenuated by protective components, design the PCB based on the following guidelines:

- Place protective components close to the USB port connector.
- Use the TVS pipes with low parasitic capacitors as protective components.
- Connect parasitic capacitors that are less than 2 pF to the protective components on the high-speed USB 2.0 port.

2.2.2 Audio Circuit

- The Hi3518E provides an analog audio CODEC. AC_VREF must be connected to a 2.2 μF external capacitor and 470-kilohm resistor in parallel and then to GND.
- You are advised to connect an audio amplifier and filtering circuit to the audio output pins AC_OUTL and AC_OUTR. For details, see the schematic diagram of the Hi3518E peripheral board.
- Place protective components close to the port connector.
- Use the TVS pipes with low parasitic capacitors as protective components.

2.2.3 VI and VO Interfaces

The Hi3518E has a VO interface and a VI interface. The following are routing requirements:

- The VO data signal trace is routed based on the CLK signal trace. The maximum length deviation is 1000 mils.
- The traces of the VI data signal, row sync signal, and field sync signal are routed based on the CLK signal trace. The maximum length deviation is 1000 mils.
- The VI interface has 1.8 V and 3.3 V power domains. Route the traces of the VI data signal, row sync signal, field sync signal, and SPI 0 at the top layer by referring to the GND plane. This avoids sharp changes of characteristic impedance when signal traces are routed by referring to the 1.8 V or 3.3 V power plane.
- If the 1.8 V power domain is selected for the VI interface, the maximum signal trace length is 4 inches.

3 Thermal Design Recommendations

3.1 Working Condition

For details about the parameters related to power consumption, temperature, and thermal resistance, see section 2.6 "Electrical Specifications" in the *Hi3518E 720p IP Camera SoC Data Sheet.*

3.2 Reference Thermal Design for Circuits

CAUTION

The thermal design is recommended based on the small-sized board with high thermal design requirements, such as the board (38 mm x 38 mm) integrating the Hi3518E and sensor.

3.2.1 Schematic DiagramPower Supply

To design multiple power supplies with different power consumption on an integrated board, note the following:

- Avoid too many DC-DC conversion hierarchies in a board power tree (the power conversion efficiency may be lowered) and avoid too many branches in a single power tree (too many DC-DC inductors will occupy much PCB space).
- Avoid using LDO components with large voltage in the board power tree to reduce the heat generated during power conversion.
- Use the power chips with high conversion efficiency.
- Configure low-power mode for functional modules. For example, if IR-CUT switching is supported, when the IR-CUT state is switched, its power supply is powered off to reduce power consumption.

When designing the board, design an appropriate power tree and power scheme based on actual conditions such as the power supply requirements and PCB space.

Configuring the Low-Power Mode

In some Hi3518E applications, modules such as the USB and SD card may not be used. You can set the modes of these modules to low-power mode.

3.2.2 PCB

Component Layout

Based on the product architecture and thermal dissipation design, you are advised to lay out components as follows:

- Evenly lay out the components that consume much power such as the Hi3518E, power components, and the Ethernet PHY to avoid local overheating that may further affect the reliability and efficiency of components. Keep an appropriate distance between the Hi3518E and power components, and between the Hi3518E or power components and the positioning hole. This ensures that the main thermal dissipation source can dissipate the heat through screw holes and the enclosure.
- Lay out temperature-sensitive components such as the sensor and flash memory far away from power-consuming components. This minimizes the impact of heat on the power-consuming components and avoids the overheating of the sensitive components, which may further affect the system stability and the picture quality. You can place the sensor/flash memory and power-consuming components at different layers.
- The copper areas on the four screw holes of the PCB should be exposed. The exposed areas should be as large as possible if allowed. This ensures the full contact between the PCB and the enclosure.

Trace

The trace recommendations are as follows:

- Select the full connection style but not the thermal connection style to improve the thermal dissipation efficiency of the board.
- The GND signals and 1.2 V, 1.8 V, and 3.3 V power signals of the Hi3518E are connected on copper planes. When the maximum signal current capability is ensured, it is recommended that more vias be punched on copper planes to improve the thermal dissipation capacity.

NOTE

For details about thermal features, see the *Hi3518E Evaluation Board Thermal Performance Test Report*.