HDMI Compliance Test Software: Measurement Report

Tektronix Enabling Innovation

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Source Tests Report

Configuration

Setup Configuration

Oscilloscope Info	DPO73304S - 10.8.5 Build 4
TDSHT3 Version	5.3.6 Build 54

Device Configuration

Device Details	HDMI Device
Clock Frequency(Mhz)	74.2501
Resolution	1920x1080i
Refresh Rate	60Hz

Compliance Summary

Total Tests Supported	9
Tests Completed	29
Pass	29
Fail	0

Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.02*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.02*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.02*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.02*Tbit	Pass
5	7-6 : Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0*TPixel	Pass
6	7-6 : Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0*TPixel	Pass
7	7-6 : Source Inter-Pair Skew	D2 - D0	Skew < 0.2*TPixel;	0*TPixel	Pass
8	7-4 : Source Rise Time	CK	75.00ps < TRISE;	157.36ps	Pass
9	7-4 : Source Rise Time	D0	75.00ps < TRISE;	114.21ps	Pass
10	7-4 : Source Rise Time	D1	75.00ps < TRISE;	121.14ps	Pass
11	7-4 : Source Rise Time	D2	75.00ps < TRISE;	121.91ps	Pass
12	7-4 : Source Fall Time	CK	75.00ps < TFALL;	147.00ps	Pass
13	7-4 : Source Fall Time	D0	75.00ps < TFALL;	115.59ps	Pass
14	7-4 : Source Fall Time	D1	75.00ps < TFALL;	116.88ps	Pass
15	7-4 : Source Fall Time	D2	75.00ps < TFALL;	114.13ps	Pass
16	7-8 : Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	50.49%	Pass
17	7-8 : Min Duty Cycle	CK	40.0% < Min Duty Cycle;	49.6%	Pass
18	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	CK+	2.700V < VL < 2.900V;	2.8456V	Pass
19	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D0+	2.700V < VL < 2.900V;	2.8343V	Pass
20	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	CK-	2.700V < VL < 2.900V;	2.8476V	Pass
21	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D0-	2.700V < VL < 2.900V;	2.8328V	Pass
22	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D1+	2.700V < VL < 2.900V;	2.8208V	Pass
23	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D2+	2.700V < VL < 2.900V;	2.8606V	Pass
24	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D1-	2.700V < VL < 2.900V;	2.8239V	Pass
25	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D2-	2.700V < VL < 2.900V;	2.8600V	Pass
26	7-7 : Source Intra-Pair Skew	CK	Skew < 0.15*Tbit;	0.018*Tbit	Pass
27	7-7 : Source Intra-Pair Skew	D0	Skew < 0.15*Tbit;	0.012*Tbit	Pass
28	7-7 : Source Intra-Pair Skew	D1	Skew < 0.15*Tbit;	0.018*Tbit	Pass
29	7-7 : Source Intra-Pair Skew	D2	Skew < 0.15*Tbit;	0.006*Tbit	Pass

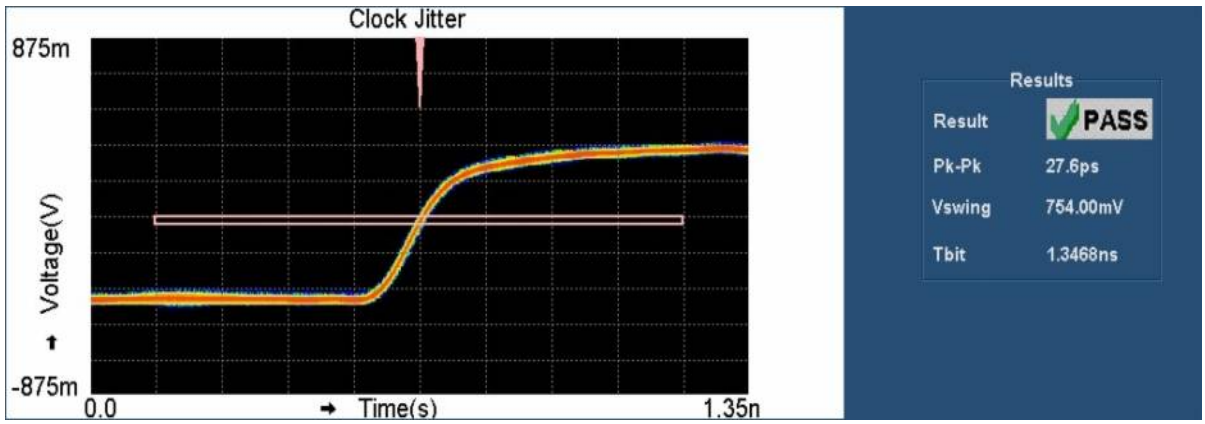
Detailed Results

7-9 : Source Clock Jitter : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Result
Clock Jitter < 0.25*Tbit;	0.02*Tbit	1.3468ns	754.00mV	0.23*Tbit	50.000M	Pass

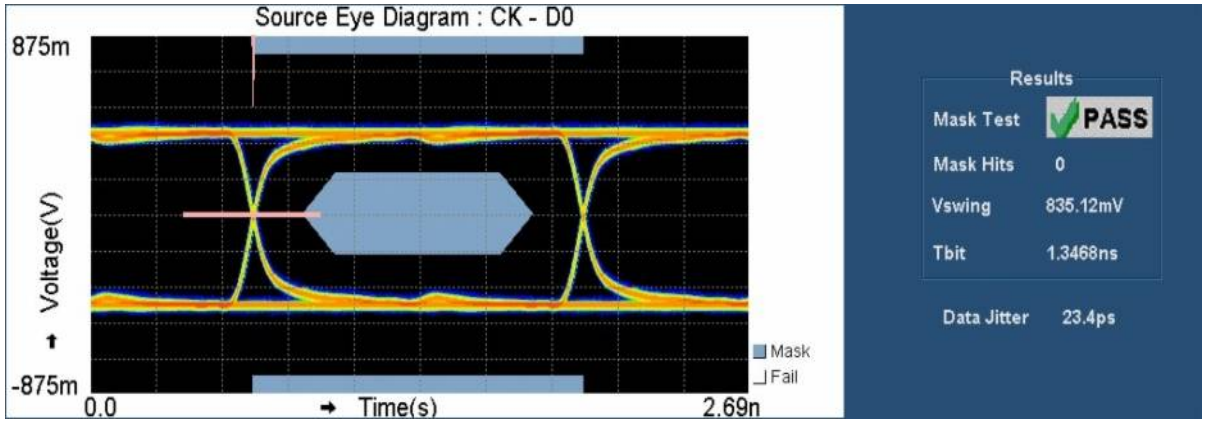
Waveform/Plot



- **7-10 : Source Eye Diagram : CK - D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.02*Tbit	1.3468ns	835.12mV	0.28*Tbit	50.000M	0	Pass

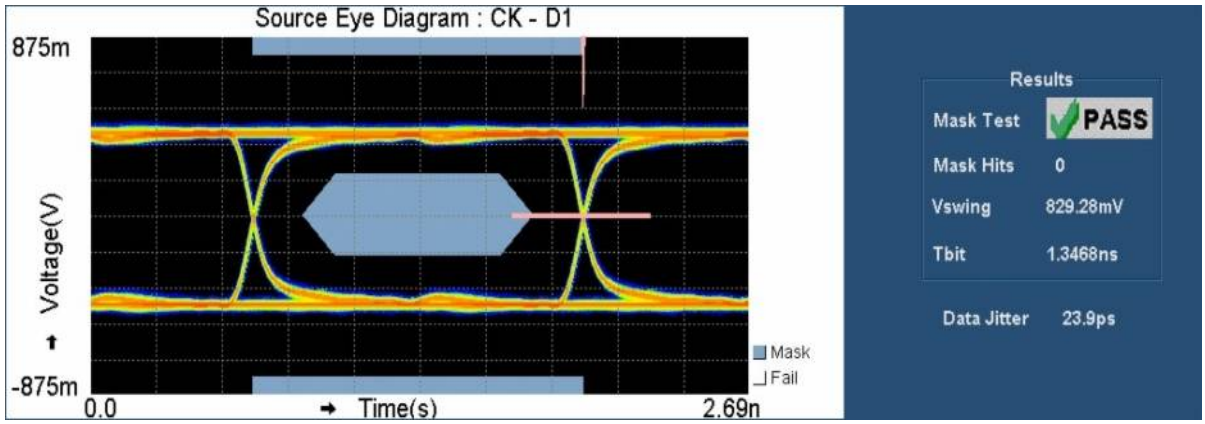
  - **Waveform/Plot**



- **7-10 : Source Eye Diagram : CK - D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.02*Tbit	1.3468ns	829.28mV	0.28*Tbit	50.000M	0	Pass

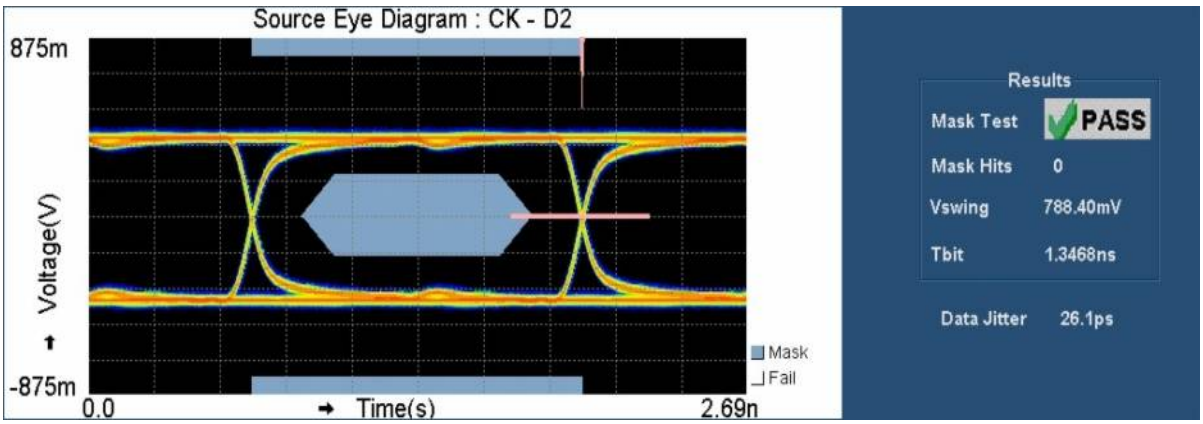
  - **Waveform/Plot**



- **7-10 : Source Eye Diagram : CK - D2**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.02*Tbit	1.3468ns	788.40mV	280.6m*Tbit	50.000M	0	Pass

  - **Waveform/Plot**



- **7-6 : Source Inter-Pair Skew : D0 - D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs(D0 - D1)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0*TPixel	1.3468ns	= 835.12mV, Vs = 829.28mV	473.68f	10.000p	4.7483p	Pass

- **7-6 : Source Inter-Pair Skew : D1 - D2**
  - **Results**

Spec Range	Meas Value	Tbit	Vs(D1 - D2)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0*TPixel	1.3468ns	= 829.28mV, Vs = 788.40mV	210.53f	4.7619p	2.0269p	Pass

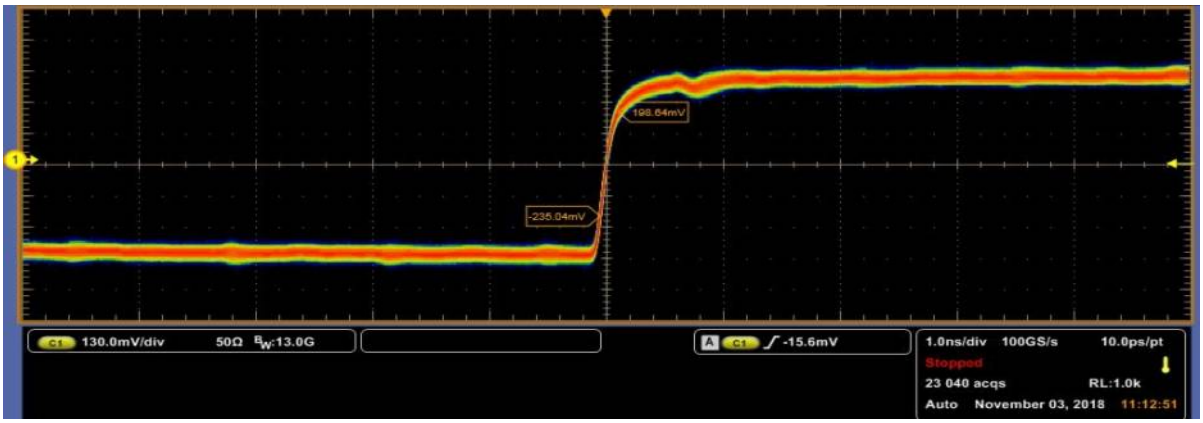
- **7-6 : Source Inter-Pair Skew : D2 - D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs(D2 - D0)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0*TPixel	1.3468ns	= 788.40mV, Vs = 835.12mV	952.38f	6.0000p	3.0985p	Pass

- **7-4 : Source Rise Time : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	157.36ps	1.3468ns	722.80mV	82.36ps	Pass

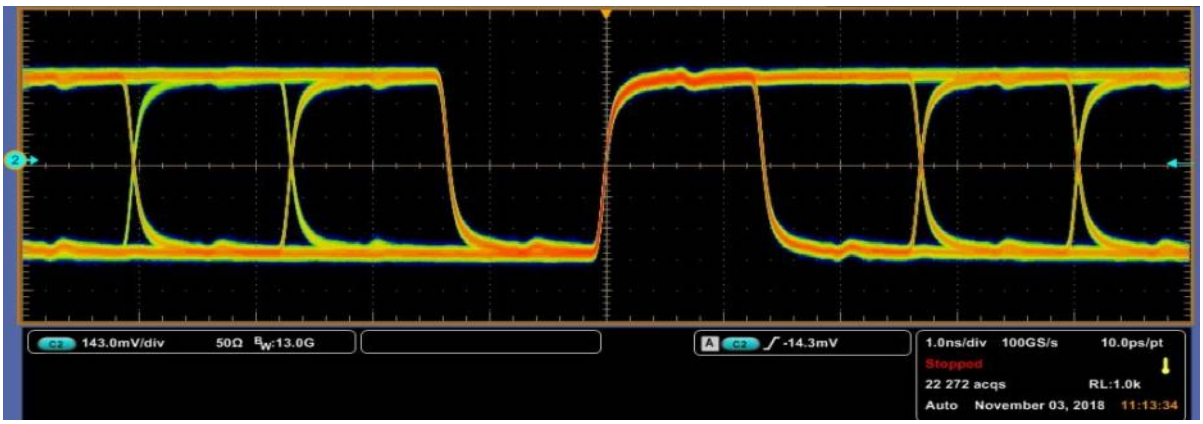
  - **Waveform/Plot**



- **7-4 : Source Rise Time : D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	114.21ps	1.3468ns	806.52mV	39.21ps	Pass

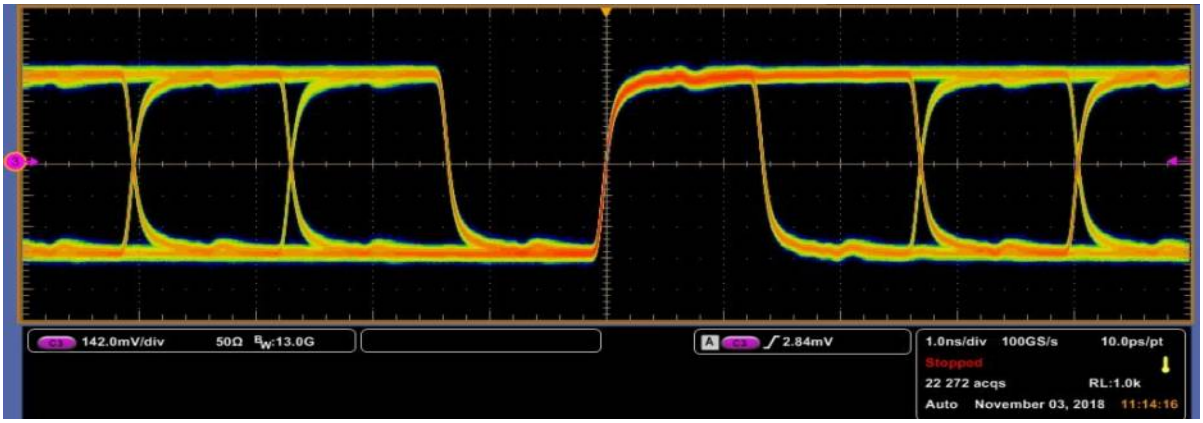
  - **Waveform/Plot**



- **7-4 : Source Rise Time : D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	121.14ps	1.3468ns	806.56mV	46.14ps	Pass

  - **Waveform/Plot**



- **7-4 : Source Rise Time : D2**
  - **Results**

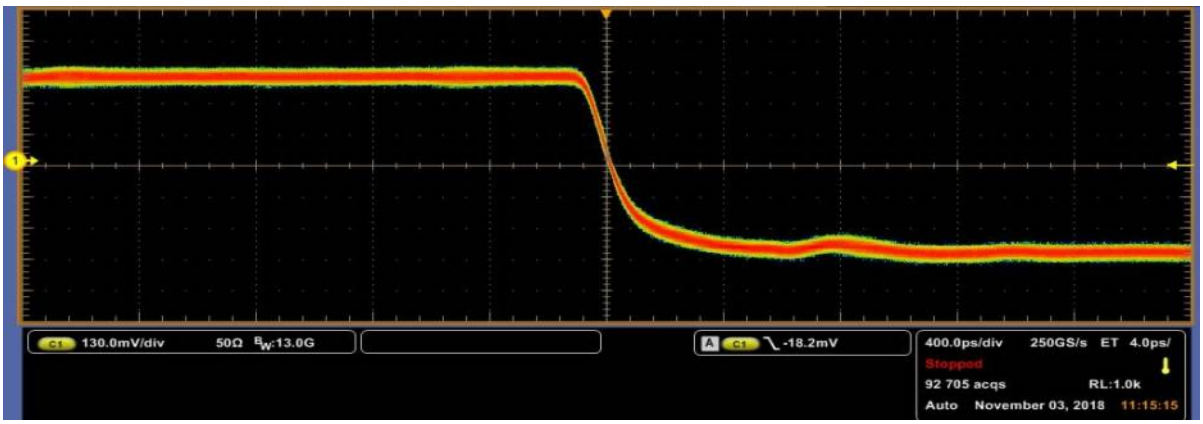
Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	121.91ps	1.3468ns	766.80mV	46.91ps	Pass

  - **Waveform/Plot**

- **7-4 : Source Fall Time : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	147.00ps	1.3468ns	722.80mV	72.00ps	Pass

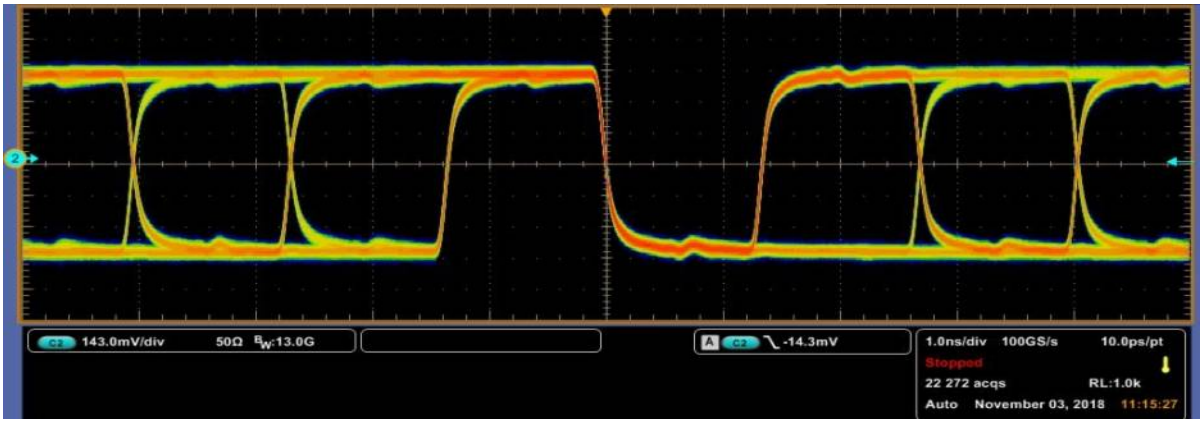
  - **Waveform/Plot**



- **7-4 : Source Fall Time : D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	115.59ps	1.3468ns	806.52mV	40.59ps	Pass

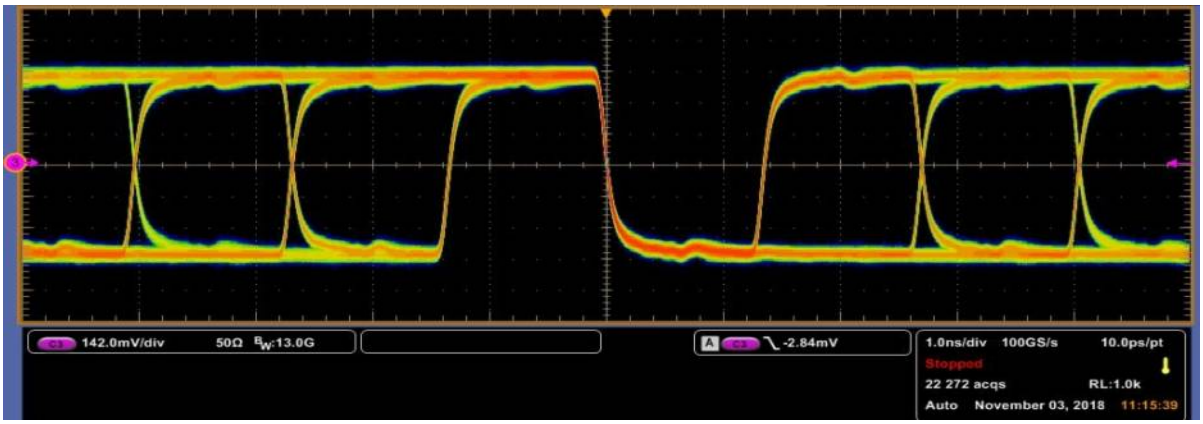
  - **Waveform/Plot**



- **7-4 : Source Fall Time : D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	116.88ps	1.3468ns	806.56mV	41.88ps	Pass

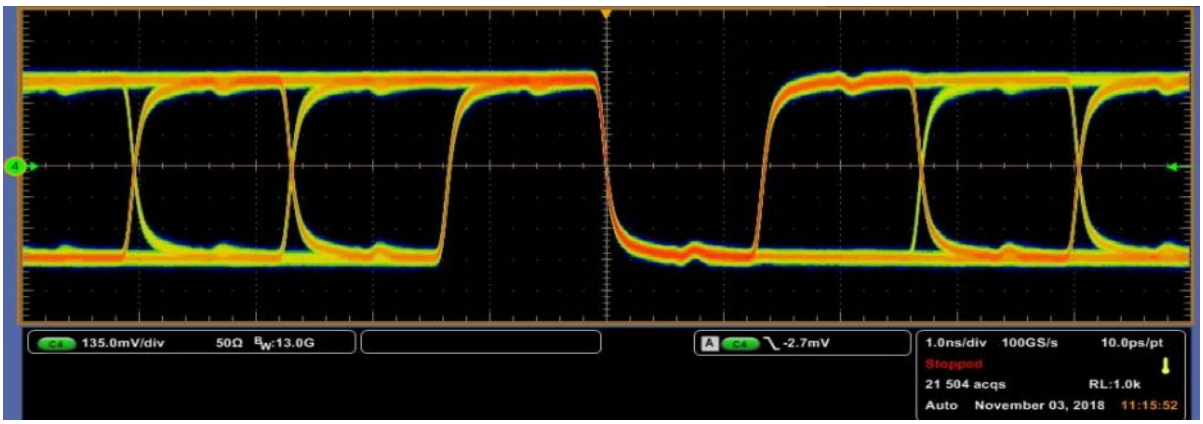
  - **Waveform/Plot**



- **7-4 : Source Fall Time : D2**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	114.13ps	1.3468ns	766.80mV	39.13ps	Pass

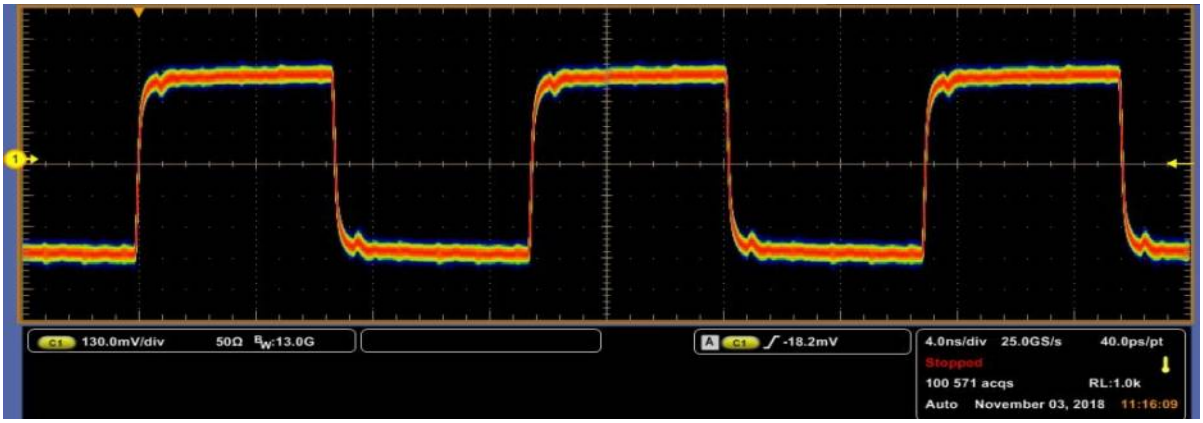
  - **Waveform/Plot**



- **7-8 : Max Duty Cycle : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Max Duty Cycle < 60.0%;	50.49%	1.3468ns	9.51%	Pass

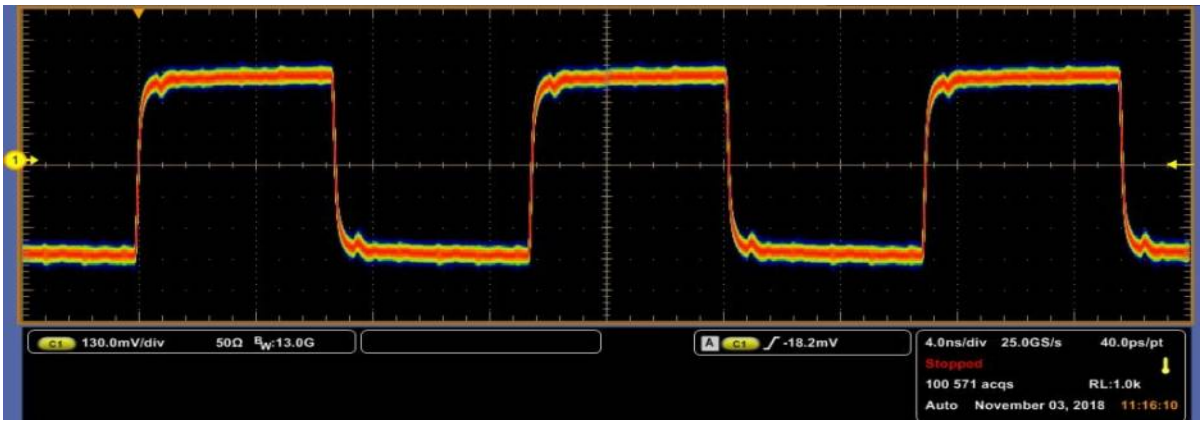
  - **Waveform/Plot**



- **7-8 : Min Duty Cycle : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
40.0% < Min Duty Cycle;	49.6%	1.3468ns	9.6%	Pass

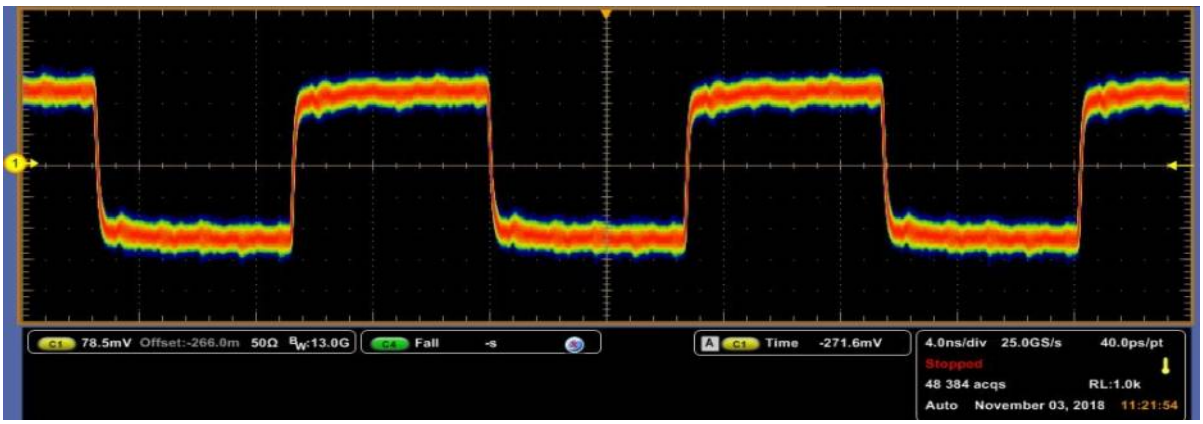
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : CK+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8456V	54.40mV	145.6mV	Pass

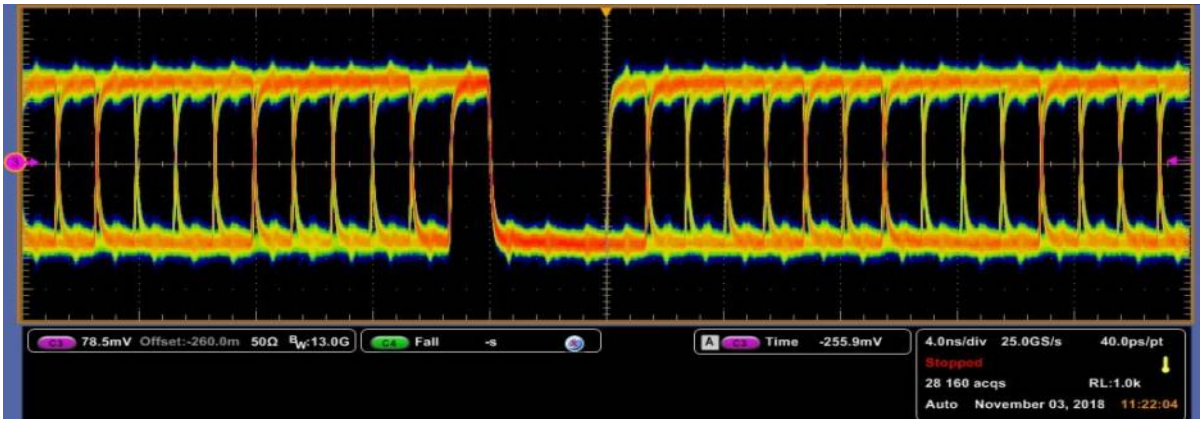
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D0+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8343V	65.67mV	134.3mV	Pass

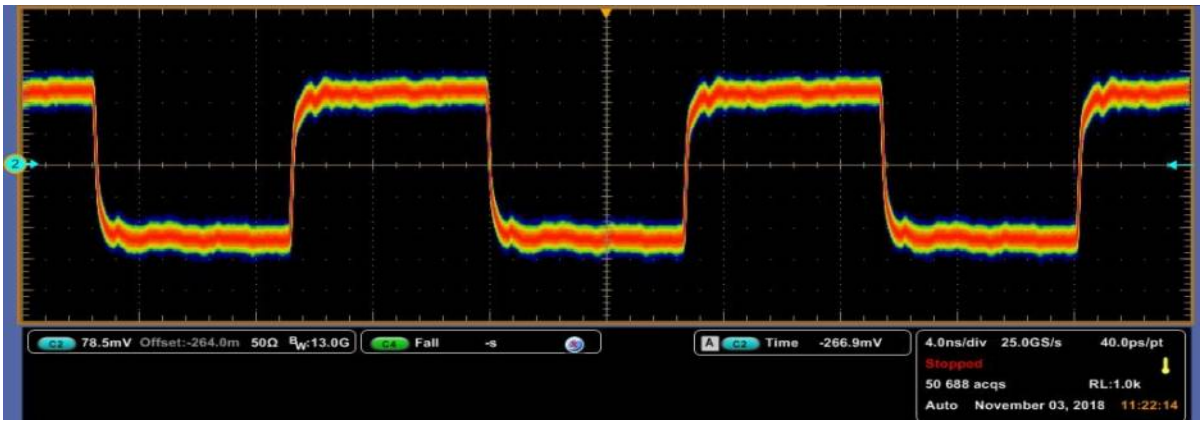
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : CK-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8476V	52.40mV	147.6mV	Pass

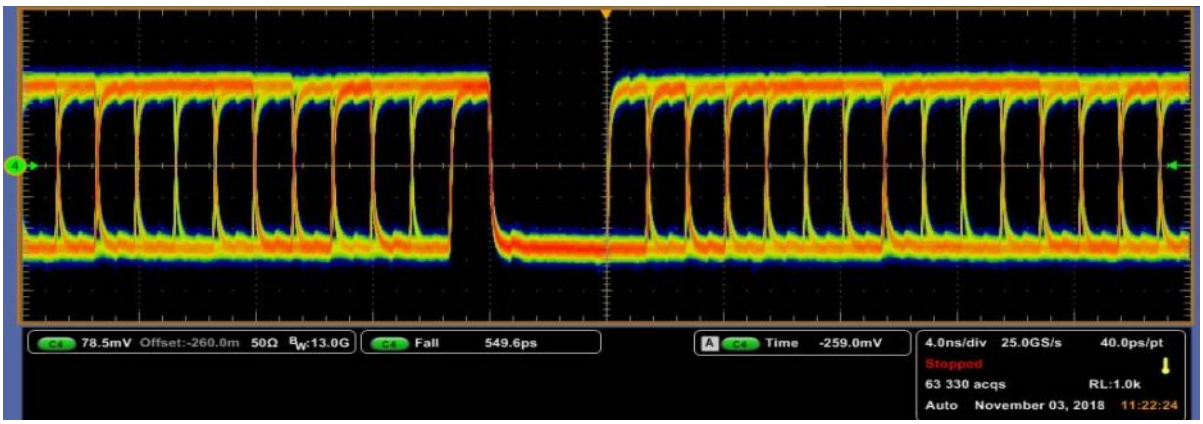
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D0-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8328V	67.24mV	132.8mV	Pass

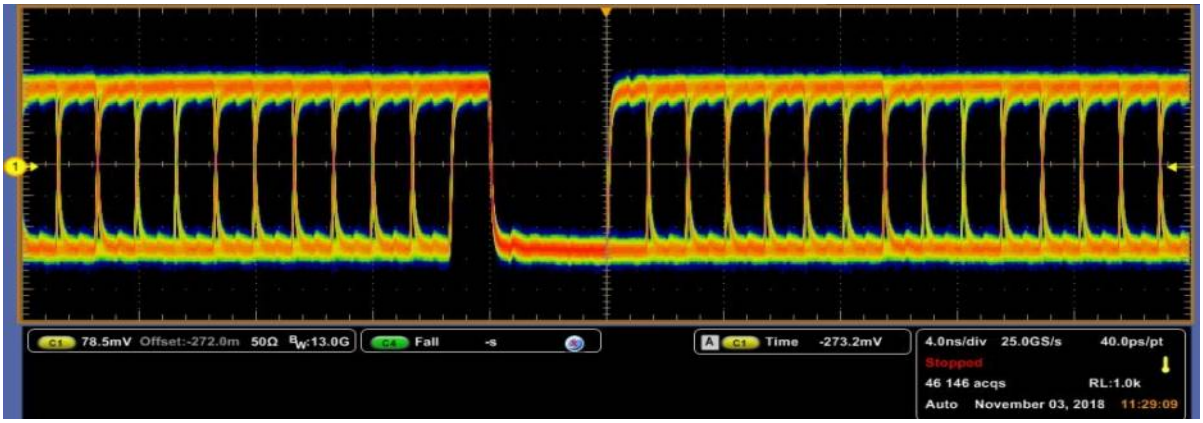
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D1+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8208V	79.24mV	120.8mV	Pass

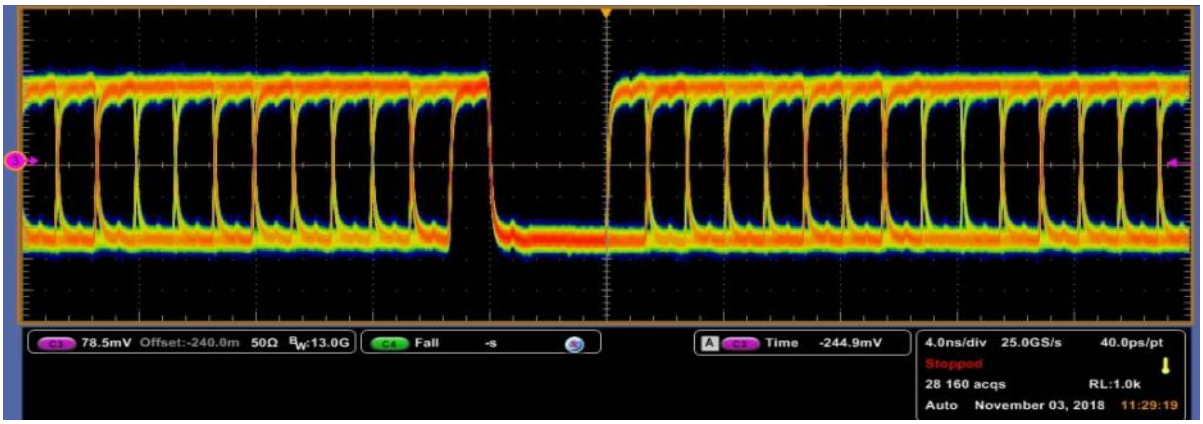
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D2+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8606V	39.39mV	160.6mV	Pass

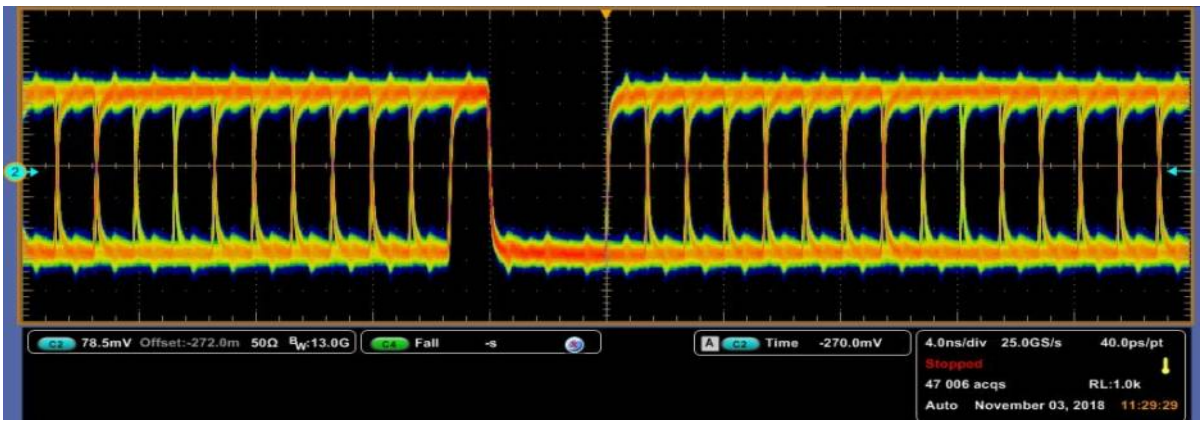
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D1-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8239V	76.10mV	123.9mV	Pass

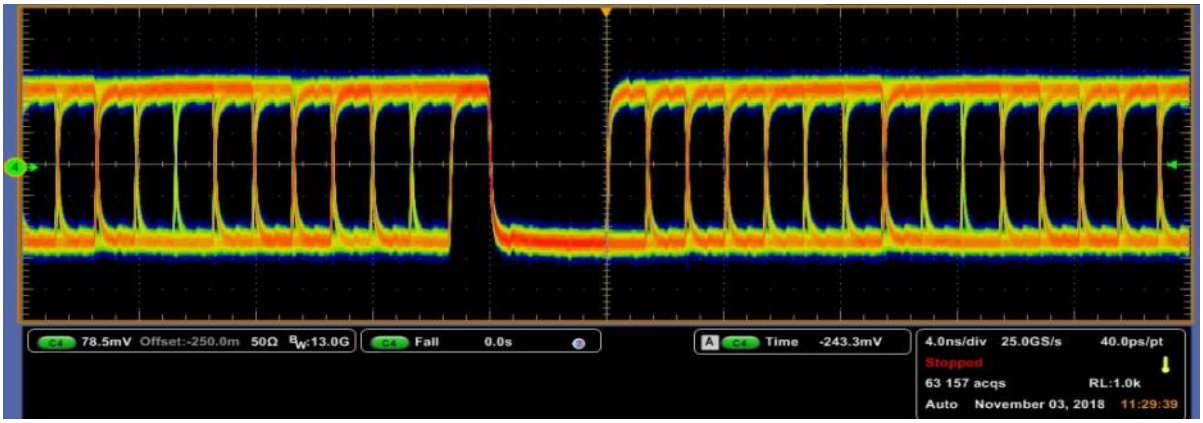
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D2-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8600V	39.97mV	160.0mV	Pass

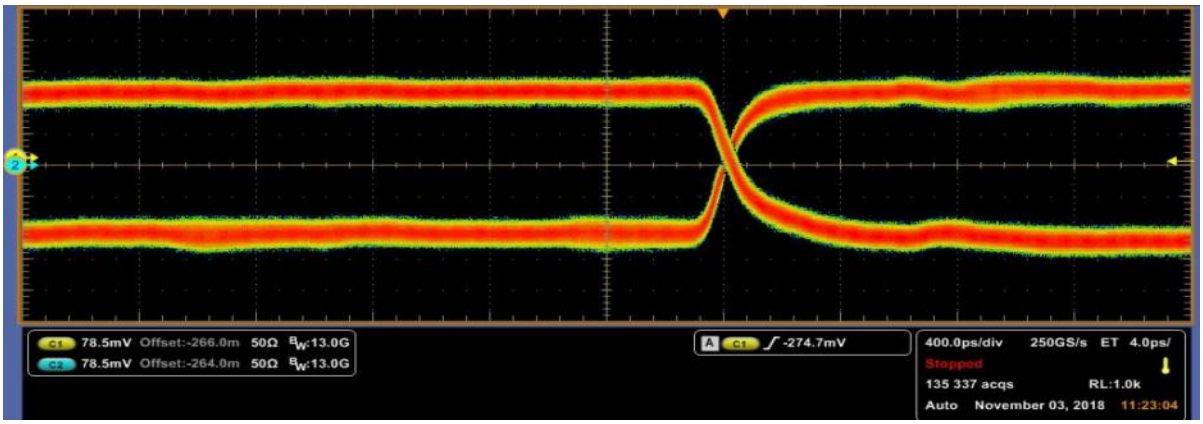
  - **Waveform/Plot**



- **7-7 : Source Intra-Pair Skew : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.018*Tbit	1.3468ns	0.13*Tbit	Pass

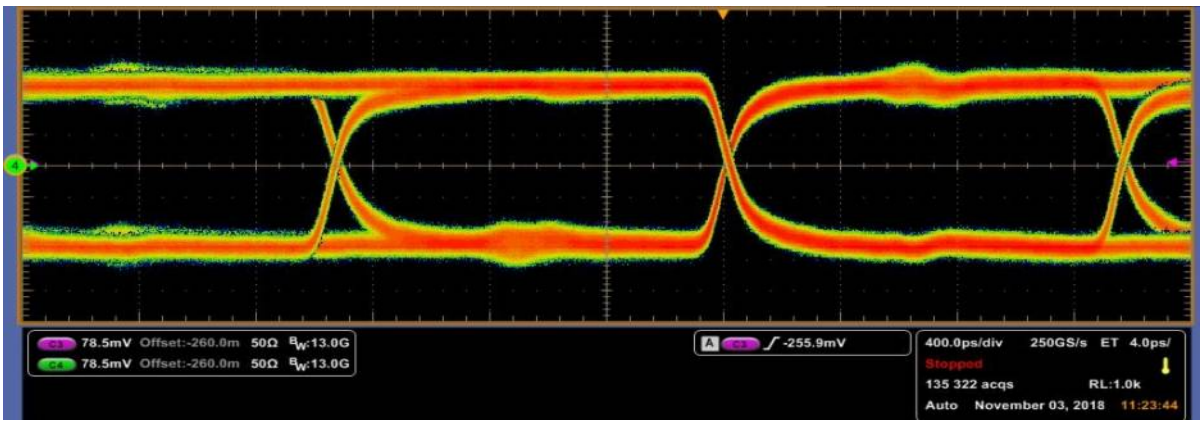
  - **Waveform/Plot**



- **7-7 : Source Intra-Pair Skew : D0**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.012*Tbit	1.3468ns	0.14*Tbit	Pass

  - **Waveform/Plot**

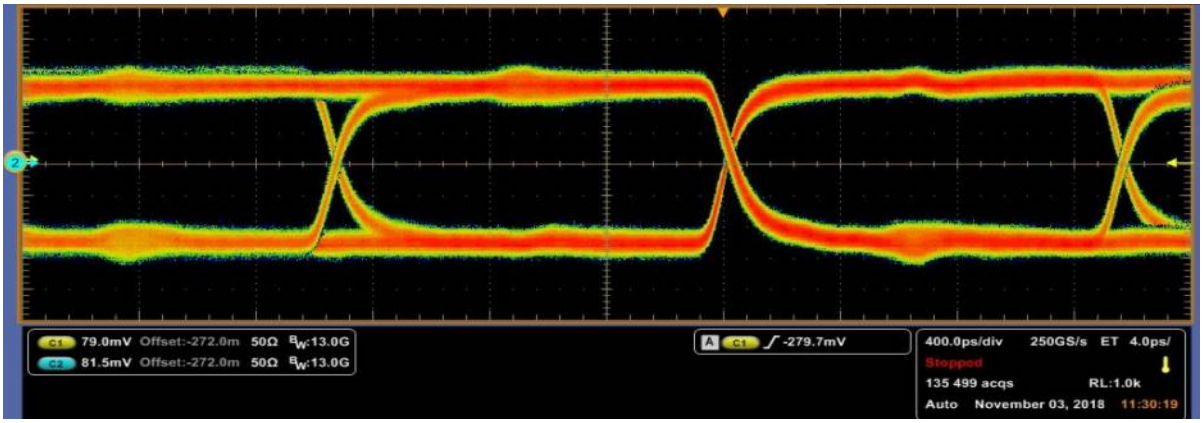


7-7 : Source Intra-Pair Skew : D1

Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.018*Tbit	1.3468ns	0.13*Tbit	Pass

Waveform/Plot

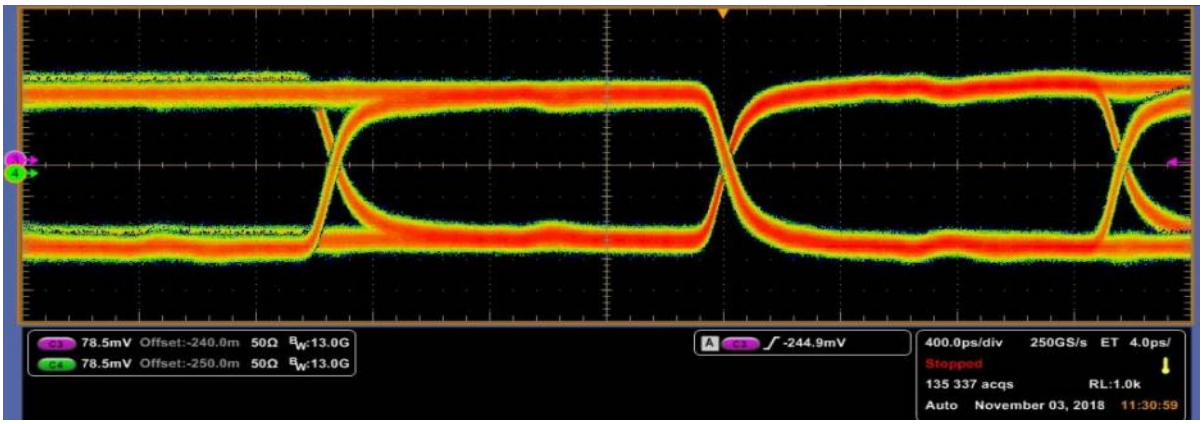


7-7 : Source Intra-Pair Skew : D2

Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.006*Tbit	1.3468ns	0.14*Tbit	Pass

Waveform/Plot



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