DDR DQ Window Check Method and Result Analysis

Issue **00B02**

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About This Document

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3516C	V500
Hi3516D	V300
Hi3516A	V300
Hi3559	V200
Hi3556	V200

Intended Audience

This document is intended for:

- Technical support engineers
- Software development engineers

Change History

Changes between document issues are cumulative. The latest document issue contains all changes made in previous issues.

Issue 00B02 (2019-02-28)

This issue is the second draft release.

The description of Hi3516A V300 is added.

Issue 00B01 (2018-11-20)

This issue is the first draft release.

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1.1 Check Method

1.1.1 Procedure

Step 1 Prepare a board which can start normally, and connect the serial port of the board with the PC to enable proper communication.

Step 2 Enable the board to stay under U-Boot, and run the **mw** command to configure the registers to enable DDR training. The configuration depends on the actual DDR specifications used by the board. The following table describes the switch configurations of the DDR training registers.

Register Address	Register Description	Register Value	Configurations
0x120200a0	Training control register	0x0	Enable training for PHY 0 and PHY 1.
		0x1	Enable training for PHY 1 only.
		0x2	Enable training for PHY 0 only.
		0xffffffff	Disable training for PHY 0 and PHY 1.

Step 3 Run the **ddr dataeye** command to view the DDR DQ window.

----End

1.1.2 Examples

Window Check Example for DDR3 SDRAM

Use the DDR3 as an example. You only need to input the following commands in U-Boot:

mw 0x120200a0 0x2 //Enable PHY0 training.

ddr dataeye //Check the DQ window.

NOTE

- The chip has only one PHY (that is, PHY0). During window check, the control bit for PHY1 cannot to be enabled.
- The command for window check is irrelevant to the DDR3, LPDDR3, or DDR4.

NOTICE

The preceding operations are all performed in U-Boot.

No modules except the CPU can access the DDR SDRAM in U-Boot; otherwise, the check result becomes inaccurate.

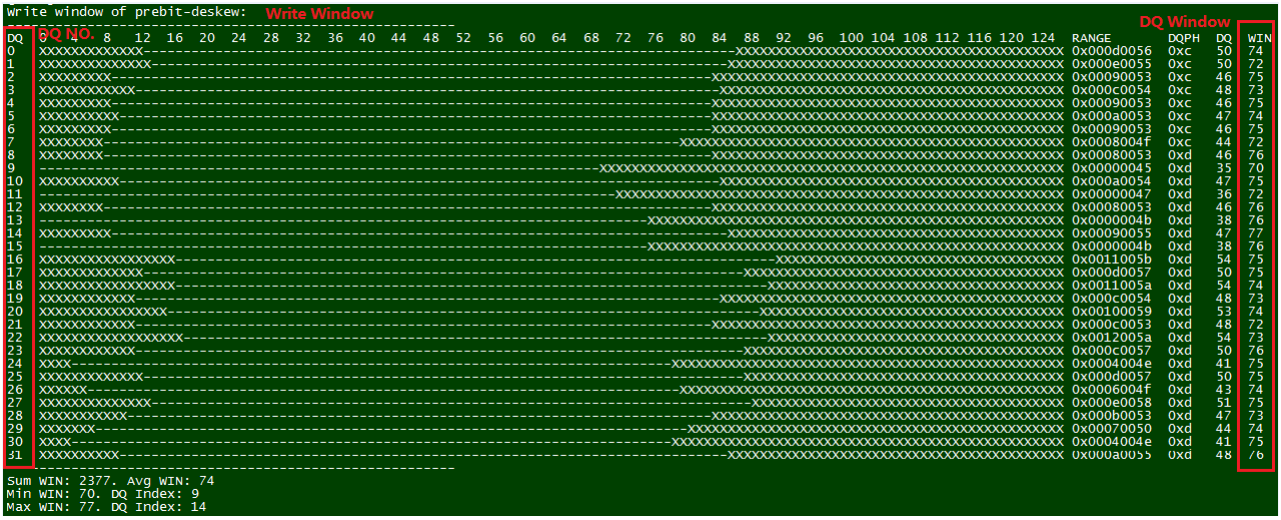
1.2 Result Analysis

The window check results are displayed in the read and write directions. The window size is focused.

1.2.1 Write Window

The write window has following features:

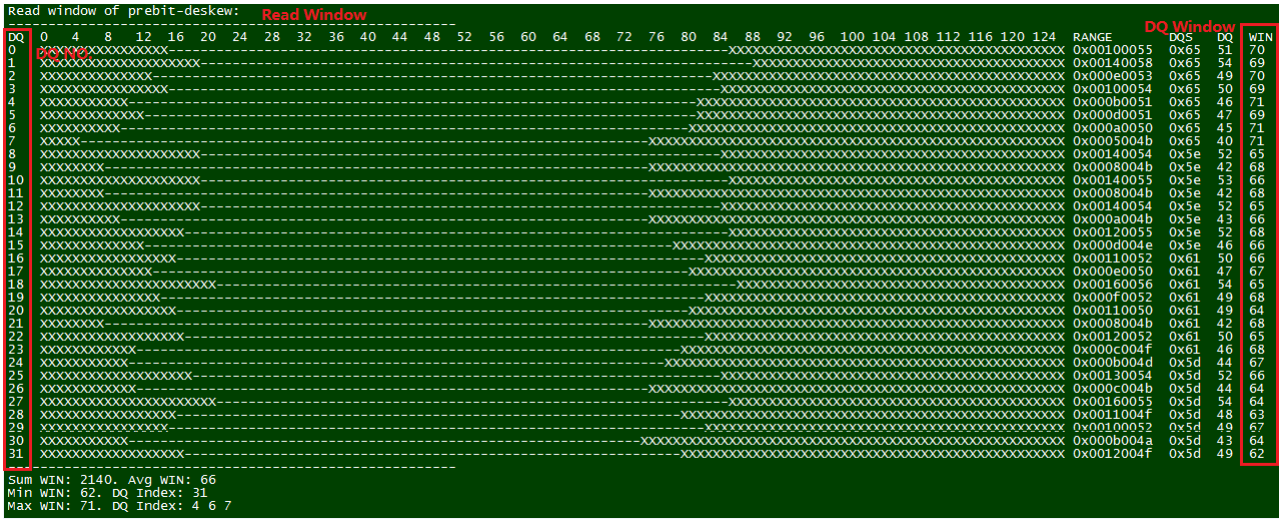
- The flag of write window is shown at the top of the print result.
- The DQ sequence numbers are displayed on the left.
- The window size of each DQ is listed on the right.
- The DQ statistics result is provided at the bottom, including the minimum value, the maximum value, and the average value.



1.2.2 Read Window

The read window has following features:

- The flag of read window is shown at the top of the print result.
- The DQ sequence numbers are displayed on the left.
- The window size of each DQ is listed on the right.
- The DQ statistics result is provided at the bottom, including the minimum value, the maximum value, and the average value.



1.2.3 Window Judgment Standard

Table 1-1 describes the standard levels of the write and read windows based on the test result of the demo board. If the standard requirements are not met, the DDR SDRAM may have unstable factors.

Table 1-1 Standard levels

DDR	Standard Levels
1600 Mbit/s	≥ 52 levels
1800 Mbit/s	≥ 48 levels
2133 Mbit/s	≥ 45 levels

Statement: The DDR DQ window results serve as the data and methods that are provided for you to analyze DDR problems. Even if the standards are satisfied, the DDR performance cannot be ensured. You need to verify the DDR reliability according to your own test standards.