



Hi3518E 720p IP Camera SoC

Brief Data Sheet

Issue	01
Date	2014-01-10
Initial Release Date	2014-01-10

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Hi3518E 720p IP Camera SoC

Key Specifications

Processor Core

- ARM9@Max. 440 MHz, 16 KB I-cache, and 16 KB D-cache

Video Encoding Protocols

- H.264 main profile
- H.264 baseline profile
- MJPEG/JPEG baseline encoding

Video Encoding Performance

- 2-megapixel maximum resolution for H.264 encoding
- Maximum real-time encoding performance of H.264&JPEG streams: 720p@25 fps+720p@3 fps JPEG snapshot
- Multi-stream encoding
- Bit rate control in CBR, VBR, or ABR mode, bit rate ranging from 16 kbit/s to 20 Mbit/s
- Encoding frame rate ranging from 1/16 fps to 30 fps
- Encoding of eight ROIs
- OSD overlay of eight regions before encoding

Integrated Memory

- Integrated 16-bit DDR2
- Maximum capacity of 512 Mbits

Intelligent Video Analysis

- Integrated IVE, supporting various intelligent analysis applications such as motion detection, boundary security, and video diagnosis

Video and Graphics Processing

- Video pre-processing, including 3D denoising, image enhancement, edge enhancement, and deinterlacing
- Anti-flicker for output videos and graphics
- 1/16x to 8x video scaling
- 1/2x to 2x graphics scaling
- OSD overlay pre-processing for eight regions
- Hardware graphics overlay post-processing for the videos at two layers (video layer and graphics layer 1)

ISP

- AE and AWB for adjustment
- Highlight compensation, backlight compensation, gamma correction, and color enhancement
- Defect pixel correction, denoising, and digital image stabilizer
- ISP tuning tools for PCs

Audio Encoding/Decoding

- Voice encoding/decoding in compliance with multiple protocols by using software
- G.711, ADPCM, and G.726 protocols
- Echo cancellation

Security Engine

- Various encryption and decryption algorithms using hardware, such as AES, DES, and 3DES
- Digital watermark

Video Interfaces

- Input
 - 8-, 10-, or 12-bit RGB bayer inputs, a maximum of 74.25 MHz clock frequency
 - BT.601 and BT.656
 - Compatibility with mainstream HD CMOS sensors provided by SONY, Aptina, OV, and Panasonic
 - Compatibility with CCD sensors
 - Various sensor levels supported
 - Programmable sensor clock output
 - Video inputs at 1080p@30 fps or 720p@30 fps
- Output
 - One BT.1120 VO interface for connecting to the external HDMI or SDI, maximum performance of 1080p@30 fps

Audio Interfaces

- Integrated audio CODEC, supporting 16-bit audio inputs and outputs

Peripheral Interfaces

- POR and external reset
- One integrated high-precision RTC
- One integrated low-speed ADC with dual channels
- Three UART interfaces
- One IR interface, one I²C interface, one SPI master/slave interface, multiple GPIO interfaces
- One SDIO 2.0 interface, supporting SDHC
- Maximum four PWM interfaces
- One USB 2.0 host port
- RMII and MII modes; 10/100 Mbit/s full-duplex or half-duplex mode, PHY clock output

External Memory Interfaces

- SPI NOR flash interface
 - 1-, 2-, or 4-bit SPI NOR flash
- Booting from the NOR flash

SDK

- SDK based on Linux-3.0.y
- High-performance H.264 PC decoding library

Physical Specifications

- Power consumption
 - Typical power consumption of 900 mW
 - Multi-level power-saving mode
- Operating voltages
 - 1.2 V core voltage
 - 3.3 V I/O voltage, and 3.8 V margin voltage
 - 1.8 V voltage of the internal SDRAM
 - Operating temperature ranging from 0 °C (32 °F) to +70 °C (158 °F)
- Package

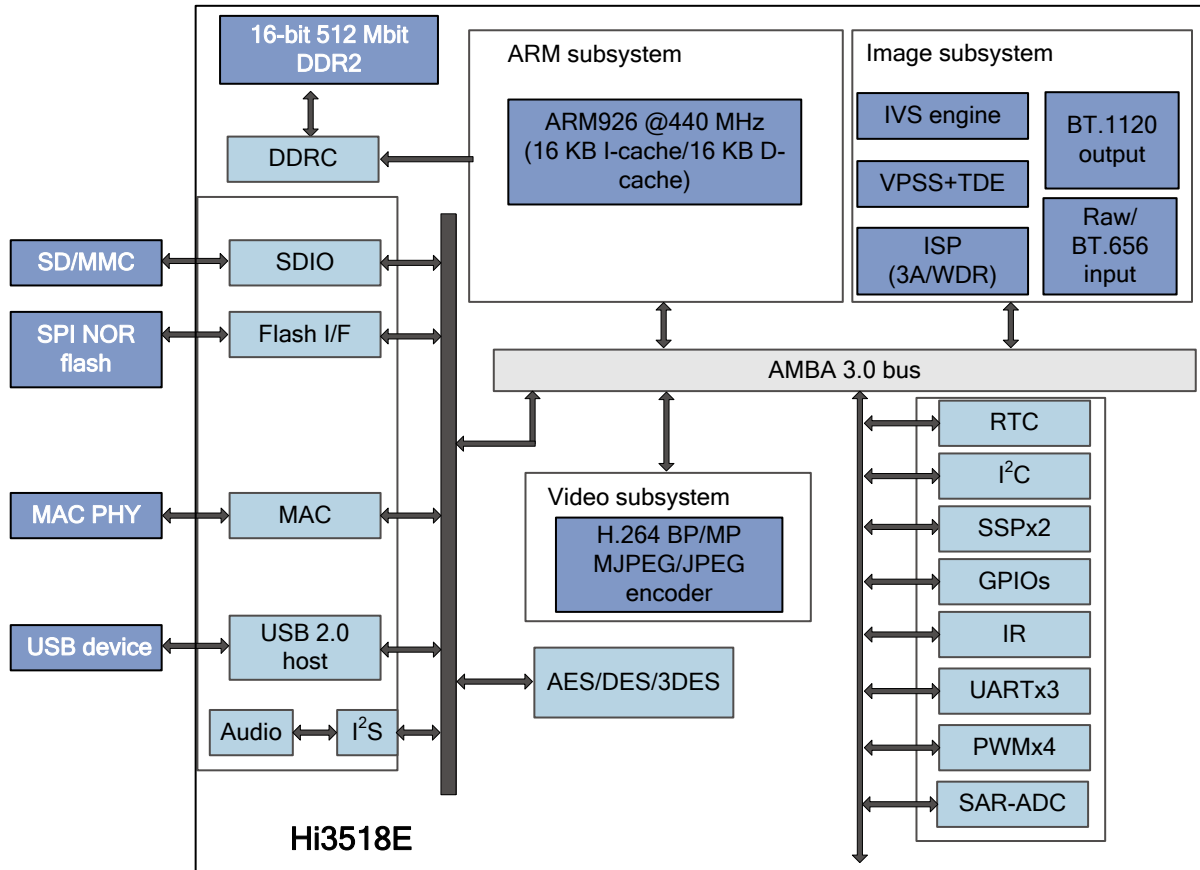


Hi3518E 720p IP Camera SoC

- RoHS, BGA220
- Ball pitch of 0.65 mm (0.026 in.) and body size of 11

mm x 11 mm (0.43 in. x 0.43 in.)

Functional Block Diagram

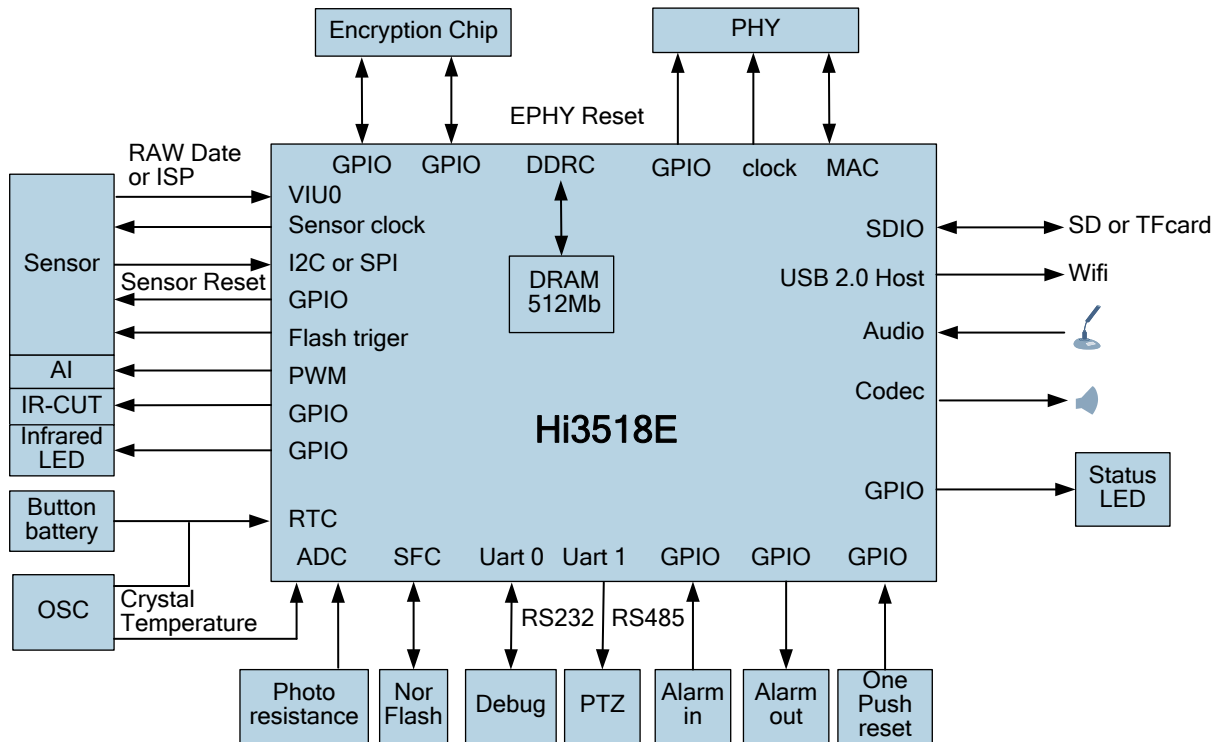


The Hi3518E is a new-generation IP camera SoC for civilian use. It has an integrated ISP, optimized algorithm for graphics processing before encoding, and an H.264 encoder. By using the advanced low-power technology and low-power architecture, the Hi3518E is industry-leading in the aspects of low bit rate, high picture quality, and low power consumption. The EBOM costs for the Hi3518E IP camera are significantly reduced by integrating the DRAM, POR, RTC, and audio CODEC and supporting various sensor levels and clock outputs. Similar to other HiSilicon DVR and NVR SDKs, the Hi3518E SDK allows rapid mass production and facilitates system layout of IP cameras, DVRs, and NVRs.



Hi3518E 720p IP Camera SoC

Hi3518E IP Camera Solution



Acronyms and Abbreviations

3DES	triple data encryption standard
ABR	average bit rate
AE	automatic exposure
AES	advanced encryption standard
AWB	automatic white balance
BGA	ball grid array
CBR	constant bit rate
CCD	charge coupled device
CMOS	complementary metal-oxide semiconductor
CODEC	coder/decoder
DES	data encryption standard
DVR	digital video recorder
GPIO	general purpose input/output
HD	high-definition



Hi3518E 720p IP Camera SoC

HDMI	high-definition multimedia interface
I²C	inter-integrated circuit
IR	infrared
ISP	image signal processor
IVE	intelligent video engine
MII	media independent interface
NVR	network video recorder
OSD	on-screen display
PHY	physical
POR	power-on-reset
PWM	pulse-width modulation
RGB	red-green-blue
RMII	reduced media independent interface
RoHS	restriction of hazardous substances
ROI	region of interest
RTC	real-time clock
SDHC	secure digital high capacity
SDI	serial digital interface
SDIO	secure digital input/output
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SoC	system-on-chip
SPI	serial peripheral interface
UART	universal asynchronous receiver transmitter
VBR	variable bit rate
VO	video output