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User Guide

Issue

Date

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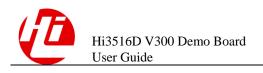
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About This Document

Purpose

This document describes the functional features, hardware features, and hardware configurations of the Hi3516D V300 demo board. It also describes how to debug the Hi3516D V300 demo board by using software.

Related Version

The following table lists the product version related to this document.

Product Name	Version Rolls 1
Hi3516D	V300 ,,, o

Intended Audience

This document isontended for:

- Technical support engineers
- Board hardware development engineers

Change History

Changes between document issues are cumulative. The latest document issue contains all changes made in previous issues.

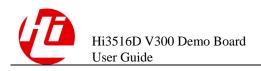
Issue 00B02 (2019-01-15)

This issue is the second draft release, which incorporates the following changes:

Section 3.2 and 3.3 are modified.

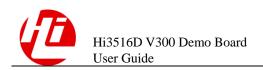
Issue 00B01 (2018-09-04)

This issue is first draft release.



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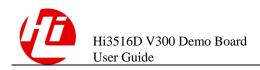
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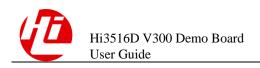
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1 Introduction

1.1 Overview

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The Hi3516D V300 demo board is a function demonstration board that is developed based on the HiSilicon media processor Hi3516D V300. The demo board provides superior multimedia processing functions, various peripheral interfaces, and hardware reference designs based on the Hi3516D V300. You can complete hardware development by modifying only module circuits on the demo board.

1.2 Deliverables

The Hi3516D V300 demo board package provides the following items:

- One Hi3516D V300 dente board: Hi3516DV300DMEB
- One sensor board
- One power adapted with the specifications of 100–240 V AC input, 50 Hz and 12 V DC output, 2 A
- Two 16-bitwide DDR3 SDRAMs, 2 Gb x 2, with the H5TQ2G63GFR model
- 16 MBSPI NOR flash with the MX25L12835 model

1.3 Related Components

The following components are not included in the Hi3516D V300 demo board package; however, they are required for program debugging. Therefore, you must prepare them.

- Network cables
- Audio/Video receiving devices such as the TV set, stereo equipment, and camera
- Serial cables



2 Hardware

2.1 Architecture and Interfaces

Figure 2-1 shows the interfaces on the Hi3516D V300 demo bookd.

Figure 2-1 Interfaces on the Hi3516D V300 demo board.

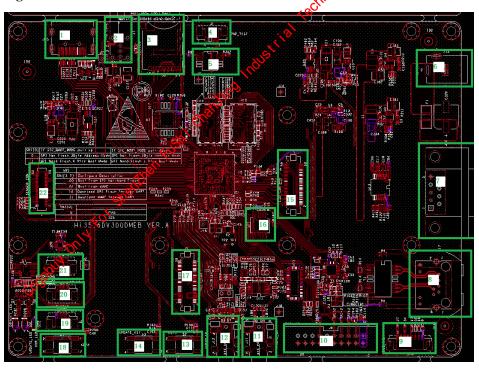
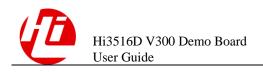


Table 2-1 describes the corresponding peripheral interfaces, keys, and switches in Figure 2-1.

Table 2-1 Peripheral interfaces on the Hi3516D V300 demo board

No.	Description
1	HDMI
2	USB 2.0 port



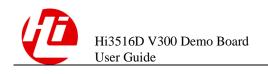
No.	Description
3	SD card holder
4	Testing interface for the core power and DDRIO power
5	Dual in-line package (DIP) SW3
6	Board power interface
7	UART0 port
8	RJ45 megabit Ethernet port
9	I ² S interface
10	JTAG interface
11	ADUIO_OUT
12	AUDIO_IN
13	KEY1
14	ADUIO_OUT AUDIO_IN KEY1 UPDATE_MODE key Liquid crystal display (LCD) consector.
15	Liquid Crystal display (LCD) Condector
16	SW1 Industri
17	SDIO1 Wi-Fi connector
18	KEY2 Chand
19	UART1 port
20	DC-IRIS interface
21	P-IRS interface
22	60-pin sensor interface

2.2 GPIO Distribution

Table 2-2 describes the GPIO distribution of the Hi3516D V300 demo board.

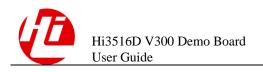
Table 2-2 GPIO distribution of the Hi3516D V300 demo board

Pin	GPIO Pin	DMEB Board
I2C7_SCL/GPIO10_6	GPIO10_6	Test point
I2C7_SDA/GPIO10_7	GPIO10_7	Test point
PWM1/GPIO6_7	GPIO6_7	DC_IRIS_PWM4/PWM_OUT0_LCD. PWM_OUT0_LCD is used by default.



Pin	GPIO Pin	DMEB Board
UART1_CTSN/GPIO5 _1/UART4_TXD	GPIO5_1	WIFI_LED control. The indicator is on when the output is high level and off when the output is low level.
UART1_RTSN/GPIO5 _0/UART4_RXD	GPIO5_0	UPDATE_LED control. The indicator is on when the output is high level and off when the output is low level.
LSADC_CH1/GPIO10 _4	GPIO10_4	Connects to the SGM8903 mute pin.
GPIO0_3/IR_IN/LCD_ DATA18	GPIO0_3	TP_RST and P_IRIS_CONTROL1 are multiplexed. TP_RST is used by default.
GPIO0_4/LCD_DATA 21	GPIO0_4	TP_INT and P_IRIS_CONTROL2 are multiplexed. TP_INT is used by default.
GPIO0_5/LCD_DATA 22	GPIO0_5	LCD_RST and P_JRIS_CONTROL3 are multiplexed. LCD_RST is used by default.
GPIO0_6/LCD_CLK/V OU_CLK	GPIO0_6	DIS_FLOW_CTRL and P_IRIS_CONTROL4 are multiplexed. DIS_FLOW_CTRL is used by default.

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3 Operation Guide

3.1 Precautions

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The Hi3516D V300 demo board applies to the laboratory or engineering development environment. Take the following precautions before performing operations:



Never perform the hot-swap operation on the board in any case.

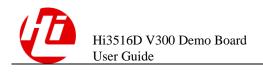
- Take antistatic measures before uppacking or installing the board to prevent the board hardware from being damager by the electrostatic discharge (ESD).
- Hold the board on the edge and do not touch the exposed metal on the board. Otherwise, the board components may be damaged by the ESD.
- Place the Hi3516D 300 demo board on a dry workstation and keep it away from heat sources, electromagnetic interference sources, radiant sources, and electromagnetic susceptibility equipment (such as the medical equipment).
- Familiarize yourself with the layout of the Hi3516D V300 demo board. See Figure 2-1. Ensure that you can identify the components such as the switches, connectors, and indicators and know their positions.

3.2 Board Settings

The operating mode of the Hi3516D V300 is selected by using the keys and selecting the resistors to be welded on the Hi3516D V300 demo board. See Table 3-1.

Table 3-1 Board settings in various boot modes

Boot Mode	Value	Resistor Connection	Remarks
BOOT_SEL[1:0]	00	SW1.3 and SW1.2 are set to 0.	Boot from the SPI flash.



Boot Mode	Value	Resistor Connection	Remarks
	01	SW1.3 is set to 0, while SW1.2 is set to 1.	Boot from the eMMC.
	10	SW1.3 is set to 1, while SW1.2 is set to 0.	FastbootUpdate SPI flash (default)
	11	SW1.3 and SW1.2 are set to 1.	FastbootUpdate eMMC (default)
[SFC_DEVICE_MODE: SFC_BOOT_MODE]	00	SW1.0 is set to 0, R188 is removed, and R367 is soldered.	SPI NOR flash. The default addressing mode is 3-byte mode.
	01	SW1.0 is set to 0, R367 is removed, and R188 is soldered.	SPI NOR flash. The default addressing mode is 4-byte mode.
	10	SW1.0 is set to 1, R188 is removed, and R367 is soldered.	SPI NAND flash. The default addressing mode is 1-wire boot mode.
	11 vanji	SW1.0 is set to 1, \$R367 is removed, and R188 is soldered.	SPI NAND flash. The default addressing mode is 4-wire boot mode.
UPDATE_MODE	sus Cr.	S3 key is pressed down.	Enable update from SDIO0 or USB.
UPDATE_MODE sherther Fi	1	S3 key is not pressed down.	Disable UPDATE_MODE (default).

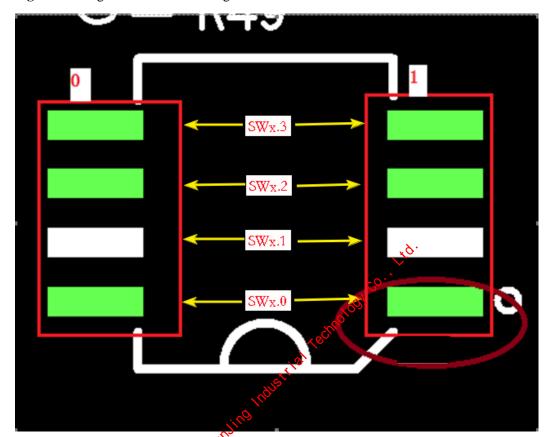
Table 3-24TAG settings

Boot Mode	Value	Instructions	Remarks
JTAG/SPI1/I2S	0	SW3.0 is set to 0.	JTAG
	1	SW3.0 is set to 1.	SPI1/I2S (SPI1 and I2S are soldered by using resistors.)

3.3 DIP Switch Usage

As shown in Figure 3-1, the right side of the DIP switch is 1 while the left side is 0.

Figure 3-1 Diagram of DIP switch usage



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