



# Hi3516D V300 DDR3L Test Report

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# System History

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Date	Contents	Remarks
2018-11-16	The test is performed based on the DDR3L 1866MHz AC135 standard	
Note: All the test data in this report is the test result of the HiSilicon test sample and is only for reference. Note that the tests conducted by HiSilicon cannot replace customers' related tests.		

# Information



Chipset	Hi3516DV300
Board Name	HI3516DV300MEBLITE VER.A
DRAM Part Number	MT41K256M16TW-093:P
Oscilloscope	DSA72004C TEKTRONIX
Temperature	25°C
DRAM Operating Frequency	900MHz(DDR3L)
VPP/Vdd/Vref_CA/Vref_DQ/Vcore	1.35V/0.675V/0.675V/0.9V
DRAM_ODT	120ohm
SOC_ODT	120ohm
DRAM RON	40ohm
SOC RON	CK=34ohm 1T(CS/CKE/ODT)=34ohm 2T=34ohm DQ=40ohm DQS=40ohm



# Signal Integrity Summary& Conclusion

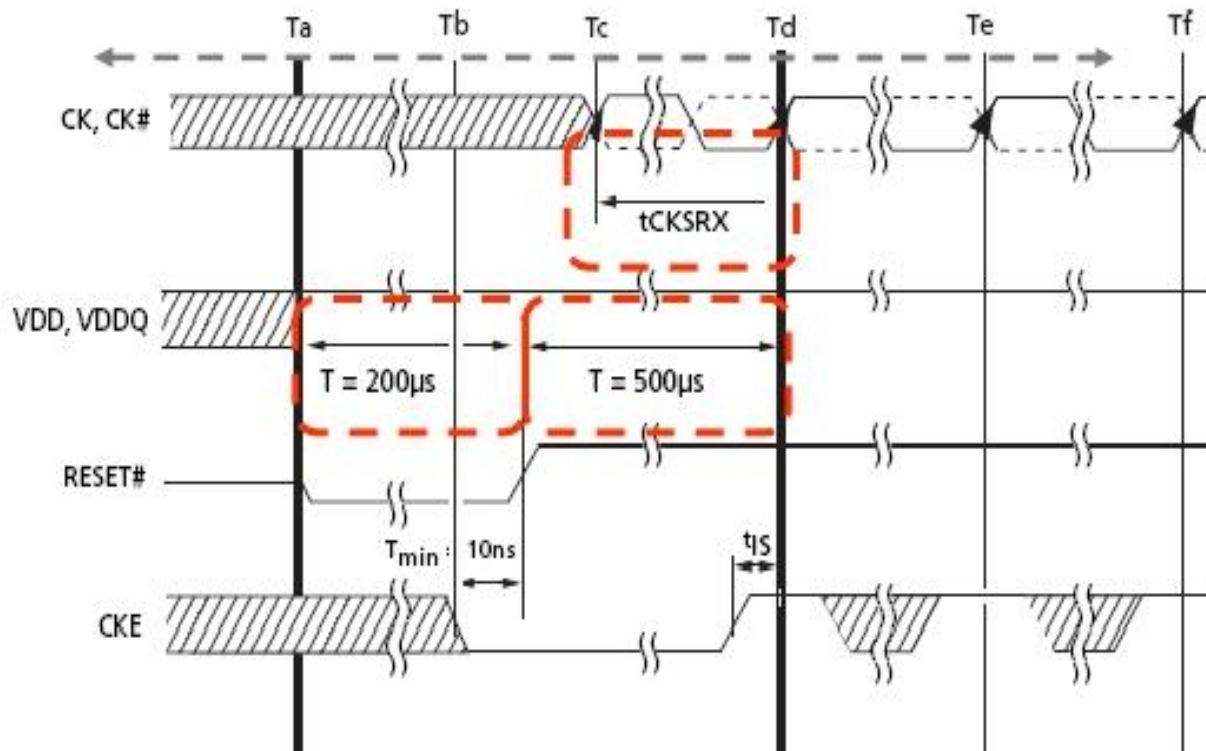
Judgment&Summary		
<p>1.tDQSH, tDQSL fail</p> <p>Impact: This indicator affects the window size in the write direction of the DQ. The margin of the measured window is sufficient. The risk of this indicator failure is low.</p>		
Measurement Item	Result	Remark
Sequence Check	PASS	
Power Check	PASS	
Signal Integrity Check	FAIL	

# Power Up Initialization Sequence Check Result



## ▣ SPEC

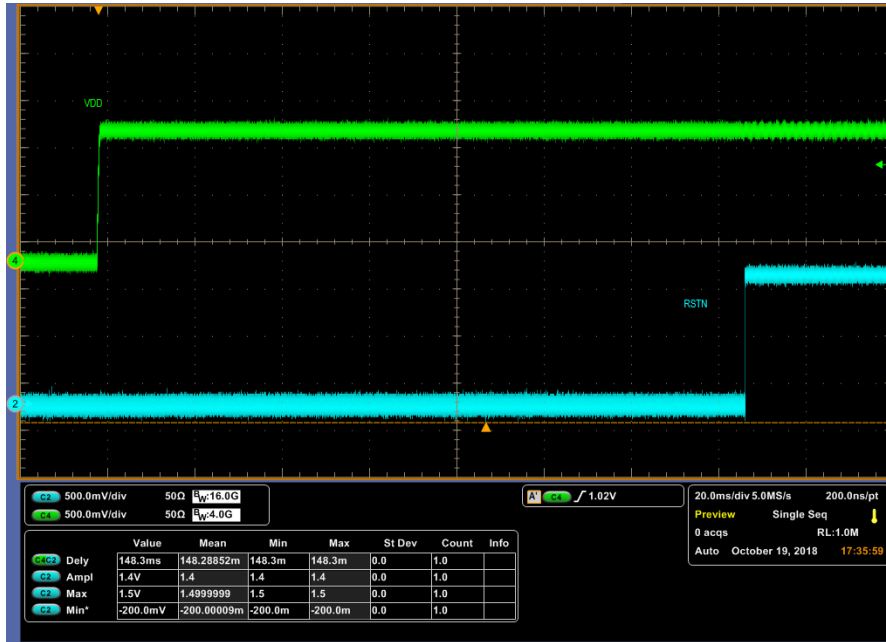
### 3.3.1 Power-up Initialization Sequence (Cont'd)



# Power Up Initialization Sequence Check Result



## ▣ Stable VDD to /Reset Up

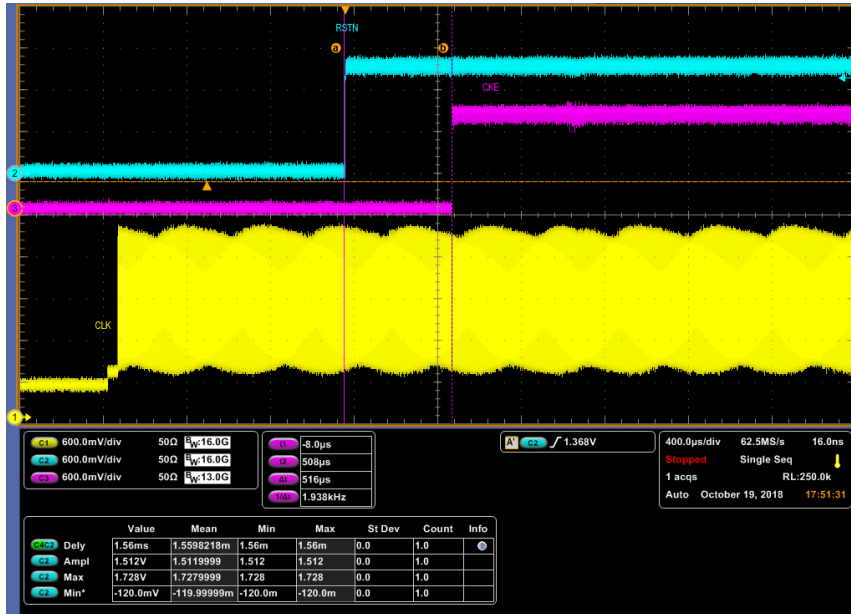


Parameter	Time	Spec	Result	Remark
Stable VDD to /Reset Up	148.3ms	Min:200us	PASS	RESET_n needs to be maintained for minimum 200us with stable power

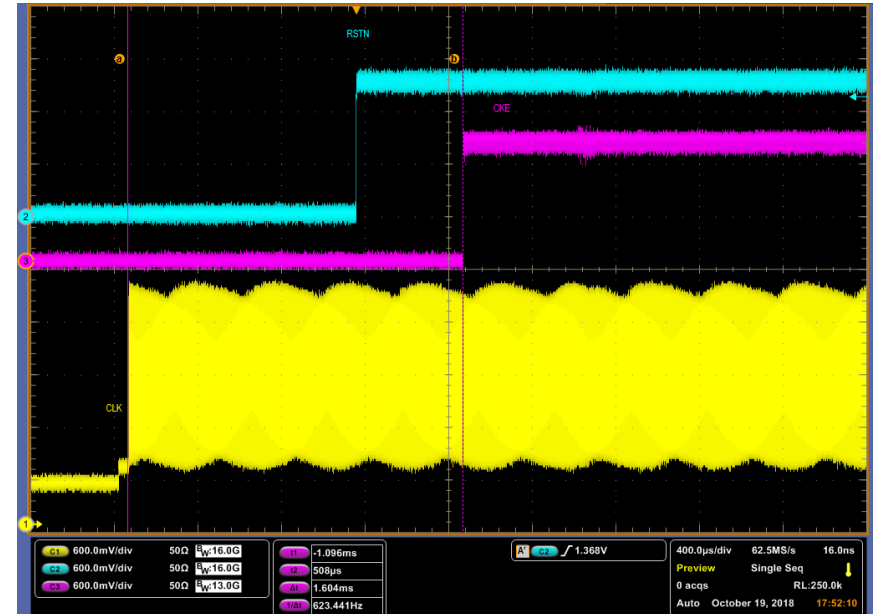
# Power Up Initialization Sequence Check Result



## □ /Reset Up To CKE Up



## □ tCKSRX



Parameter	Time	Spec	Result	Remark
/Reset Up To CKE Up	516us	Min:500us	PASS	After /RESET is de-asserted. Wait for another 500us until CKE becomes active.(JEDEC spec.)
tCKSRX	1.6ms	Min:Max(5nCK,10ns)	PASS	Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active.(JEDEC spec.)

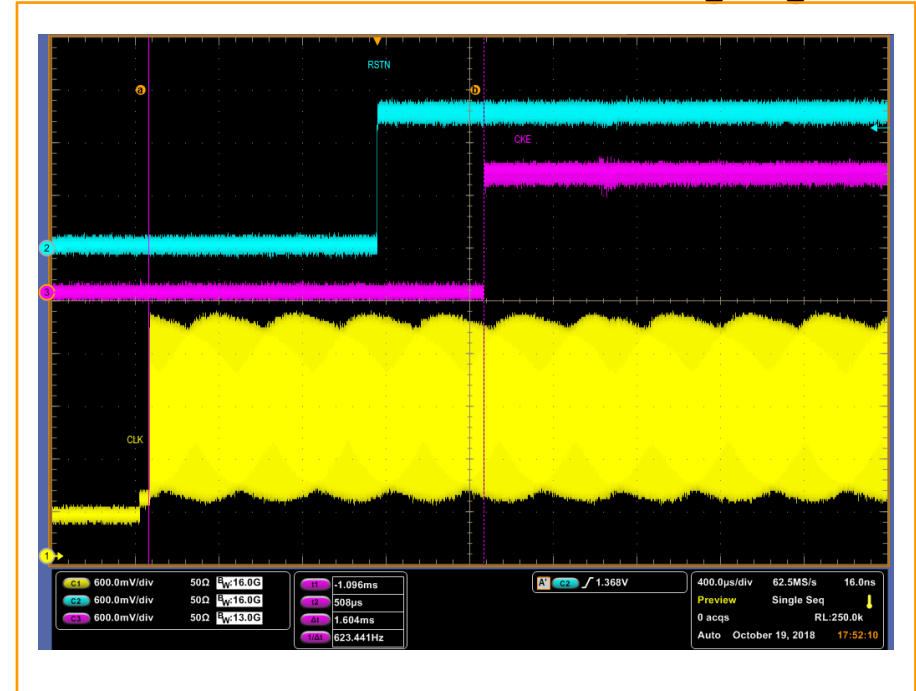
# Power Up Initialization Sequence Check Result



## ▣ VDD Rising Time



## ▣ CKE Hold LOW Time To Reset Rising Edge



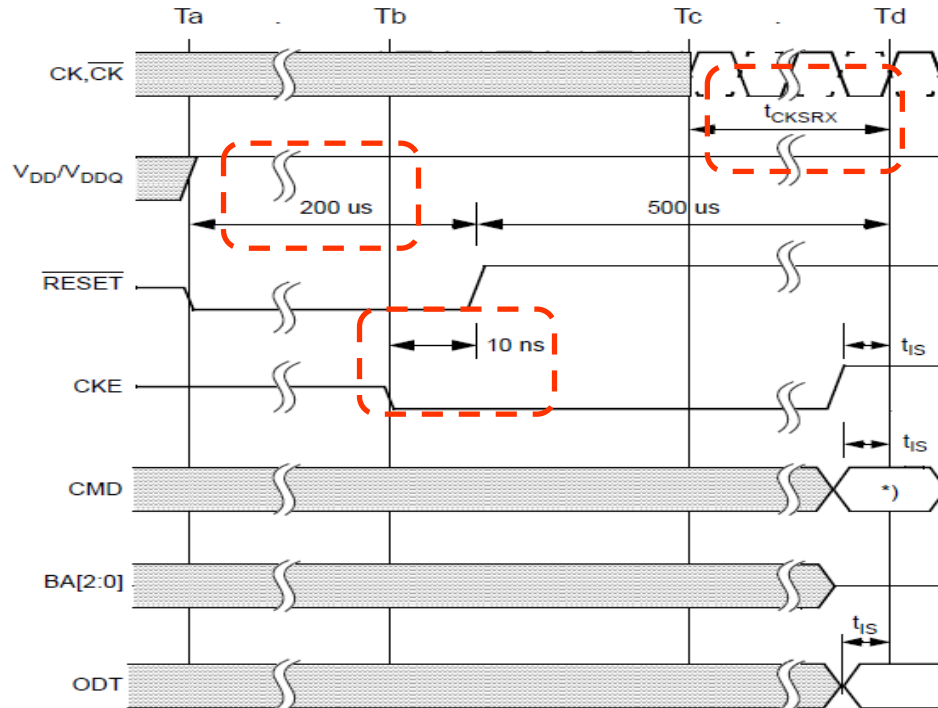
Parameter	Time	Spec	Result	Remark
VDD Rising Time	414us	Max:200ms	PASS	The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms.(JEDEC spec.)
CKE Falling Edge to Reset Rising Edge	> 10ns	Min:10ns	PASS	CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns).





# Reset Initialization Sequence Check Result

## ■ SPEC



## ■ CKE Hold LOW Time To Reset Rising Edge\_DDR

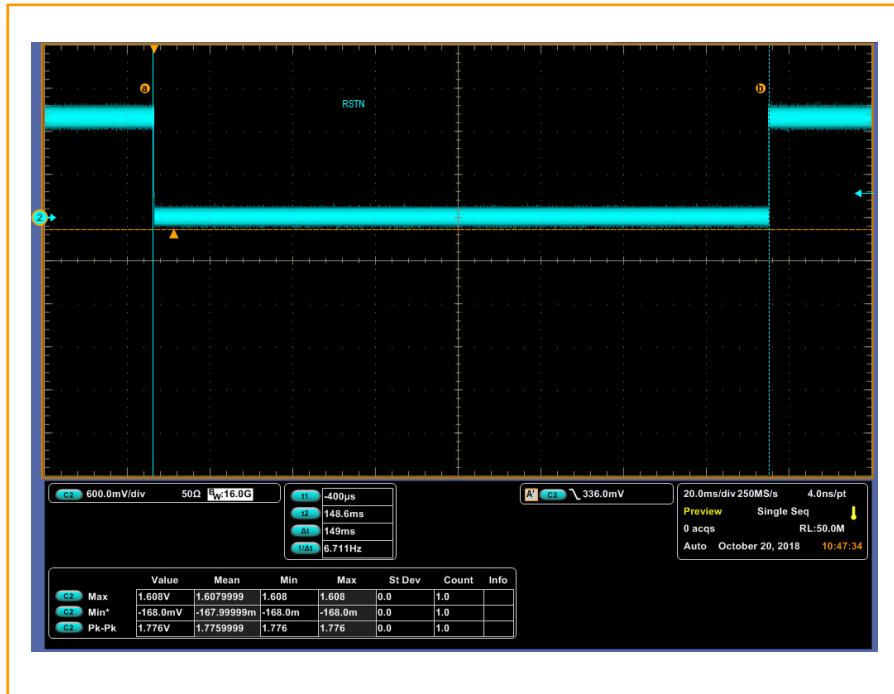


Parameter	Time	Spec	Result	Remark
CKE Falling Edge To Reset Rising Edge	> 10ns	Min:10ns	PASS	CKE is pulled “Low” anytime before RESET# being de-asserted (min. time 10 ns).

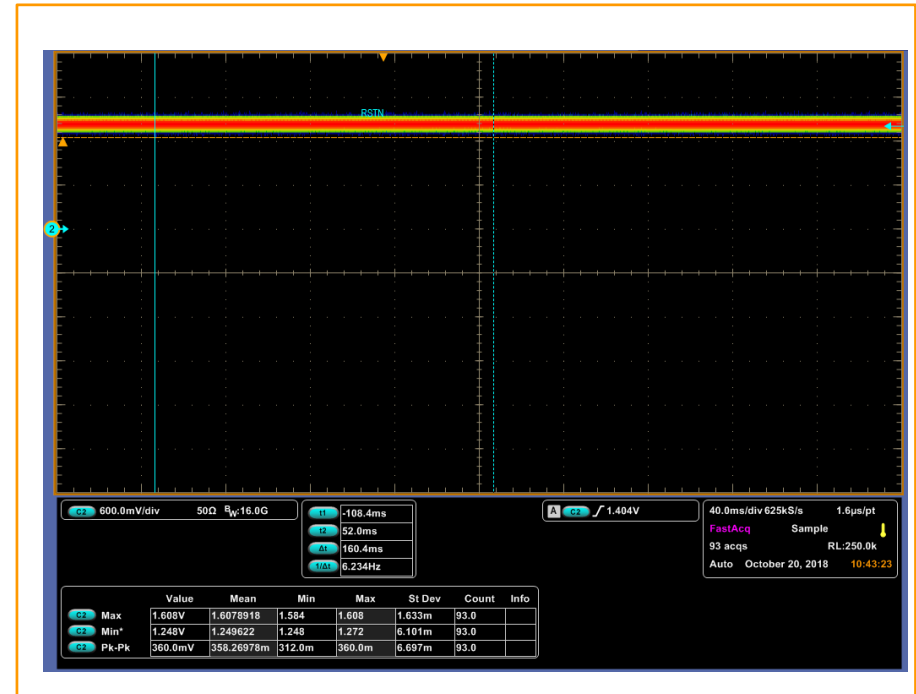


# Reset Initialization Sequence Check Result

## Reset Low Level Voltage



## Reset High Level Voltage



Parameter	Voltage	Spec	Result	Remark
Reset Low Level Voltage	80mV	Max:300mV	PASS	Reset Low Level Voltage must be within 300mV.
Reset High Level Voltage	1.608V	Min:1.2V	PASS	Reset High Level Voltage must be above 1.2V.



# Average Periodic Refresh Interval Check Result

## □ SPEC

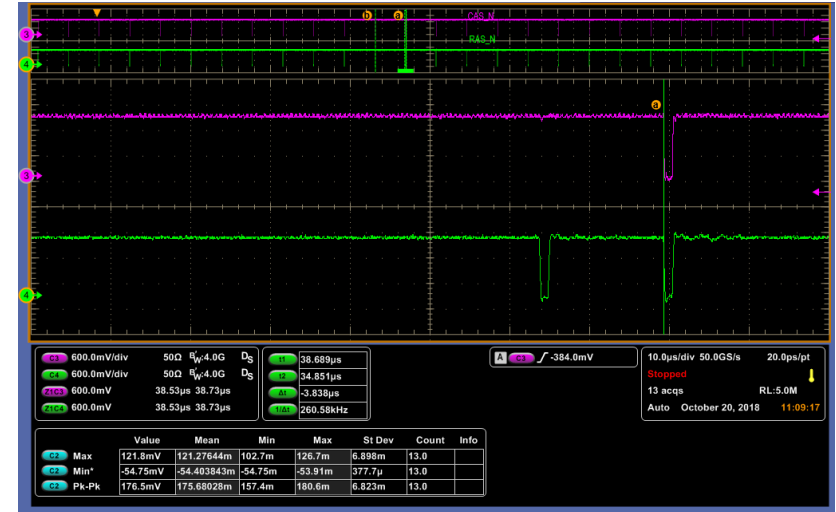
### 12.2 Refresh parameters by device density

Table 61 — Refresh parameters by device density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units	Notes
REF command to ACT or REF command time	tRFC		90	110	160	300	350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T <sub>CASE</sub> ≤ 85 °C	7.8	7.8	7.8	7.8	7.8	μs	
		85 °C < T <sub>CASE</sub> ≤ 95 °C	3.9	3.9	3.9	3.9	3.9	μs	1

NOTE 1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

## □ Average Periodic Refresh Interval



Parameter	Time	Spec	Result	Remark
tREFI	3.838us	Max:7.8us	PASS	



# Power Check Result

## ▣ AC Peak-Peak Noise Check Result

Parameter	Spec (PK-PK)	Value (PK-PK)	Unit	Result	Position	Test Point
VDD_IO	NA	71.2	mV	NA	DRAM	C282
VREFCA	30	17.8	mV	PASS	DRAM	C153
VREFDQ	30	20.8	mV	PASS	DRAM	C161

## ▣ VDD\_IO Supply Voltage

Parameter	Spec	Value	Unit	Result	Position	Test Point
VDD_IO	Min:1.283 Max:1.45	1.341	V	PASS	SOC	C3
		1.342	V	PASS	DDR	C157



# Signal Integrity Test Result (Clock)

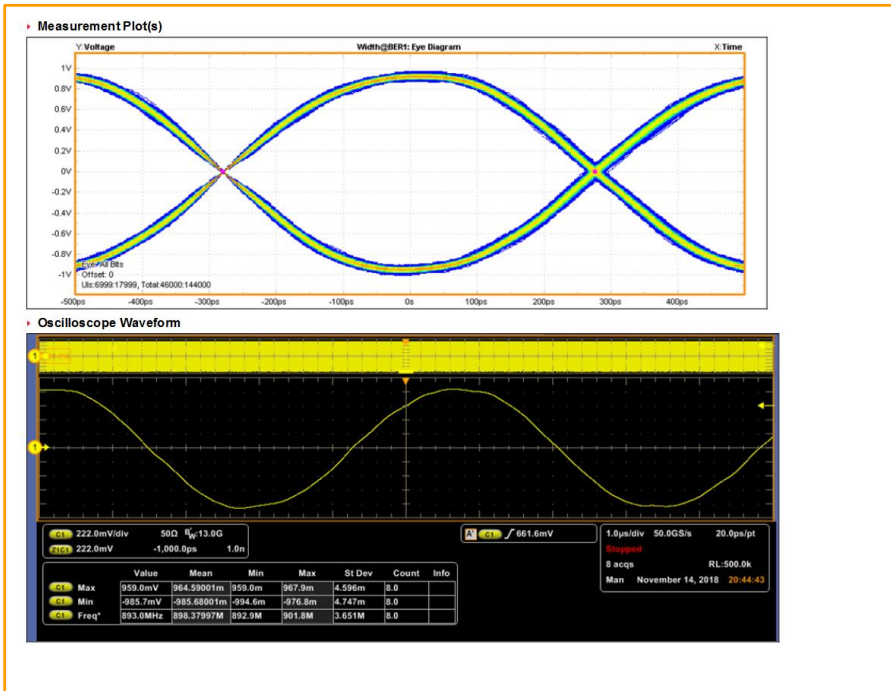
## ▣ Clock Signal Integrity Test Result

Parameter	Spec (Min)	Spec (Max)	Measurement data (Min)	Measurement data (Max)	Unit	Remark
Vix	-150	150	-110.96	25.51	mV	PASS
tCK(avg)	1.07	1.25	1.1108	1.1114	ps	PASS
tCH(avg)	470	530	498.44	501.98	mtCK(avg)	PASS
tCL(avg)	470	530	497.95	501.54	mtCK(avg)	PASS
tJIT(per)	-70	70	-17.288	18.08	ps	PASS
tJIT(cc)	-140	140	-30.073	28.823	ps	PASS
InputSlew-Diff-Rise	-	-	-	6.568	V/ns	-
InputSlew-Diff-Fall	-	-	-	-6.6804	V/ns	-

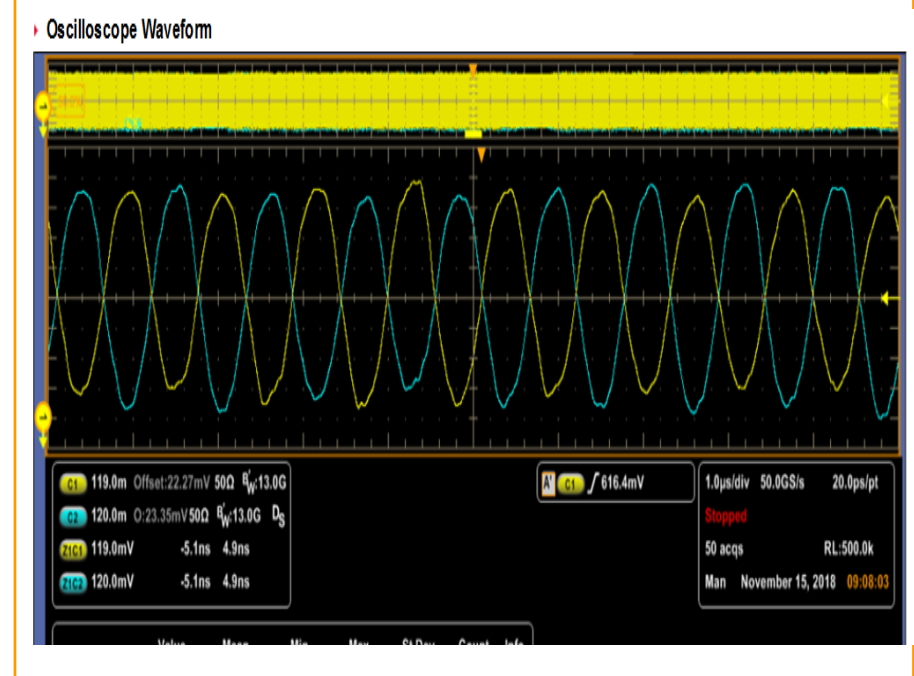


# Signal Integrity Test Result (Clock)

## CLK Different mode signal



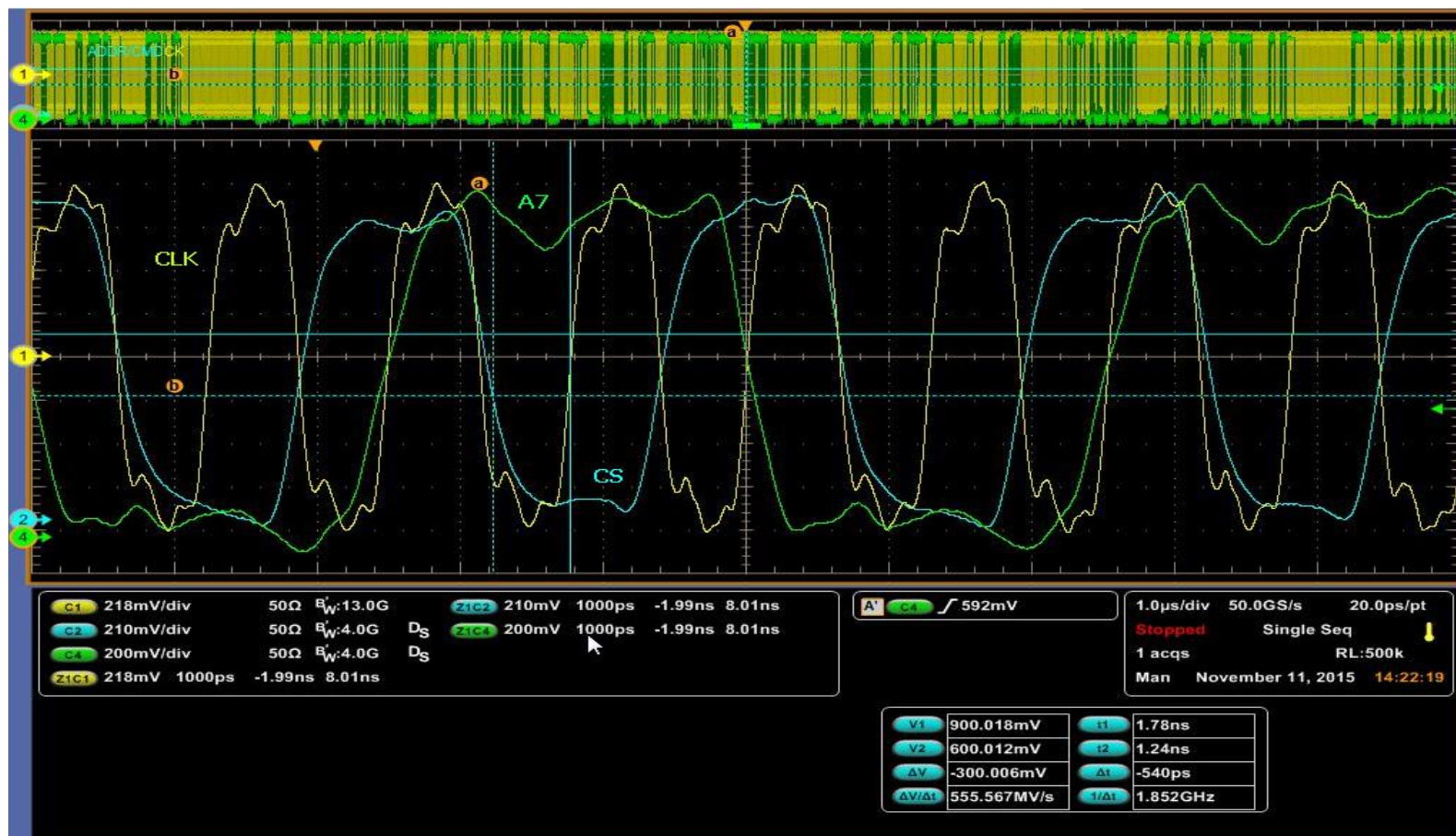
## CLK Single signal



# About 1T&2T signal test



1 T signal include: CS, ODT, CKE; other address and cmd signal are 2T signal. For 1T signal, you can test the signal using DDR3 test analysis module, but for 2T signal you can't test using the test module.





# Signal Integrity Test Result (CMD&ADDR)

## ■ SPEC

Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units
tIS(base) AC175	$V_{IH/L(ac)}$	200	125	65	45	-	-	ps
tIS(base) AC150	$V_{IH/L(ac)}$	350	275	190	170	-	-	ps
tIS(base) AC135	$V_{IH/L(ac)}$	-	-	-	-	65	60	ps
tIS(base) AC125	$V_{IH/L(ac)}$	-	-	-	-	150	135	ps
tIH(base) DC100	$V_{IH/L(dc)}$	275	200	140	120	100	95	ps

$\Delta tIS, \Delta tIH$ derating in [ps] AC/DC based Alternate AC125 Threshold $\rightarrow V_{IH(ac)}=V_{REF(dc)}+135mV, V_{IL(ac)}=V_{REF(dc)}-135mV$																	
		CK,CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$
CMD/ ADD Slew rate V/ns	2.0	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
	1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
	0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
	0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
	0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
	0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
	0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10





# Signal Integrity Test Result (CMD&ADDR)

## ▣Command Signal Integrity Test Result

CMD /ADD	Input SetupTime (tIS)@AC150 tIS(min)(ps)	Input Hold Time (tIH)@DC100 tIH(min) (ps)	Input Slew Rate (RisingTime) (V/ns)	Input Slew Rate (FallingTime) (V/ns)
SPEC	133	150		
CS_N	616.35	295.46	4.3141	-4.3011
ODT	588.71	390.77	3.9206	-3.4875



# Signal Integrity Test Result (CMD&ADDR)

▣ 1T\_CMD\_ADDR CS#



▣ 1T\_CMD\_ADDR ODT





# Signal Integrity Test Result (CMD&ADDR)

## Address Signal Integrity Test Result

CMD /ADD	Input SetupTime (tIS)@AC150 tIS(min)(ps)	Input Hold Time (tIH)@DC100 tIH(min) (ps)	Input Slew Rate (RisingTime) (V/ns)	Input Slew Rate (FallingTime) (V/ns)
SPEC	133	150		
A7	893.48	1033.5	3.2578	-3.6947
A13	958.5	1020.8	3.3281	-3.5203



# Signal Integrity Test Result (CMD&ADDR)

2T\_CMD\_ADDR A7



2T\_CMD\_ADDR A13



# Signal Integrity Test Result (DATA)



## ■ SPEC

Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units	Notes
tDS(base) AC175	$V_{IH/L(ac)}$ SR=1V/ns	75	25	-	-	-	-	ps	2
tDS(base) AC150	$V_{IH/L(ac)}$ SR=1V/ns	125	75	30	10	-	-	ps	2
tDS(base) AC135	$V_{IH/L(ac)}$ SR=1V/ns	165	115	60	40			ps	2, 3
tDS(base) AC135	$V_{IH/L(ac)}$ SR=2V/ns	-	-	-	-	68	53	ps	1
tDH(base) DC100	$V_{IH/L(dc)}$ SR=1V/ns	150	100	65	45	-	-	ps	2
tDH(base)DC100	$V_{IH/L(dc)}$ SR=2V/ns					70	55	ps	1

$\Delta tDS, \Delta tDH$ derating in [ps] AC/DC based Alternate AC135 Threshold -> $V_{IH(ac)}=V_{REF(dc)}+135mV$ , $V_{IL(ac)}=V_{REF(dc)}-135mV$ Alternate DC 100 Threshold -> $V_{IH(dc)}=V_{REF(dc)}+100mV$ , $V_{IL(dc)}=V_{REF(dc)}-100mV$																									
		DQS,DQS# Differential Slew Rate																							
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$
DQS Slew rate V/ns	4.0	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.0	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
	2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
	1.0	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-38	-76	-30	-60

# Signal Integrity Test Result (DATA)



## ▣ Data Signal Integrity Test Result

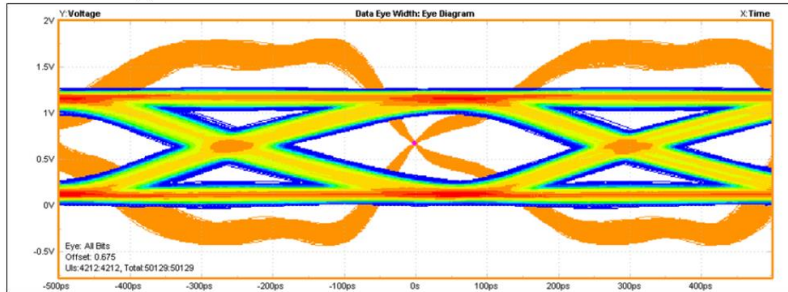
Parameter	Spec	Unit	DQ10	DQ12	Remarks
Input Slew Rate(Setup-time)	-	V/ns	2.6952	3.0897	-
Input Slew Rate(Hold-time)	-	V/ns	-3.079	-3.5422	-
Input Setup-Time(tDS)@AC135 [tDS(base)=68ps]	min:91	ps	101.07	98.945	PASS
Input Hold-Time(tDH)@DC100 [tDH(base)=70ps]	min:87	ps	174.77	208.58	PASS



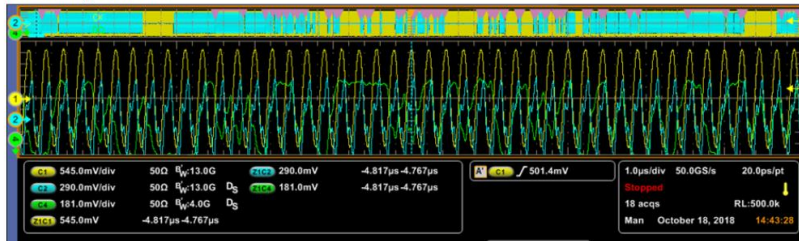
# Signal Integrity Test Result (DATA)

## DDR0-DQ10

### Measurement Plot(s)

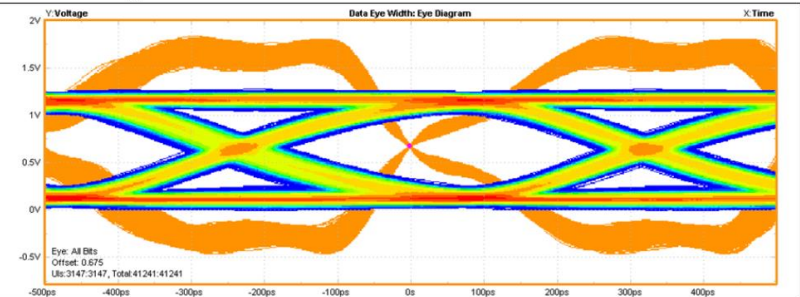


### Oscilloscope Waveform

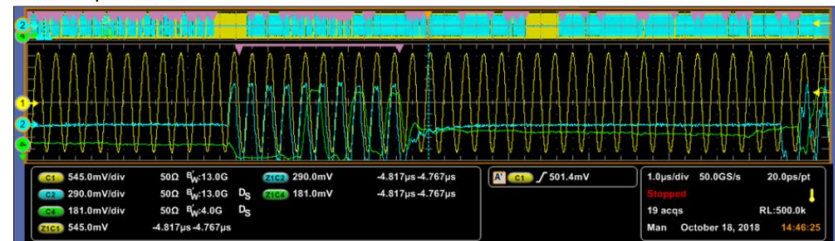


## DDR0-DQ12

### Measurement Plot(s)



### Oscilloscope Waveform





# Signal Integrity Test Result (DATA)

## ▣ tDQSH, tDQSL fail

### ▶ Pass/Fail Information

Measurement	tDQSH			
Source1	DQS(Ch2)			
	Value	High Limit	Low Limit	Pass Fail
Min	496.82mtCK(avg)		450.00mtCK(avg)	Pass
Max	579.24mtCK(avg)	550.00mtCK(avg)		Fail

### ▶ Pass/Fail Information

Measurement	tDQSL			
Source1	DQS(Ch2)			
	Value	High Limit	Low Limit	Pass Fail
Min	478.36mtCK(avg)		450.00mtCK(avg)	Pass
Max	551.28mtCK(avg)	550.00mtCK(avg)		Fail





Write window of prebit-deskew:

DQ	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72	76	80	84	88	92	96	100	104	108	112	116	120	124	RANGE	DQPH	DQ	WIN
0	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00250059	0x7	63	53
1	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00210057	0x7	60	55
2	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00240059	0x7	63	54
3	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00220055	0x7	60	52
4	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00220059	0x7	62	56
5	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x001e0053	0x7	57	54
6	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x0025005c	0x7	65	56
7	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00190051	0x7	53	57
8	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00200057	0x7	60	56
9	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00200057	0x7	60	56
10	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00220058	0x7	61	55
11	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x0024005b	0x7	64	56
12	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x0024005b	0x7	64	56
13	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x0026005a	0x7	64	53
14	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00200055	0x7	59	54
15	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00220059	0x7	62	56
16	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x001e0053	0x8	57	54
17	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00220054	0x8	59	51
18	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x001c0050	0x8	54	53
19	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00200057	0x8	60	56
20	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x001d0051	0x8	55	53
21	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00210058	0x8	61	56
22	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x001f0053	0x8	57	53
23	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00220055	0x8	60	52
24	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x0029005d	0x7	67	53
25	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x002b005c	0x7	68	50
26	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x002c005d	0x7	69	50
27	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x0029005d	0x7	67	53
28	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x002c0063	0x7	72	56
29	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x0028005d	0x7	67	54
30	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x00290061	0x7	69	57
31	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX																							XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX									0x002c0061	0x7	71	54

Sum WIN: 1734. Avg WIN: 54  
Min WIN: 50. DQ Index: 25 26  
Max WIN: 57. DQ Index: 7 30



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Read window of prebit-deskew:
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[illegible]



**Thank you**