Hi3518E Hardware Design

Checklist

Issue **00B02**

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About This Document

Purpose

This document describes the check items for Hi3518E solutions.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3518E	V100

Intended Audience

This document is intended for:

- Technical support engineers
- Hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B02 (2014-02-28)

This issue is the first draft release.

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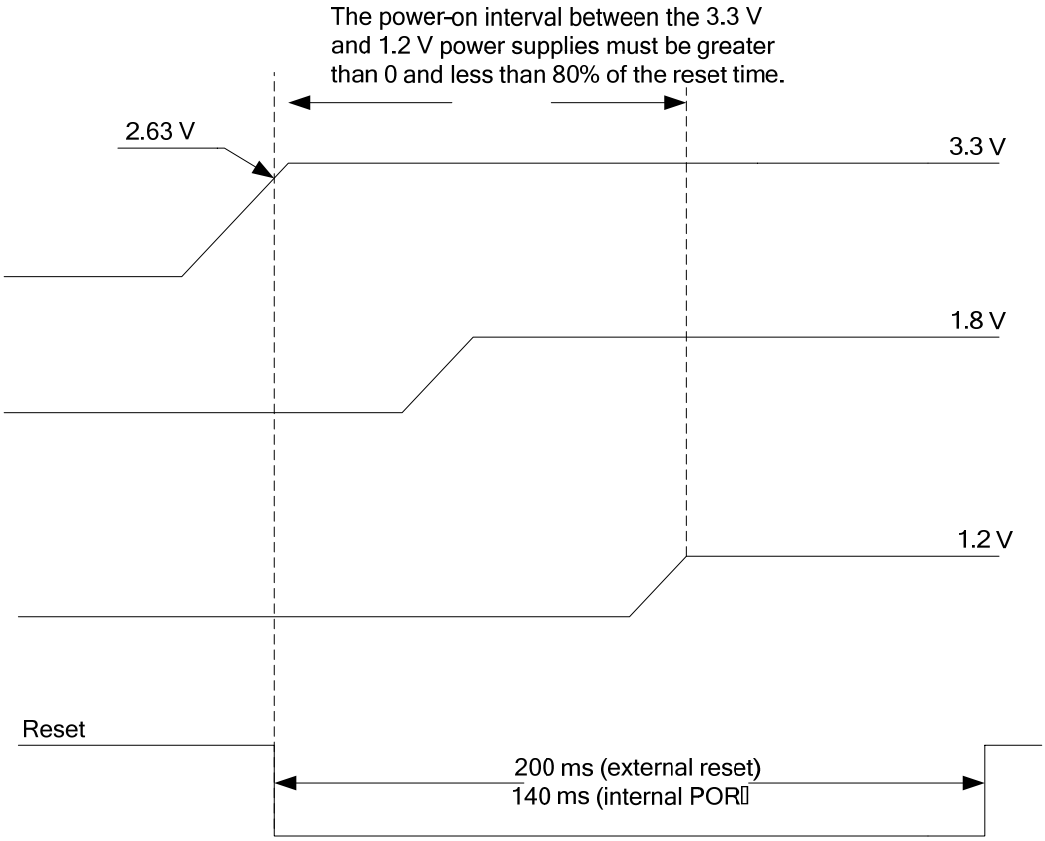
1 Checklist

1.1 Design Requirements on Power Supplies and GND

√	Items
	The core power pins DVDD12 are connected to the 1.2 V digital power. A 1 A power chip is recommended. Power noises are reduced to ensure that the power voltage deviation is within ±5% defined in electrical specifications.
	The high level is always greater than the low level during power-on. That is, power on the 3.3 V, 1.8 V, and 1.2 V power supplies in sequence. The power-on interval between the 3.3 V power and the 1.2 power cannot be longer than 80% of the reset time, see Figure 1-1.
	The phase-locked loop (PLL) power pins AVDD12_PLL and AVDD33_PLL are isolated from the power pins DVDD12 and DVDD33 of the Hi3518E. For details about circuits, see the schematic diagram of the Hi3518E demo board.
	Ensure that the output voltage of each power supply meets the requirements even when ripples and noises occur. For details about the power supply requirements of each module, see section 2.6 "Electrical Specifications" in the Hi3518E 720p IP Camera SoC *Data Sheet*.

Figure 1-1 Power-on sequence



1.2 Design Requirements on the Clock Circuit of the Master Chip

√	Items
	A 24 MHz external clock is required. The load capacitors and clocks must match, and the maximum frequency deviation of the 24 MHz system clock is 30 ppm. For details about the circuit component specifications, see the latest schematic diagram of the Hi3518E demo board.

1.3 Design Requirements on the Reset Circuit

√	Items
	The Hi3518E is reset at low level. The low pulse width of the input power-on reset (POR) signal is greater than 12 XIN crystal cycles.

√	Items
	The watchdog is open drain (OD) output. When the watchdog is used, pull-up resistors are required. The 1−4.7 kΩ pull-up resistors are recommended.
	The chip reset mode is selected by configuring the POR_SEL pin. During power-on, if POR_SEL is **0**, the internal POR circuit is enabled to reset the entire chip. If POR_SEL is **1**, the internal POR circuit is disabled. In this case, chip reset depends on the status of the RSTN pin.
	If the embedded POR is selected to reset the chip, the reset signal from the SYS_RSTN_OUT pin cannot be used to reset the peripherals such as the SPI flash that require the reset duration (Treset) be longer than 21.3 μs.
	When internal reset is selected, the RSTN and WDG_RSTN pins are floated. Peripherals need to be reset before the Hi3518E is reset or peripherals and the Hi3518E are reset at the same time.

1.4 Design Requirements on the Internal RTC

√	Items
	The timing accuracy of the embedded real-time clock (RTC) is affected by the manufacturing accuracy and temperature offset of the external crystal oscillator. For details about correction schemes, see the *RTC Correction Scheme Application Notes*. If high timing accuracy is required, you are advised to select the external RTC with an embedded crystal oscillator or a crystal oscillator with the temperature compensation function.

1.5 Design Requirements on the DDR Circuit

√	Items
	The VDD_DQ power for Hi3518E DDRs should be qualified to ensure the proper running of the Hi3518E. For details, see the *Hi3518E Hardware Design User Guide*.
	The reference power for Hi3518E DDRs is obtained by dividing the 1.8 V voltage over two 1% 1 kΩ (or smaller) voltage-divided resistors connected in serial to ensure optimum voltage.
	A 1% 240 Ω resistor is used as the ZQ calibration resistor for Hi3518E DDRs.

1.6 Design Requirements on the SPI Circuit

√	Items
	If an SPI flash is connected, the system can boot from the CS. You are advised to connect 1−4.7 kΩ pull-up resistors to the CS and HOLD signals and a 1−4.7 kΩ pull-down resistor to the WP signal.
	If the embedded POR is selected to reset the chip, the reset signal from the SYS_RSTN_OUT pin cannot be used to reset the SPI flash that requires the reset duration (T) be longer than 21.3 μs.
	The Hi3518E does not support the NAND flash.

1.7 Design Requirements on the I²C Circuit

√	Items
	Inter-integrated circuit (I^2C) signals SCL and SDA must be connected to external pull-up resistors, because the signal pins are OD outputs. The impedance depends on the bus load. The 1−4.7 kΩ pull-up resistors are recommended.
	The addresses for the components on the I^2C bus do not conflict with each other.

1.8 Design Requirements on the Video Circuit

√	Items
	A video input (VI) interface is supported. The VI interface supports the raw data input, a maximum of 12-bit width, and a maximum of 74.25 MHz frequency. For the 12-bit sensor, the raw data pins are connected to D0−D11 pins of the VI interface in sequence. For the 10-bit sensor, the raw data pins are connected to any of 10-bit pins of the VI interface in sequence. The pins D2 to D11 are recommended. You are advised to connect any unused pin to a 4.7 kΩ resistor and then to GND. Ensure that the traces of VI data signals have the same length, and signal current return paths are provided during PCB routing. For details, see the description of PCB design in the *Hi3518E Hardware Design User Guide*.

√	Items
	A video output (VO) interface is supported. If the VOU interface acts as the BT.1120 output, the bit width is 16 bits, and the maximum interface frequency is 74.25 MHz. The VOU interface does not provide external row synchronization and field synchronization signals and supports only internal synchronization. The VOU interface signal is multiplexed with the Ethernet (ETH) interface signal. If the ETH interface is used, the VOU interface is unavailable. For a BT.1120 signal, the upper eight bits are the Y (luminance) signal, and the lower eight bits are the C (chrominance) signal. Ensure that the connection is correct.

1.9 Design requirements on the Audio Circuit

√	**Items**
	The Hi3518E provides an analog audio CODEC. AC_VREF must be connected to a 2.2 μF external capacitor and 470 kΩ resistor in parallel and then to GND.
	You are advised to connect an audio amplifier and filtering circuit to the audio output pins AC_OUTL and AC_OUTR. For details, see the schematic diagram of the Hi3518E peripheral board.

1.10 Design Requirements on the Circuit

√	**Items**
	It is recommended that a 1% 43.2 Ω resistor be connected to the USB_REXT pin close to the Hi3518E and then to GND.
	Never cross plane splits when routing USB differential traces. It is recommended that differential traces be surrounded with GND traces. The impedance of each USB differential trace must be 90 Ω±10%.

1.11 Design Requirements on the ETH Circuit

√	**Items**
	As the management data input/output (MDIO) signal is OD output, it is recommended that a 1−4.7 kΩ pull-up resistor be connected to the MDIO pin.

√	Items
	It is recommended that a 22 Ω or 33 Ω resistor be connected to the MDCK signal in series close to the Hi3518E to ensure the signal quality.
	The connection mode of the transformer center tap varies according to ETH PHY vendors. Connect the transformer center tap by following the application notes and reference design documents provides by ETH PHY vendors.
	In reduced media independent interface (RMII) mode, the Hi3518E reference clock can be set to input or output. For details about the circuit design and configurations, see the application notes and reference design provided by ETH PHY vendors.

1.12 Design Requirements on JTAG and System Control Circuits

√	Items
	The TDI, TDO, and TMS pins are connected to 1−4.7 kΩ pull-up resistors. The TCK pin is connected to a 1−4.7 kΩ pull-down resistor. The TRST pin is connected to a 10 kΩ pull-down resistor. In addition, a pull-up resistor is reserved for the TRST pin. If the JTAG pin is not used, multiplex it as a GPIO pin by changing the pull-up/pull-down status of the JTAG_EN pin.
	The TESTMODE pin is connected to a 10 kΩ pull-down resistor.

1.13 Design Requirements on the SD Card Circuit

√	Items
	Data and command signals are connected to pull-up resistors and then to DVDD33. The 1−4.7 kΩ resistors are recommended.
	The data or command signal is connected to a pull-up resistor and then to VCC_SDIO. The 4.7 pull-up kΩ resistor is recommended.
	SDIO_CDATA3 does not support card detection.
	The components that consume much power are not placed on the back side of the SD card during PCB layout. This prevents the SD card from being damaged by high temperature.
	The SDIO DETECT signal must be connected to the DETECT pin of the SD card, that is, the SDIO DETECT signal cannot be floated.

1.14 Design Requirements on the UART Circuit

√	Items
	The debugging serial port must be led out. UART 0 is used for debugging by default.

1.15 Design Requirements on Heat Dissipation

√	Items
	The product structure is considered during heat dissipation design. The size of the heat dissipation layer is as large as possible when the space is sufficient.

1.16 Design Requirements on Sensor Design

√	Items
	To ensure picture quality, you are advised to use a low dropout (LDO) regulator to supply power to the sensor. Pay attention to the analog power and PLL power of the sensor. Typically, the core units of the sensor require a large current. The efficiency and heat dissipation of the LDO regulator need to be considered.
	The analog part and digital part of the sensor are separated. To be specific, the analog GND and digital GND are separated and connected by using 0 Ω resistors in single-point mode. The analog power branch has an independent LDO regulator and does not share a power branch with the digital power. During design of PCB layout and stacked architecture, ensure that the digital part and analog part do not intersect, avoiding interference and coupling.
	Decoupling capacitors are connected close to the power pins of the sensor. Ensure that a decoupling capacitor is connected to each analog power pin, and at least a decoupling capacitor is connected to two other power pins.
	If the sensor board connects to the main board by using a connector, ensure that current return paths are provided for the data signals from the connector when specifying signals for connector pins. This avoids signal crosstalk. That is, each data signal trace or clock signal trace connects to an independent GND trace to form a current return path. Note that a clock signal trace is designed between two GND traces, and two data signal traces are designed between two GND traces. For details, see the Hi3518E schematic diagram.