HDMI Compliance Test Software: Measurement Report

Tektronix Enabling Innovation

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Source Tests Report

Configuration

Setup Configuration

Oscilloscope Info	DPO73304S - 10.8.5 Build 4
TDSHT3 Version	5.3.6 Build 54

Device Configuration

Device Details	HDMI Device
Clock Frequency(Mhz)	148.500
Resolution	1920x1080p 8 bit
Refresh Rate	60Hz

Compliance Summary

Total Tests Supported	9
Tests Completed	29
Pass	29
Fail	0

Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.037*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.03*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.04*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.04*Tbit	Pass
5	7-6 : Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0.001*TPixel	Pass
6	7-6 : Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0*TPixel	Pass
7	7-6 : Source Inter-Pair Skew	D2 - D0	Skew < 0.2*TPixel;	0*TPixel	Pass
8	7-4 : Source Rise Time	CK	75.00ps < TRISE;	140.43ps	Pass
9	7-4 : Source Rise Time	D0	75.00ps < TRISE;	94.804ps	Pass
10	7-4 : Source Rise Time	D1	75.00ps < TRISE;	104.84ps	Pass
11	7-4 : Source Rise Time	D2	75.00ps < TRISE;	101.95ps	Pass
12	7-4 : Source Fall Time	CK	75.00ps < TFALL;	145.58ps	Pass
13	7-4 : Source Fall Time	D0	75.00ps < TFALL;	101.76ps	Pass
14	7-4 : Source Fall Time	D1	75.00ps < TFALL;	101.31ps	Pass
15	7-4 : Source Fall Time	D2	75.00ps < TFALL;	98.506ps	Pass
16	7-8 : Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	50.79%	Pass
17	7-8 : Min Duty Cycle	CK	40.0% < Min Duty Cycle;	49.6%	Pass
18	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	CK+	2.700V < VL < 2.900V;	2.8546V	Pass
19	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D0+	2.700V < VL < 2.900V;	2.8403V	Pass
20	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	CK-	2.700V < VL < 2.900V;	2.8460V	Pass
21	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D0-	2.700V < VL < 2.900V;	2.8372V	Pass
22	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D1+	2.700V < VL < 2.900V;	2.8292V	Pass
23	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D2+	2.700V < VL < 2.900V;	2.8432V	Pass
24	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D1-	2.700V < VL < 2.900V;	2.8307V	Pass
25	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D2-	2.700V < VL < 2.900V;	2.8486V	Pass
26	7-7 : Source Intra-Pair Skew	CK	Skew < 0.15*Tbit;	0.05*Tbit	Pass
27	7-7 : Source Intra-Pair Skew	D0	Skew < 0.15*Tbit;	0.03*Tbit	Pass
28	7-7 : Source Intra-Pair Skew	D1	Skew < 0.15*Tbit;	0.042*Tbit	Pass
29	7-7 : Source Intra-Pair Skew	D2	Skew < 0.15*Tbit;	0.033*Tbit	Pass

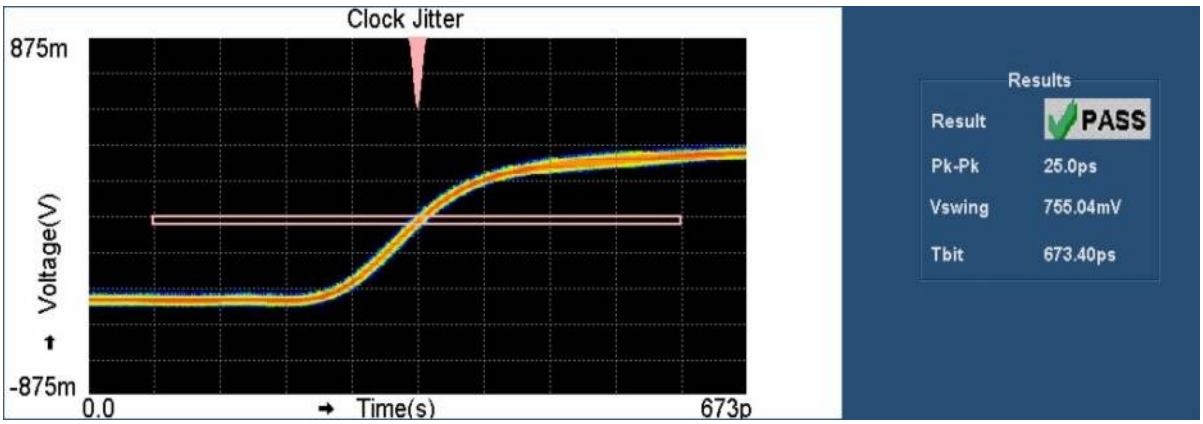
Detailed Results

7-9 : Source Clock Jitter : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Result
Clock Jitter < 0.25*Tbit;	0.037*Tbit	673.40ps	755.04mV	0.21*Tbit	50.000M	Pass

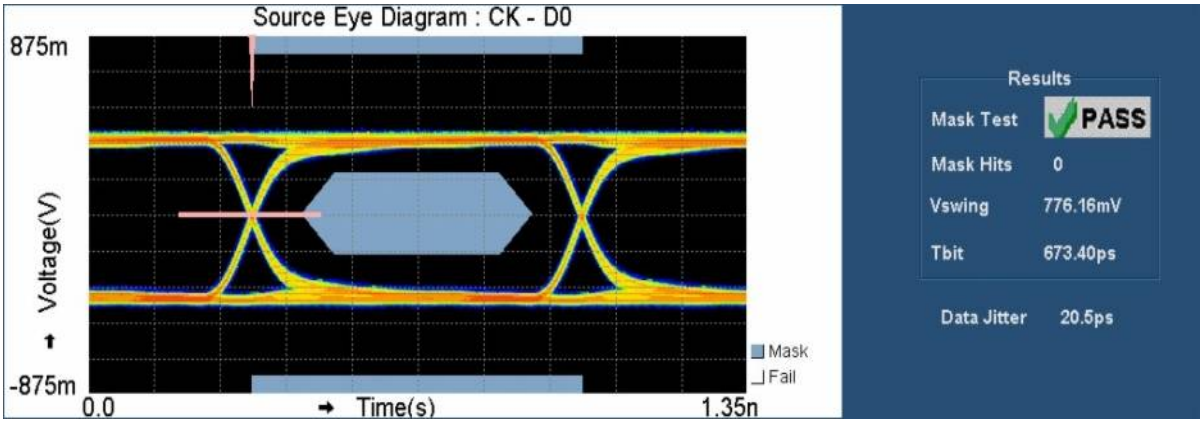
Waveform/Plot



- **7-10 : Source Eye Diagram : CK - D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.03*Tbit	673.40ps	776.16mV	0.27*Tbit	50.000M	0	Pass

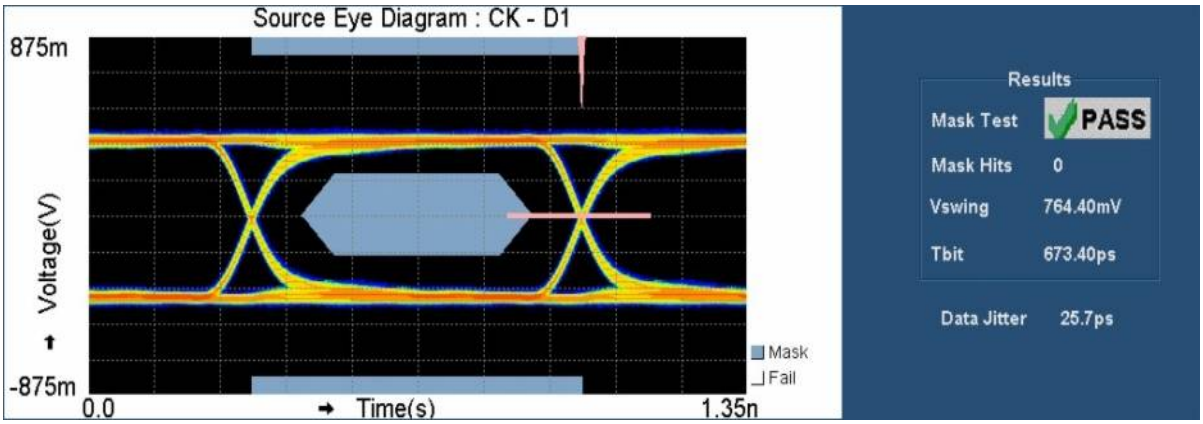
  - **Waveform/Plot**



- **7-10 : Source Eye Diagram : CK - D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.04*Tbit	673.40ps	764.40mV	0.26*Tbit	50.000M	0	Pass

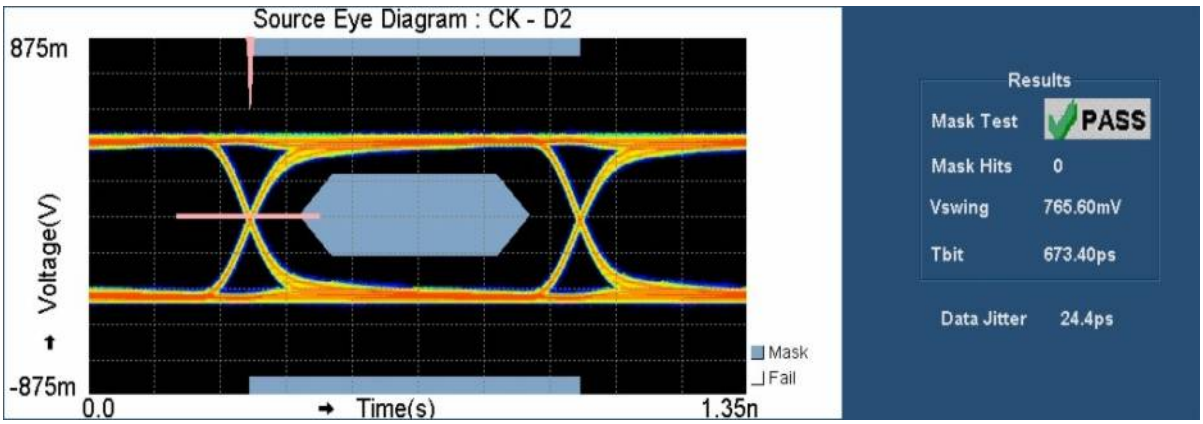
  - **Waveform/Plot**



- **7-10 : Source Eye Diagram : CK - D2**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.04*Tbit	673.40ps	765.60mV	263.8m*Tbit	50.000M	0	Pass

  - **Waveform/Plot**



- **7-6 : Source Inter-Pair Skew : D0 - D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs(D0 - D1)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.001*TPixel	673.40ps	= 776.16mV, Vs = 764.40mV	1.9697p	9.2857p	5.3476p	Pass

- **7-6 : Source Inter-Pair Skew : D1 - D2**
  - **Results**

Spec Range	Meas Value	Tbit	Vs(D1 - D2)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0*TPixel	673.40ps	= 764.40mV, Vs = 765.60mV	0.00	4.7205p	2.2802p	Pass

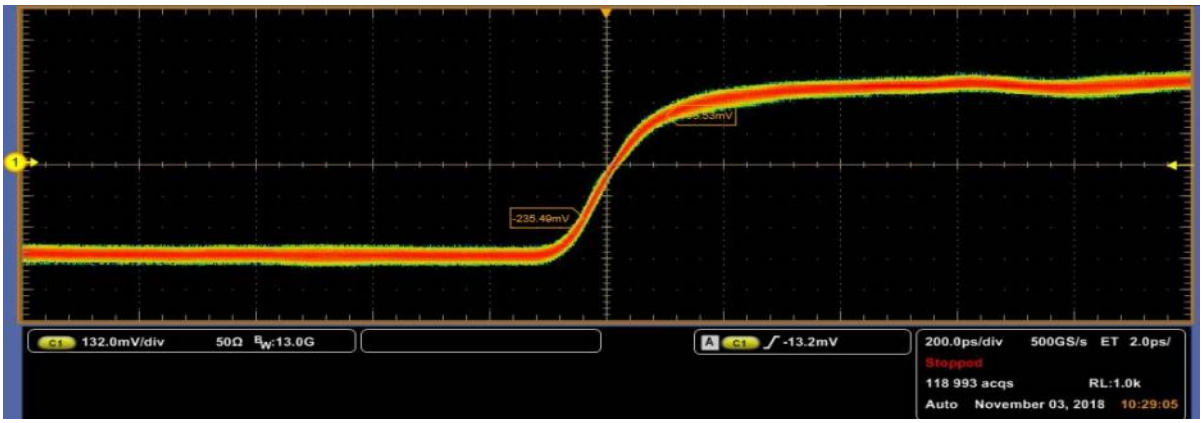
- **7-6 : Source Inter-Pair Skew : D2 - D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs(D2 - D0)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0*TPixel	673.40ps	= 765.60mV, Vs = 776.16mV	869.57f	5.4348p	3.0724p	Pass

- **7-4 : Source Rise Time : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	140.43ps	673.40ps	723.36mV	65.43ps	Pass

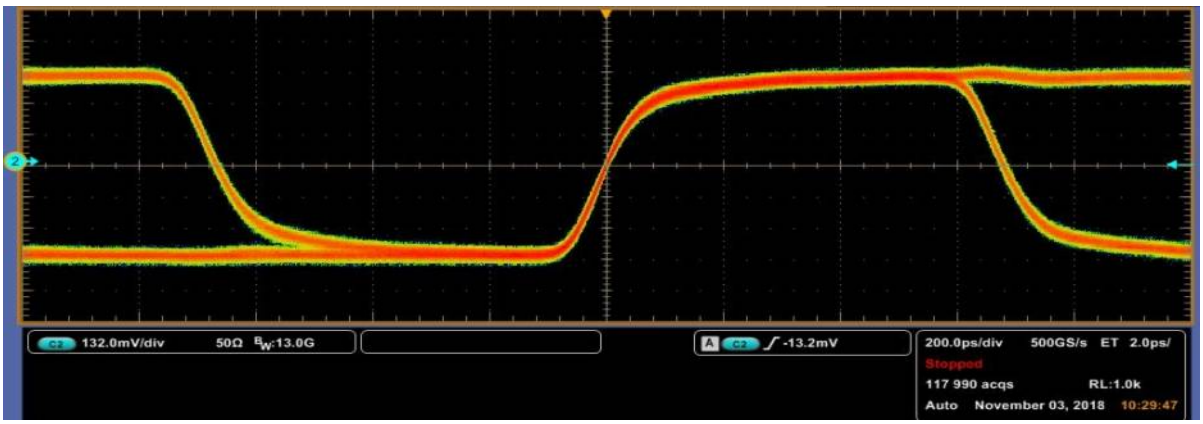
  - **Waveform/Plot**



- **7-4 : Source Rise Time : D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	94.804ps	673.40ps	749.76mV	19.80ps	Pass

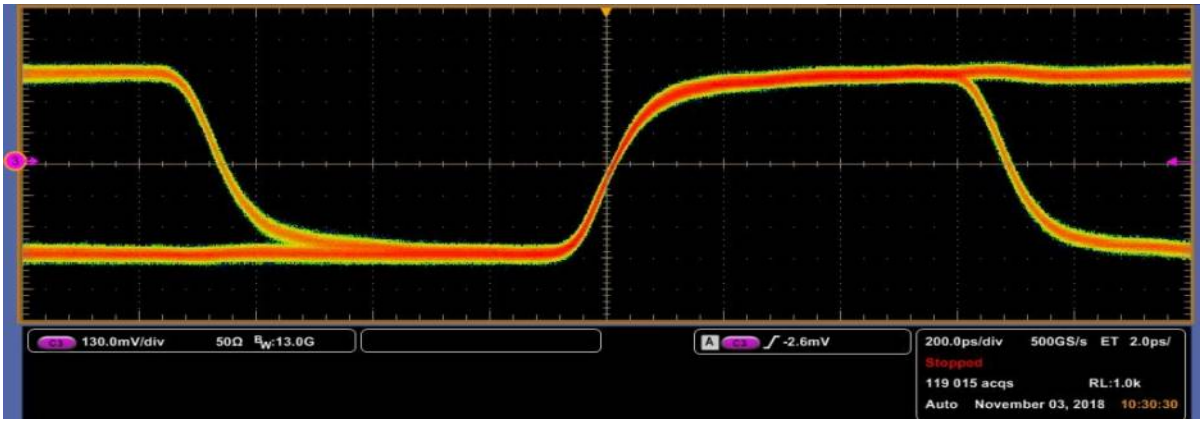
  - **Waveform/Plot**



- **7-4 : Source Rise Time : D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	104.84ps	673.40ps	748.80mV	29.84ps	Pass

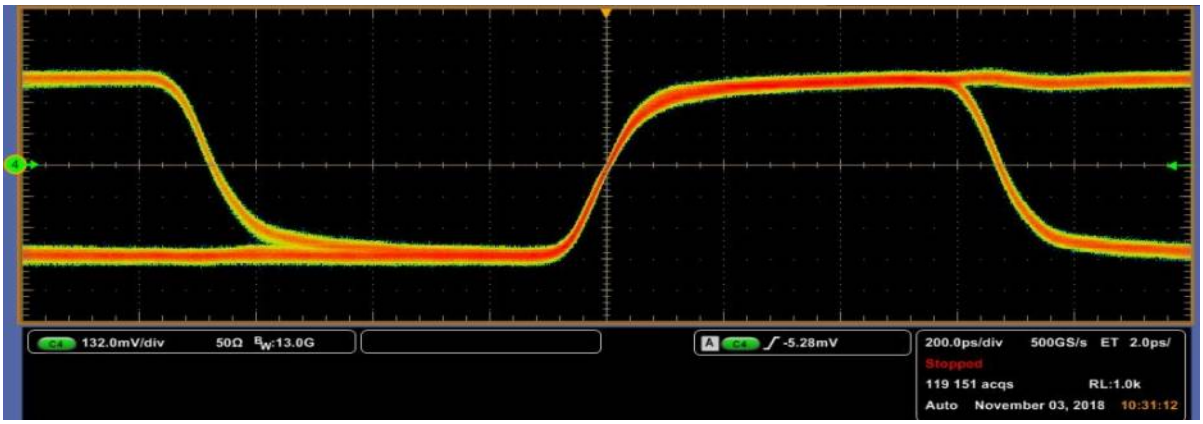
  - **Waveform/Plot**



- **7-4 : Source Rise Time : D2**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	101.95ps	673.40ps	744.48mV	26.95ps	Pass

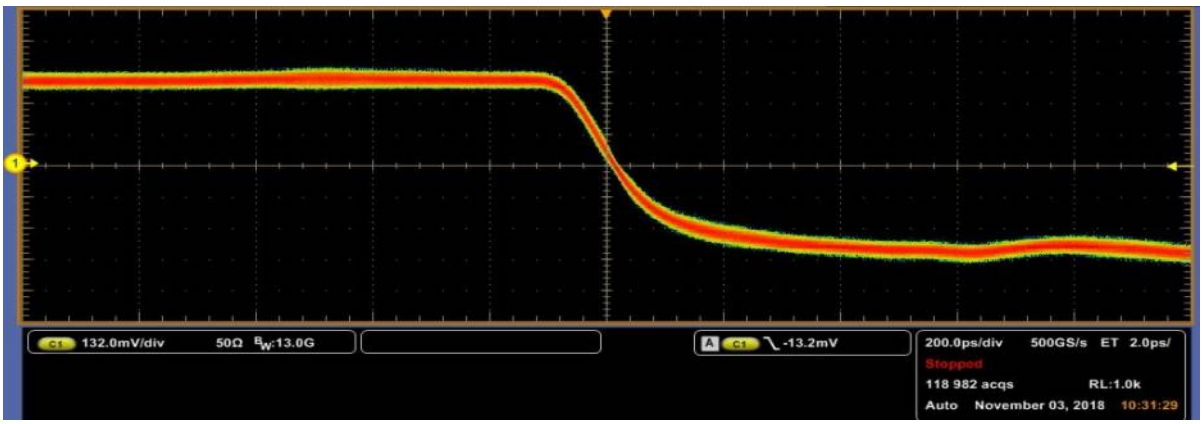
  - **Waveform/Plot**



- **7-4 : Source Fall Time : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	145.58ps	673.40ps	723.36mV	70.58ps	Pass

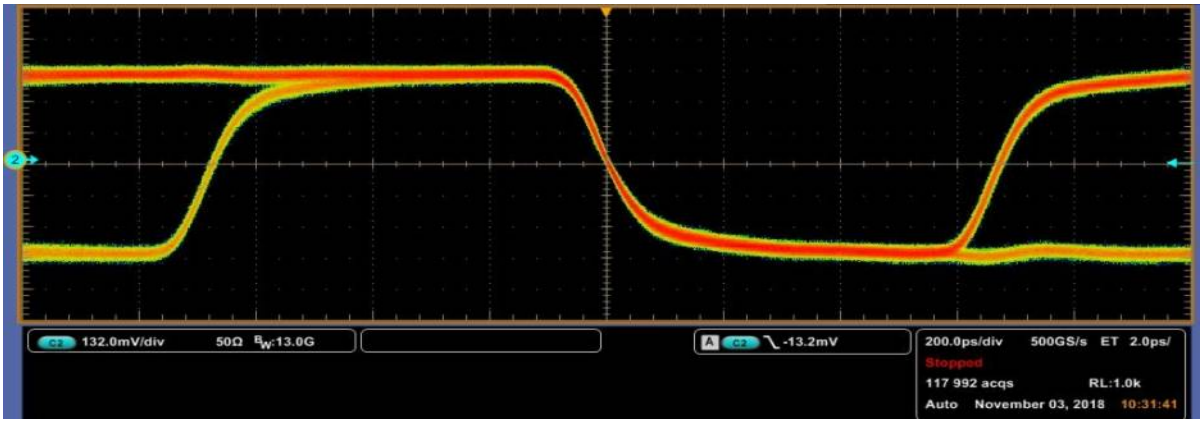
  - **Waveform/Plot**



- **7-4 : Source Fall Time : D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	101.76ps	673.40ps	749.76mV	26.76ps	Pass

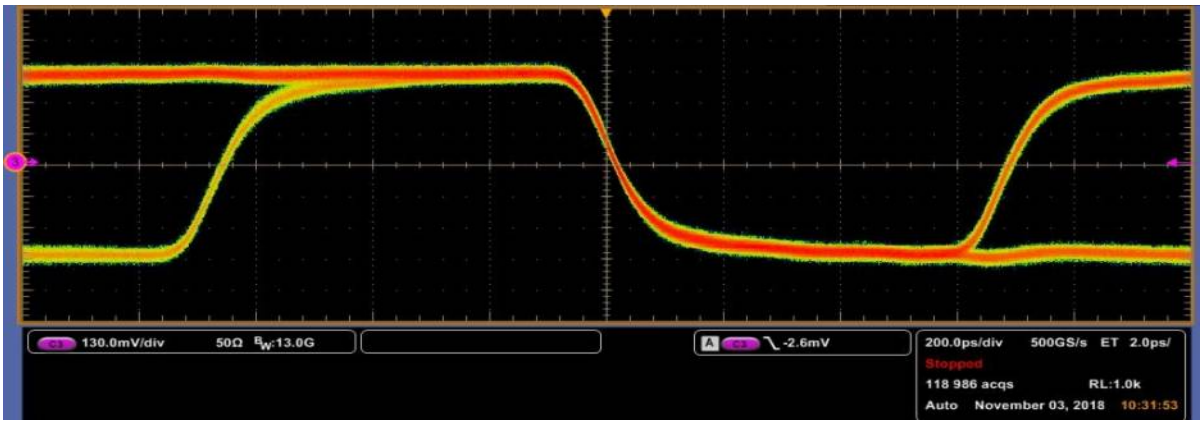
  - **Waveform/Plot**



- **7-4 : Source Fall Time : D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	101.31ps	673.40ps	748.80mV	26.31ps	Pass

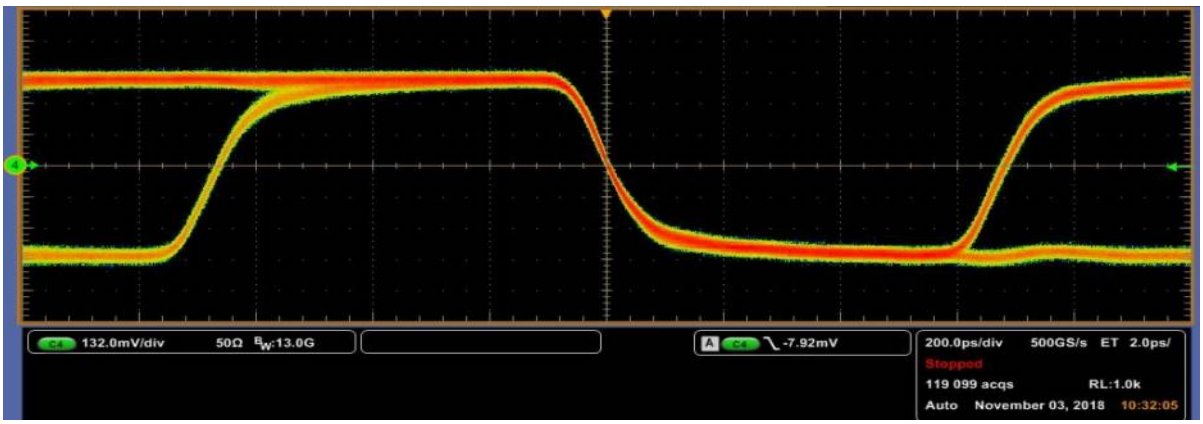
  - **Waveform/Plot**



- **7-4 : Source Fall Time : D2**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	98.506ps	673.40ps	744.48mV	23.51ps	Pass

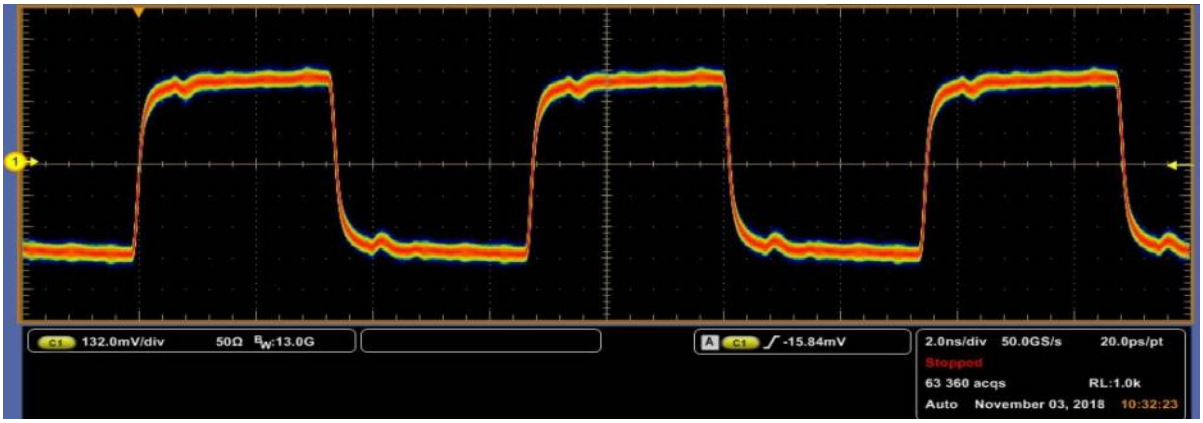
  - **Waveform/Plot**



- **7-8 : Max Duty Cycle : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Max Duty Cycle < 60.0%;	50.79%	673.40ps	9.21%	Pass

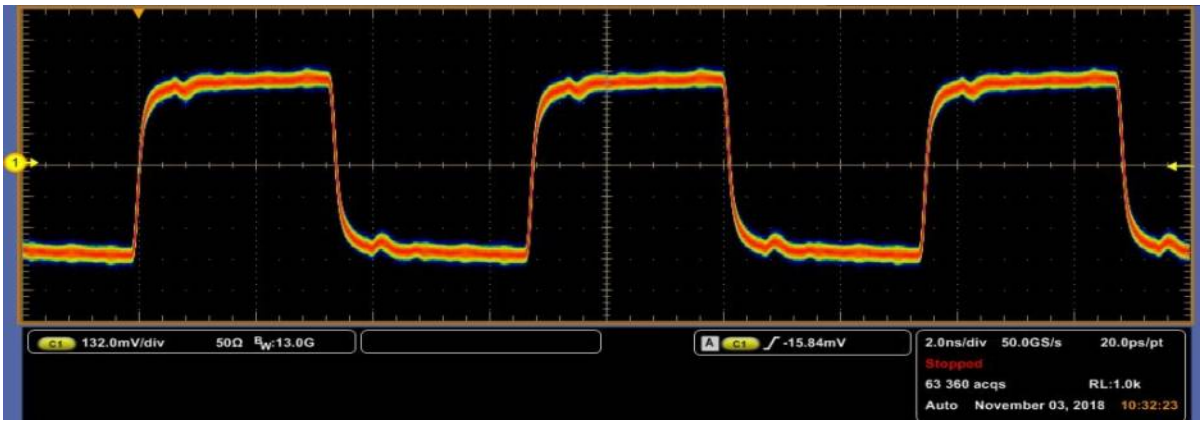
  - **Waveform/Plot**



- **7-8 : Min Duty Cycle : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
40.0% < Min Duty Cycle;	49.6%	673.40ps	9.6%	Pass

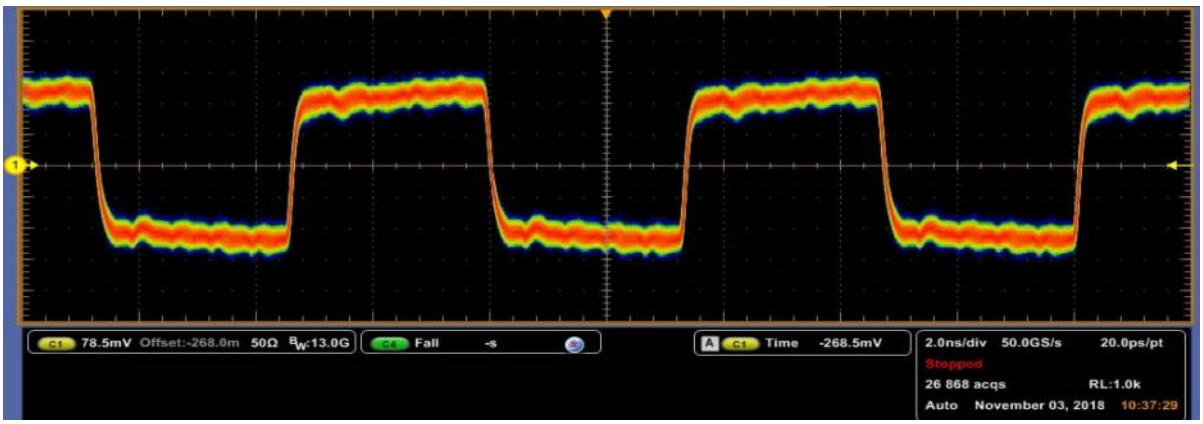
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : CK+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8546V	45.41mV	154.6mV	Pass

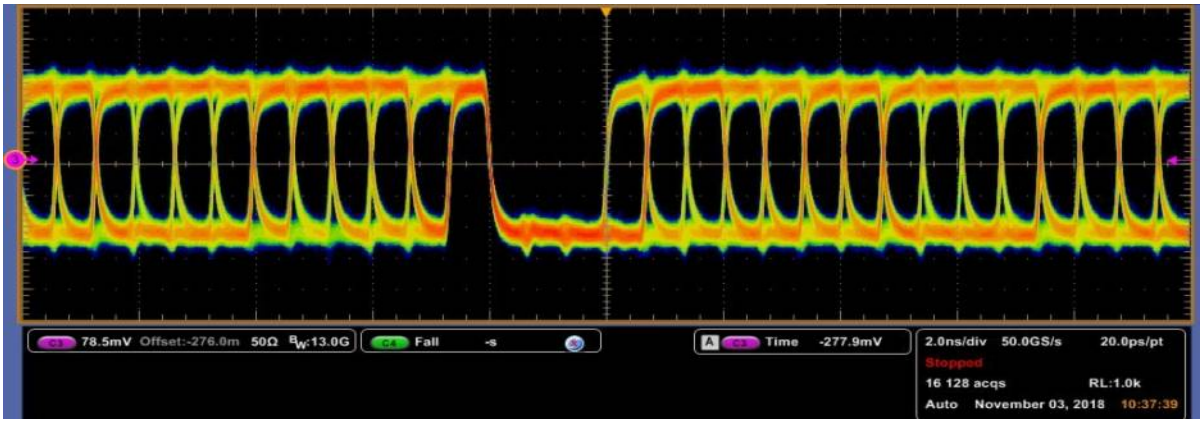
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D0+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8403V	59.69mV	140.3mV	Pass

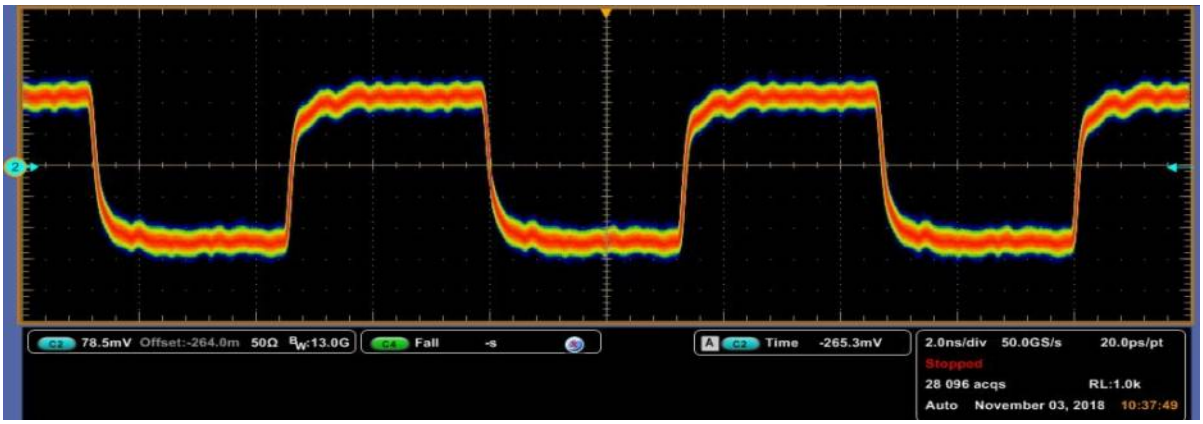
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : CK-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8460V	53.97mV	146.0mV	Pass

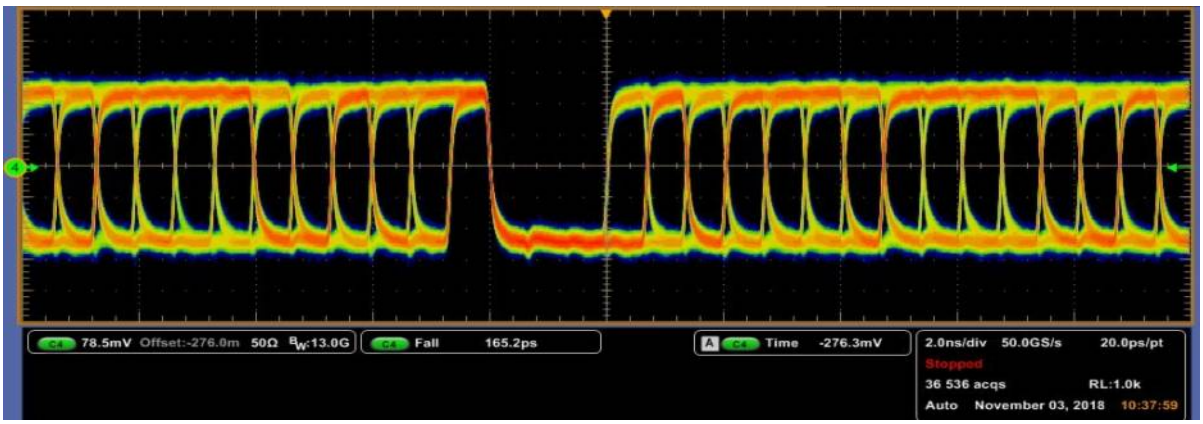
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D0-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8372V	62.83mV	137.2mV	Pass

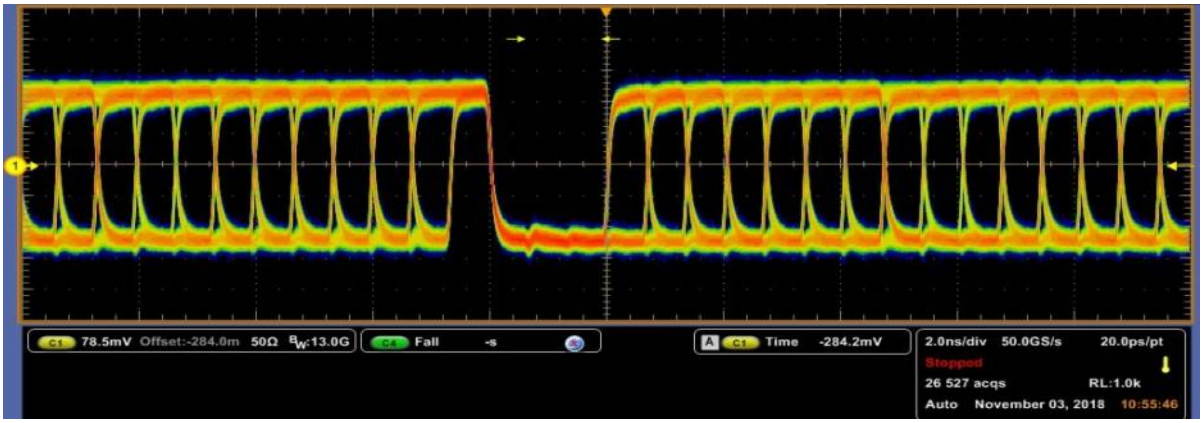
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D1+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8292V	70.83mV	129.2mV	Pass

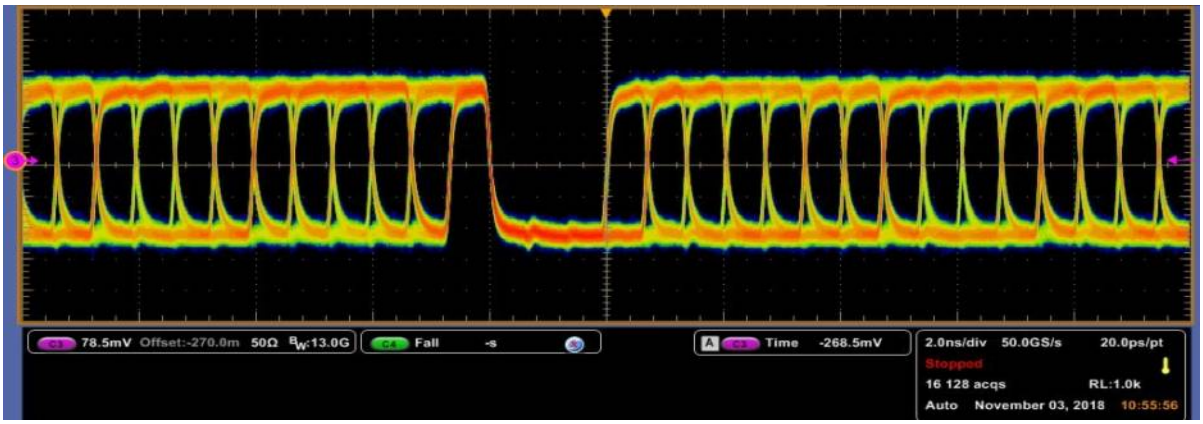
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D2+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8432V	56.83mV	143.2mV	Pass

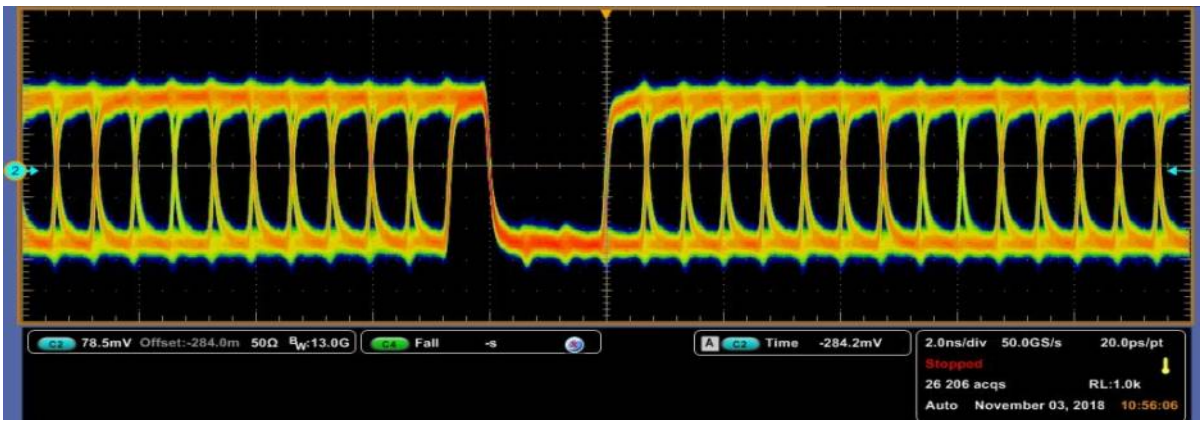
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D1-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8307V	69.26mV	130.7mV	Pass

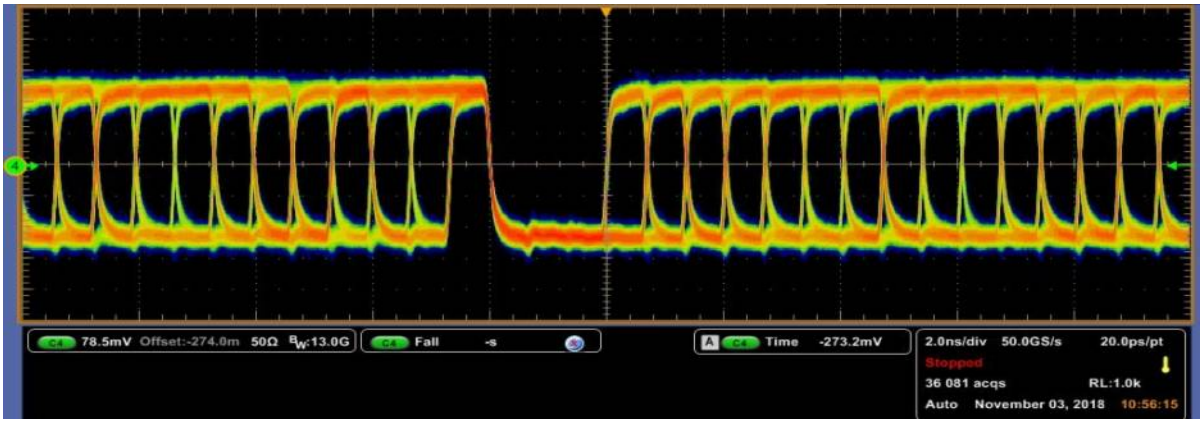
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D2-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8486V	51.41mV	148.6mV	Pass

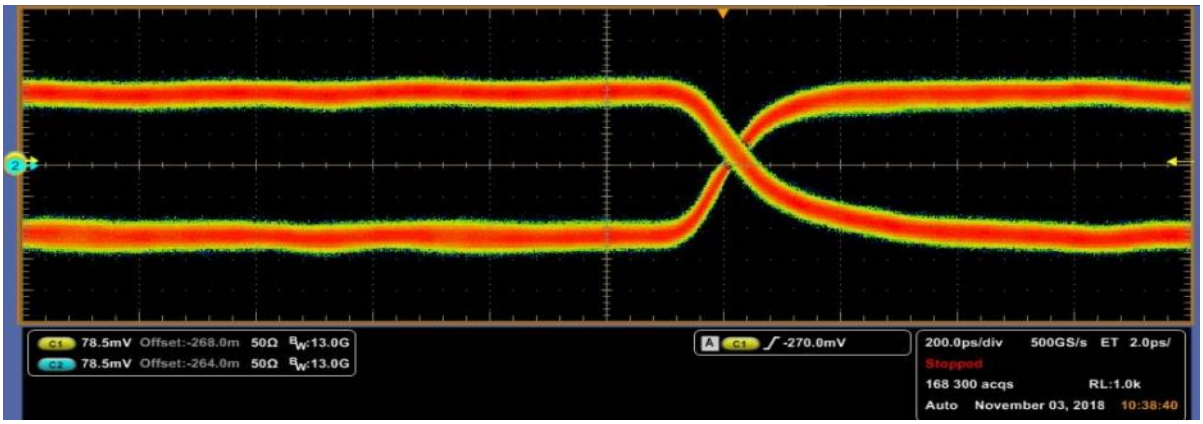
  - **Waveform/Plot**



- **7-7 : Source Intra-Pair Skew : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.05*Tbit	673.40ps	0.1*Tbit	Pass

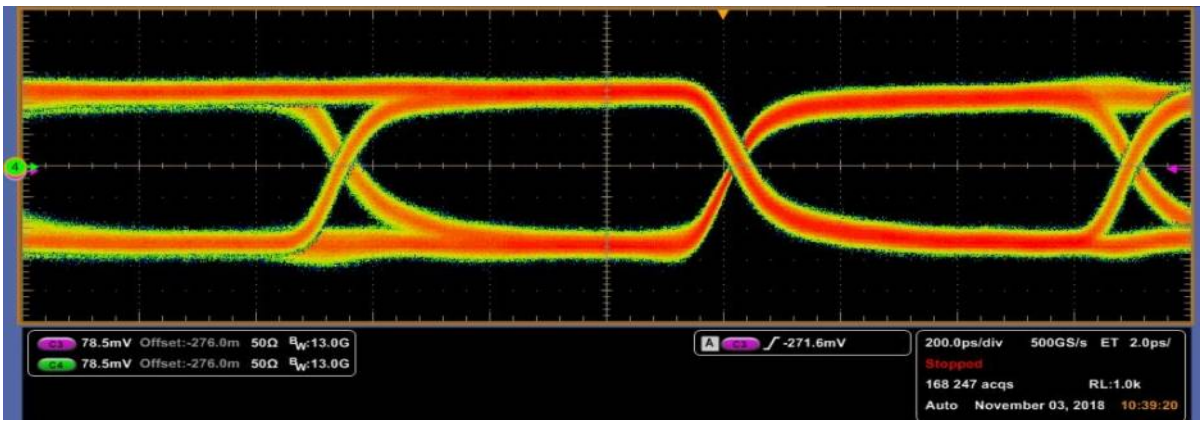
  - **Waveform/Plot**



- **7-7 : Source Intra-Pair Skew : D0**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.03*Tbit	673.40ps	0.12*Tbit	Pass

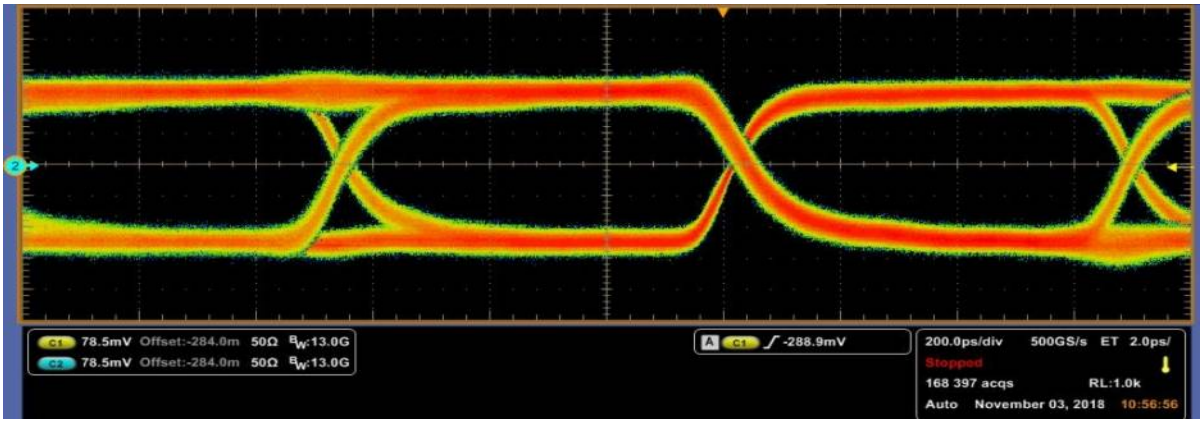
  - **Waveform/Plot**



- **7-7 : Source Intra-Pair Skew : D1**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.042*Tbit	673.40ps	0.11*Tbit	Pass

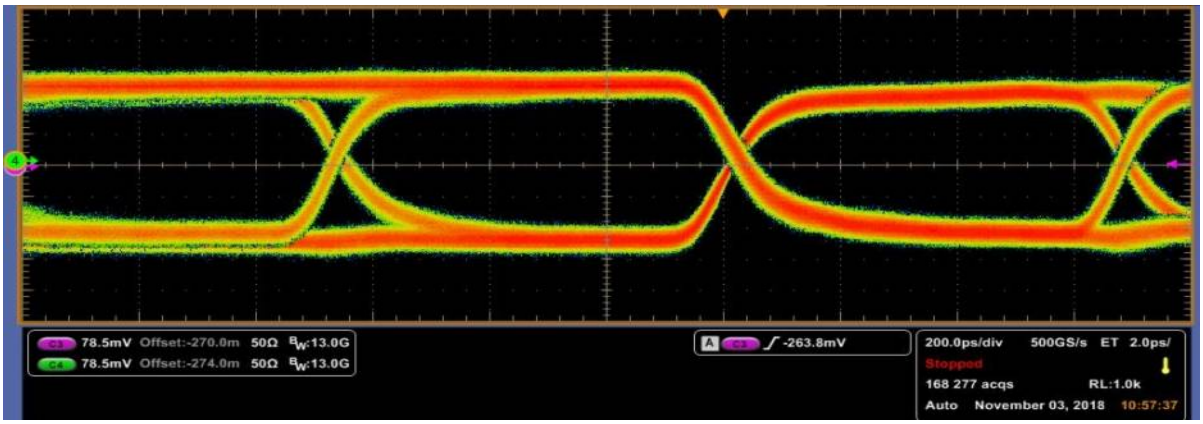
  - **Waveform/Plot**



- **7-7 : Source Intra-Pair Skew : D2**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.033*Tbit	673.40ps	0.12*Tbit	Pass

  - **Waveform/Plot**



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