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User Guide

Issue

Date

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About This Document

Purpose

This document describes the functional features, hardware features, and hardware configurations of the Hi3516C V500 demo board. It also describes how to debug the Hi3516C V500 demo board by using software.

Related Version

The following table lists the product version related to this document.

Product Name	Version dust
Hi3516C	V500 ,,,&

Intended Audience

This document isontended for:

- Technical support engineers
- Board hardware development engineers

Change History

Changes between document issues are cumulative. The latest document issue contains all changes made in previous issues.

Issue 00B02 (2019-01-15)

This issue is the second draft release, which incorporates the following changes:

Sections 3.2 and 3.3 are modified.

Issue 00B01 (2018-09-04)

This issue is first draft release.



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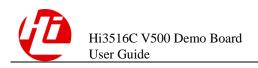
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1 Introduction

1.1 Overview

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The Hi3516C V500 demo board is a function demonstration board that is developed based on the HiSilicon media processor Hi3516C V500. The demo board provides superior multimedia processing functions, various peripheral interfaces, and hardware reference designs based on the Hi3516C V500. You can complete hardware development by modifying only module circuits on the demo board.

1.2 Deliverables

The Hi3516C V500 demo board package provides the following items:

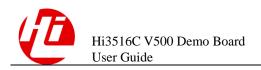
- One Hi3516C V500 demoboard: Hi3516C V500DMEB
- One sensor board
- One power adapted with the specifications of 100–240 V AC input, 50 Hz and 12 V DC output, 2 A
- 16-bit wideDDR3 SDRAM, 2 Gb, with the H5TQ2G63GFR model
- 16 MBSPI NOR flash with the MX25L12835 model

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1.3 Related Components

The following components are not included in the Hi3516C V500 demo board package; however, they are required for program debugging. Therefore, you must prepare them.

- Network cables
- Audio/Video receiving devices such as the TV set, stereo equipment, and camera
- Serial cables



2 Hardware

2.1 Architecture and Interfaces

Figure 2-1 shows the interfaces on the Hi3516C V500 demo bookd.

Figure 2-1 Interfaces on the Hi3516C V500 demo board

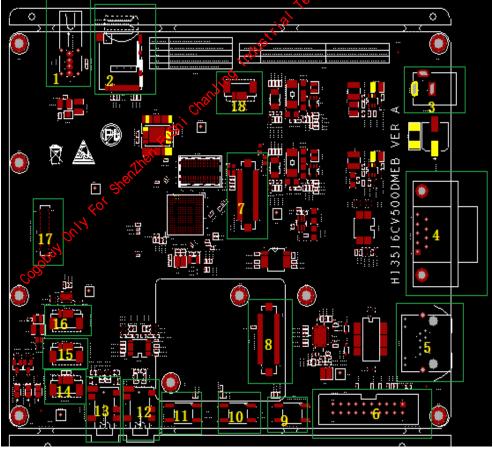


Table 2-1 describes the corresponding peripheral interfaces, keys, and switches in Figure 2-1.



Table 2-1 Peripheral interfaces on the Hi3516C V500 demo board

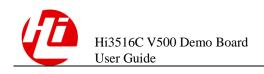
No.	Description
1	USB 2.0 port
2	Micro SD card connector
3	12 V power connector
4	UART0 connector
5	Megabit Ethernet port
6	JTAG connector
7	Liquid crystal display (LCD) connector
8	Wi-Fi connection
9	UPDATE_MODE key
10	LSADC_CH0 input key 2
11	LSADC_CH0 input key 1
12	Analog audio output connector
13	Analog audio MIC input interface of Hi3516C V500
14	2-wire UART1 port
15	DC_IRIS connector used to connect the IRIS interface and the DC_IRIS lens
16	P_IRIS connected used to connect the IRIS interface and the P_IRIS lens
17	Sensor consector used to connect Hi3516C V500 to the sensor board
18	Testing interface for the core power and DDRIO power

2.2 GPIO Distribution

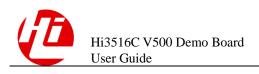
Table 2-2 describes the GPIO distribution of the Hi3516C V500 demo board.

Table 2-2 GPIO distribution of the Hi3516C V500 demo board

GPIO	Description	Board Processing Mode
GPIO0_0/UPDATE_MODE	UPDATE_MODE_N	A 10 kilohm pull-up resistor is connected. The update is triggered at a low level.
GPIO0_1/I2C3_SDA/LCD_D ATA20	I2C3_SDA	I2C3, externally connected to a 10 kilohm



GPIO	Description	Board Processing Mode
		pull-up resistor
GPIO0_2/I2C3_SCL/LCD_D ATA19	I2C3_SCL	-
GPIO0_3/IR_IN/LCD_DATA 18	P_IRIS_CONTROL1	P_IRIS_CONTROL1
GPIO0_4/LCD_DATA21	P_IRIS_CONTROL2	P_IRIS_CONTROL2
GPIO0_5/LCD_DATA22	P_IRIS_CONTROL3/LCD_ RST. LCD_RST is used for output by default, active low.	LCD_RST is soldered.
GPIO0_6/LCD_CLK/VOU_C LK	P_IRIS_CONTROL4	P_IRIS_CONTROL4
I2C7_SCL/GPIO10_6	HOST_WAKEUP_WL, indicating Wi-Fi wakeupol signal, high enable	-
I2C7_SDA/GPIO10_7	TP 100	Test point
LSADC_CH1/GPIO10_4	SGM8903 mute control output, active low	Connects to a 4.7 kilohm pull-down resistor.
UART1_CTSN/GPIO5_1/UA RT4_TXD	WIFE LED, indicating Wi-Fi status indicator control. The indicator is on when the output is high level and off when the output is low level.	-
UART1_RTSN/GPIGE_0/UA RT4_RXD specific control on the control of the control on t	UPDATE_LED, indicating update status indicator control. The indicator is on when the output is high level and off when the output is low level.	-



3 Operation Guide

3.1 Precautions

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The Hi3516C V500 demo board applies to the laboratory or engineering development environment. Take the following precautions before performing operations:



Never perform the hot-swap operation on the board in any case.

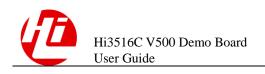
- Take antistatic measures before uppacking or installing the board to prevent the board hardware from being damager by the electrostatic discharge (ESD).
- Hold the board on the edge and do not touch the exposed metal on the board. Otherwise, the board components may be damaged by the ESD.
- Place the Hi3516 500 demo board on a dry workstation and keep it away from heat sources, electromagnetic interference sources, radiant sources, and electromagnetic susceptibility equipment (such as the medical equipment).
- Familiarize yourself with the layout of the Hi3516C V500 demo board. See Figure 2-1. Ensure that you can identify the components such as the switches, connectors, and indicators and know their positions.

3.2 Board Settings

The operating mode of the Hi3516C V500 is selected by using the keys and selecting the resistors to be welded on the Hi3516C V500 demo board. See Table 3-1.

Table 3-1 Board settings in various boot modes

Boot Mode	Value	Resistor Connection	Remarks
BOOT_SEL[1:0]	00	SW1.3 and SW1.2 are set to 0.	Boot from the SPI flash.

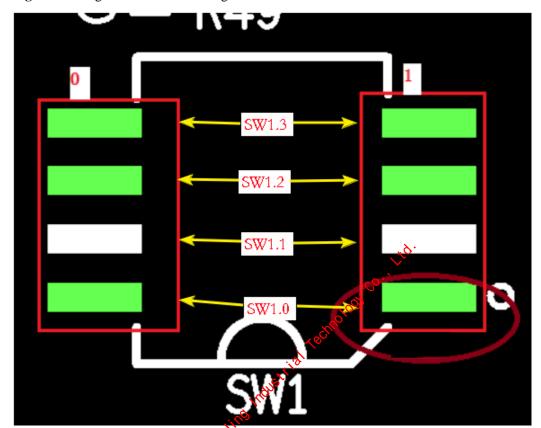


Boot Mode	Value	Resistor Connection	Remarks
	01	SW1.3 is set to 0, while SW1.2 is set to 1.	Boot from the eMMC.
	10	SW1.3 is set to 1, while SW1.2 is set to 0.	FastbootUpdate SPI flash (default)
	11	SW1.3 and SW1.2 are set to 1.	FastbootUpdate eMMC (default)
[SFC_DEVICE_MO DE: SFC_BOOT_MODE]	00	SW1.0 is set to 0, R188 is removed, and R367 is soldered.	SPI NOR flash. The default addressing mode is 3-byte mode.
	01	SW1.0 is set to 0, R367 is removed, and R188 is soldered.	SPI NOR flash. The default andressing mode is 4-byte mode.
	10	SW1.0 is set to 1, R188 is removed, and R367 is soldered.	SPI NAND flash. The default addressing mode is 1-wire boot mode.
· · ·	or rushi	WW1.0 is set to 1, R367 is removed, and R188 is soldered.	SPI NAND flash. The default addressing mode is 4-wire boot mode.
UPDATE_MODE_Next	0	S3 key is pressed down.	Enable update from SDIO0 or USB.
OPDATE_MODE; Not	1	S3 key is not pressed down.	Disable UPDATE_MODE (default).

3.3 DIP Switch Usage

As shown in Figure 3-1, the right side of the DIP switch is 1 while the left side is 0.

Figure 3-1 Diagram of DIP switch usage



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