Hi3516C V500 DDR3 Configuration Guide

Issue 00B01

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About This Document

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3516C	V500

Intended Audience

This document is intended for:

- Technical support engineers
- Software development engineers

Change History

Changes between document issues are cumulative. The latest document issue contains all the changes made in earlier issues.

Issue 00B01 (2019-01-15)

This issue is the first draft release.

Contents

1 DDR3 Driver Configuration

1.1 CLK/AC Driver Configuration

- Register address
  DDR PHY: 0x1206d018
- Register description
  - Bit[25:23]: CK driver
  - Bit[22:20]: 2T driver
  - Bit[19:17]: 1T driver
- Drive strength
  - 000: disabled
  - 001: 240 ohms
  - 010: 120 ohms
  - 011: 80 ohms
  - 100: 60 ohms
  - 101: 48 ohms
  - 110: 40 ohms
  - 111: 34 ohms

NOTE
The 1T signals refer to CKE, CSN, ODT, and RESET signals, while the 2T signals refer to the AC signals except 1T signals.

1.2 DQS/DQ Driver Configuration in the Write Direction

- Register address
  DDR PHY: 0x1206d204 (bytes 0–1)
- Register description
  - Bit[16:14]: DQS driver in the write direction
  - Bit[13:11]: DQ driver in the write direction
- Drive strength
  - 000: disabled

- 001: 240 ohms
- 010: 120 ohms
- 011: 80 ohms
- 100: 60 ohms
- 101: 48 ohms
- 110: 40 ohms
- 111: 34 ohms

1.3 DQS/DQ Driver Configuration in the Read Direction

- Register address
  DDR PHY: 0x1206c064
- Register description
  Bit[21] and bit[17]: DQS/DQ driver in the read direction
- Drive strength
  - 00: 40 ohms
  - 01: 34 ohms
  - 10: reserved
  - 11: reserved

2 DDR3 ODT Configuration

2.1 DQS/DQ ODT Configuration in the Write Direction

2.1.1 ODT Enable in the Write Direction

- Register address
  DDRC: 0x120680a0
- Register description
  - Bit[0] = 0: ODT disabled in the write direction
  - Bit[0] = 1: ODT enabled in the write direction

2.1.2 ODT in the Write Direction

- Register address
  DDR PHY: 0x1206c064
- Register description
  - Bit[25], bit[22], and bit[18]: DQS/DQ ODT configuration in the write direction
- ODT values in the write direction
  - 000: ODT disabled
  - 001: 60 ohms
  - 010: 120 ohms
  - 011: 40 ohms

NOTICE

The ODT configuration in the write direction takes effect for both DQS and DQ signals.

2.2 DQS/DQ ODT Configuration in the Read Direction

2.2.1 ODT Enable in the Read Direction

- Register address
  DDR PHY: 0x1206d248 (bytes 0–1)
- Register description
  - Bit[3] = 0: ODT enabled in the read direction
  - Bit[3] = 1: ODT disabled in the read direction

2.2.2 ODT Values in the Read Direction

- Register address
  DDR PHY: 0x1206d204 (bytes 0–1)
- Register description
  - Bit[31:29]: DQS ODT in the read direction
  - Bit[28:26]: DQ ODT in the read direction
- ODT values in the read direction
  - 000: disabled
  - 001: 120 ohms
  - 010: 60 ohms
  - 011: 40 ohms
  - 100: 30 ohms
  - 101: 24 ohms
  - 110: 20 ohms
  - 111: 17 ohms

3 DDR3 Capacity Configuration

3.1 U-Boot Table Overview

The Hi3516C V500 memory interface can connect to a DDR3 DRAM with a maximum data bit width of 16 bits in single-channel mode. The DDR configuration is implemented in the U-Boot table. Hi3516C V500 provides one DDR3 U-Boot table, corresponding to the DMEB design scheme.

DMEB U-Boot table: *Hi3516CV500-DMEB_4L-DDR3_1800M_256MB_16bit-A7_900M-SYSBUS_300M*

Table 3-1 lists the DDR specifications supported by the U-Boot tables.

Table 3-1 DDR specifications supported by the U-Boot tables

U-Boot Table	Total Capacity/Total Bit Width	Channel	DDR Type	DDR Rate (Mbit/s)	Rank Count	DDR Bit Width (Bit Width/PCS x Count)	Capacity/ PCS
DMEB U-Boot table	256 MB/16 bits or 512 MB/16 bits	Channel 0	DDR3	1800	1	16 bits x 1	2 Gbits or 4 Gbits

NOTE

The DMEB U-Boot table is compatible with the single-piece 4 Gbits or 2 Gbits DDR. You do not need to modify the configuration.

