Hi35xx Vxxx Audio Optimization Application Notes

Issue 00B02

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About This Document

Purpose

This document describes the Hi35xxVxxx audio optimization solutions.

NOTE

- This document takes Hi3516D V300 as an example. Unless otherwise specified, the contents of the Hi3516D V300 also apply to other chips.
- In this document, Hi35xxVxxx refers to Hi3516C V500, Hi3516D V300, Hi3516A V300, Hi3556 V200, and Hi3559 V200.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3516D	V300
Hi3516C	V500
Hi3559	V200
Hi3556	V200
Hi3516A	V300

Intended Audience

This document is intended for:

- Technical support engineers
- Board hardware development engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
DANGER	Indicates an imminently hazardous situation which, if not avoided, will result in death or serious injury.
WARNING	Indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.
CAUTION	Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	Indicates a potentially hazardous situation which, if not avoided, could result in equipment damage, data loss, performance deterioration, or unanticipated results. NOTICE is used to address practices not related to personal injury.
NOTE	Calls attention to important information, best practices and tips. NOTE is used to address information not related to personal injury, equipment damage, and environment deterioration.

Change History

Changes between document issues are cumulative. The latest document issue contains all changes made in previous issues.

Issue 00B02 (2019-01-07)

This issue is the second draft release, which incorporates the following changes:

The descriptions in the Hi3516C V500, Hi3559 V200, and Hi3556 V200 are added.

Issue 00B01 (2018-11-30)

This issue is the first draft release.

Contents

Figures

Tables

1 Overview

The audio optimization solutions aim to provide excellent audio quality and reduce the background noise based on Hi3516D V300. This document describes the precautions to be taken related to audio software and hardware.

2 Solution

2.1 Circuit Solution

2.1.1 MIC Input Circuit

Hi3516D V300 provides a set of dual-channel audio input (AI) interfaces (AC_INL, AC_INR), and the MIC_BIAS pin. AC_INL/R can be multiplexed as the differential input interface AC_IN_P/N.

Figure 2-1 AI pins of Hi3516D V300

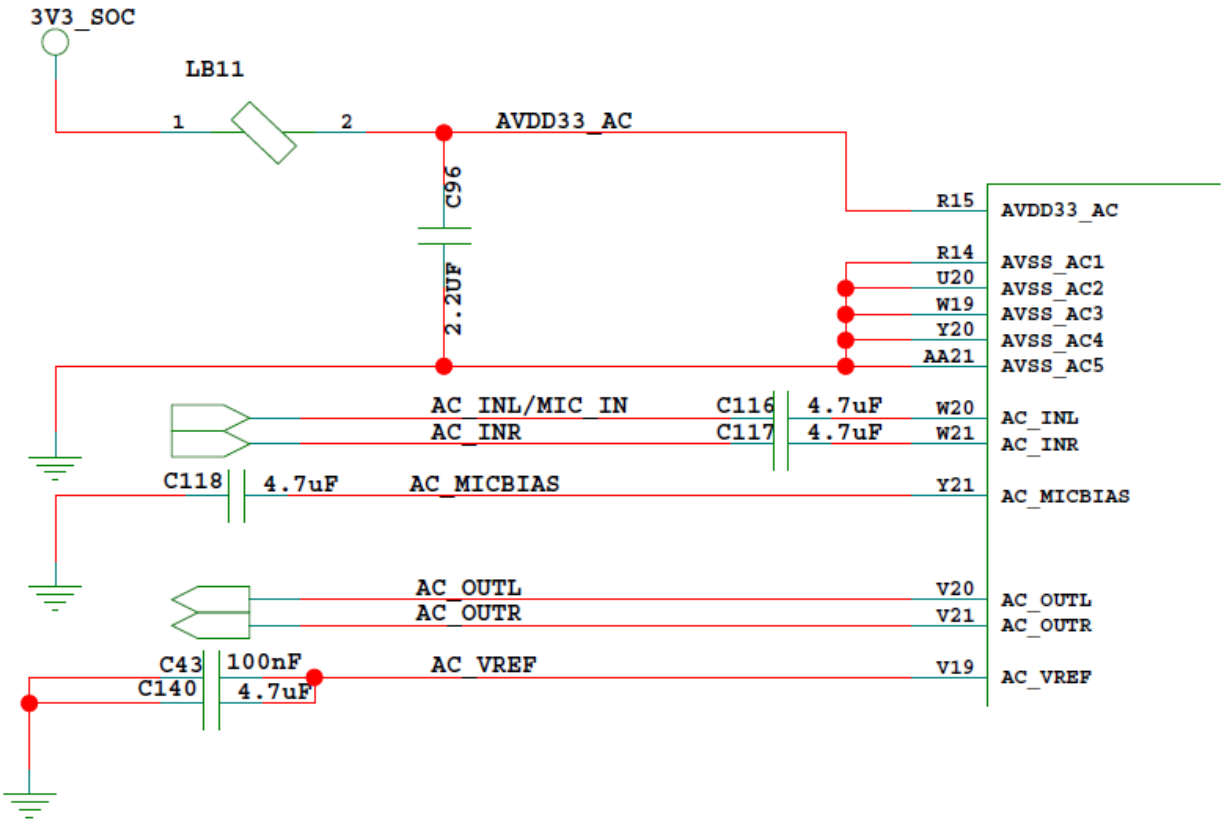


Figure 2-2 shows the recommended design of the differential MIC input circuit.

Figure 2-2 Differential MIC input circuit

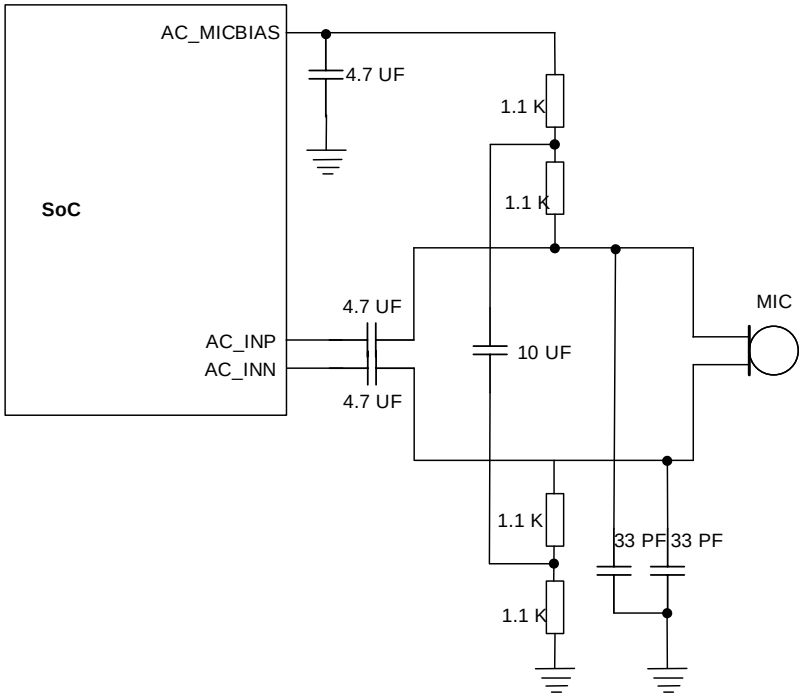
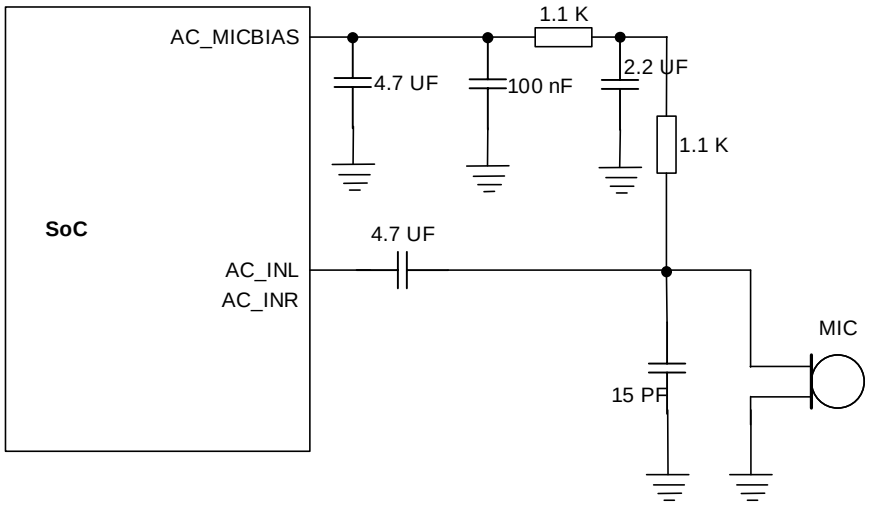


Figure 2-3 shows the recommended design of the single-ended MIC input circuit.

Figure 2-3 Single-ended MIC input circuit



The MIC input signals must be isolated before they pass the main chip. The 4.7 µF ceramic DC blocking capacitors (C116 and C117 in Figure 2-1) are recommended. On the printed circuit board (PCB), the DC blocking capacitors must be placed close to the pins of Hi3516D V300.

You need to pay attention to the configuration of the input gain. When the same AI volume is required, the gain for the differential MIC input needs to be half that for the single-ended MIC input.

NOTICE

The audio module is prone to the influence of the power supply noise and signal crosstalk. To effectively reduce the noise floor, perform the following operations based on the application scenario:

1. Scenario A (one MIC)

- You are advised to use the differential design for the MIC input circuit. The MIC can be a common single-ended MIC. In the scenarios where single-MIC differential input is used, you need to set the input mode to **ACODEC_MIXER_IN_D** by calling ACODEC_SET_MIXER_MIC and enable both audio-left and audio-right channels.
- In the case of single-ended input of one MIC, the input gain must be restricted and the register (ADUIO_ANA_CTRL_3) must be disabled for the disconnected MIC channel. The gain configuration is the same as that in scenario B.

2. Scenario B (dual MICs)

- When the MIC input circuit uses the single-ended design, you are advised to reduce the noise floor by limiting the input gain (bit[28:24] and bit[20:16] of the ADUIO_ANA_CTRL_3 register) or disabling the ADC gain boost control (bit[23] and bit[22] of the ADUIO_ANA_CTRL_1 register). You are advised to set the input gain to a value lower than 40 dB.
- If you have higher requirements for sound pickup or sound quality, you can use MICs with higher sensitivity or use an external codec.

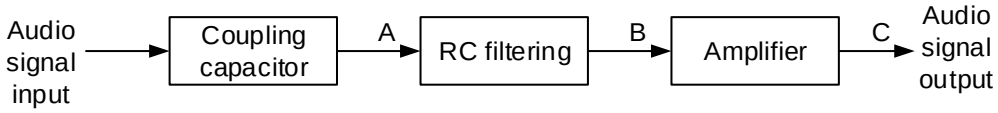
For details about the preceding registers and APIs, see section 11.2 "Audio Codec" in the *Hi35xx Vxxx xx Camera SoC Data Sheet*, and section 9.3 "API Reference" in the *HiMPP V4.0 Media Processing Software Development Reference*.

2.1.2 Analog Audio Output Circuit

Figure 2-4 shows the analog audio output (AO) processing of Hi3516D V300, which is similar to that of the IP camera (IPC).

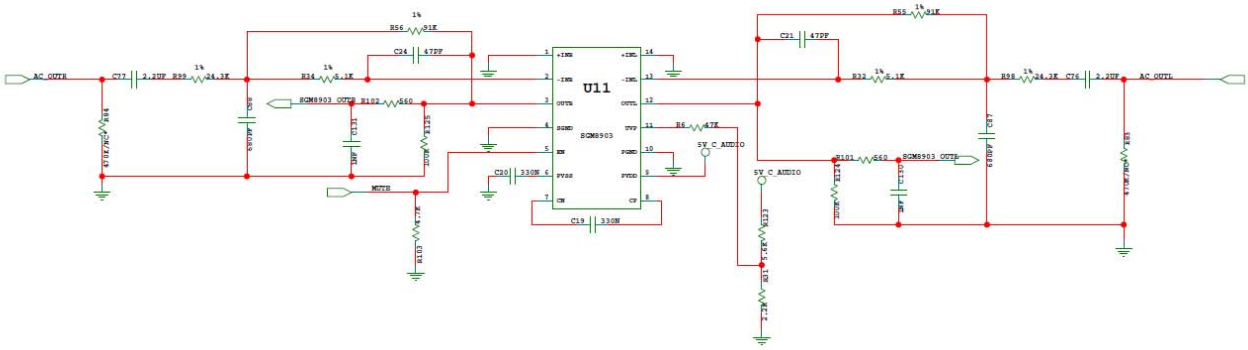
Figure 2-4 Analog AO processing on the board

Block Diagram of the AO Circuit



The recommended external operational amplifier for the circuit on the board is SGM8903, which can suppress crackles. Figure 2-5 shows the analog AO amplifier and the filter circuit on the board.

Figure 2-5 Analog AO amplifier and filter circuit on the board

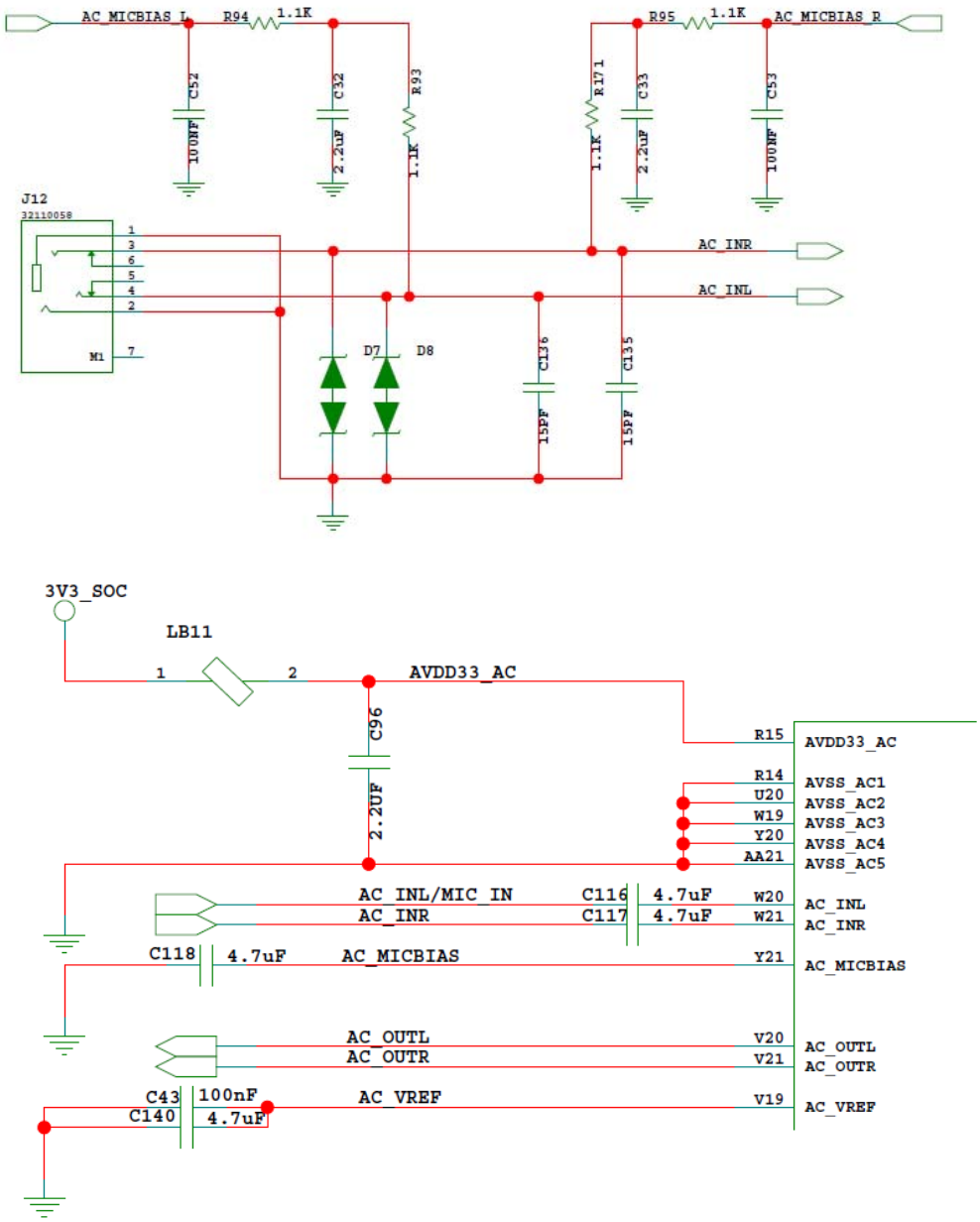


2.1.3 Precautions During the Audio Circuit PCB Design

Note the following:

- Keep the audio signals far away from digital signals to prevent interference.
- Place the capacitor connected to the AC_VREF pin close to the master chip, and ensure that the maximum spacing is less than or equal to 150 mils.
- Choose the ground (GND) as the return path of the audio signal if possible. Ensure that the audio signal does not share the return path with other signals, especially the digital signal.
- The GND of the audio module must not be directly connected to the bottom and top surfaces. You are advised to connect the input GND capacitors (C135/C136), GND capacitors of the MICBIAS signal (C32/C33/C52/C53/C110), AC_Vref filter capacitors (C43/C140), AVDD33_AC filter capacitor (C96), and VASS_AC GND pins (R14/U20/W19/Y20/AA21) to the same GND plane through via holes.
- Route the analog audio input/output signal and MICBIAS signal by using the GND layer as the reference plane, and ensure that the reference plane is complete.
- Surround the analog audio input/output signal and MICBIAS signal with GND traces, and evenly place the GND vias between adjacent signal traces.
- Ensure that parameters of the MICBIAS circuit are consistent with those for Hi3516D V300 demo board.
- To ensure the audio quality during MIC circuit design, it is recommended that the AC_MICBIAS signal be divided into two channels at Hi3516D V300 end and the two signals correspond to the bias levels of the audio-left and audio-right channels respectively.
- Place the 4.7 μF capacitor (C118) close to the master chip. Place the 1.1-kilohm resistors (R93/R94/R95/R171), 2.2 μF capacitors (C32/C33), and 100 nF capacitors (C52/C53) closet to the input end.

Figure 2-6 Analog AI circuit of Hi3516D V300



2.2 Optimization of the Echo Structure for Audio Intercom

If Hi3516D V300 is used for the IPC that features small size and high integration, the distance between the MIC and handset may be too small. When the audio gain is large, the speaker exerts severe interference on the MIC input (the echo cancellation function must be enabled), and therefore echoes are generated during intercom. To solve this problem, note the following during product structure design:

- Keep the MIC far away from the speaker and control the angle between the MIC and the speaker to minimize the coupling of voice signals.
- Enclose the MIC chamber to prevent voices from passing through mechanical parts to the MIC. Enclose the speaker as required.
- Ensure that the ratio of the total area of the speaker sound chamber opening to the cross-sectional area of the chamber is greater than 15%.
- Generally, the sound effect of the medium- and low-frequency parts of the voice is improved and the power is decreased when the sound chamber of the speaker is enlarged. Therefore, the sound chamber of the speaker is expected to be large. However, other factors also need to be considered for the structure design of the product.
- Open round holes with a diameter of 0.8–1.2 mm on the MIC. Control the size of the front sound chamber of the MIC and reserve one straight hole.
- Enclose the MIC by using rubber, foam, or a voice guide sleeve (preferable). If the MIC is not enclosed, voice may leak from the speaker to the MIC, increasing the difficulty of echo cancellation. Generally, the voice guide sleeve is assembled on the product to prevent voice leakage, provide sealing effect, and avoid resonance.
- Ensure that the sound chamber mechanical part is designed with the anti-vibration function during the speaker structure design to prevent the vibration passing from the cover of the mechanical part to the RX end of the MIC. In addition, the sound chamber must be sound-proofing to avoid crosstalk caused by sound leak of the sound chamber.

2.3 Audio Register Configuration

2.3.1 Audio Input/Output Gain Control

The audio input gain includes the digital gain control and analog gain control.

- The recommended digital gain is 0 dB–4 dB, and should not exceed 8 dB. A too large digital gain may affect the sound quality. The corresponding register is AUDIO_ADC_REG_0, and the register address is 0x113c003c. Take the digital gain of the audio-left channel for example, AUDIO_ADC_REG_0 bit [30:24] are used to control the digital gain input from audio-to-digital converter (ADC) of the audio-left channel. For details, see the *Hi3516D V300 Professional Smart IP Camera SoC Data Sheet.*
- For analog gain control, the 0–50 dB analog gain can be configured. The corresponding registers are AUDIO_ANA_CTRL_1 and AUDIO_ANA_CTRL_3, whose register addresses are 0x113c0018 and 0x113c0020 respectively. Take the analog gain of the audio-left channel as an example. Bit[20:16] of AUDIO_ANA_CTRL_3 are the gain_mic control bits of the audio-left channel, and bit[23] of AUDIO_ANA_CTRL_1 is the gain_boost control bit of the audio-left channel. When this bit is set to **0**, the gain is not amplified. When this bit is set to **1**, the gain is amplified by 20 dB.
- For the input gain, you are advised to preferentially configure the analog gain. If more gains need to be increased after the analog gain is configured to the maximum amplitude, you can choose to configure the digital gain.
- To obtain an appropriate AO volume, you can set an appropriate output gain value by configuring AUDIO_DAC_REG_1 bit[30:24]. Typically, when the output gain is 0 dB, the requirements on the AO volume on the board can be met. The maximum AO gain is 6 dB. You can set the AO output gain based on products. Note that the output gain value cannot be too large; otherwise, crackles may occur.

2.4 AI/AO Interfaces and Functions

2.4.1 AI/AO Gain Interfaces

The audio gain interface adjusts the gain of each part based on the required gain and configures the corresponding register to adjust the gain and minimize the background noise. Four AI/AO gain adjustment interfaces are added in the new solution, which are implemented by calling the ioctl interface of the audio codec. The interfaces are described as follows:

- ACODEC_SET_INPUT_VOL: configures the AI gain. The value range of the parameter is [−78 dB, +80 dB]. Both the analog gain and digital gain are included. A larger value indicates higher volume. For example, the value 80 indicates the maximum volume, and the value −78 indicates the minimum volume (muted status). The volume adjustment takes effect simultaneously in the audio-left and audio-right channels. The recommended volume range is [19 dB, 50 dB]. Within this range, the noises are lowest because only the analog gain is adjusted, and the voice quality can be ensured.
- ACODEC_SET_OUTPUT_VOL: configures the AO gain. The value range of the parameter is [−121 dB, +6 dB]. A larger value indicates higher volume. For example, the value 6 indicates the maximum volume of 6 dB, and the value −121 indicates the minimum volume (muted status). The volume adjustment takes effect simultaneously in the audio-left and audio-right channels. This interface is used to adjust the AO digital gain. Typically, 0 dB gain can meet requirements. When you adjust the gain, take the amplification multiple of the external operational amplifier circuit on the board into account. The output gain value cannot be too large; otherwise, crackles may occur due to clipping.
- ACODEC_GET_INPUT_VOL: obtains the AI gain. This interface is used to obtain the gain value configured by using the ACODEC_SET_INPUT_VOL interface. The value range of the AI gain is [−78 dB, +80 dB].
- ACODEC_GET_OUTPUT_VOL: obtains the AO gain. This interface is used to obtain the gain value configured by using the ACODEC_SET_OUTPUT_VOL interface. The value range of the AO gain is [−121 dB, +6 dB].

2.5 Interface Description

2.5.1 Interface for the Audio 3A Algorithm

For details about the usage, see the description of voice quality enhancement (VQE) in chapter 9 "Audio" of the *HiMPP V4.0 Media Processing Software Development Reference*.

2.5.2 Enabling Software ANR Algorithm

2.5.2.1 Voice Quality Enhancement Algorithm

To obtain better audio effect, it is recommended that you enable the audio noise reduction (ANR) algorithm.

2.5.2.2 Software Process

Pop tones may appear during AI initialization. You will need to modify the upper-layer software behavior to obtain better audio experience. You can select either of the following recommended modification solutions based on your requirements.

- Solution 1: Enable the AI channel when starting the device, and keep the AI channel enabled and resident.
- Solution 2: Enable the disabled AI channel during usage. You will need to mute or discard the data recorded during the first 1 to 2 seconds to avoid pop tones when enabling the AI channel.

2.6 Constraints on the MIC Sensitivity

MIC sensitivity affects the sound pickup distance. According to the sound pickup distance requirements of different application scenarios, after the hardware bias voltage is added, the MIC sensitivity specifications must be constrained as shown in Table 2-1.

Table 2-1 Constraints on MIC sensitivity specifications

Sound Pickup Distance	**MIC Sensitivity Specification**	
	Gain of 40 dB Analog 40 dB	Gain of 36 dB Analog 36 dB
Short distance (20-50 cm)	Unlimited	Unlimited
About 1 m	Unlimited	≥ –38 dB
About 3 m	≥ –38 dB	≥ –32 dB

NOTE

The table recommends selecting MIC when the maximum gain is configured. When a MIC with a higher sensitivity is selected, you must configure an appropriate gain based on testing results to avoid clipping distortion.

3 Summary

The audio quality is optimal when the following conditions are met:

- The audio amplifier and filter circuit are used in the external audio circuits. For details, see the latest schematic diagrams.
- The recommended crackle suppression audio amplifiers such as SGM8903 are used.
- The echo cancellation function is enabled and the product structure meets the requirements for canceling echoes generated in audio intercom.
- The registers must be properly configured, and the interfaces and functions must be correctly called.
- The correct interface function must be called to implement gain configuration.

