TDSHT3v1-3 Page 1 of 10

HDMI Compliance Test Software: Measurement Report



Sat Nov 03 08:02:26 GMT 2018

Source Tests Report

Configuration

Setup Configuration

Oscilloscope Info DPO73304S - 10.8.5 Build 4

TDSHT3 Version 5.3.6 Build 54

▶ Device Configuration

 Device Details
 HDMI Device

 Clock Frequency(Mhz)
 27.0000

 Resolution
 720x576p

 Refresh Rate
 60Hz

▶ Compliance Summary

 Total Tests Supported
 9

 Tests Completed
 29

 Pass
 29

 Fail
 0

▶ Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.009*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.01*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.01*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.01*Tbit	Pass
5	7-6 : Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0*TPixel	Pass
6	7-6 : Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0*TPixel	Pass
7	7-6 : Source Inter-Pair Skew	D2 - D0	Skew < 0.2*TPixel;	0*TPixel	Pass
8	7-4 : Source Rise Time	CK	75.00ps < TRISE;	162.56ps	Pass
9	7-4 : Source Rise Time	D0	75.00ps < TRISE;	122.56ps	Pass
10	7-4 : Source Rise Time	D1	75.00ps < TRISE;	130.27ps	Pass
11	7-4 : Source Rise Time	D2	75.00ps < TRISE;	127.34ps	Pass
12	7-4 : Source Fall Time	CK	75.00ps < TFALL;	163.20ps	Pass
13	7-4 : Source Fall Time	D0	75.00ps < TFALL;	125.17ps	Pass
14	7-4 : Source Fall Time	D1	75.00ps < TFALL;	125.84ps	Pass
15	7-4 : Source Fall Time	D2	75.00ps < TFALL;	121.71ps	Pass
16	7-8 : Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	50.49%	Pass
17	7-8 : Min Duty Cycle	CK	40.0% < Min Duty Cycle;	49.95%	Pass
18	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	CK+	2.700V < VL < 2.900V;	2.8380V	Pass
19	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D0+	2.700V < VL < 2.900V;	2.8319V	Pass
20	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	CK-	2.700V < VL < 2.900V;	2.8433V	Pass
21	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D0-	2.700V < VL < 2.900V;	2.8332V	Pass
22	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D1+	2.700V < VL < 2.900V;	2.8181V	Pass
23	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D2+	2.700V < VL < 2.900V;	2.8626V	Pass
24	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D1-	2.700V < VL < 2.900V;	2.8220V	Pass
25	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D2-	2.700V < VL < 2.900V;	2.8622V	Pass
26	7-7 : Source Intra-Pair Skew	CK	Skew < 0.15*Tbit;	0.008*Tbit	Pass
27	7-7 : Source Intra-Pair Skew	D0	Skew < 0.15*Tbit;	0.005*Tbit	Pass
28	7-7 : Source Intra-Pair Skew	D1	Skew < 0.15*Tbit;	0.005*Tbit	Pass
29	7-7 : Source Intra-Pair Skew	D2	Skew < 0.15*Tbit;	0.003*Tbit	Pass

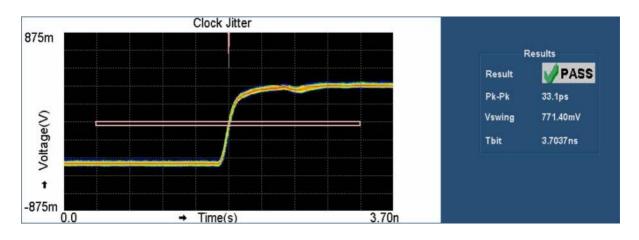
▶ Detailed Results

▶ 7-9 : Source Clock Jitter : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Result
Clock Jitter < 0.25*Tbit;	0.009*Tbit	3.7037ns	771.40mV	0.24*Tbit	50.000M	Pass

TDSHT3v1-3 Page 2 of 10

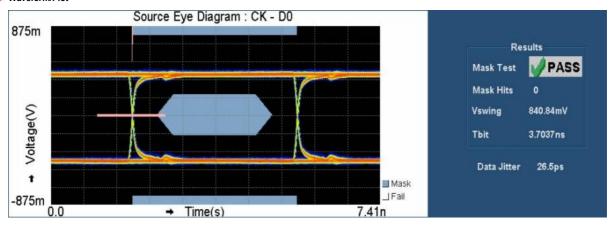


▶ 7-10 : Source Eye Diagram : CK - D0

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.01*Tbit	3.7037ns	840.84mV	0.29*Tbit	50.000M	0	Pass

Waveform/Plot

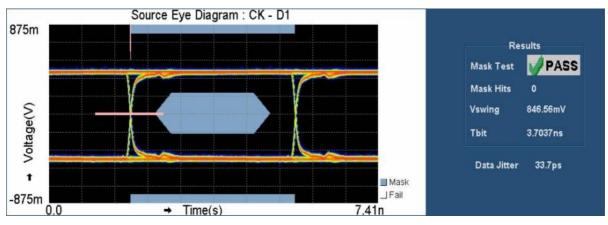


▶ 7-10 : Source Eye Diagram : CK - D1

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.01*Tbit	3.7037ns	846.56mV	0.29*Tbit	50.000M	0	Pass

Waveform/Plot

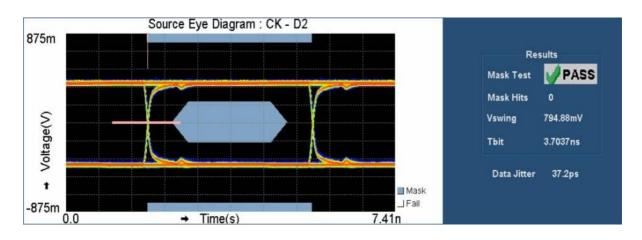


▶ 7-10 : Source Eye Diagram : CK - D2

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.01*Tbit	3.7037ns	794.88mV	0.29*Tbit	50.000M	0	Pass

TDSHT3v1-3 Page 3 of 10



▶ 7-6 : Source Inter-Pair Skew : D0 - D1

Results

Spec Range	Meas Value	Tbit	Vs(D0 - D1)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0*TPixel	3.7037ns	= 840.84mV, Vs = 846.56mV	143.54f	6.5317p	2.2820p	Pass

7-6 : Source Inter-Pair Skew : D1 - D2

Results

Spec Range	Meas Value	Tbit	Vs(D1 - D2)	Min	Max	Avg	Result
Skew < 0.2*TPixel:	0*TPixel	3.7037ns	= 846.56mV. Vs = 794.88mV	261.90f	4.8120p	2.3752p	Pass

7-6 : Source Inter-Pair Skew : D2 - D0

Results

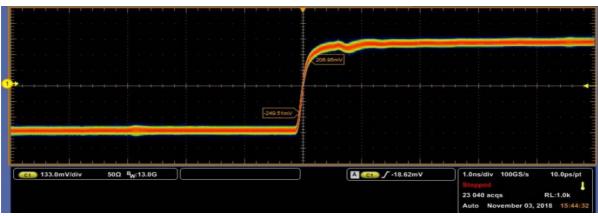
Spec Range	Meas Value	Tbit	Vs(D2 - D0)	Min	Max	Avg	Result
Skew < 0.2*TPixel:	0*TPixel	3.7037ns	= 794.88mV. Vs = 840.84mV	170.88f	6.1421p	2.2048p	Pass

7-4 : Source Rise Time : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	162.56ps	3.7037ns	760.76mV	87.56ps	Pass

Waveform/Plot



7-4 : Source Rise Time : D0

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	122.56ps	3.7037ns	829.08mV	47.56ps	Pass

TDSHT3v1-3 Page 4 of 10

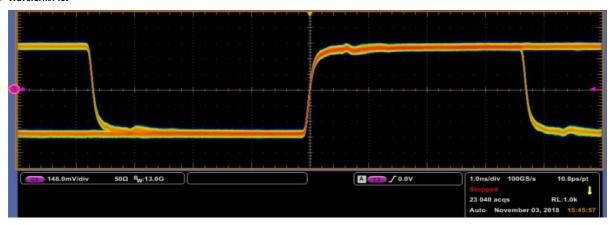


▶ 7-4 : Source Rise Time : D1

Results

Spec Range	Meas Value		Vs	Margin	
75.00ps < TRISE;	130.27ps	3.7037ns	834.72mV	55.27ps	Pass

Waveform/Plot



▶ 7-4 : Source Rise Time : D2

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	127.34ps	3.7037ns	778.32mV	52.34ps	Pass

Waveform/Plot



▶ 7-4 : Source Fall Time : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	163.20ps	3.7037ns	760.76mV	88.20ps	Pass

TDSHT3v1-3 Page 5 of 10

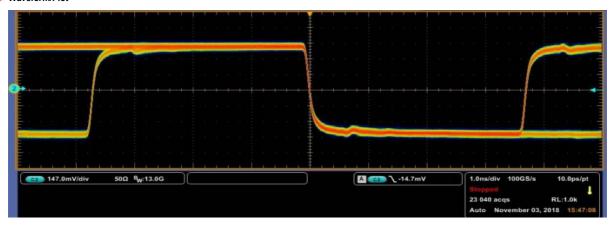


▶ 7-4 : Source Fall Time : D0

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	125.17ps	3.7037ns	829.08mV	50.17ps	Pass

Waveform/Plot

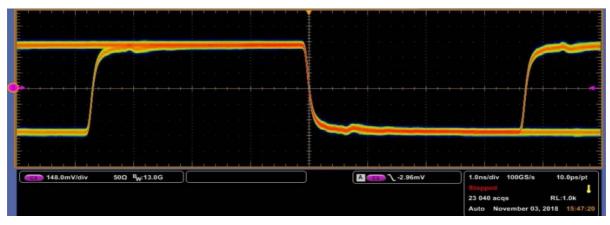


▶ 7-4 : Source Fall Time : D1

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	125.84ps	3.7037ns	834.72mV	50.84ps	Pass

Waveform/Plot

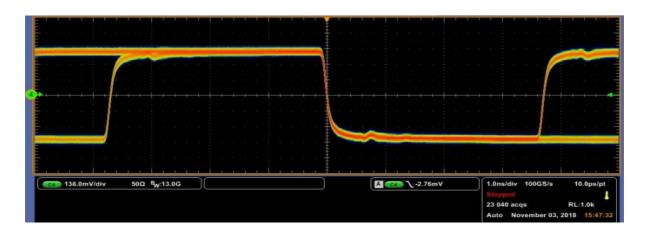


▶ 7-4 : Source Fall Time : D2

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	121.71ps	3.7037ns	778.32mV	46.71ps	Pass

TDSHT3v1-3 Page 6 of 10

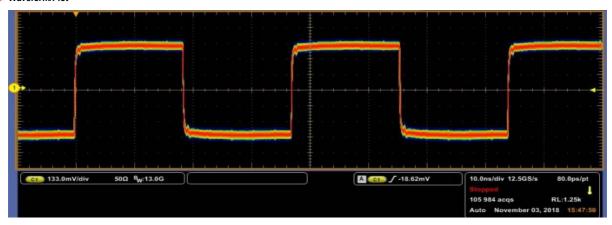


▶ 7-8 : Max Duty Cycle : CK

Results

Spec Range	Meas Value	Tbit	Margin	Result
Max Duty Cycle < 60.0%;	50.49%	3.7037ns	9.51%	Pass

Waveform/Plot

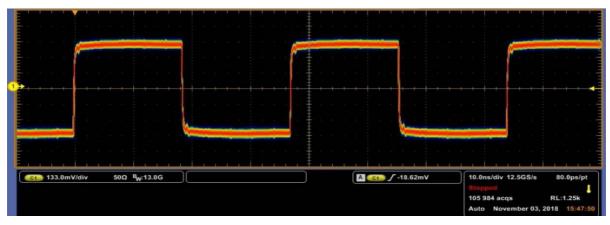


▶ 7-8 : Min Duty Cycle : CK

Results

Spec Range	Meas Value	Tbit	Margin	Result
40.0% < Min Duty Cycle;	49.95%	3.7037ns	9.95%	Pass

Waveform/Plot

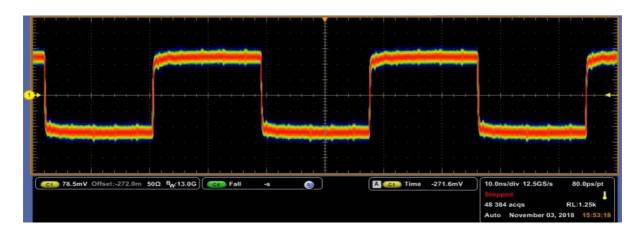


▶ 7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : CK+

Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8380V	61.97mV	138.0mV	Pass

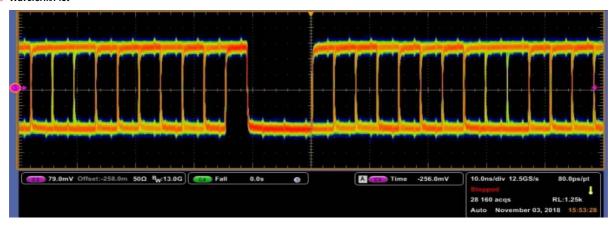
TDSHT3v1-3 Page 7 of 10



- ▶ 7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D0+
 - Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8319V	68.14mV	131.9mV	Pass

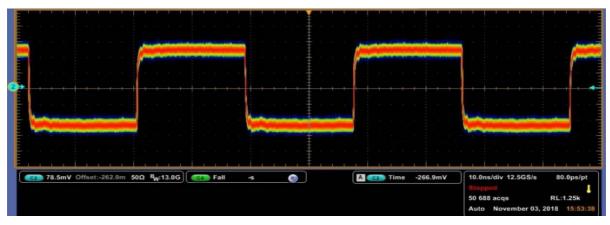
Waveform/Plot



- ▶ 7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : CK-
 - Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8433V	56.68mV	143.3mV	Pass

Waveform/Plot



- ▶ 7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D0-
 - Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8332V	66.81mV	133.2mV	Pass

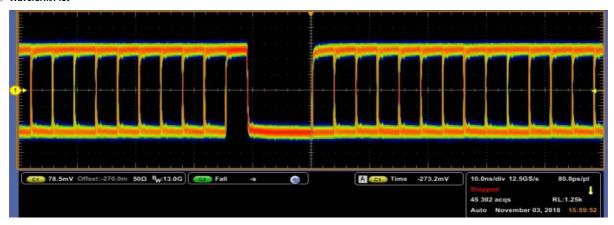
TDSHT3v1-3 Page 8 of 10



- ▶ 7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D1+
 - Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V:	2.8181V	81.95mV	118.1mV	Pass

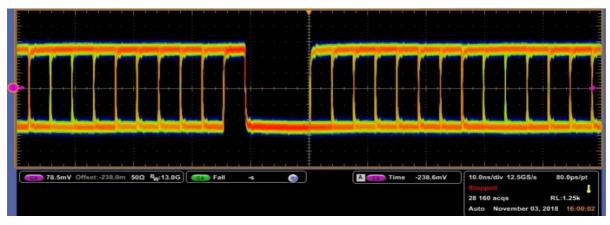
Waveform/Plot



- ▶ 7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D2+
 - Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8626V	37.39mV	162.6mV	Pass

Waveform/Plot



- ▶ 7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D1-
 - Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8220V	77.95mV	122.0mV	Pass

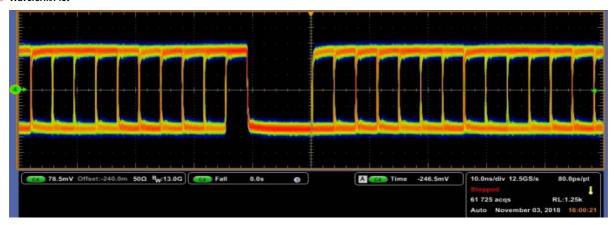
TDSHT3v1-3 Page 9 of 10



- ▶ 7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D2-
 - Results

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8622V	37.82mV	162.2mV	Pass

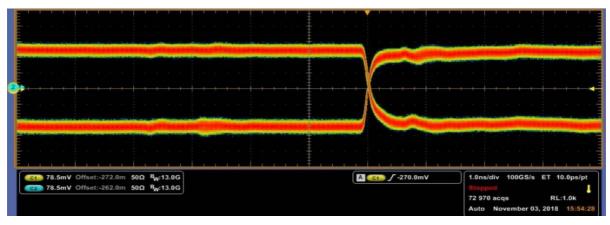
Waveform/Plot



- ▶ 7-7 : Source Intra-Pair Skew : CK
 - Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.008*Tbit	3.7037ns	0.14*Tbit	Pass

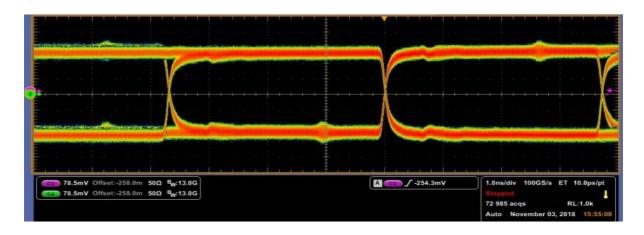
Waveform/Plot



- ▶ 7-7 : Source Intra-Pair Skew : D0
 - Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.005*Tbit	3.7037ns	0.14*Tbit	Pass

TDSHT3v1-3 Page 10 of 10

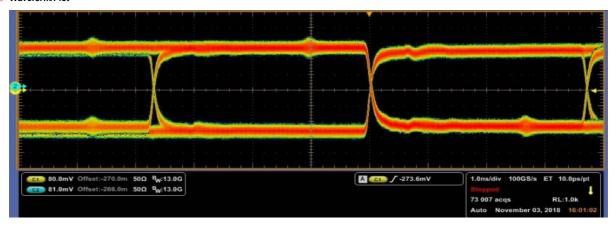


7-7: Source Intra-Pair Skew: D1

Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.005*Tbit	3.7037ns	0.14*Tbit	Pass

Waveform/Plot

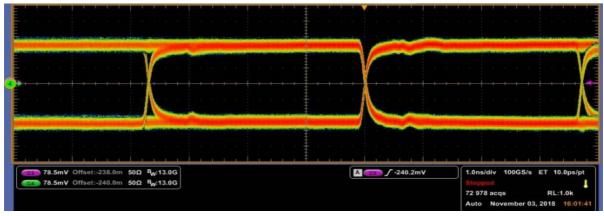


7-7 : Source Intra-Pair Skew : D2

Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.003*Tbit	3.7037ns	0.15*Tbit	Pass

Waveform/Plot



▲ Return to Test Summary

Return to top