Hi3516AV300 DDR4 Signal Integrity Report

System History

Date	Contents	Remarks
2018-10-16	The test is performed based on the DDR4 2133MHz standard	
Note: All the test data in this report is the test result of the HiSilicon test sample and is only for reference. Note that the tests conducted by HiSilicon cannot replace customers' related tests.		

Information

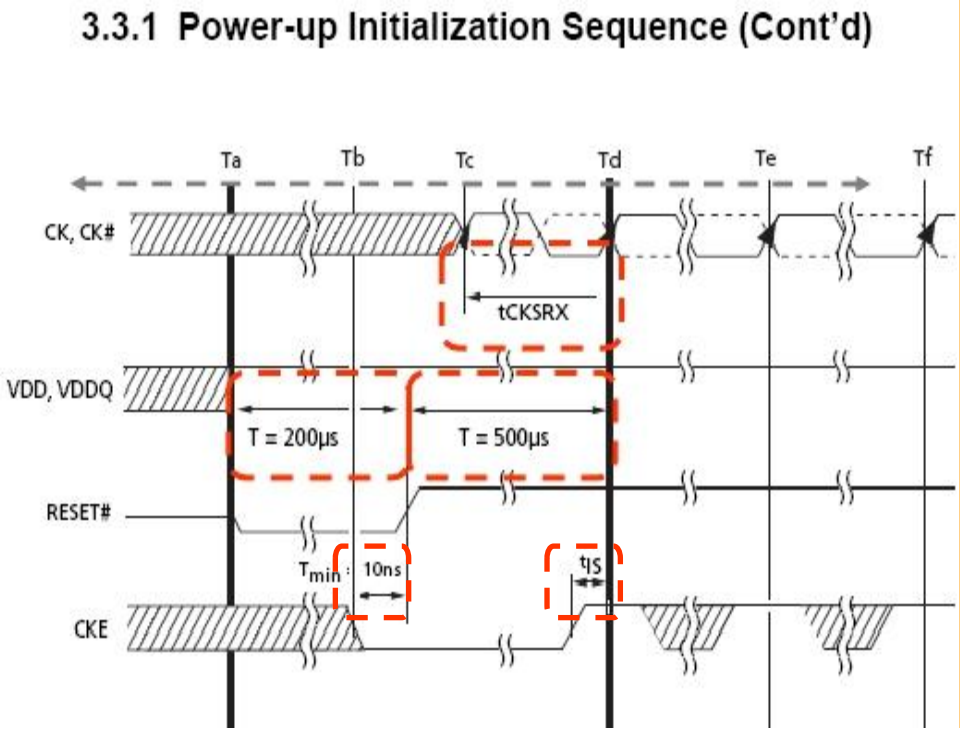
Chipset	Hi3516AV300
Board Name	HI3516AV300DMEBLITE VER.A
DRAM Part Number	MT41K256M16TW-107:P
Oscilloscope	DSA72004C TEKTRONIX
Temperature	25ºC
DRAM Operating Frequency	1066MHz(DDR4)
Vdd/Vref_CA/Vref_DQ/Vcore	1.2V/0.6V/Tranning/0.9V
DRAM_ODT	120ohm
SOC_ODT	120ohm
DRAM_RON	40ohm
SOC_RON	CK=34ohm 1T(CS/CKE/ODT)=34ohm 2T=34ohm DQ=40ohm DQS=40ohm

Signal Integrity Summary& Conclusion

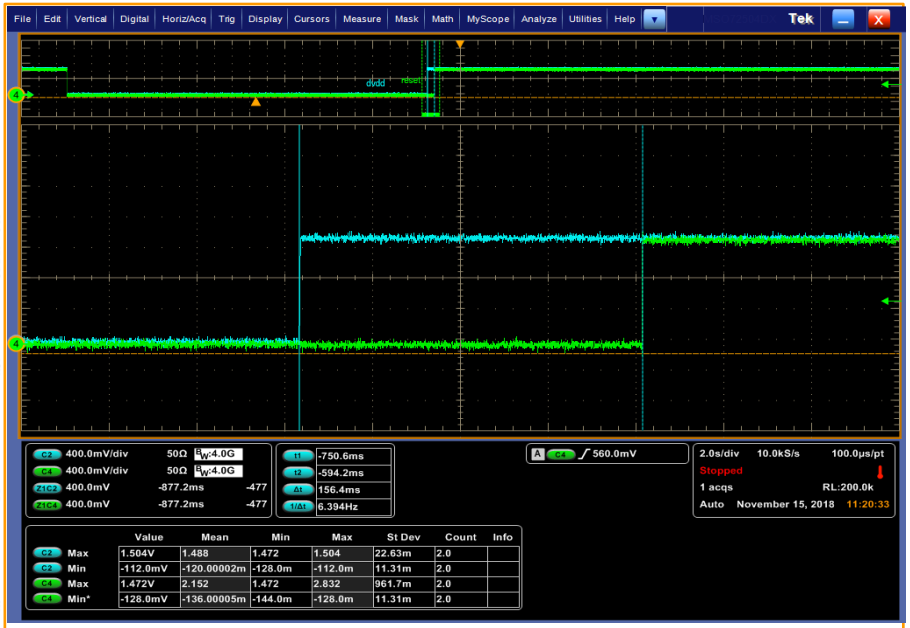
Judgment&Summary		
Measurement Item	**Result**	**Remark**
Sequence Check	**PASS**	
Power Check	**PASS**	
Signal Integrity Check	**PASS**	

Power Up Initialization Sequence Check Result

- **SPEC**



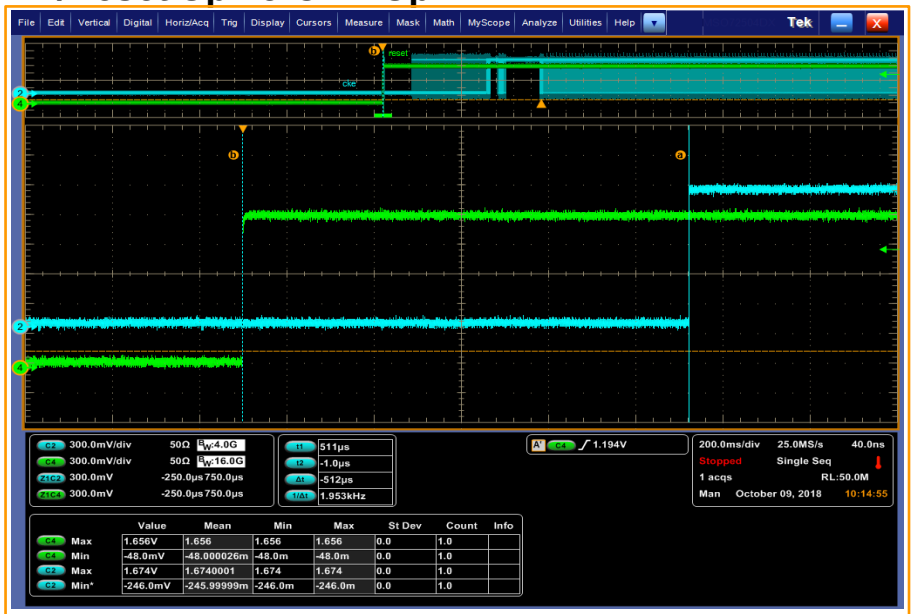
- **Stable VDD to /Reset Up**



Parameter	Time	Spec	Result	Remark
Stable VDD to /Reset Up	156ms	Min:200us	PASS	/RESET needs to be maintained for minimum 200us with stable power. (JEDEC spec.)

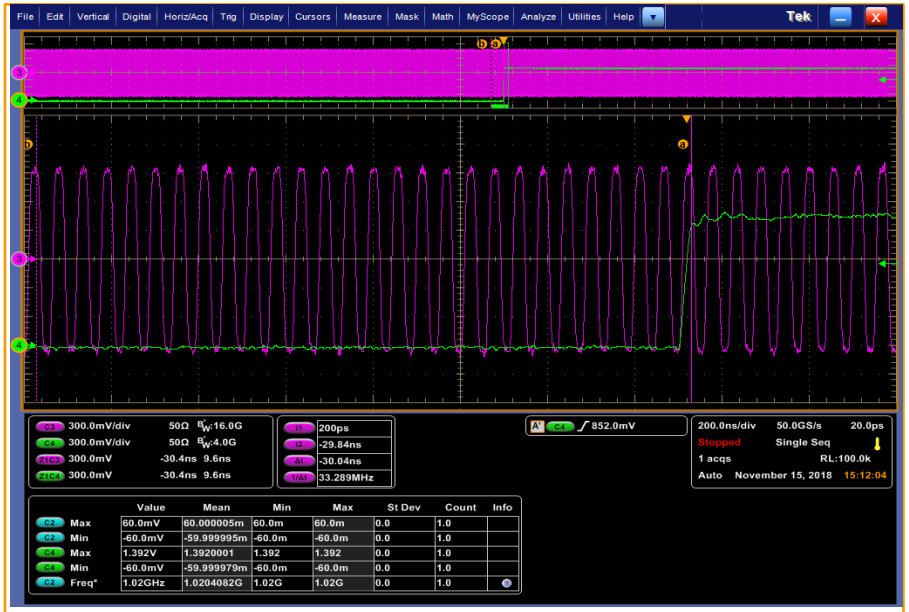
Power Up Initialization Sequence Check Result

- /Reset Up To CKE Up



CH4-RESET
CH2-CKE

- tCKSRX

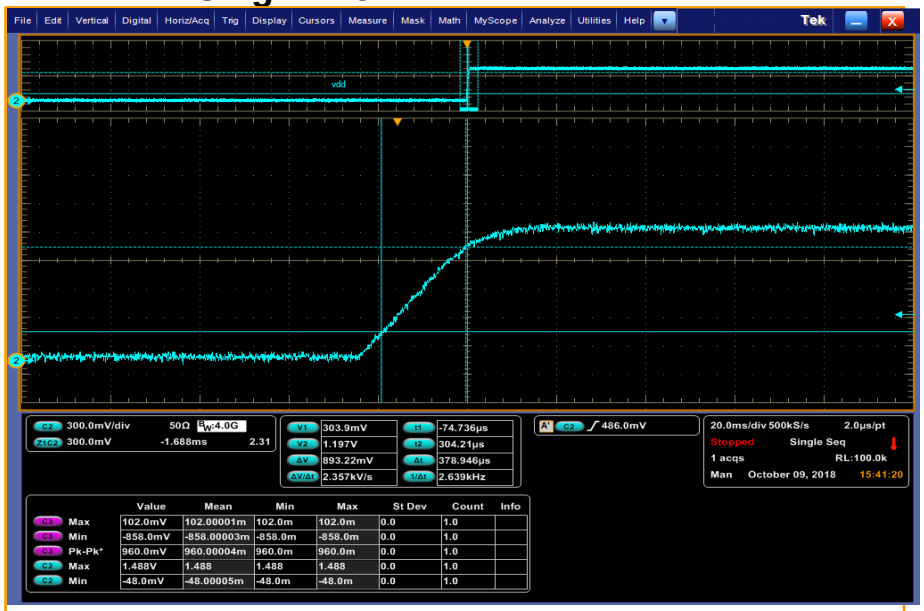


CH2-CKE
CH3-CK

Parameter	Time	Spec	Result	Remark
/Reset Up To CKE Up	512us	Min:500us	PASS	After /RESET is de-asserted. Wait for another 500us until CKE becomes active.(JEDEC spec.)
tCKSRX	>30ns	Min: Max(5nCK,10ns)	PASS	Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active.(JEDEC spec.)

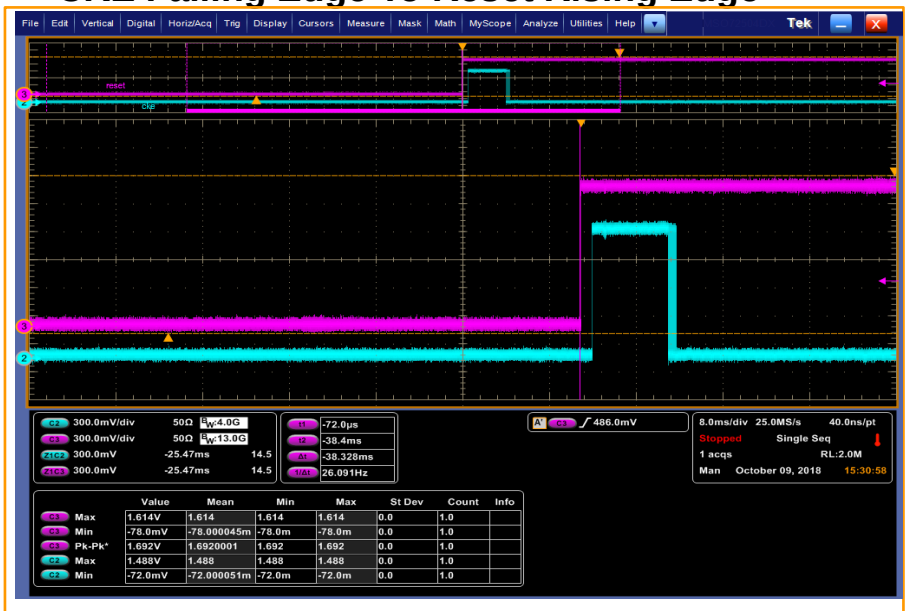
Power Up Initialization Sequence Check Result

VDD Rising Time



CH2-VDD

CKE Falling Edge To Reset Rising Edge

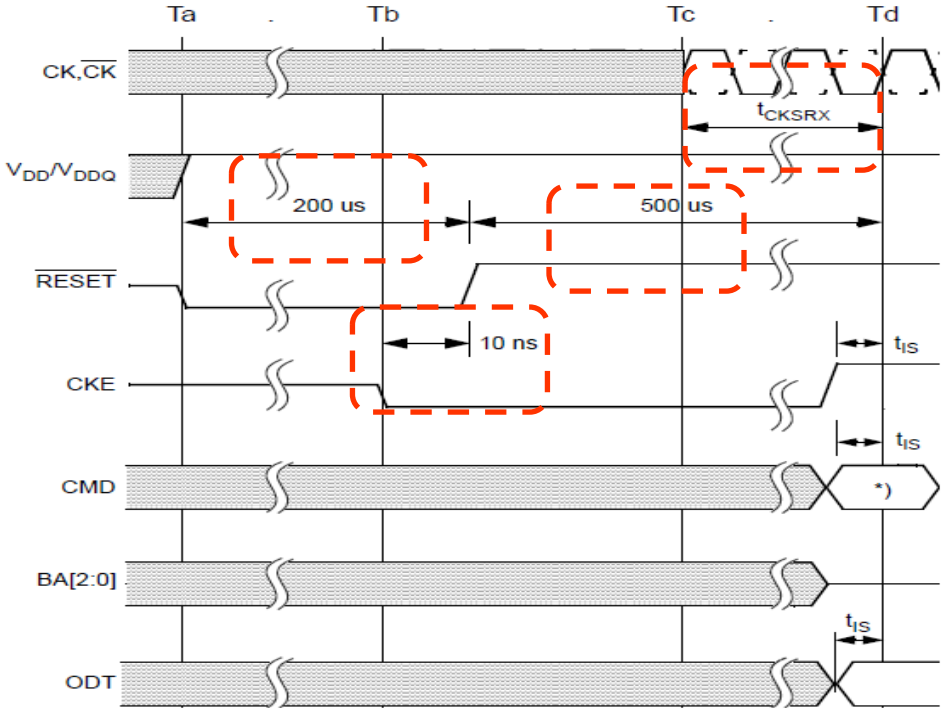


CH3-RESET
CH2-CKE

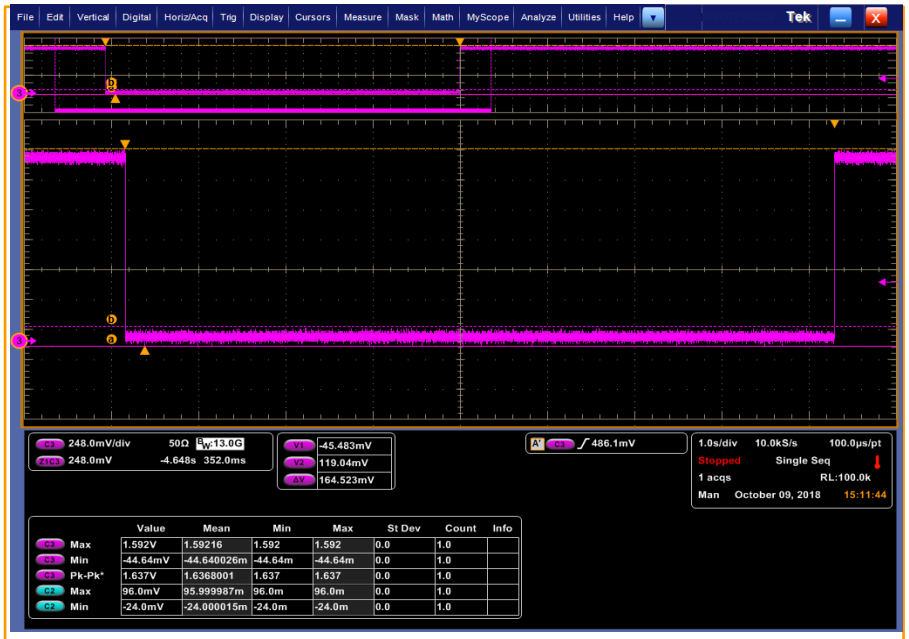
Parameter	Time	Spec	Result	Remark
VDD Rising Time	379us	Max:200ms	PASS	The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms.(JEDEC spec.)
CKE Falling Edge to Reset Rising Edge	>38.4ms	Min:10ns	PASS	CKE is pulled “Low” anytime before RESET# being de-asserted (min. time 10 ns).

Reset Initialization Sequence Check Result

SPEC



Reset Low Level Voltage



CH3-RESET

Parameter	Voltage	Spec	Result	Remark
Reset Low Level Voltage	164.5mV	Max: 300mV	PASS	Reset Low Level Voltage must be within 300 mV.

Average Periodic Refresh Interval Check Result

SPEC

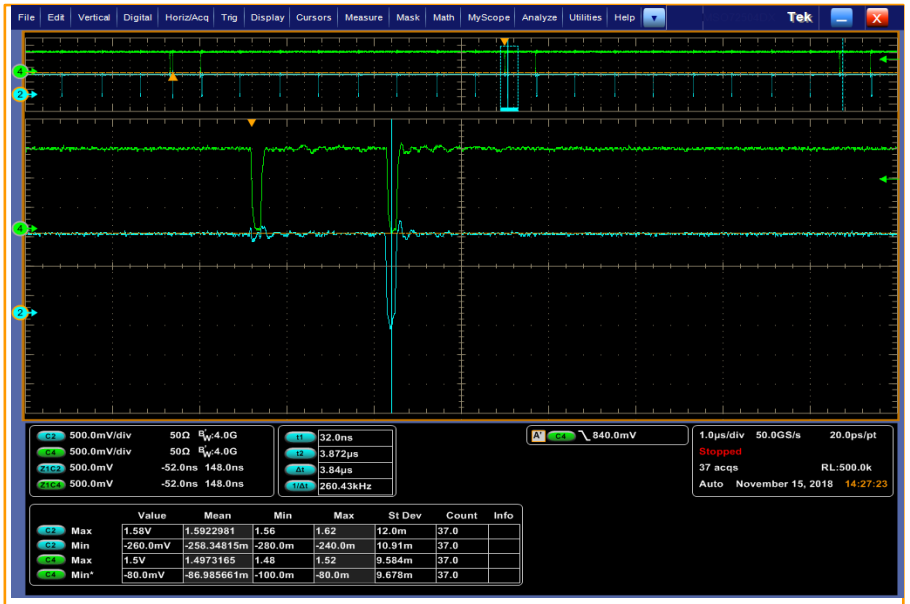
12.2 Refresh parameters by device density

Table 61 — Refresh parameters by device density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units	Notes
REF command to ACT or REF command time	tRFC		90	110	160	300	350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85 °C	7.8	7.8	7.8	7.8	7.8	µs	
		85 °C < T_{CASE} ≤ 95 °C	3.9	3.9	3.9	3.9	3.9	µs	1

NOTE 1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

Average Periodic Refresh Interval



CH2-RASN
CH1-CASN

Parameter	Time	Spec	Result	Remark
tREFI	3.84us	Max:7.8us	PASS	

Power Check Result

- **AC Peak-Peak Noise Check Result**

Parameter	Spec (PK-PK)	Value (PK-PK)	Unit	Result	Position	Test Point
VDD_IO	NA	34	mV	NA	DRAM	C283
VREFCA	30	14.2	mV	PASS	DRAM	C153
VREFDQ	30	14.4	mV	PASS	DRAM	C156

- **VDD_IO Supply Voltage**

Parameter	Spec	Value	Unit	Result	Position	Test Point
VDD_IO	Min:1.283 Max:1.45	1.355	V	PASS	SOC	LB20
		1.356	V	PASS	DDR	R174

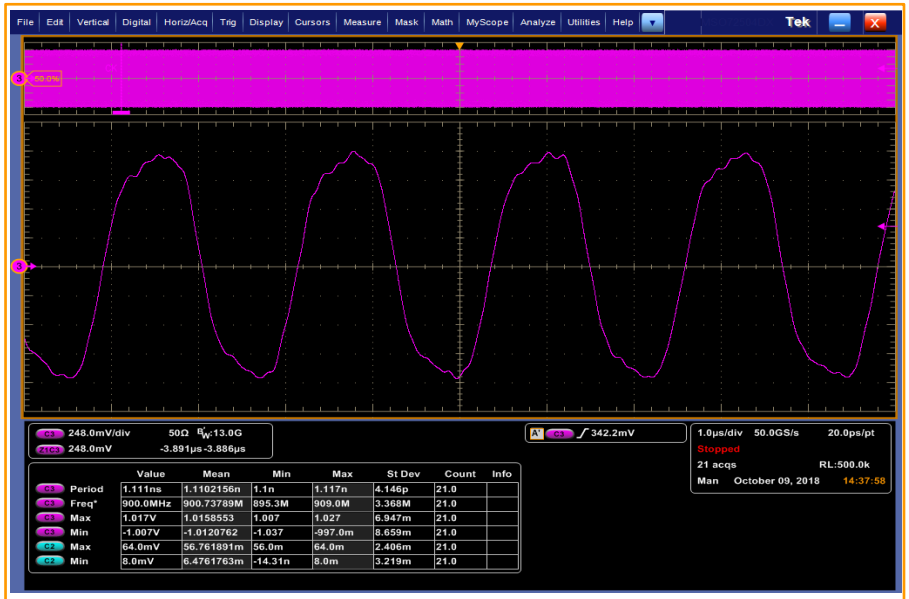
Signal Integrity Test Result (Clock)

- **Clock Signal Integrity Test Result**

Parameter	Spec (Min)	Spec (Max)	Measurement data (Min)	Measurement data (Max)	Unit	Remark
Vix	-150	150	-114.33	93	mV	PASS
tCK(avg)	1.07	1.25	1.110	1.112	ps	PASS
tCH(avg)	470	530	506	508	mtCK(avg)	PASS
tCL(avg)	470	530	491	494	mtCK(avg)	PASS
tJIT(per)	-70	70	-17.3	20.5	ps	PASS
tJIT(cc)	-140	140	-15.5	18.8	ps	PASS
InputSlew-Diff-Rise	-	-	-	10.108	V/ns	-
InputSlew-Diff-Fall	-	-	-	-6.3436	V/ns	-

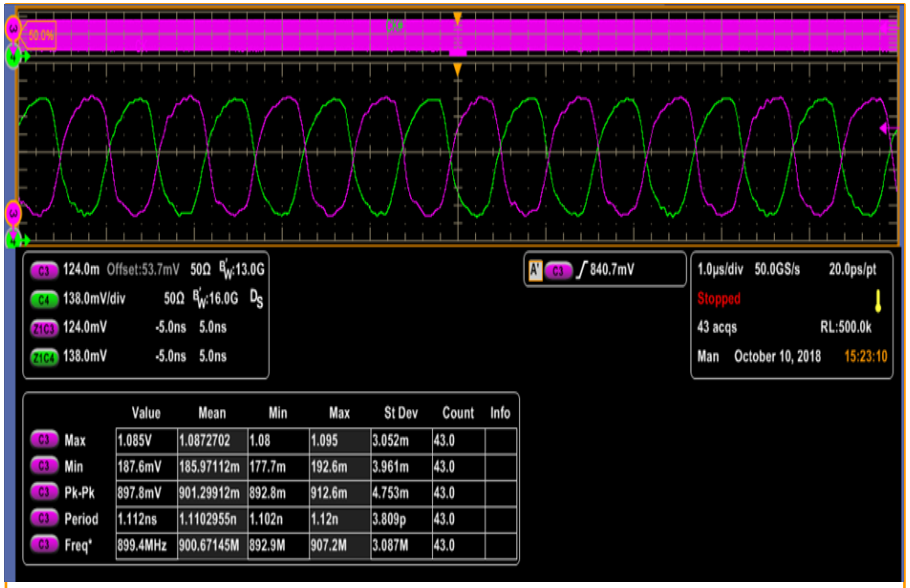
Signal Integrity Test Result (Clock)

- **CLK With Differential Measurement**



CH3 -CLK(Diff)

- **CLK Vix With High Voltage Trigger**



CH4-CLK+
CH3-CLK-

Signal Integrity Test Result (CMD&ADDR)

- **SPEC**

Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units
tIS(base) AC175	$V_{IH/L(ac)}$	200	125	65	45	-	-	ps
tIS(base) AC150	$V_{IH/L(ac)}$	350	275	190	170	-	-	ps
tIS(base) AC135	$V_{IH/L(ac)}$	-	-	-	-	65	60	ps
tIS(base) AC125	$V_{IH/L(ac)}$	-	-	-	-	150	135	ps
tIH(base) DC100	$V_{IH/L(dc)}$	275	200	140	120	100	95	ps

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC125 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV																	
		CK,CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
	1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
	0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
	0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
	0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
	0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
	0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10

Signal Integrity Test Result (CMD&ADDR)

- **Command Signal Integrity Test Result**

CMD /ADD	Input Setup Time (tIS)@AC150 tIS(min)(ps）	Input Hold Time (tIH)@DC100 tIH(min)（ps）	Input Slew Rate (Rising Time)（V/ns）	Input Slew Rate (Falling Time)（V/ns）
SPEC	133	150		
CS_N	552	476	2.08	-3.16
ODT	533	491	2.25	-2.54

Signal Integrity Test Result (CMD&ADDR)

- 1T_CMD_ADDR CS_N

- 1T_CMD_ADDR ODT

Signal Integrity Test Result (CMD&ADDR)

Address Signal Integrity Test Result

CMD /ADD	Input SetupTime (tIS)@AC150 tIS(min)(ps）	Input Hold Time (tIH)@DC100 tIH(min)（ps）	Input Slew Rate (RisingTime)（V/ns）	Input Slew Rate (FallingTime)（V/ns）
SPEC	133	150		
A4	1001.5	1069.9	3.6	-2.4734
A7	1023.1	1042.7	3.6	-2.8045

Signal Integrity Test Result (CMD&ADDR)

- 2T_CMD_ADDR A4

- 2T_CMD_ADDR A7

Signal Integrity Test Result (DATA)

- **SPEC**

Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units	Notes
tDS(base) AC175	$V_{IH/L(ac)}$ SR=1V/ns	75	25	-	-	-	-	ps	2
tDS(base) AC150	$V_{IH/L(ac)}$ SR=1V/ns	125	75	30	10	-	-	ps	2
tDS(base) AC135	$V_{IH/L(ac)}$ SR=1V/ns	165	115	60	40			ps	2, 3
tDS(base) AC135	$V_{IH/L(ac)}$ SR=2V/ns	-	-	-	-	68	53	ps	1
tDH(base) DC100	$V_{IH/L(dc)}$ SR=1V/ns	150	100	65	45	-	-	ps	2
tDH(base)DC100	$V_{IH/L(dc)}$ SR=2V/ns					70	55	ps	1

ΔtDS, ΔtDH derating in [ps] AC/DC based
Alternate AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV
Alternate DC 100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV

		DQS,DQS# Differential Slew Rate																							
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQS Slew rate V/ns	4.0	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.0	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
	2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
	1.0	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-38	-76	-30	-60

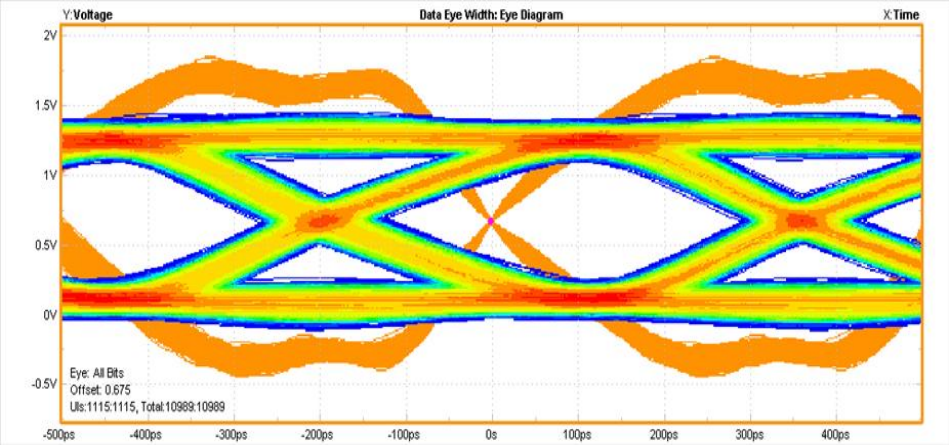
Signal Integrity Test Result (DATA)

- **Data Signal Integrity Test Result**

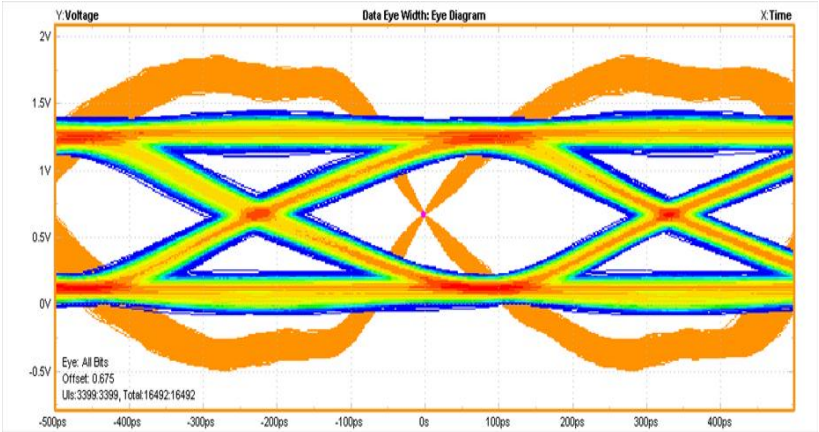
Parameter	Spec	Unit	DQ7	DQ14	Remarks
Input Slew Rate(Setup-time)	-	V/ns	5.7	3.12	-
Input Slew Rate(Hold-time)	-	V/ns	-5.7	-3.51	-
Input Setup-Time(tDS)@AC135 [tDS(base)=68ps]	min:99	ps	128.65	107.41	PASS
Input Hold-Time(tDH)@DC100 [tDH(base)=70ps]	min:95	ps	214.09	241.41	PASS

Signal Integrity Test Result (DATA)

- DQ7-Write



- DQ14-Write



DDR Training write window

```
[PHY0][RANK0]:
Write window of prebit-deskew:
-----------------------------------------------------
DQ  0   4   8   12  16  20  24  28  32  36  40  44  48  52  56  60  64  68  72  76  80  84  88  92  96  100 104 108 112 116 120 124  RANGE       DQPH  DQ  WIN
0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX----------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXX 0x00250067  0x8   70  67
1   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX--------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX 0x0020005e  0x8   63  63
2   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXX 0x00220065  0x8   68  68
3   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXX 0x00220065  0x8   68  68
4   XXXXXXXXXXXXXXXXXXXXXXXXX----------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX 0x001b0059  0x8   58  63
5   XXXXXXXXXXXXXXXXXXXXXXXXX----------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX 0x001a005b  0x8   59  66
6   XXXXXXXXXXXXXXXXXXXXXXXXXX--------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX 0x001c005d  0x8   61  66
7   XXXXXXXXXXXXXXXXXXXXXXXXXX--------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX 0x001c005b  0x8   60  64
8   XXXXXXXXXXXXXXXXXXXXXXXXXX----------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX 0x001c0059  0x8   59  62
9   XXXXXXXXXXXXXXXXXXXXXXXXXXXX------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXX 0x00230063  0x8   67  65
10  XXXXXXXXXXXXXXXXXXXXXXXXXXXXX-----------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXX 0x00210063  0x8   66  67
11  XXXXXXXXXXXXXXXXXXXX--------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX 0x00170056  0x8   55  64
12  XXXXXXXXXXXXXXXXXXXXXXXXXX--------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX 0x001c0059  0x8   59  62
13  XXXXXXXXXXXXXXXXXXXXXXXXXXXXX-----------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXX 0x00220060  0x8   65  63
14  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXX 0x00270063  0x8   69  61
15  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX--------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXX 0x00210061  0x8   65  65
-----------------------------------------------------
Sum WIN: 1034. Avg WIN: 64
Min WIN: 61. DQ Index: 14
Max WIN: 68. DQ Index: 2 3
```

DDR Training-read window

```
Read window of prebit-deskew:
--------------------------------------------------------
DQ  0   4   8   12  16  20  24  28  32  36  40  44  48  52  56  60  64  68  72  76  80  84  88  92  96  100 104 108 112 116 120 124  RANGE       DQS   DQ  WIN
0   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX-------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXX 0x00240065  0x35  69  66
1   XXXXXXXXXXXXXXXXXXXXXXXXXX-----------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x001d005d  0x35  61  65
2   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX---------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXX 0x00230065  0x35  68  67
3   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX-------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXX 0x00260067  0x35  71  66
4   XXXXXXXXXXXXXXXXXXXXXX-------------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x00190059  0x35  57  65
5   XXXXXXXXXXXXXXXXXXXXXXXX-----------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x001c005b  0x35  60  64
6   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX-----------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x0021005f  0x35  64  63
7   XXXXXXXXXXXXXXXXXXXXXXXXXXXX-------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x001e005c  0x35  61  63
8   XXXXXXXXXXXXXXXXXXXXXXXXXXXX-------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x001d005b  0x38  60  63
9   XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX-----------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXX 0x00280066  0x38  71  63
10  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX-----------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXX 0x00270067  0x38  71  65
11  XXXXXXXXXXXXXXXXXXXXXXXX-----------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x001b0058  0x38  58  62
12  XXXXXXXXXXXXXXXXXXXXXXXXXX-----------------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x001d0059  0x38  59  61
13  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX-----------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x00220060  0x38  65  63
14  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX---------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x00240060  0x38  66  61
15  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX-------------------------------------------------------------XXXXXXXXXXXXXXXXXXXXXXXXXX 0x00240061  0x38  67  62
--------------------------------------------------------
Sum WIN: 1019. Avg WIN: 63
Min WIN: 61. DQ Index: 12 14
Max WIN: 67. DQ Index: 2
```

Thank you