



# **Hi3516C V500 DDR4 Configuration Guide**


**Issue**        **01**

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## **HiSilicon (Shanghai) Technologies Co., Ltd.**

Address: New R&D Center, 49 Wuhe Road, Bantian,  
Longgang District,  
Shenzhen 518129 P. R. China

Website: <http://www.hisilicon.com/en/>

Email: [support@hisilicon.com](mailto:support@hisilicon.com)



# About This Document

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## Related Version

The following table lists the product version related to this document.

| Product Name | Version |
|--------------|---------|
| Hi3516C      | V500    |

## Intended Audience

This document is intended for:

- Technical support engineers
- Software development engineers

## Change History

Changes between document issues are cumulative. The latest document issue contains all the changes made in earlier issues.

### Issue 01 (2019-05-25)

This issue is the first official release.



# Contents

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|  |           |
|--|-----------|
| <b>About This Document.....</b>                              | <b>i</b>  |
| <b>Contents .....</b>  | <b>ii</b> |
| <b>1 DDR3 Driver Configuration .....</b>                     | <b>1</b>  |
| 1.1 CLK/AC Driver Configuration .....                        | 1         |
| 1.2 DQS/DQ Driver Configuration in the Write Direction ..... | 1         |
| 1.3 DQS/DQ Driver Configuration in the Read Direction .....  | 2         |
| <b>2 DDR3 ODT Configuration.....</b>                         | <b>3</b>  |
| 2.1 DQS/DQ ODT Configuration in the Write Direction.....     | 3         |
| 2.1.1 ODT Enable in the Write Direction.....                 | 3         |
| 2.1.2 ODT in the Write Direction.....                        | 3         |
| 2.2 DQS/DQ ODT Configuration in the Read Direction .....     | 4         |
| 2.2.1 ODT Enable in the Read Direction .....                 | 4         |
| 2.2.2 ODT Values in the Read Direction.....                  | 4         |
| <b>3 DDR3 Capacity Configuration .....</b>                   | <b>5</b>  |
| 3.1 U-Boot Table Overview .....                              | 5         |



# 1 DDR4 Driver Configuration

## 1.1 CLK/AC Driver Configuration

- Register address  
DDR PHY: 0x1206d018
- Register description
  - Bit[25:23]: CK driver
  - Bit[22:20]: 2T driver
  - Bit[19:17]: 1T driver
- Drive strength
  - 000: disabled
  - 001: 240 ohms
  - 010: 120 ohms
  - 011: 80 ohms
  - 100: 60 ohms
  - 101: 48 ohms
  - 110: 40 ohms
  - 111: 34 ohms

**NOTE**

The 1T signals refer to CKE, CSN, ODT, and RESET signals, while the 2T signals refer to the AC signals except 1T signals.

## 1.2 DQS/DQ Driver Configuration in the Write Direction

- Register address  
DDR PHY: 0x1206d204 (bytes 0–1)
- Register description
  - Bit[16:14]: DQS driver in the write direction
  - Bit[13:11]: DQ driver in the write direction
- Drive strength
  - 000: disabled



- 001: 240 ohms
- 010: 120 ohms
- 011: 80 ohms
- 100: 60 ohms
- 101: 48 ohms
- 110: 40 ohms
- 111: 34 ohms

## 1.3 DQS/DQ Driver Configuration in the Read Direction

- Register address  
DDR PHY: 0x1206c064
- Register description  
Bit[18] and bit[17]: DQS/DQ driver in the read direction
- Drive strength
  - 00: 34 ohms
  - 01: 48 ohms
  - 10: reserved
  - 11: reserved



# 2 DDR4 ODT Configuration

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## 2.1 DQS/DQ ODT Configuration in the Write Direction

### 2.1.1 ODT Enable in the Write Direction

- Register address  
DDRC: 0x120680a0
- Register description
  - Bit[0] = 0: ODT disabled in the write direction
  - Bit[0] = 1: ODT enabled in the write direction

### 2.1.2 ODT in the Write Direction

- Register address  
DDR PHY: 0x1206c064
- Register description
  - Bit[26:24]: DQS/DQ ODT configuration in the write direction
- ODT values in the write direction
  - 000: Disable
  - 001: 60 ohms
  - 010: 120 ohms
  - 011: 40 ohms
  - 100: 240 ohms
  - 101: 48 ohms
  - 110: 80 ohms
  - 111: 34 ohms

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#### **NOTICE**

The ODT configuration in the write direction takes effect for both DQS and DQ signals.

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## 2.2 DQS/DQ ODT Configuration in the Read Direction

### 2.2.1 ODT Enable in the Read Direction

- Register address  
DDR PHY: 0x1206d248 (bytes 0–1)
- Register description
  - Bit[3] = 0: ODT enabled in the read direction
  - Bit[3] = 1: ODT disabled in the read direction

### 2.2.2 ODT Values in the Read Direction

- Register address  
DDR PHY: 0x1206d204 (bytes 0–1)
- Register description
  - Bit[31:29]: DQS ODT in the read direction
  - Bit[28:26]: DQ ODT in the read direction
- ODT values in the read direction
  - 000: disabled
  - 001: 240 ohms
  - 010: 120 ohms
  - 011: 80 ohms
  - 100: 60 ohms
  - 101: 48 ohms
  - 110: 40 ohms
  - 111: 34 ohms





# 3

## DDR4 Capacity Configuration

### 3.1 U-Boot Table Overview

The Hi3516C V500 memory interface can connect to a DDR4 DRAM with a maximum data bit width of 16 bits in single-channel mode. The DDR configuration is implemented in the U-Boot table. Hi3516C V500 provides one DDR4 U-Boot table, corresponding to the DDR4 DMEB design scheme.

DDR4 DMEB U-Boot table: *Hi3516CV500-DDR4DMEB\_4L-DDR4\_1800M\_1GB\_16bit-A7\_900M-SYSBUS\_300M*

Table 3-1 lists the DDR specifications supported by the U-Boot tables.

**Table 3-1** DDR specifications supported by the U-Boot tables

| U-Boot Table          | Total Capacity/Total Bit Width       | Channel   | DDR Type | DDR Rate (Mbit/s) | Rank Count | DDR Bit Width (Bit Width/PCS x Count) | Capacity/PCS       |
|-----------------------|--------------------------------------|-----------|----------|-------------------|------------|---------------------------------------|--------------------|
| DDR4DMEB U-Boot table | 512 MB/16 bits<br>or<br>1 GB/16 bits | Channel 0 | DDR4     | 1800              | 1          | 16 bits x 1                           | 4 Gbits or 8 Gbits |



#### NOTE

The DDR4DMEB U-Boot table is compatible with the single-piece 8 Gbits or 4 Gbits DDR. You do not need to modify the configuration.