Mapping Between Hi35xx Vxxx SVB Voltages and Registers

Issue 00B01

Date 2018-11-20

HiSilicon (Shanghai) Technologies Co., Ltd.

Address: New R&D Center, 49 Wuhe Road, Bantian,
Longgang District,
Shenzhen 518129 P. R. China

Website: http://www.hisilicon.com/en/

Email: support@hisilicon.com

About This Document

Related Version

The following table lists the product versions related to this document.

Product Name	Version
Hi3516C	V500
Hi3516D	V300
Hi3556	V200
Hi3559	V200
Hi3516A	V300

Intended Audience

This document is intended for technical support engineers.

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
DANGER	Indicates an imminently hazardous situation which, if not avoided, will result in death or serious injury.
WARNING	Indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.
CAUTION	Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury.

Symbol	Description
NOTICE	Indicates a potentially hazardous situation which, if not avoided, could result in equipment damage, data loss, performance deterioration, or unanticipated results. NOTICE is used to address practices not related to personal injury.
NOTE	Calls attention to important information, best practices and tips. NOTE is used to address information not related to personal injury, equipment damage, and environment deterioration.

Change History

Changes between document issues are cumulative. The latest document issue contains all changes made in previous issues.

Issue 00B01 (2018-11-20)

This issue is the first draft release.

Contents

Tables

1 Mapping Between Hi35xx Vxxx SVB Voltages and Registers

NOTE
In this document, Hi35xxVxxx refers to Hi3516C V500, Hi3516D V300, Hi3516A V300, Hi3556 V200, and Hi3559 V200.

To facilitate customers to check whether the actual SVB circuit precision of products meets the design requirements, Table 1-1 lists the configured values of core power registers and the corresponding output voltages for customers' reference.

Table 1-1 Mapping between Hi35xx Vxxx SVB voltages and registers

No.	Mapping Between Vcore and Registers Register Address Corresponding to the Core Power: 0x120300b0 Voltage Range: 0.64 V–1.05 V			
	Register Value	Configured Value (V)	Measured Value (V)	Error Tolerance (V)
15	0x00210c75	0.973	0.980	±0.03
16	0x00230c75	0.972	0.975	±0.03
17	0x00260c75	0.968	0.970	±0.03
18	0x00280c75	0.964	0.965	±0.03
19	0x002B0c75	0.958	0.960	±0.03
20	0x002D0c75	0.954	0.955	±0.03
21	0x002F0c75	0.95	0.950	±0.03
22	0x00320c75	0.944	0.945	±0.03
23	0x00340c75	0.94	0.940	±0.03
24	0x00370c75	0.934	0.935	±0.03
25	0x00390c75	0.93	0.930	±0.03
26	0x003C0c75	0.923	0.925	±0.03

No.	Mapping Between Vcore and Registers Register Address Corresponding to the Core Power: 0x120300b0 Voltage Range: 0.64 V–1.05 V			
	Register Value	Configured Value (V)	Measured Value (V)	Error Tolerance (V)
27	0x003E0c75	0.92	0.920	±0.03
28	0x00400c75	0.915	0.915	±0.03
29	0x00430c75	0.909	0.910	±0.03
30	0x00450c75	0.905	0.905	±0.03
31	0x00480c75	0.899	0.900	±0.03
32	0x004A0c75	0.895	0.895	±0.03
33	0x004D0c75	0.889	0.890	±0.03
34	0x004F0c75	0.885	0.885	±0.03
35	0x00510c75	0.881	0.880	±0.03
36	0x00540c75	0.874	0.875	±0.03
37	0x00560c75	0.871	0.870	±0.03
38	0x00590c75	0.865	0.865	±0.03
39	0x005B0c75	0.86	0.860	±0.03
40	0x005E0c75	0.854	0.855	±0.03
41	0x00600c75	0.85	0.850	±0.03
42	0x00620c75	0.846	0.845	±0.03
43	0x00650c75	0.84	0.840	±0.03
44	0x00670c75	0.836	0.835	±0.03
45	0x006A0c75	0.83	0.830	±0.03
46	0x006C0c75	0.826	0.825	±0.03

NOTE

- The preceding table is for reference only.
- The preceding table applies only to the verification of SVB circuit and the impedance and capacitance parameters recommended in section 1.2.6 "SVB Dynamic Voltage Scaling" in *Hi35xx Vxxx Hardware Design User Guide*.
- The SVB circuit solutions applied to products must strictly conform to the design requirements in section 1.2.6 "SVB Dynamic Voltage Scaling" in the latest version of *Hi35xx Vxxx Hardware Design User Guide*. HiSilicon shall not be responsible for any issues resulted from modified SVB circuit designs by users.

