



Hi3516C V500/Hi3516D V300/Hi3516A V300 High-Speed Signal Test Guide

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About This Document

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3516C	V500
Hi3516D	V300
Hi3516A	V300

Intended Audience

This document is intended for:

- Technical support personnel
- Software development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B02 (2019-01-15)

This issue is the second draft release, which incorporates the following changes:

Sections 1.3 and 2.3 are modified.

Issue 00B01 (2018-10-15)

This issue is the first draft release.



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1 Testing the USB 2.0 Host

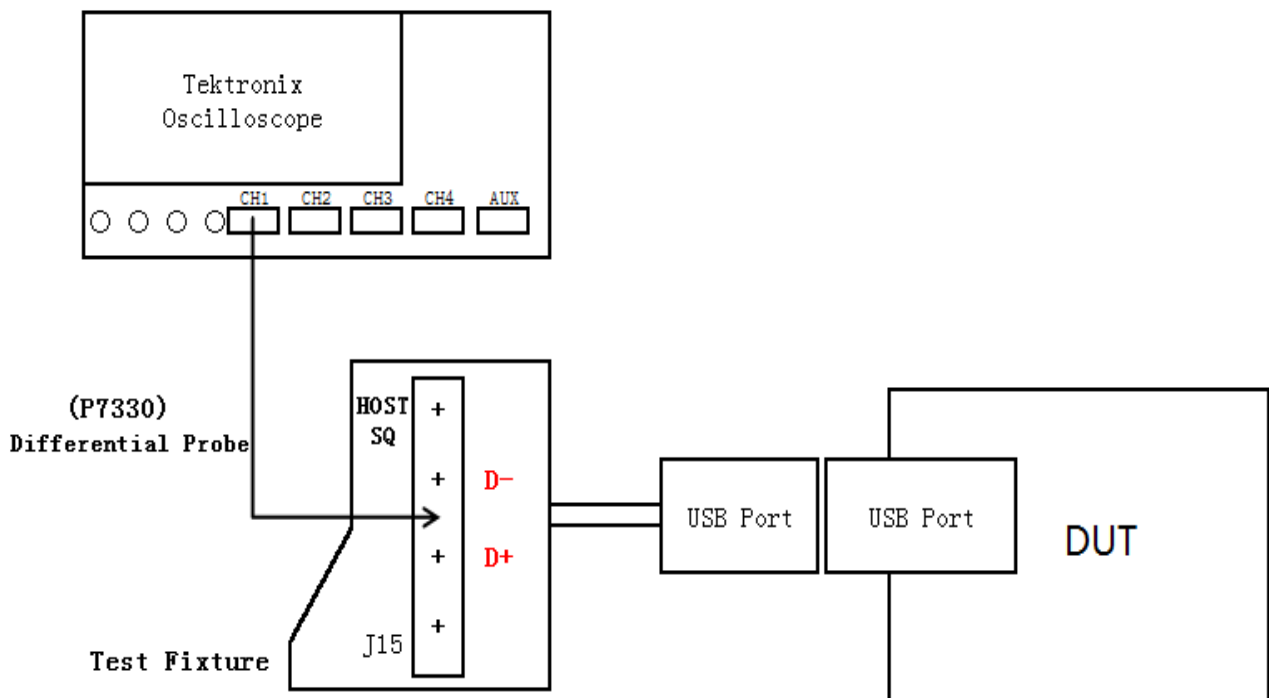
1.1 Test Tool

- Oscilloscope: Tektronix DSA72004C
- Differential probe: 3.5 GHz Tektronix (P7330 x 1)
- USB 2.0 test fixture

1.2 Test Networking

Figure 1-1 shows the test networking.

Figure 1-1 Test networking





NOTE

DUT is short for Device Under Test.

1.3 Test Register Configuration

//Test Packet

himm 0x100e0424 0x40000000



2 Testing TX Signals from the 100 Mbit/s Network Port

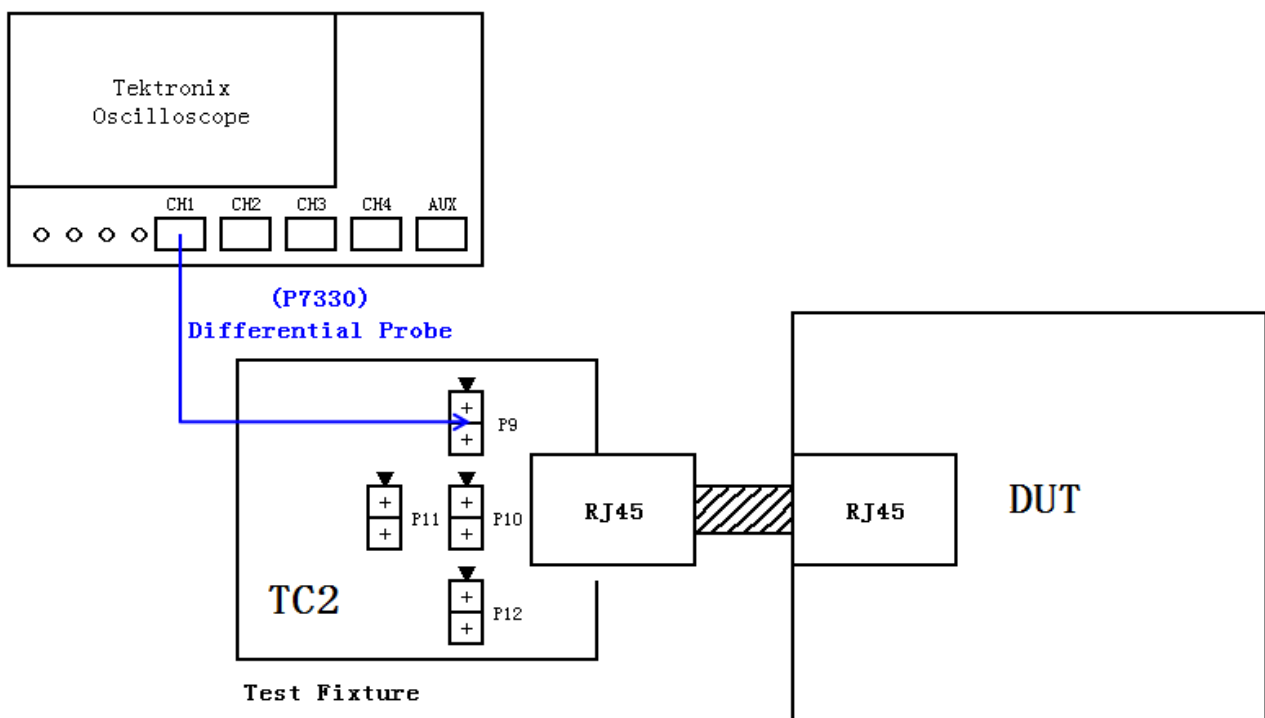
2.1 Test Tool

- Oscilloscope: Tektronix DSA72004C
- Differential probe: 3.5 GHz Tektronix (P7330 x 1)
- Fixture for testing the network port (TC2 module)

2.2 Test Networking

Figure 2-1 shows the test networking.

Figure 2-1 Test networking





NOTE

DUT is short for Device Under Test.

2.3 Test Register Configuration (RTL8201FI)

The PHY is forced to enter the megabit test mode. The configuration of related registers is provided by the PHY chip vendor.

Figure 2-2 Initialization setting

Initial setting :

Before all waveform (10/100M) measurement please set parameters as below:

Write Reg. 31 Data=0x0004

Write Reg. 16 Data=0x4077

Write Reg. 21 Data=0xC5A0

Write Reg. 31 Data=0x0000

Initialization:

himm 0x10011100 0x4211f;

himm 0x10011100 0x40772110;

himm 0x10011100 0xc5a02115;

himm 0x10011100 0x211f;



Figure 2-3 Register configuration for the 100M-TX test of the network port

100Mbps Test Mode Register:

Measuring From Channel A:

Write Reg. 0 Data=0x8000 (Reset PHY)

Write Reg. 24 Data=0x0310 (Disable ALDPS)

Write Reg. 28 Data=0x40C2 (Force MDI)

Write Reg. 0 Data=0x2100 (Force 100M/Full Duplex)

Measure channel A MLT3 Test

P.S: Channel A is the RJ45 pair 1, 2.

Measuring From Channel B:

Write Reg. 0 Data=0x8000 (Reset PHY)

Write Reg. 24 Data=0x0310 (Disable ALDPS)

Write Reg. 28 Data=0x40C0 (Force MDIX)

Write Reg. 0 Data=0x2100 (Force 100M/Full Duplex)

Measure channel B MLT3 Test

P.S: Channel B is the RJ45 pair 3, 6.

Configuration for testing: (Select channels as required)

//Channel A is the RJ45 pair 1, 2

himm 0x10011100 0x80002100;

himm 0x10011100 0x3102118;

himm 0x10011100 0x40c2211c;

himm 0x10011100 0x21002100;

//Channel B is the RJ45 pair 3, 6

himm 0x10011100 0x80002100;

himm 0x10011100 0x3102118;



himm 0x10011100 0x40c0211c;

himm 0x10011100 0x21002100;