Hi3516C V500 Hardware Design

User Guide

Cogobuy Only For ShenZhen FuBai ChanJing Industrial Technology Co., Ltd.

Issue 01

Date 2019-09-12

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About This Document

Purpose

This document describes the design recommendations for the schematic diagrams, printed circuit board (PCB), and board heat dissipation of Hi3516C V500.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3516C	V500

Intended Audience

This document is intended for:

- Technical support engineers
- Board hardware development engineers

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Change History

Changes between document issues are cumulative. The latest document issue contains all the changes made in earlier issues.

Issue 01 (2019-09-12)

This issue is the first official release, which incorporates the following changes:

In section 1.3.2.5, Table 1-12 and Table 1-13 are modified.

Issue 00B03 (2019-01-15)

This issue is the third draft release, which incorporates the following changes:

In section 1.1.1, Figure 1-1 is updated.

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Section 1.2.1 is modified.

Sections 1.4.3 and 1.5 are added.

Issue 00B02 (2018-10-15)

This issue is the second draft release, which incorporates the following changes:

Section 1.2.1, section 1.3.2.4, section 1.3.2.5, section 2.4, section 2.5, section 2.6, section 2.7, section 2.9, section 2.10, and section 2.11 are modified.

Issue 00B01 (2018-08-30)

This issue is the first draft release.

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1 Schematic Diagram Design

1.1 Requirements on External Circuits for Small System

1.1.1 Clocking Circuit

The system clock circuit can be generated by combining the internal feedback circuit of Hi3516C V500 with a 24 MHz external crystal oscillator circuit.

Figure 1-1 shows the recommended connection mode of the crystal oscillator.

NOTICE

The selected capacitors must match the load capacitor of the crystal oscillator, and the NPO capacitors are recommended. You are advised to select the 4-pin surface mount device (SMD) crystal oscillator and fully connect its two GND pins to the board GND to improve the anti-ESD interference capability of the system clock.

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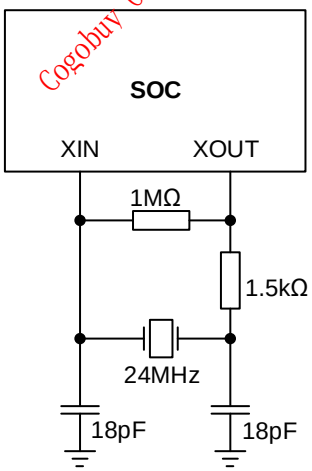
Figure 1-1 Crystal oscillator circuit



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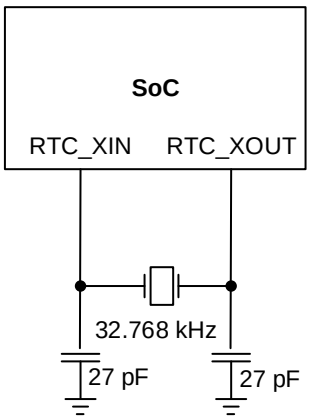
Hi3516C V500 integrates a real-time clock (RTC), for which the board must provide a clock circuit. Figure 1-2 shows the connection mode of the RTC crystal oscillator and component parameters.

Figure 1-2 Connection mode of the RTC crystal oscillator and component parameters



The restriction on the model selection of the RTC crystal oscillator is described as follows:

The internal resistance of the crystal oscillator does not exceed 75 kilohms.

NOTE

- The capacitance of the capacitors must match the load capacitance of the actual crystal oscillator. The frequency deviation is 30 ppm. The inherent load capacitance varies according to the brand and model of the crystal oscillator.
- If the system 24 MHz clock or RTC clock uses the active crystal, which is input from the XIN pin or the RTC_XIN pin, float the XOUT or RTC_XOUT pin.

1.1.2 Reset Circuit

- Hi3516C V500 supports power-on reset (POR) and does not support external reset.
- After the master chip is powered on, the internal POR circuit is used to reset the entire chip (the pulse width of the reset signal is about 32 ms).
- You are advised to use the reset signal output by the M2 pin (SYS_RSTN_OUT) of Hi3516C V500 to reset the peripherals related to the small system (such as the boot flash memory). SYS_RSTN_OUT connects to a 1 kilohm pull-down resistor.
- The level of the SYS_RSTN_OUT signal is consistent with that of DVDD3318_FLASH (L4 pin of Hi3516C V500).

NOTICE

Peripherals related to the small system (such as the boot flash memory) must release the reset signal before Hi3516C V500 or they release the reset signals simultaneously to ensure that the system boots properly. Otherwise, exceptions such as system boot failure may occur.

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1.1.3 JTAG Interface

Table 1-1 describes the signals of the JTAG interface.

Table 1-1 Signals of the JTAG interface

Signal	Description
TCK	JTAG clock input. This signal must connect to a 1-kilohm external pull-down resistor on the board.
TDI	JTAG data input. This signal must connect to a 4.7-kilohm external pull-up resistor on the board.
TMS	JTAG mode select input. This signal must connect to a 4.7-kilohm external pull-up resistor on the board.
TRSTN	JTAG reset input. To ensure that Hi3516C V500 works properly, this signal must connect to a 10-kilohm external pull-down resistor on the board.
TDO	JTAG data output. This signal must connect to a 4.7-kilohm external pull-up resistor on the board.

Hi3516C V500 can be set to normal mode or test mode by configuring the TEST_MODE pin. For details, see Table 1-2.

Table 1-2 TEST_MODE pin configuration

TEST_MODE	Description
0	Hi3516C V500 works in normal mode.
1	Hi3516C V500 works in test mode. The test mode is not used by the actual product.

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Figure 1-3 shows the JTAG connection mode and standard connector pins.

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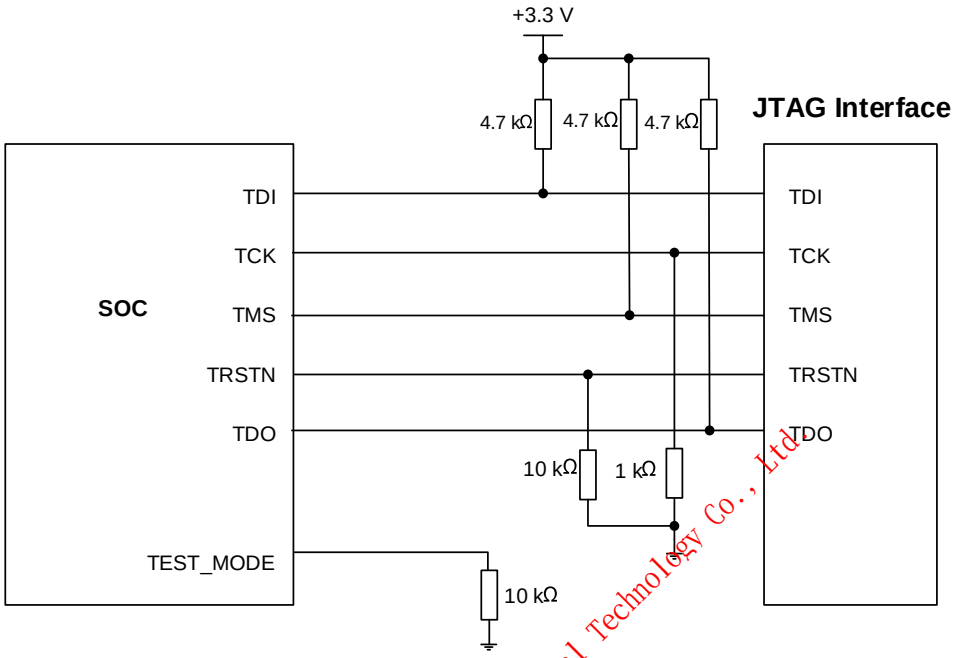
Figure 1-3 JTAG connection mode



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1.1.4 PMC

1.1.4.1 Interface Introduction

The power management control (PMC) module can enable or disable the power module in the non-always-on area and receive the key-pressing signal/rising edge signal to control the power on or power off state and wakeup signals from peripherals to implement the standby and wakeup functions.

For details about the functions and power-on/power-off logic of this module, see section 3.10 "Power Management and Low-Power Mode Control" in the *Hi3516C V500 Professional Smart IP Camera SoC Data Sheet*.

1.1.4.2 Circuit Design

The pins for supplying power of the PMC module are AVDD_BAT and DVDD3318_PC.

- AVDD_BAT: power supply of the RTC module. The voltage ranges from 1.6 V to 3.6 V. When modules in the always-on area are used, this pin must be connected to the battery or other non-power-off power.
- DVDD3318_PC: 1.8 V or 3.3 V power of the PMC always-on area.

In the hardware design of PMC module, pay attention to the following pins:

- PWR_RSTN: reset pin of the PMC module, active low. An RC reset circuit must be designed on the pin. For details about the resistor and capacitor selection, see the HI3516CV500DMEB schematic diagram design document.
- When the PMC module is used to implement the standby and wakeup function of Hi3516C V500, the working clock of the PMC module sources from the RTC module. Therefore, when the PMC module is used, the RTC module must be used for power supply and the RTC circuit must be designed properly.

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- PWR_BUTTON connects to the power key, PWR_STARTUP triggers startup on the rising edge, PWR_SEQ0 is used to enable the controlled DC-DC or LDO, and PWR_WAKEUP is used to receive the wakeup signal.

1.1.4.3 Power Supply Scheme for the RTC and PMC in Standby Mode

In different standby states, the RTC and PMC have the following combinations. For details about the power supply solutions in different combinations, see Table 1-3.

Table 1-3 Power supply solutions for the RTC and PMC in different standby states

Solution No.	Operating Status		Processing Mode of Power Pins	
	RTC	PMC/GPIO	AVDD_BAT	DVDD3318_PC
Solution 1	Not used	Not used	Floated	DVDD3318_PC connects to the 1.8 V or 3.3 V digital power.
Solution 2	Not used	Used GPIO	Floated	DVDD3318_PC connects to the 1.8 V or 3.3 V digital power.
Solution 3	Used	Not used	AVDD_BAT connects to the battery (the voltage does not exceed 3.6 V) or other always-on power supplies.	DVDD3318_PC connects to the 1.8 V or 3.3 V digital power.
Solution 4	Used	Used GPIO	AVDD_BAT connects to the battery (the voltage does not exceed 3.6 V) or other always-on power supplies.	DVDD3318_PC connects to the 1.8 V or 3.3 V digital power.
Solution 5	Used	Used PMC	AVDD_BAT and DVDD3318_PC connect to 1.8 V or 3.3 V always-on power supplies.	

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In Table 1-3:

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- Solution 1 and solution 3: PWR_BUTTON, PWR_RSTN, PWR_SEQ0, PWR_STARTUP, and PWR_WAKEUP can be floated.
- Solution 2 and solution 4: PWR_BUTTON, PWR_RSTN, and PWR_STARTUP can be floated.
- Solution 5: When the PMC function is used, the RTC circuit must be designed properly.

1.1.5 System Configuration Circuit for Hi3516C V500 Hardware Initialization

The working mode of each module is configured based on the pull-up and pull-down resistor status of configuration pins during the Hi3516C V500 initialization. Table 1-4 describes hardware configuration signals.

Table 1-4 Hardware configuration signals

Signal	Direction	Description
TEST_MODE	I	Mode select 0: functional mode 1: test mode
BOOT_SEL[1:0]	I	Boot source select 00: booting from the NOR/NAND flash 01: booting from the eMMC 10: fast boot. The SPI NOR/NAND flash memory is burnt over the serial port. 11: fast boot. The eMMC is burnt over the serial port.
SFC_DEVICE_MODE	I	SPI flash select 0: SPI NOR flash 1: SPI NAND flash
SFC_BOOT_MODE	I	Boot mode select of the SPI NOR flash memory when BOOT_SEL[1:0] is **00** and SFC_DEVICE_MODE is **0**. 0: 3-byte address mode 1: 4-byte address mode Boot mode select of the SPI NAND flash memory when BOOT_SEL[1:0] is **00** and SFC_DEVICE_MODE is **1**. 0: 1-wire I/O boot mode 1: 4-wire I/O boot mode
UPDATE_MODE	I	SDIO0 and USB burning function enable 0: enabled 1: disabled **Note: After the SDIO0 and USB burning function is enabled, the boot mode specified by BOOT_SEL[1:0] and SFC_DEVICE_MODE does**

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Signal	Direction	Description
		not take effect. When the chip is started during power-on, it detects whether an SD card or USB flash drive exists on the SDIO0 interface. If yes, the boot stored in the SD card or USB flash drive is burnt to the boot medium specified by BOOT_SEL[1:0] and SFC_DEVICE_MODE. **SDIO1 does not support this function.**

NOTICE

Some of the system configuration pins listed in Table 1-4 are multiplexed with RMII, sensor, or SFC pins. If these configuration pins connect to pins of the peripherals, pull-up and pull-down resistors must be designed for the configuration pins to determine their initial states. The recommended value is 4.7 kilohms.

1.1.6 DDR SDRAM Circuit Design

1.1.6.1 Introduction

- The Hi3516C V500 DDRC interface supports the DDR3(L)/DDR4 SDRAM.
- Hi3516C V500 has one DDRC, and can be connected to one piece of 16-bit DDR3(L)/DDR4 SDRAM.
- For details about the specifications, see section 4.1 "DDRC" in the *Hi3516C V500 Professional Smart IP Camera SoC Data Sheet*.

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1.1.6.2 DDR SDRAM Topology

To facilitate PCB layout, different wire sequences are used for connecting 16-bit DDR3(L)/DDR4 SDRAMs. For details about the pin swap information, see Table 1-5.

Table 1-5 Pin swap information

Pin ID	Pin name	Signal Name		
		DDR3(L) on 4-Layer PCB	DDR3(L) on 2-Layer PCB	DDR4 on 4-Layer PCB
A5	DDR_A0	DDR_A0	DDR_A0	DDR4_A15
A6	DDR_A1	DDR_A1	DDR_A1	DDR4_BA1
B7	DDR_A2	DDR_A2	DDR_A2	DDR4_A1
B5	DDR_A3	DDR_A3	DDR_A3	DDR4_A10
A7	DDR_A4	DDR_A4	DDR_A4	DDR4_A5
B6	DDR_A5	DDR_A5	DDR_A5	DDR4_A3
A8	DDR_A6	DDR_A6	DDR_A6	DDR4_A9

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Pin ID	Pin name	Signal Name		
		DDR3(L) on 4-Layer PCB	DDR3(L) on 2-Layer PCB	DDR4 on 4-Layer PCB
B9	DDR_A7	DDR_A7	DDR_A7	DDR4_A7
A9	DDR_A8	DDR_A8	DDR_A8	DDR4_A13
B8	DDR_A9	DDR_A9	DDR_A9	DDR4_A6
C4	DDR_A10	DDR_A10	DDR_A10	DDR4_ACT_N
C8	DDR_A11	DDR_A11	DDR_A11	DDR4_A8
C7	DDR_A12	DDR_A12	DDR_A12	DDR4_A16
C9	DDR_A13	DDR_A13	DDR_A13	DDR4_A11
D9	DDR_A14	DDR_A14	DDR_A14	DDR4_A2
C6	DDR_A15	DDR_A15	DDR_A15	DDR4_A0
A4	DDR_BA0	DDR_BA0	DDR_BA0	DDR4_A4
C5	DDR_BA1	DDR_BA1	DDR_BA1	DDR4_BA0
B4	DDR_BA2	DDR_BA2	DDR_BA2	DDR4_BG0
A2	DDR_CASN	DDR_CASN	DDR_CASN	DDR4_A14
B1	DDR_RASN	DDR_RASN	DDR_RASN	DDR4_A12
C3	DDR_WEN	DDR_WEN	DDR_WEN	-
B2	DDR_CKE	DDR_CKE	DDR_CKE	DDR4_CKE
A3	DDR_CSN	DDR_CSN	DDR_CSN	DDR4_CSN
B3	DDR_ODT	DDR_ODT	DDR_ODT	DDR4_ODT
C10	DDR_RESETN	DDR_RESETN	DDR_RESETN	DDR4_RESETN
B10	DDR_ZQ	DDR_ZQ	DDR_ZQ	DDR4_ZQ
D1	DDR_DQ0	DDR_DQ6	DDR_DQ6	DDR4_DQ6
D3	DDR_DQ1	DDR_DQ4	DDR_DQ7	DDR4_DQ2
E2	DDR_DQ2	DDR_DQ2	DDR_DQ3	DDR4_DQ0
E1	DDR_DQ3	DDR_DQ0	DDR_DQ2	DDR4_DQ4
E3	DDR_DQ4	DDR_DQ7	DDR_DQ5	DDR4_DQ7
F3	DDR_DQ5	DDR_DQ5	DDR_DQ0	DDR4_DQ3
G1	DDR_DQ6	DDR_DQ1	DDR_DQ4	DDR4_DQ5
H2	DDR_DQ7	DDR_DQ3	DDR_DQ1	DDR4_DQ1
J3	DDR_DQ8	DDR_DQ12	DDR_DQ11	DDR4_DQ11

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Pin ID	Pin name	Signal Name		
		DDR3(L) on 4-Layer PCB	DDR3(L) on 2-Layer PCB	DDR4 on 4-Layer PCB
K2	DDR_DQ9	DDR_DQ13	DDR_DQ15	DDR4_DQ8
K1	DDR_DQ10	DDR_DQ11	DDR_DQ12	DDR4_DQ12
K3	DDR_DQ11	DDR_DQ10	DDR_DQ13	DDR4_DQ13
L3	DDR_DQ12	DDR_DQ14	DDR_DQ9	DDR4_DQ9
L2	DDR_DQ13	DDR_DQ9	DDR_DQ10	DDR4_DQ14
L1	DDR_DQ14	DDR_DQ15	DDR_DQ14	DDR4_DQ10
M1	DDR_DQ15	DDR_DQ8	DDR_DQ8	DDR4_DQ15
H3	DDR_DM0	DDR_DM0	DDR_DM0	DDR4_DM0
G3	DDR_DM1	DDR_DM1	DDR_DM1	DDR4_DM1
F1	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR4_DQS0_N
F2	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR4_DQS0_P
J2	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR4_DQS1_N
J1	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR4_DQS1_P
C1	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR4_CLK_N
C2	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR4_CLK_P

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NOTICE

The DDR3(L) layout and trace routing on the 2-layer PCB must be the same as that of the HI3516CV500DMEBLITE, the DDR3(L) layout and trace routing on the 4-layer PCB must be the same as that of the HI3516CV500DMEB, and the DDR4 layout design on the 4-layer PCB must be the same as that of the HI3516CV500DDR4DMEB. For details about the design, see the hardware documents in the release package.

1.1.6.3 Design Recommendations for Matched Modes

Bidirectional DQ and DQS Signals

The DQ, DQS_P, and DQS_N signals of Hi3516C V500 connect directly to the DQ, DQS_P, and DQS_N signals of the DDR SDRAM respectively.

Differential Clocks

When Hi3516C V500 connects to DDR3(L)/DDR4 SDRAMs, DDR_CLK_N/P uses the one-drive-one topology, and connects to a 100-ohm capacitor near the SDRAM, as shown in Figure 1-5.

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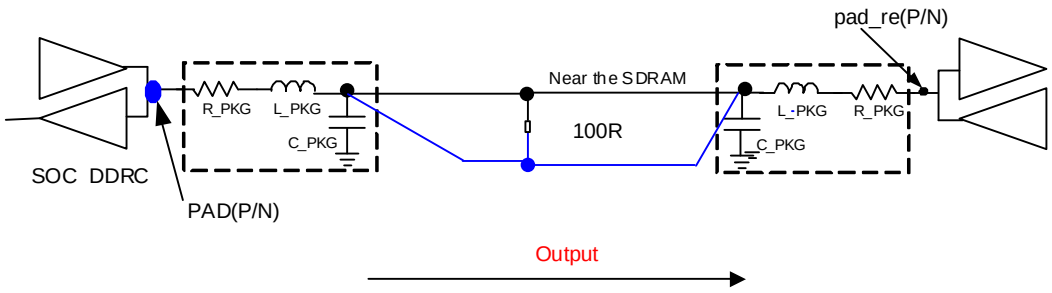
Figure 1-5 One-drive one mode applied to the differential clock signals of DDR3(L)/DDR4 SDRAM



1.1.6.4 Address Signals and Command Signals

In the Hi3516C V500 DDR SDRAM application:

- When the 4-layer PCB is designed to connect to a 16-bit DDR3(L)/DDR4 SDRAM, connect the DDR_CS_N and DDR_ODT pins according to the Thevenin's theorem. Other address and command signals can be directly connected.
- When the 2-layer PCB is designed to connect to a 16-bit DDR3(L) SDRAM, all address and command signals are connected to the 33-ohm resistor in series close to the SoC.

1.1.6.5 DM Signals

In the DDR SDRAM applications, DM0/DM1 signals are connected in point-to-point mode. Therefore, you only need to directly connect them.

1.1.6.6 External Resistor for the DDR SDRAM

The 240-ohm±1% external resistor (ZQ) is selected.

1.1.7 Schematic Diagram Design of the Flash

1.1.7.1 Introduction

The flash controller supports the SPI NOR flash, SPI NAND flash, and eMMC.

1.1.7.2 Signal Processing

Design of the SPI Flash Memory

The 4-layer PCB design and 2-layer PCB design differ from each other in the match of SPI flash memories.

For the 4-layer PCB design, Table 1-6 shows the recommended SPI flash match design, and Figure 1-4 shows the recommended connection mode.

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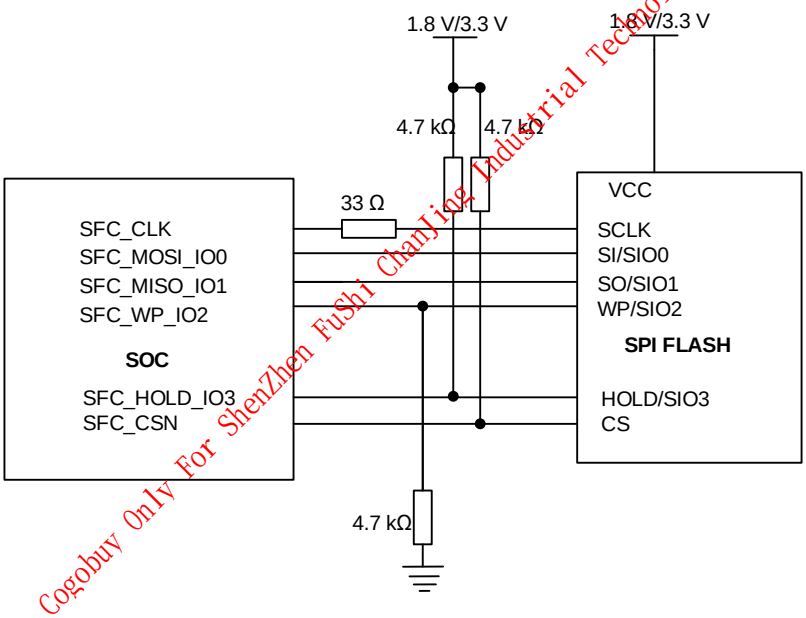
Table 1-6 SPI flash match design method for 4-layer PCB design

Signal	Design Method
SFC_CLK	In one-drive-one mode, the Hi3516C V500 source end is connected to a 33-ohm resistor in series. The signal trace length cannot be greater than 3 inches.
SFC_MOSI_IO0 SFC_MISO_IO1 SFC_WP_IO2 SFC_HOLD_IO3 SFC_CSN	The signals are connected directly. You are advised to connect a 4.7-kilohm pull-down resistor to SFC_WP_IO2 and 4.7-kilohm pull-up resistors to SFC_HOLD_IO3 and SFC_CSN. In one-drive-one mode, when the signal trace length is less than or equal to 1.5 inches, the signals are connected directly; when the signal trace length is greater than 1.5 inches and less than 3 inches, a 33-ohm resistor is connected in series at the source end.

Figure 1-4 Diagram of SPI flash connection on the 4-layer PCB



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For the 2-layer PCB design, Table 1-7 shows the recommended SPI flash match design, and Figure 1-5 shows the recommended connection mode.

Table 1-7 SPI flash match design method for 2-layer PCB design

Signal	Design
SFC_CLK	In one-drive-one mode, the Hi3516C V500 source end is connected to a 51-ohm resistor in series. The signal trace length cannot be greater than 3 inches.

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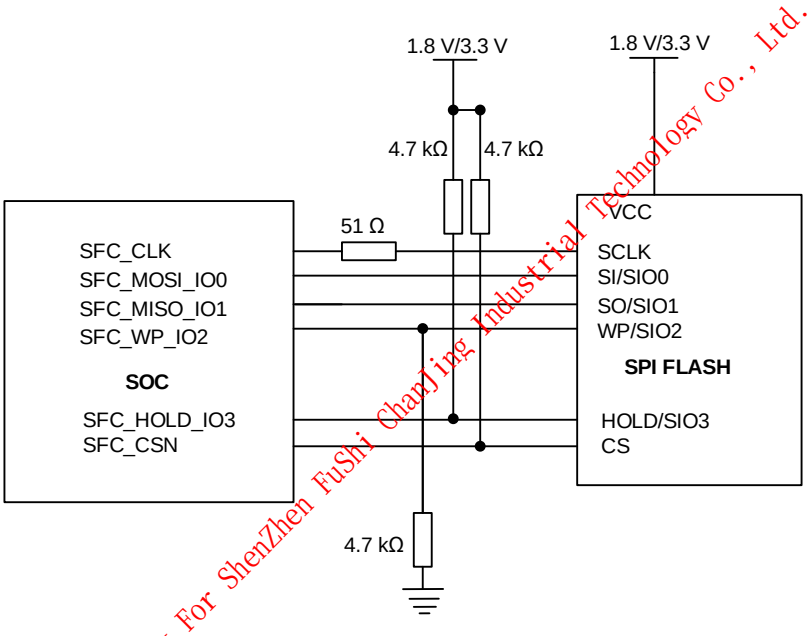
Signal	Design
SFC_MOSI_IO0 SFC_MISO_IO1 SFC_WP_IO2 SFC_HOLD_IO3 SFC_CSN	The signals are connected directly. You are advised to connect a 4.7-kilohm pull-down resistor to SFC_WP_IO2 and 4.7-kilohm pull-up resistors to SFC_HOLD_IO3 and SFC_CSN. In one-drive-one mode, when the signal trace length is less than or equal to 1.5 inches, the signals are connected directly; when the signal trace length is greater than 1.5 inches and less than 3 inches, a 51-ohm resistor is connected in series at the source end.

Figure 1-5 Diagram of SPI flash connection on the 2-layer PCB



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The SPI flash with the reset function is recommended. If the SPI flash does not have the reset function, the system may fail to restart because the SPI flash cannot be reset synchronously when the watchdog of the master chip takes effect and resets the system.

Matched Design of eMMC Signals

The 4-layer PCB design and 2-layer PCB design differ from each other in the match of eMMC flash memories.

- Figure 1-6 shows the eMMC connection on the 4-layer PCB.

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Figure 1-6 Diagram of eMMC connection on the 4-layer PCB

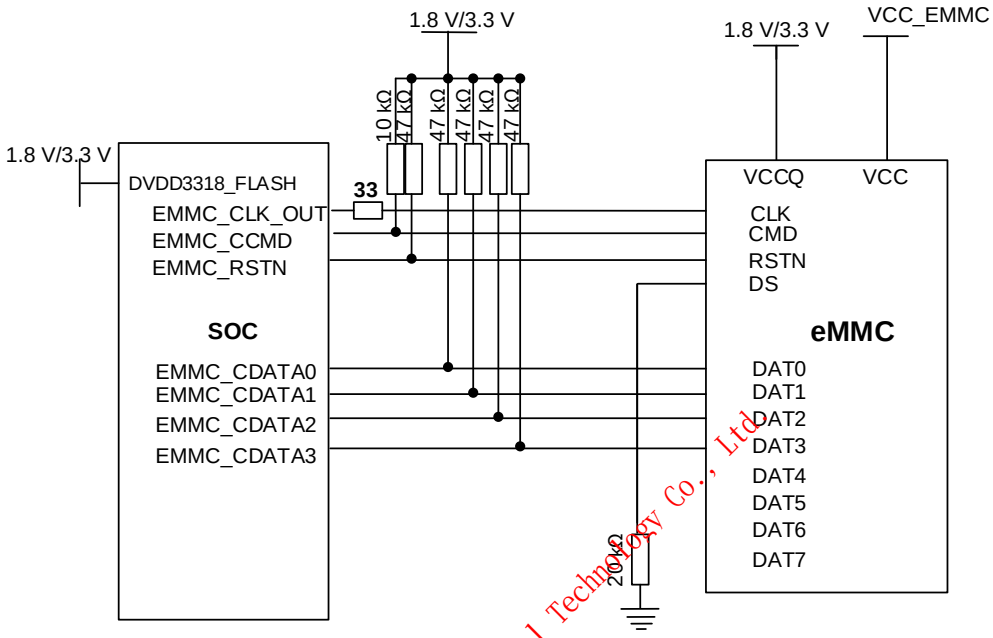

Table 1-8 describes the recommended match design.

Table 1-8 Recommended match design when the external eMMC is connected

Signal	Design
EMMC_CLK	The signal is connected to a 33-ohm resistor in series at the Hi3516C V500 end. The signal trace length cannot be greater than 2.5 inches.
EMMC_DATA[0:3]	The signal is directly connected, and you are advised to connect a 47-kilohm pull-up resistor to it. The signal trace length cannot be greater than 2.5 inches.
EMMC_CMD	The signal is directly connected, and you are advised to connect a 10-kilohm pull-up resistor to it. The signal trace length cannot be greater than 2.5 inches.
EMMC_RST_N	The signal is directly connected, and you are advised to connect a 47-kilohm pull-up resistor to it.

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- Figure 1-7 shows the eMMC connection on the 2-layer PCB.

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Figure 1-7 Diagram of eMMC connection on the 2-layer PCB

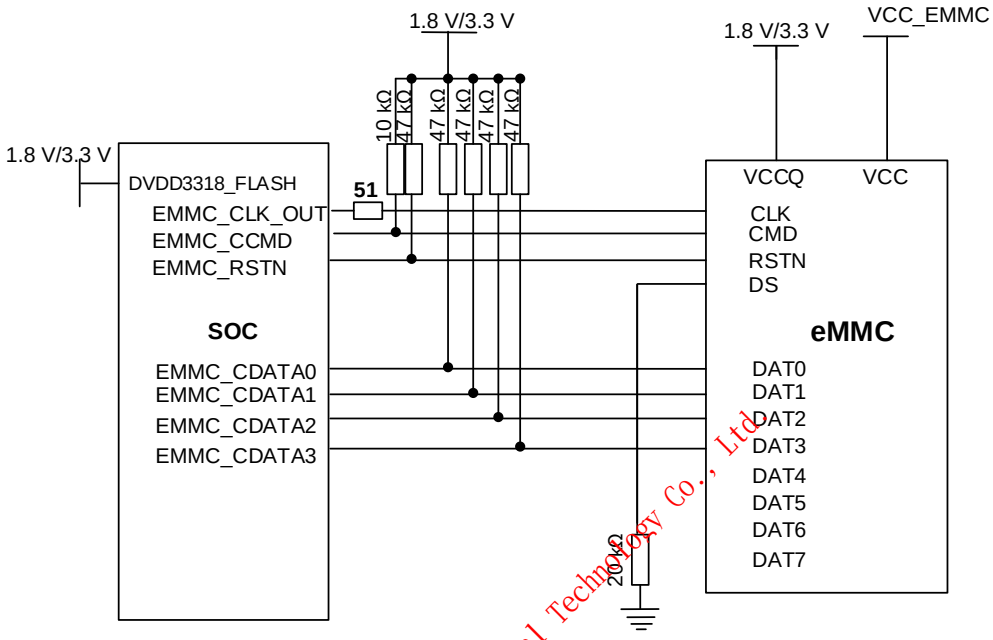

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Table 1-9 describes the recommended match design.

Table 1-9 Recommended match design when the external eMMC is connected

Signal	Design
EMMC_CLK	The signal is connected to a 51-ohm resistor in series at the Hi3516C V500 end. The signal trace length cannot be greater than 2.5 inches.
EMMC_DATA[0:3]	The signal is directly connected, and you are advised to connect them to 47-kilohm pull-up resistors. The signal trace length cannot be greater than 2.5 inches.
EMMC_CMD	The signal is directly connected, and needs to connect to a 10-kilohm pull-up resistor. The signal trace length cannot be greater than 2.5 inches.
EMMC_RST_N	The signal is directly connected, and needs to connect to a 47-kilohm pull-up resistor.

NOTICE

The EMMC_RST_N pin is multiplexed with the SYS_RST_N pin. When the EMMC_RST_N function is used, other GPIO pins are used to reset peripherals.

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1.2 Design Recommendations on the Power Supply

For details about the power supply design parameters for Hi3516C V500, see section 2.5 "Electrical Specifications" in the *Hi3516C V500 Professional Smart IP Camera SoC Data Sheet*.

For the power design of Hi3516C V500, the capacitance and quantity of the capacitors on the 2-layer PCB must completely follow the schematic diagram of the HI3516CV500DMEBLITE. The capacitance and quantity of the capacitors on the 4-layer PCB must completely follow the schematic diagram of the HI3516CV500DMEB.

1.2.1 Core Power Design

For the Hi3516C V500 core power supply DVDD, the typical voltage is 0.9 V, and the actual voltage is controlled by the selective voltage binning (SVB) dynamic voltage scaling circuit. For details, see the latest HI3516CV500DMEB schematic diagram. The power supply capability of the power chip must be no less than 3 A. You are advised to use the DC-DC that supports the COT mode.

This power supply requires that the ripple and noise be controlled within ±38mV at the pins of the chip.

1.2.2 DDR SDRAM Power Design

- Hi3516C V500 supports the DDR3(L)/DDR4 SDRAM, typical voltages of 1.5 V(1.35 V) and 1.2 V, and reference voltage (Vref) of VDDIO_DDR/2. The power supply of the DDR SDRAM must be the same as that of the DDR I/O power supply of Hi3516C V500.
- An independent power chip needs to be used on the board to supply power to the DDR SDRAM, and the DDR SDRAM I/O power pins of Hi3516C V500 (VDDIO_DDR).
- The DDR SDRAM phase-locked loop (PLL) power (pin name: AVDD33_DDR_PLL) connects to the 3.3 V power. The power must be isolated from the 3.3 V digital power of the master chip by using the 1 kilohm@100 MHz electromagnetic interference (EMI) bead
- The CK power supply (pin name: VDDIO_DDR_CK) of the master chip DDRIO must be isolated from the VDDIO_DDR power by using the 1 kilohm@100 MHz EMI bead.
- The power for Vref of the DDR SDRAM is obtained after voltage division by using the 1 kilohm±1% resistor.
- The Vref power of the Hi3516C V500 master chip is integrated, and therefore no external design is required.
- The DCDC with the fixed PWM mode must be used.

Figure 1-8 shows the reference design of the DDR4 SDRAM power voltage-division network.

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Figure 1-8 Reference design of the DDR4 SDRAM power voltage-division network

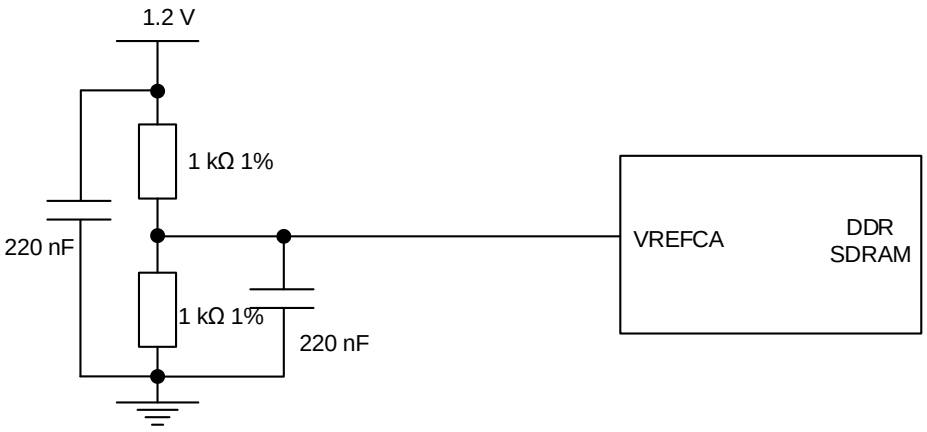
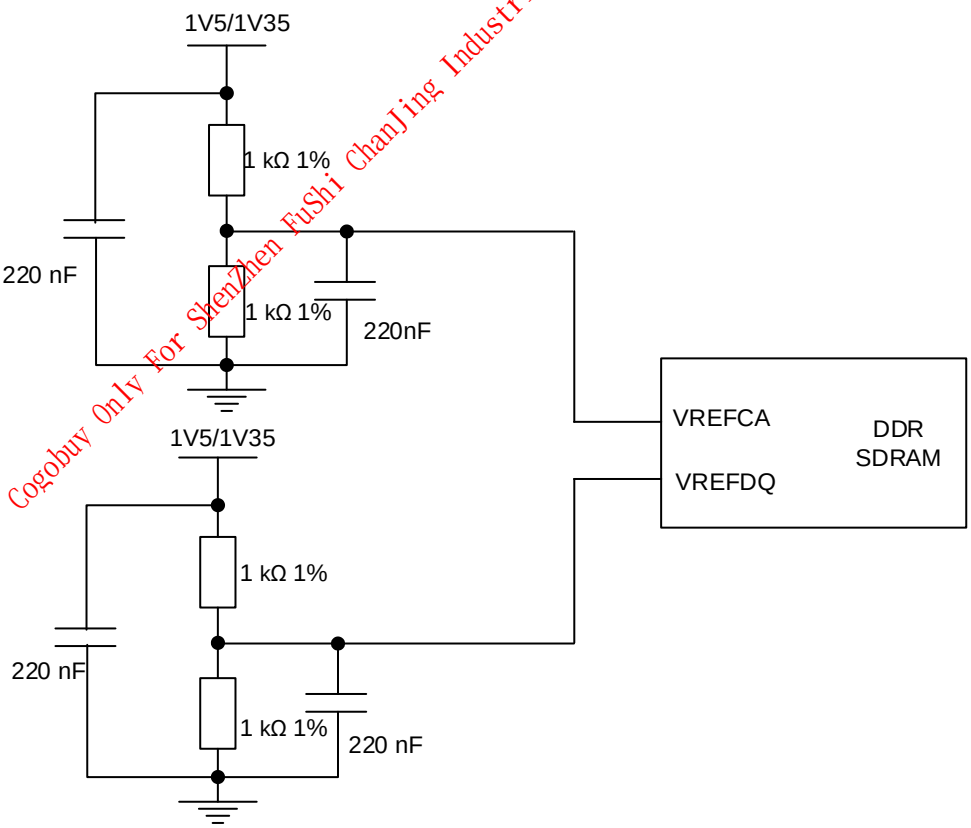


Figure 1-9 shows the reference design of the DDR3(L) Vref power.

Figure 1-9 Reference design of the DDR3(L) power voltage-division circuit



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The DDR4 SDRAM requires the 2.5 V power supply VPP. The VPP power must be turned on before the 1.2 V VDD power or the two power supplies are turned on simultaneously. Besides, the amplitude of the VPP power must always be greater than or equal to that of the 1.2 V VDD power.

1.2.3 I/O Power Design

- The I/O power pins (DVDD33) connect to the 3.3 V digital power. You are advised to use the DC-DC in **fixed PWM mode**.
- The I/O power pins (DVDD3318_FLASH) of the flash interface support the 3.3 V or 1.8 V level. The level of the connected power must be the same as the interface level of the connected chip.
- The I/O power (DVDD3318_SENSOR) of the sensor clock, reset, and configuration pins support the 3.3 V or 1.8 V power. The level of the connected power must be the same as the interface level of the connected chip.
- The mobile industry processor interface (MIPI)/low-voltage differential signaling (LVDS) interface power pins (AVDD3318_MIPI) support the 3.3 V or 1.8 V power.

  The MIPI/LVDS pins of Hi3516C V500 can be multiplexed as the parallel data function and support the 3.3 V or 1.8 V level. The level of the connected power must be the same as the interface level of the connected chip.
  - When the MIPI or LVDS module is used, AVDD3318_MIPI must connect to the 1.8 V power.
  - When the MIPI/LVDS pins are multiplexed as the parallel data function, AVDD3318_MIPI must connect to the 3.3 V or 1.8 V power.
- The power pins of the video input (VI) interface (DVDD3318_VI) support the 3.3 V or 1.8 V power.

  The VI pins of Hi3516C V500 can be multiplexed as the parallel data function, and form a 16-bit BT.1120 input interface with the parallel data interface multiplexed by the MIPI/LVDS pins, or form an input interface that supports up to 14-bit parallel data. The level of the connected power must be the same as the interface level of the connected chip.
  - The VI pin can be independently multiplexed as the VI BT.656 interface.
  - The VI pin can be independently multiplexed as the VO BT.656 interface.
- The power pin of the UART1 interface (DVDD3318_UART1) supports the 3.3 V or 1.8 V power.
- The power pin of the SDIO1 interface (DVDD3318_SDIO1) supports the 3.3 V or 1.8 V power.
- The always-on area power pin (DVDD3318_PC) supports the 3.3 V or 1.8 V power.

1.2.4 PLL Power Design

Hi3516C V500 has two PLL power supplies:

- AVDD09_PLL: This power supply must be isolated from the DVDD power by using the 1 kilohm@100 MHz EMI bead.
- AVDD33_PLL: This power supply must be isolated from the 3.3 V digital power by using the 1 kilohm@100 MHz EMI bead

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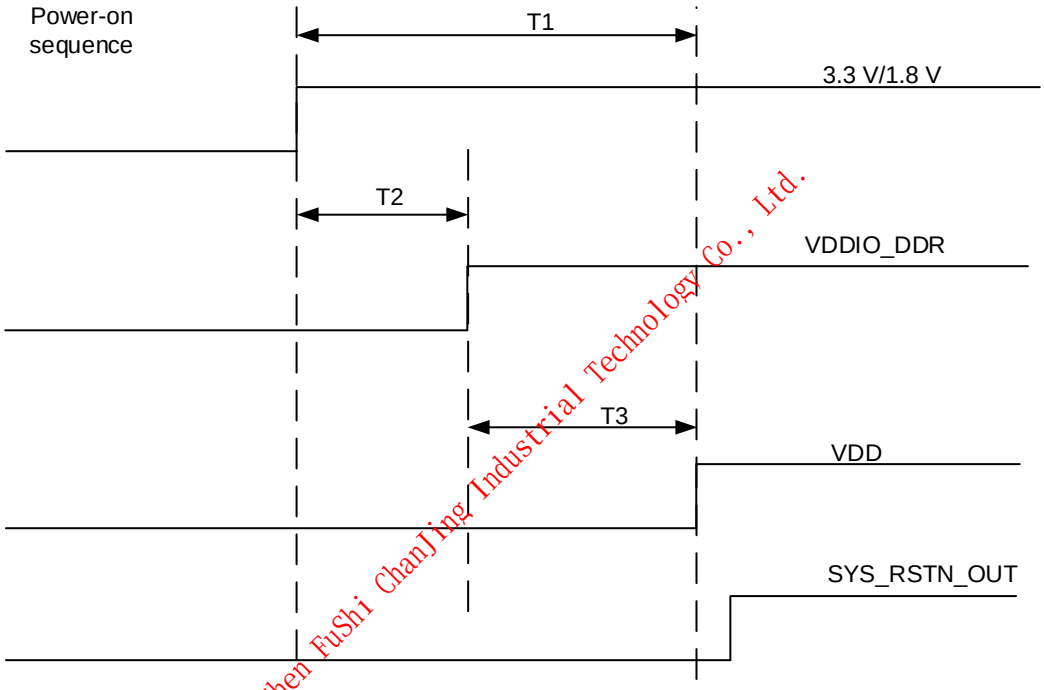
For details about the circuit design, see the schematic diagram of the Hi3516C V500 demo board.

1.2.5 Power-On and Power-Off Sequences

Figure 1-10 and Figure 1-11 show the requirements on the power-on and power-off sequences of the core power supplies, DDR power supplies, and I/O power supplies, respectively.

Figure 1-10 Power-on sequence diagram



$0 < T1 \leq 10$ ms, $T2 \geq 0$ ms, $T3 > 0$ ms. The 3.3 V/1.8 V power, DDRIO power, and core power are turned on in sequence.

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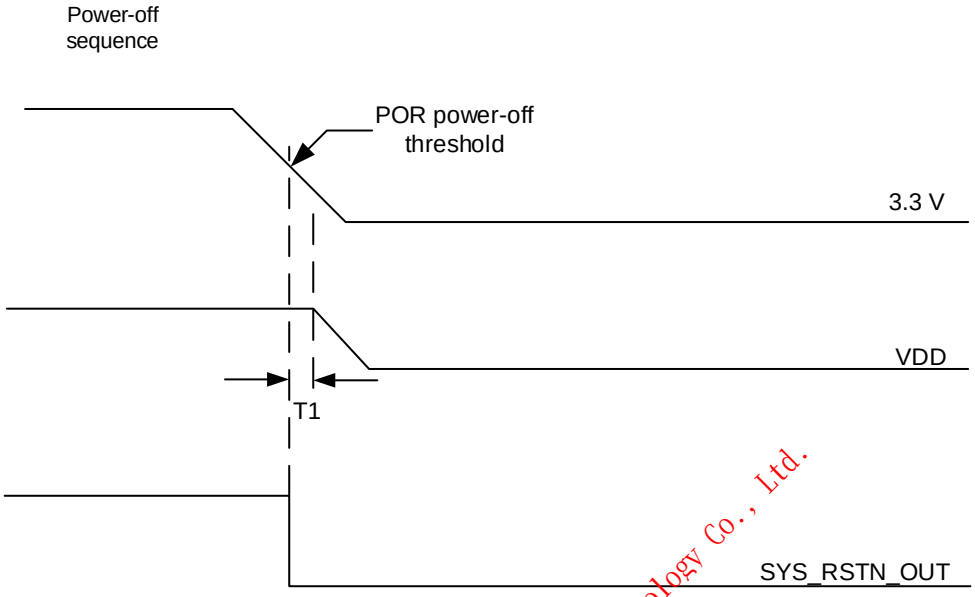
Figure 1-11 Power-off sequence diagram



T1 > 0. During power-off, 3.3 V/1.8 V is powered off first. When the level of the 3.3 V power is decreased to the POR threshold (2.1 V), a POR reset is triggered. Then, the core powers can be powered off.

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The power pins corresponding to the POR module are DVDD33 pins (D14, M15, and P4).

The power-on threshold of the POR is 2.6 V, and the power-off threshold of the POR is 2.1 V. During power-down, the POR works in any of the following modes:

- When the DVDD33 voltage decreases from 3.3 V to 2.6 V, sequence starts. At 5 us, if the DVDD33 voltage is greater than 2.6 V, the POR does not trigger a reset, and the SYS_RSTN_OUT pin maintains high.
- When the DVDD33 voltage decreases from 3.3 V to 2.6 V, sequence starts. At 5 us, if the DVDD33 voltage is greater than 2.1 V and less than or equal to 2.6 V, the POR triggers a reset, and the SYS_RSTN_OUT pin is at low level.
- When the DVDD33 voltage decreases from 3.3 V to 2.6 V, sequence starts. Within 5 us, if the DVDD33 voltage is less than or equal to 2.1 V, the POR triggers a reset, and the SYS_RSTN_OUT pin is at low level.

1.2.6 SVB Dynamic Voltage Scaling

The dynamic voltage scaling function must be added to the core power supplies of Hi3516C V500. The implementation method is as follows:

Transmit the signal from the PWM waveform output pins (SVB_PWM). The pins output the DC levels ranging from 0 V to 3.3 V after RC filtering. The DC levels are overlapped at the input end of the DC-DC feedback voltage through the resistor network to implement DC-DC output voltage scaling. Then adjust the PWM frequency and duty cycle by configuring related registers of Hi3516C V500. In this way, the DC-DC output voltage is dynamically scaled. See Figure 1-12.

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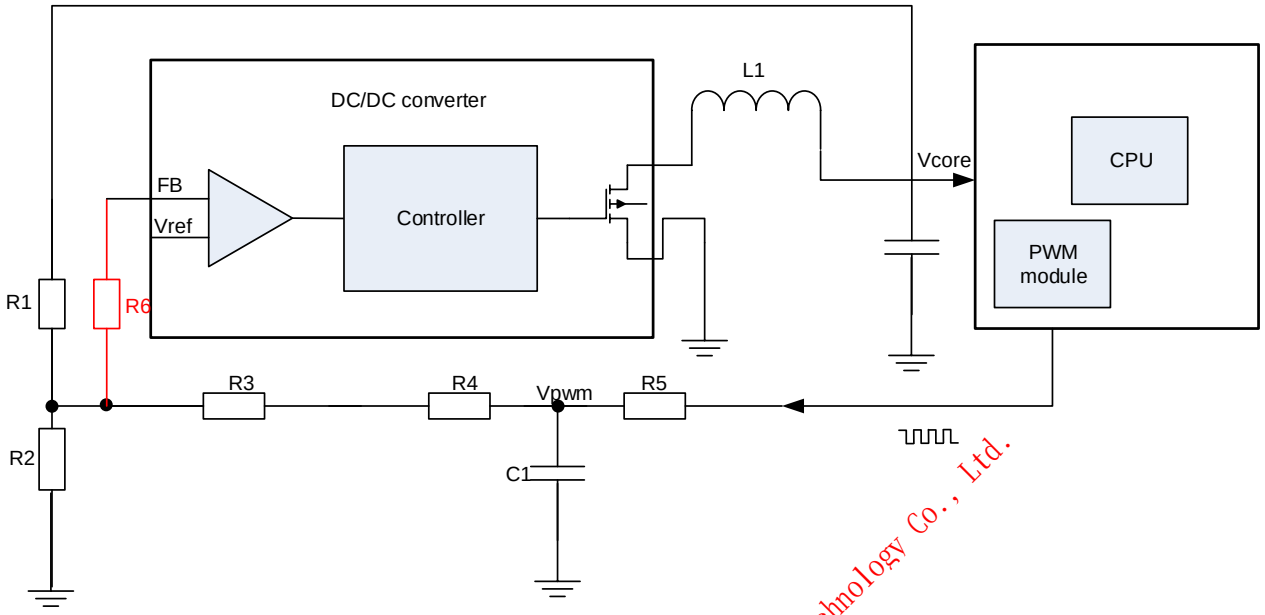
Figure 1-12 Schematic diagram of dynamic voltage scaling



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During SVB circuit design, connect the PWM pin of Hi3516C V500 to the SVB circuit and then to the FB pin of the DC-DC circuit for the core power supply. Note the following during design:

- PWM is used to control the voltage of the DVDD power.
- The error range of the DC voltage of the 3.3 V power for the Hi3516C V500 must be within ±50 mV.
- A resistor (R6) needs to be reserved before the FB pin in the DC-DC circuit to ensure the loop stability of the DC-DC component.

  The impedance of R6 can be calculated by using the following equation (this calculation method applies only to the MPS DC-DC. You need to confirm with the vendors whether this equation applies to the DC-DC of other solutions):

  R6 x (Vout/Vref) + R1 = 200 kilohms

  where

  Vout is the nominal voltage of the DC-DC output, Vref is the reference voltage of the DC-DC, and R1 is the voltage-division resistor on the FB pin of the DC-DC.

  The value 200 kilohms in the right of the equation is an empirical value, and it can be changed to 100 kilohms if the capacitance of the DC-DC output capacitor is greater than the reference capacitance in the DC-DC manual.

  The obtained impedance of R6 is a reference value. The actual impedance fluctuates around the calculation result, and is close to the reference value.
- The DC-DC reference voltage (Vref) must be less than 0.65 V, and the precision deviation of the DC-DC Vref cannot be greater than 2%.

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The precision of all the resistors must be 1%, and the material of the capacitors must be X7R or X7S.

The parameter configuration of the SVB circuit must be consistent with those in Table 1-10.

Table 1-10 RC parameters for DVDD in the SVB voltage scaling circuit

Vref (V)	R1 (kilohm)	R2 (kilohm)	R3 (kilohm)	R4 (kilohm)	R5 (kilohm)	C (μF)
0.45	24	20	120	47	1	2.2
0.6	15	24	100	20	1	2.2
0.608	15	24	120	24	1	2.2

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1.3 Design Recommendations on Peripheral Interfaces

1.3.1 MAC Interface

MAC Interface

The Hi3516C V500 MAC supports the RMII mode instead of the RGMII or MII mode. Figure 1-13 shows the signal connection in RMII mode.

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Figure 1-13 Hi3516C V500 signal connection in RMII mode

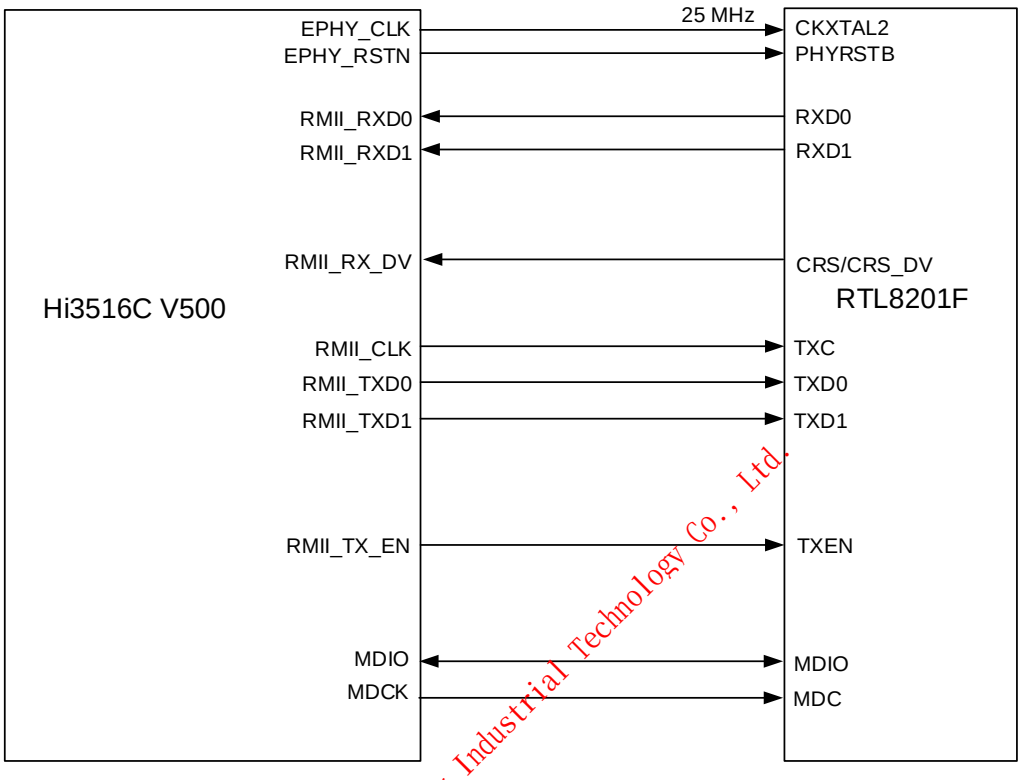

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Table 1-11 describes the design requirements on the ETH MAC signals.

Table 1-11 Design of the ETH MAC signals

Signal	Design Method
RMII_CLK	4-layer PCB design: The signal is connected to a 33-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 8 inches. 2-layer PCB design: The signal is connected to a 51-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 8 inches.
RMII_TXD[0:1] RMII_TX_EN	2-layer and 4-layer PCB design: The signals are connected directly. The trace length cannot be greater than 8 inches.
RMII_RXD[0:1] RMII_RX_DV	2-layer and 4-layer PCB design: The signals are connected directly. The trace length cannot be greater than 8 inches.

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Signal	Design Method
MDCK	4-layer PCB design: The signal is connected to a 33-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 8 inches. 2-layer PCB design: The signal is connected to a 51-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 8 inches.
MDIO	2-layer and 4-layer PCB design: The signal directly connects to a 1.5-kilohm pull-up resistor. The trace length cannot be greater than 8 inches.
EPHY_CLK	4-layer PCB design: The signal is connected to a 33-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 8 inches. 2-layer PCB design: The signal is connected to a 51-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 8 inches.

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1.3.2 Audio and Video Interfaces

1.3.2.1 Design of Analog Audio Interfaces

Hi3516C V500 provides one group of dual-channel audio input interfaces (AC_INL/R) and one group of dual-channel audio output interfaces (AC_OUTL/R).

AC_INL/R can be multiplexed as a differential input interface AC_IN_P/N. The audio output interfaces do not support differential outputs.

- The analog power AVDD33_AC for the audio module must be isolated from the 3.3 V system power by using an EMI bead.
- The filter capacitors of the AC_VREF pin should be the 4.7 µF + 100 nF low ESR ceramic capacitors.
- The input interfaces of the audio module can act as the line-in or MIC_IN input channels. If the input device is a passive MIC device, the MIC_BIAS bias voltage needs to be provided. If the output device is an active line-in device (such as a PC), the bias voltage is not required.
- The blocking capacitors connected to the audio input signal must be placed close to Hi3516C V500. The 4.7 µF capacitors are recommended.
- Hi3516C V500 provides one MIC_BIAS pin. A 4.7 µF capacitor needs to be placed close to the AC_MICBIAS pin.
- You are advised to connect an audio amplifier and filter circuit to the audio output pins AC_OUTL and AC_OUTR, which ensures excellent audio quality.

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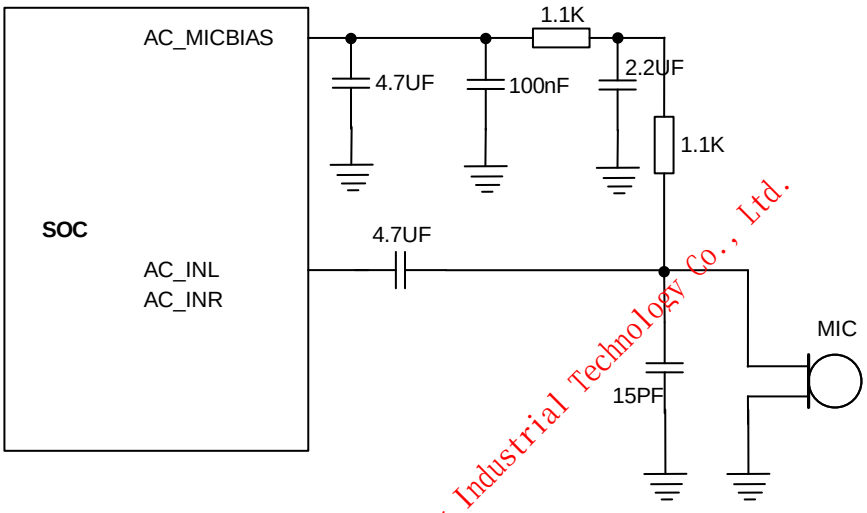
- ESD protection measures must be taken on the audio output signal traces to enhance the anti-interference performance of the interface.

Design of the Single-Ended MIC Input Circuit

Figure 1-14 shows the single-ended MIC input reference circuit.

Figure 1-14 Single-ended MIC input circuit



Design of the MIC Differential Input Circuit

Figure 1-15 shows the MIC differential input reference circuit. The microphone used in the figure is a common single-end MIC.

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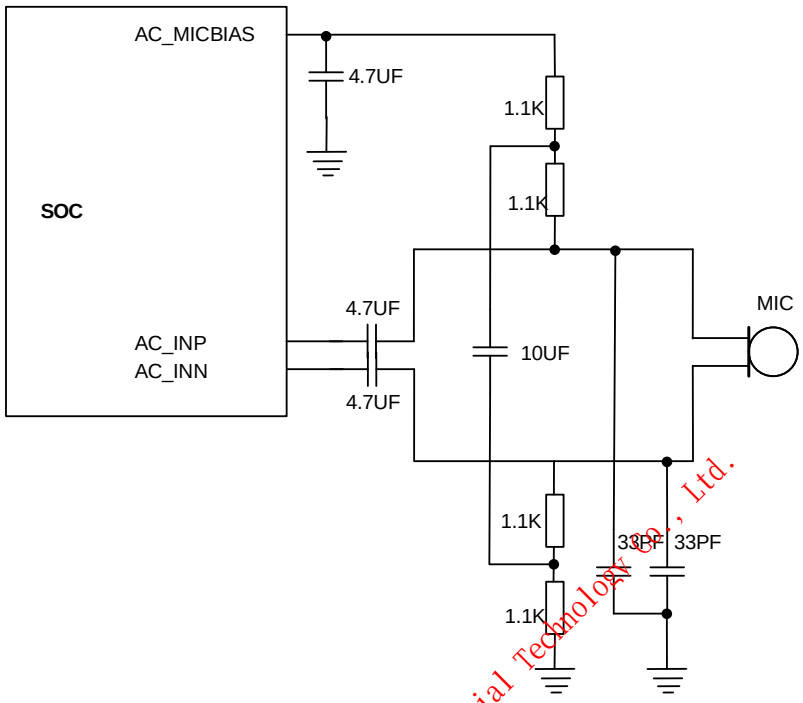
Figure 1-15 MIC differential input circuit



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The audio module is prone to be affected by the power noise and signal crosstalk, To obtain better audio quality during product development, you are advised to use a differential input circuit for single MIC input. A common single-ended MIC is recommended.

1.3.2.2 I²S Interface

Hi3516C V500 has an inter-IC sound (I^2S) interface that is multiplexed with the JTAG interface. Figure 1-16 and Figure 1-17 show the 5-wire connections in I^2S master mode and I^2S slave mode, respectively.

NOTICE

The audio coder/decoder (codec) and the I^2S interface share the same channel and cannot be used at the same time.

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Figure 1-16 5-wire connection in I²S master mode

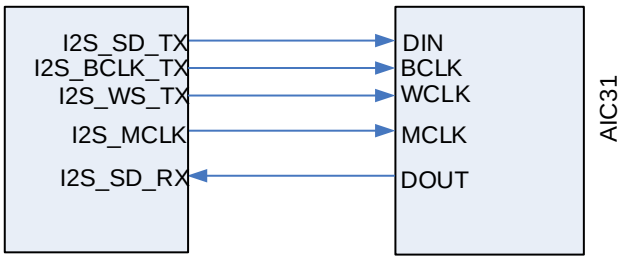
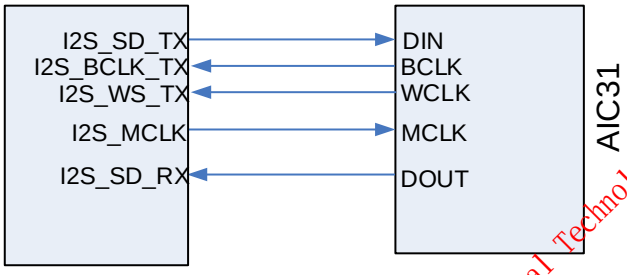


Figure 1-17 5-wire connection in I²S slave mode



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1.3.2.3 Design of the Sensor Configuration Interface

The Hi3516C V500 supports only one sensor. The configuration interface of the sensor contains the following signals:

- SENSOR0_RSTN, SENSOR0_CLK, SENSOR_HS, and SENSOR_VS
- SPI0/I2C0

The signal functions are described as follows:

- SENSOR0_RSTN can output the reset signal for resetting the sensor through register configuration.
- SENSOR0_CLK provides working clocks for various mainstream sensors 0. For details, see the configuration information about the CRG register in the *Hi3516C V500 Professional Smart IP Camera SoC Data Sheet*. In the design of the 4-layer PCB, SENSOR0_CLK needs to connect to a 33-ohm resistor in series at the Hi3516C V500 end. In the design of the 2-layer PCB, SENSOR0_CLK needs to connect to a 51-ohm resistor in series.
- SPI0/I2C0 is used for configuring sensor
  - I2C0_SCL is multiplexed with SPI0_SCLK, and I2C0_SDA is multiplexed with SPI0_SDO. The sensor configuration interface supports a 3-wire SPI that is multiplexed with SPI 0 and is used for interconnection with some Panasonic sensors.
  - During design, the I2C0 signal needs to connect to an external pull-up resistor. The pull-up resistance must be 1 kilohm.
- SENSOR_HS and SENSOR_VS output the horizontal sync (HS) signal and vertical sync (VS) signal, and are used to support sensors in slave mode.
- The sensor reset signal needs to connect to 1 nF grounding capacitors in the circuit design of the sensor board to ensure the electrostatic discharge (ESD) performance.

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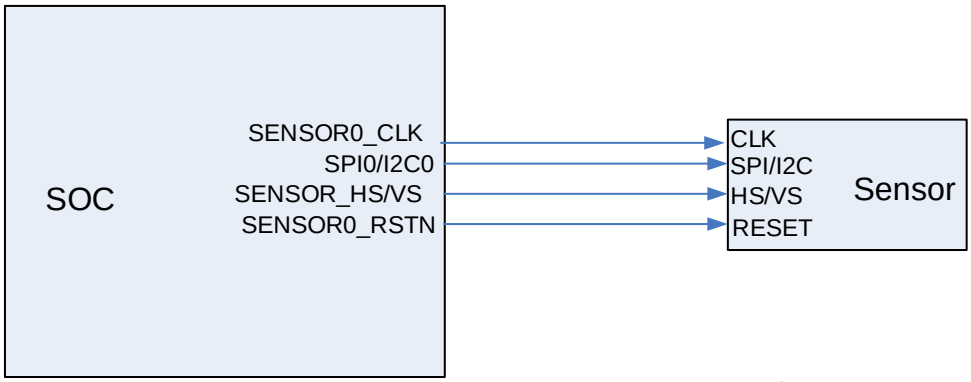
Figure 1-18 shows the connection methods recommended when sensors are connected.

Figure 1-18 Interface configuration sensor



1.3.2.4 VI Interface Design

The video input (VI) interface can be multiplexed as the parallel complementary metal-oxide-semiconductor (CMOS) VI interface or differential VI interface (MIPI Rx interface).

- The parallel CMOS VI interface supports data in the formats of raw, BT.1120, BT.656, and BT.601, and its maximum frequency is 148.5 MHz.
  - If the raw data signal is connected, the signal connects to the VI interface from the lower bits to the upper bits in sequence. For example, the 12-bit raw data signal connects to D0−D11 of the VI interface.
  - If the BT.1120 signal is connected, the Y signal connects to the upper 8 bits of the VI interface in sequence and the C signal connects to the lower 8 bits of the VI interface in sequence. Both the internal synchronization mode and external synchronization mode are supported.
  - If the BT.656 or BT.601 signal is connected, the signal connects to the VI interface from the lower bits to the upper bits in sequence.
- The differential VI interface has one group of differential clock signals and four groups of differential data signals. It supports 2-lane and 4-lane MIPI RX inputs.
  - For 4-lane MIPI RX, the MIPI_RX_CK0P/N performs sampling on MIPI_RX_D0P/N, MIPI_RX_D1P/N, MIPI_RX_D2P/N, and MIPI_RX_D3P/N.
  - For 2-lane MIPI RX, MIPI_RX_CK0P/N performs sampling on any two of the 4 lanes. It is recommended that MIPI_RX_D0P/N and MIPI_RX_D2P/N be selected preferentially during design.
- The MIPI RX interface has an embedded 100-ohm bridge matched resistor. Therefore, no external resistor needs to be designed or reserved.
- For details about the connection mode of the VI interface, see the *Hi3516C V500 Sensor Input Level Scenario List*.

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When the non—MIPI RX function is used, the PHY_MODE_LINK and PHY_EN_LINK registers must be set to 0x30100 and 0x0, respectively. For details, see section 9.3.6 in the chip data sheet. In this way, the MIPI RX PHY can be set to CMOS mode.

1.3.2.5 Parallel VO Interface Design

The parallel VO interface of Hi3516C V500 supports the BT.656, BT.1120, and RGB output, but does not support the BT.601 output.

The RGB output is used for the interconnection with the liquid crystal display (LCD), and supports 6-bit and 8-bit serial RGB data, and 16-bit, 18-bit, and 24-bit parallel RGB data. Table 1-12 describes the mapping between the signal interface mode and pins.

Table 1-12 Mapping between the signal interface mode and pins

Signal Interface Mode	Corresponding Pins
BT.1120	Y (luminance): VOU1120_DATA[15:8] C (chrominance): VOU1120_DATA[7:0] Clock: VOU1120_CLK
BT.656	DATA: VOU656_DATA [7:0] CLOCK: VOU656_CLK
6-bit serial RGB	DATA: LCD_DATA [5:0] CLOCK: LCD_CLK HSYNC: LCD_HSYNC VSYNC: LCD_VSYNC DE: LCD_DE
8-bit serial RGB	LCD_DATA [7:0] Clock: LCD_CLK HSYNC: LCD_HSYNC VSYNC: LCD_VSYNC DE: LCD_DE
16-bit parallel RGB (RGB565)	R[4:0]: LCD_DATA [15:11] G[5:0]: LCD_DATA [10:5] B[4:0]: LCD_DATA [4:0] HSYNC: LCD_HSYNC VSYNC: LCD_VSYNC DE: LCD_DE

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Signal Interface Mode	Corresponding Pins
18 bit Parallel RGB (RGB666)	B[5:0]: LCD_DATA [17:12] G[5:0]: LCD_DATA [11:6] R[5:0]: LCD_DATA [5:0] HSYNC: LCD_HSYNC VSYNC: LCD_VSYNC DE: LCD_DE
24-bit parallel RGB (RGB888)	R[7:0]: LCD_DATA [23:16] G[7:0]: LCD_DATA [15:8] B[7:0]: LCD_DATA [7:0] HSYNC: LCD_HSYNC VSYNC: LCD_VSYNC DE: LCD_DE

LCD signals are multiplexed on MIPI TX, RMII, GPIO, and JTAG. The 16-bit parallel RGB (RGB565) LCD signal comes from MIPI TX and RMII. The 24-bit parallel RGB (RGB888) LCD signal comes from MIPI TX, RMII, GPIO, and JTAG_TDI. For details, see the *Hi3516C V500 VO Scenario Description*.

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NOTICE

When the non—MIPI TX function is used, the PHY_RSTZ and PHY_TST_CTRL0 registers must be set to 0x0 and 0x1, respectively. For details, see section 9.4.6 in the chip data sheet. In this way, the MIPI TX PHY is disabled.

Table 1-13 describes the methods of designing parallel VO signals.

Table 1-13 Design requirements on parallel VO signals

Signal	Design Method
VOU1120_CLK	148 MHz single-edge 2-layer PCB design: The signal is connected to a 51-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 2 inches. 148 MHz single-edge 4-layer PCB design: The signal is connected to a 33-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 2 inches. 37 MHz single-edge 2-layer PCB design: The signal is connected to a 51-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 10 inches. 37 MHz single-edge 4-layer PCB design: The signal is connected to a 33-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 10 inches.

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Signal	Design Method
VOU1120_DATA	74 MHz single-edge PCB design: The signal is connected directly. The trace length cannot be greater than 2 inches. 18.5 MHz single-edge PCB design: The signal is connected directly. The trace length cannot be greater than 10 inches.
LCD_CLK	74 MHz single-edge 2-layer PCB design: The signal is connected to a 51-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 5 inches. 74 MHz single-edge 4-layer PCB design: The signal is connected to a 33-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 5 inches. 37 MHz single-edge 2-layer PCB design: The signal is connected to a 51-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 10 inches. 37 MHz single-edge 4-layer PCB design: The signal is connected to a 33-ohm resistor in series at the Hi3516C V500 end. The trace length cannot be greater than 10 inches.
LCD_DATA	37 MHz single-edge PCB design: The signal is connected directly. The trace length cannot be greater than 5 inches. 18.5 MHz single-edge PCB design: The signal is connected directly. The trace length cannot be greater than 10 inches.

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1.3.2.6 MIPI TX Design

Hi3516C V500 has an embedded MIPI TX PHY, which is used to connect the LCD screen with MIPIs.

- The AVDD3318_MIPITX power pin must be isolated from the chip digital power by using an EMI bead and a 2.2 μF filter capacitor needs to be placed at the chip pin.
- DSI_D0P/N, DSI_D1P/N, DSI_D2P/N, and DSI_D3P/N implement sampling by referring to the DSI_CKP/N differential clock.
- For details, see the schematic diagram of the Hi3516C V500 demo board.

1.3.3 SPI and I²C Interfaces

- Hi3516C V500 has three groups of SPI interfaces. SPI0 is used to configure the sensor. SPI1 and SPI2 are used to control peripherals.
- Hi3516C V500 has seven groups of I²C interfaces. I2C0 and I2C1 are used to configure the sensor and are multiplexed with the SPI0 interface. For details about the multiplexing relationship, see the *Hi3516C V500_PINOUT_EN*.

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- For the 2-layer PCB design, it is recommended that the I^2C signal is connected to an external 1.5-kilohm pull-up resistor.
- For the 4-layer PCB design, it is recommended that the I^2C signal is connected to an external 1-kilohm pull-up resistor.

NOTICE

The I2C7_SCL and I2C7_SDA pull-up power supplies must be consistent with the DVDD3318_SDIO1 power supply.

1.3.4 SDIO Design

Hi3516C V500 has two SDIO interfaces.

SDIO0 supports SDIO 3.0 and SDXC storage cards.

SDIO1 can connect to the Wi-Fi module only and support the 1.8 V and 1.3 V levels.

SDIO0_CARD_DETECT and SDIO0_CARD_POWER_EN support only the 3.3 V level.

Table 1-14 describes the design requirements on SDIO signals.

Table 1-14 Design requirements on SDIO signals

Signal	Design
SDIO0_VOUT	A 470 nF capacitor is connected to the ground at the SoC end.
SDIO0_CCLK_OUT	**2-layer PCB design:** The signal is connected to a 51-ohm resistor in series at the SoC end. The trace length cannot be greater than 4 inches. **4-layer PCB design:** The signal is connected to a 33-ohm resistor in series at the SoC end.The trace length cannot be greater than 4 inches.
SDIO0_CDATA[0:3] SDIO0_CMD	**2-layer PCB design:** The signal is connected to a 51-ohm resistor in series at the SoC end. The trace length cannot be greater than 4 inches, and a 47-kilohm pull-up resistor is reserved. When the trace length is less than or equal to 2 inches, you do not have to connect a resistor at the SoC end. **4-layer PCB design:** The signal is connected to a 33-ohm resistor in series at the SoC end. The trace length cannot be greater than 4 inches, and a 47-kilohm pull-up resistor is reserved. When the trace length is less than or equal to 2 inches, you do not have to connect a resistor at the SoC end.

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Signal	Design
SDIO0_CARD_DETECT	When an SD card is connected, the SDIO0_CARD_DETECT signal must connect to an external pull-up resistor and then to the 3.3 V power. A 10-kilohm resistor is recommended.
SDIO1_CCLK_OUT	**2-layer PCB design:** The signal is connected to a 51-ohm resistor in series at the SoC end. The trace length cannot be greater than 4 inches. **4-layer PCB design:** The signal is connected to a 33-ohm resistor in series at the SoC end. The trace length cannot be greater than 4 inches.
SDIO1_CDATA[0:3] SDIO1_CMD	**2-layer PCB design:** The trace length cannot be greater than 4 inches. You do not have to connect a resistor at the SoC end, and a 47-kilohm pull-up resistor is reserved.

1.3.5 USB 2.0 Interface

Hi3516C V500 provides one USB 2.0 interfaces that support the host or device function but not the on-the-go (OTG) function.

- AVDD33_USB is combined with the 3.3 V system power. A 2.2 µF capacitor is placed close to the pin.
- USB_VBUS uses two 10-kilohm resistors to divide the voltages of 5V0_USBS for input detection. This pin is used only in host mode and can be floated.
- ESD protection measures must be taken for the USB 2.0 signal. The parasitic capacitor of the ESD component must be less than 1 pF. The ESD component must be placed close to the USB port.

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1.3.6 ADC

Hi3516C V500 supports two analog signal inputs for AD conversion. The two pins can be multiplexed as general-purpose input/output (GPIO) signals.

1.3.7 RTC

In fixed frequency-division mode, the sequence accuracy of the embedded RTC depends on the external crystal oscillator. Select an appropriate crystal oscillator based on its frequency deviation and temperature offset. If high sequence accuracy is required, the external integrated RTC is recommended.

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NOTICE

- RTC_XIN is the input pin of the RTC.
- When the DVDD3318_RC is powered off, AVDD_BAT must keep supplying power. Otherwise, the time is reset.

1.3.8 PWM

Hi3516C V500 has three PWMs. SVB_PWM of the SoC can only be used to adjust the core voltage, while PWM_OUT[0:1] is used to connect to peripherals.

All the PWM interfaces can be multiplexed as GPIOs when they are not used.

1.3.9 UART

Hi3516C V500 supports four UART interfaces. Only UART0/4 is a 2-wire serial port, while other UARTs are 4-wire serial ports.

UART0 is used for system debugging.

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1.4 Descriptions of Special Pins

1.4.1 Methods for Processing Unused Pins

Table 1-15 describes the processing recommendations for unused module power and pins.

Table 1-15 Processing recommendations for unused module power and pins

Net Name	POWER	STATUS(IF NOT USED)	NOTES
AVDD33_AC	-	TIED TO 3.3 V	-
AVSS_AC	-	TIED TO VSS	-
AC_INL	AVDD33_AC	N.C.	-
AC_INR			-
AC_MICBIAS			-
AC_OUTL			-
AC_OUTR			-
AC_VREF			-
AVDD3318_MIPITX	-	TIED TO 1.8 V/ 3.3 V	-
DSI_CKN	AVDD3318_MIPITX	N.C.	-
DSI_CKP			-

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Net Name	POWER	STATUS(IF NOT USED)	NOTES
DSI_D0N			-
DSI_D0P			-
DSI_D1N			-
DSI_D1P			-
DSI_D2N			-
DSI_D2P			-
DSI_D3N			-
DSI_D3P			-
GPIO0_0	DVDD33	N.C.	-
GPIO0_1			-
GPIO0_2			-
GPIO0_3			-
GPIO0_4			-
GPIO0_5			-
GPIO0_6			-
I2C2_SCL	DVDD33	N.C.	-
I2C2_SDA			-
I2C7_SCL	DVDD3318_SDIO1	N.C.	-
I2C7_SDA			-
JTAG_TCK	DVDD33	N.C.	-
JTAG_TDI			-
JTAG_TDO			-
JTAG_TMS			-
JTAG_TRSTN			-
LSADC_CH0	DVDD33	N.C.	-
LSADC_CH1			-
AVDD3318_MIPIRX	-	TIED TO 1.8 V/ 3.3 V	-
AVSS_MIPIRX	-	TIED TO VSS	-
MIPI_RX_CK0N	AVDD3318_MIPIRX	N.C.	-

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Net Name	POWER	STATUS(IF NOT USED)	NOTES
MIPI_RX_CK0P			-
MIPI_RX_D0N			-
MIPI_RX_D0P			-
MIPI_RX_D1N			-
MIPI_RX_D1P			-
MIPI_RX_D2N			-
MIPI_RX_D2P			-
MIPI_RX_D3N			-
MIPI_RX_D3P			-
VI_DATA8			-
VI_DATA9			-
SVB_PWM	DVDD33	N.C.	-
PWM0			-
PWM1			-
AVDD_BAT	-	N.C.	-
AVSS_RTC	-	TIED TO VSS	-
RTC_XIN	-	N.C.	-
RTC_XOUT	-	N.C.	-
DVDD3318_PC	-	TIED TO 1.8 V/ 3.3 V	-
PWR_BUTTON	DVDD3318_PC	N.C.	-
PWR_RSTN			-
PWR_SEQ0			-
PWR_STARTUP			-
PWR_WAKEUP			-
RMII_CLK	DVDD33	N.C.	
RMII_RX_DV			-
RMII_RXD0			-
RMII_RXD1			-
RMII_TX_EN			-

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Net Name	POWER	STATUS(IF NOT USED)	NOTES
RMII_TXD0			-
RMII_TXD1			-
MDCK			-
MDIO			-
DVDD18_SDIO0	-	TIED TO 1.8 V	-
SDIO0_CARD_DETECT	DVDD33	N.C.	-
SDIO0_CARD_POWER_EN			-
SDIO0_CCLK_OUT	DVDD33 or DVDD18 (switched using the power switch)	N.C.	-
SDIO0_CCMD			-
SDIO0_CDATA0			-
SDIO0_CDATA1			-
SDIO0_CDATA2			-
SDIO0_CDATA3			-
SDIO0_VOUT			-
DVDD3318_SDIO1	-	TIED TO 1.8 V/ 3.3 V	-
SDIO1_CCLK_OUT	DVDD3318_SDIO1	N.C.	-
SDIO1_CCMD			-
SDIO1_CDATA0			-
SDIO1_CDATA1			-
SDIO1_CDATA2			-
SDIO1_CDATA3			-
DVDD3318_SENSOR	-	TIED TO 1.8 V/ 3.3 V	-
SENSOR0_CLK	DVDD3318_SENSOR	N.C.	-
SENSOR0_RSTN			-
SPI0_CSN			-
SPI0_SCLK			-
SPI0_SDI			-
SPI0_SDO			-

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Net Name	POWER	STATUS(IF NOT USED)	NOTES
UART0_RXD	DVDD33	N.C.	-
UART0_TXD			-
DVDD3318_UART1	-	TIED TO 1.8 V/ 3.3 V	-
UART1_CTSN	DVDD3318_UART1	N.C.	-
UART1_RTSN			-
UART1_RXD			-
UART1_TXD			-
AVDD33_USB	-	TIED TO 3.3 V	-
AVSS_USB	-	TIED TO VSS	-
USB_DM	AVDD33_USB	N.C.	-
USB_DP			-
USB_OVRCUR	DVDD33	N.C.	-
USB_PWREN			-
USB_VBUS			-
DVDD3318_VI	-	TIED TO 1.8 V/ 3.3 V	-
VI_CLK	DVDD3318_VI	N.C.	-
VI_DATA0			-
VI_DATA1			-
VI_DATA2			-
VI_DATA3			-
VI_DATA4			-
VI_DATA5			-
VI_DATA6			-
VI_DATA7			-
VI_HS			-
VI_VS			-

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NOTE
N.C.: floated

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1.4.2 5 V Tolerance Pins

Table 1-16 5 V tolerance pins

Pin	Description
I2C2_SCL	5V tolerance
I2C2_SDA	
USB_VBUS	

1.4.3 Fail-Safe GPIO Pins

For the Hi3516C V500 chip, all GPIO pins support the fail-safe design, except the GPIO pins shown in Table 1-17.

Table 1-17 GPIO pins that do not support fail-safe

Pin No.	Pin Name	Power Supply
T2	SDIO0_CCLK_OUT/GPIO1_2	DVDD18_SDIO0/DVDD33
M2	EMMC_RST_N/GPIO0_5	DVDD3318_FLASH
P2	EMMC_DATA2/GPIO0_7	DVDD3318_FLASH

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1.5 Description of the GPIO Ports with Glitches During the DVDD33 Power-on

There is a probability that 100–900 mV glitches occur on some GPIO ports during the power-on process of the Hi3516C V500 DVDD33. The I/O glitches occur when the DVDD33 voltage is between 400 mV and 950 mV, and the glitch width is 100 µs to 150 µs.

If the GPIO ports are connected to implement switch control or enable control in the application scenario, check whether the I/O port glitch affects the functions of the connected circuit. For low-speed level signals, you are advised to add 47 nF–100 nF ground capacitors for GPIO ports to remove possible glitches given that the circuit functions and performance are not affected.

Table 1-18 Statistics of the GPIO ports with glitches during the Hi3516C V500 DVDD33 power-on

Pin No.	Pin Name	Multiplexed Function
B12	GPIO0_0	UPDATE_MODE
B11	GPIO0_1	I2C3_SDA/LCD_DATA20

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Pin No.	Pin Name	Multiplexed Function
A11	GPIO0_2	I2C3_SCL/LCD_DATA19
C11	GPIO0_3	IR_IN/LCD_DATA18
D11	GPIO0_4	LCD_DATA21
C12	GPIO0_5	LCD_DATA22
E18	GPIO0_6	LCD_CLK/VOU_CLK
P2	GPIO0_7	EMMC_DATA2/SFC_CSN
V2	GPIO1_0	SDIO0_CARD_POWER_EN/JTAG_TCK
T3	GPIO1_1	SDIO0_CARD_DETECT
T2	GPIO1_2	SDIO0_CCLK_OUT/JTAG_TRSTN
P3	GPIO1_3	SDIO0_CCMD
T1	GPIO1_4	SDIO0_CDATA0
R3	GPIO1_5	SDIO0_CDATA1/JTAG_TMS
U2	GPIO1_6	SDIO0_CDATA2/JTAG_TDO
U1	GPIO1_7	SDIO0_CDATA3/JTAG_TDI
A13	GPIO10_0	DSI_D0P/LCD_DATA8/VOU_DATA15/LCD_DE
B13	GPIO10_1	DSI_D0N/LCD_DATA9/VOU_DATA14/LCD_VSYNC
N15	GPIO10_3	LSADC_CH0
L15	GPIO10_4	LSADC_CH1
M2	GPIO10_5	EMMC_RST_N/SYS_RSTN_OUT
G16	GPIO10_6	I2C7_SCL
F16	GPIO10_7	I2C7_SDA/RMII_CLK
J18	GPIO11_0	PWR_WAKEUP
H16	GPIO11_1	PWR_SEQ0
V3	GPIO2_0	USB_OVRCUR
R4	GPIO2_1	USB_VBUS
U3	GPIO2_2	USB_PWREN
V12	GPIO2_3	VI_CLK/VOU_CLK/I2C5_SCL
V16	GPIO3_0	VI_DATA0/VOU_DATA0/I2C5_SDA
U15	GPIO3_1	VI_DATA1/VOU_DATA1/I2C6_SCL
V15	GPIO3_2	VI_DATA2/VOU_DATA2/I2C6_SDA
U14	GPIO3_3	VI_DATA3/VOU_DATA3/UART2_RTSN

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Pin No.	Pin Name	Multiplexed Function
V14	GPIO3_4	VI_DATA4/VOU_DATA4/UART2_CTSN/SPI2_SCLK
U13	GPIO3_5	VI_DATA5/VOU_DATA5/UART2_RXD/SPI2_SDO
V13	GPIO3_6	VI_DATA6/VOU_DATA6/UART2_TXD/SPI2_SDI
U12	GPIO3_7	VI_DATA7/VOU_DATA7/SHUTTER_TRIG/SPI2_CSN
T12	GPIO4_0	SENSOR0_CLK
T11	GPIO4_1	SENSOR0_RSTN/BOOT_SEL1
R11	GPIO4_2	SPI0_SCLK/I2C0_SCL/SPI_3LINE_SCLK
U11	GPIO4_3	SPI0_SDO/I2C0_SDA/SPI_3LINE_SDATA
T10	GPIO4_4	SPI0_SDI/I2C1_SDA/SENSOR_VS
T9	GPIO4_5	SPI0_CSN/I2C1_SCL/SPI_3LINE_CSN/SENSOR_HS
T14	GPIO4_6	VI_VS/SENSOR_VS
T13	GPIO4_7	VI_HS/FLASH_TRIG/SENSOR_HS
R14	GPIO5_0	UART1_RTSN/UART4_RXD
T15	GPIO5_1	UART1_CTSN/UART4_TXD
R16	GPIO5_2	UART1_RXD
R17	GPIO5_3	UART1_TXD
R18	GPIO5_4	UART0_RXD
P17	GPIO5_5	UART0_TXD
P16	GPIO5_6	I2C2_SDA
P15	GPIO5_7	I2C2_SCL
H18	GPIO6_0	SDIO1_CCLK_OUT/RMII_RX_DV
F15	GPIO6_1	SDIO1_CCMD/EPHY_CLK
G18	GPIO6_2	SDIO1_CDATA0/MDCK
G17	GPIO6_3	SDIO1_CDATA1/MDIO
F17	GPIO6_4	SDIO1_CDATA2/RMII_TX_EN
G15	GPIO6_5	SDIO1_CDATA3/EPHY_RSTN
P18	GPIO6_6	PWM0
N18	GPIO6_7	PWM1
C17	GPIO7_0	RMII_TX_EN/LCD_DATA2/VOU_DATA5
D12	GPIO7_1	RMII_TXD0/LCD_DATA0/VOU_DATA7
C18	GPIO7_2	RMII_CLK/LCD_HSYNC

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Pin No.	Pin Name	Multiplexed Function
D13	GPIO7_3	RMII_RX_DV/LCD_DATA6/VOU_DATA1
C14	GPIO7_4	RMII_RXD1/LCD_VSYNC
C15	GPIO7_5	RMII_RXD0/LCD_DE
B18	GPIO7_6	EPHY_RSTN/LCD_DATA3/VOU_DATA4/SFC_DEVICE_MODE
D16	GPIO7_7	EPHY_CLK/LCD_DATA7/VOU_DATA0
E15	GPIO8_0	JTAG_TRSTN/SPI1_SCLK/RMII_TXD1/I2S_MCLK
D15	GPIO8_1	JTAG_TCK/SPI1_SDO/RMII_RXD1/I2S_BCLK_TX
F18	GPIO8_2	JTAG_TMS/SPI1_CSN0/RMII_TXD0/I2S_WS_TX
E16	GPIO8_3	JTAG_TDO/SPI1_SDI/RMII_RXD0/I2S_SD_TX
E17	GPIO8_4	JTAG_TDI/SPI1_CSN1/LCD_DATA23/I2S_SD_RX
D18	GPIO8_5	MDIO/LCD_DATA5/VOU_DATA2
D17	GPIO8_6	MDCK/LCD_DATA4/VOU_DATA3/BOOT_SEL0
C16	GPIO8_7	RMII_TXD1/TEST_CLK/VOU_DATA6/LCD_DATA1
A17	GPIO9_0	DSI_D3P/LCD_DATA16/SHUTTER_TRIG/LCD_DATA5
B17	GPIO9_1	DSI_D3N/LCD_DATA17/FLASH_TRIG/LCD_CLK
A16	GPIO9_2	DSI_D2N/LCD_DATA14/VOU_DATA9/LCD_DATA3
B16	GPIO9_3	DSI_D2P/LCD_DATA15/VOU_DATA8/LCD_DATA4
A15	GPIO9_4	DSI_CKP/LCD_DATA12/VOU_DATA11/LCD_DATA1
B15	GPIO9_5	DSI_CKN/LCD_DATA13/VOU_DATA10/LCD_DATA2
A14	GPIO9_6	DSI_D1N/LCD_DATA10/VOU_DATA13/LCD_HSYNC
B14	GPIO9_7	DSI_D1P/LCD_DATA11/VOU_DATA12/LCD_DATA0

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2 PCB Design

2.1 Power Supplies and Filter Capacitors

NOTICE

X6 or X7 is recommended for the filter capacitor material of the power supplies under the main chip, including the core power supply, PLL power supply, and AVDD3318_MIPITX.

2.1.1 DVDD Power

The capacitance, quantity, and layout of the filter capacitors for the DVDD power supply of the 2-layer PCB design are different from those of the 4-layer PCB design:

The type, quantity, and layout of filter capacitors of the 2-layer PCB must follow the HI3516CV500DMEBLITE design.

The type, quantity, and layout of filter capacitors of the 4-layer PCB must follow the HI3516CV500DMEB design.

Type, Quantity, and Layout of Filter Capacitors

The layout requirements for decoupling capacitors of the 2-layer PCB design are as follows:

- The filter capacitor combination of the DVDD power domain is (10 μF + 4.7 μF x 2 + 1 μF + 220 nF x 3).
- The positions of the filter capacitors must follow the HI3516CV500DMEBLITE design.

The layout requirements for decoupling capacitors of the 4-layer PCB design are as follows:

- The filter capacitor combination of the DVDD power domain is (4.7 μF + 220 nF + 100 nF x 4).
- The positions of the filter capacitors must follow the HI3516CV500DMEB design.

2.1.2 DDR SDRAM I/O Power

The capacitance, quantity, and layout of the filter capacitors for the DDR I/O power supply of the 2-layer PCB design are different from those of the 4-layer PCB design.

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The type, quantity, and layout of filter capacitors of the 2-layer PCB must follow the HI3516CV500DMEBLITE design.

The type, quantity, and layout of filter capacitors of the 4-layer PCB must follow the HI3516CV500DMEB design.

Type, Quantity, and Layout of Filter Capacitors

The layout requirements for decoupling capacitors of the 2-layer PCB design are as follows:

- The filter capacitor combination of the DDR I/O power domain is (10 µF + 4.7 µF x 2 + 220 nF x 3). The 10 µF capacitor is reserved and is not connected.
- The positions of the filter capacitors must follow the HI3516CV500DMEBLITE design.

The layout requirements for decoupling capacitors of the 4-layer PCB design are as follows:

- The filter capacitor combination of the DDR I/O power domain is (4.7 µF x 2 + 220 nF x 3).

The positions of the filter capacitors must follow the HI3516CV500DMEB design.

VDDIO_DDR_CK must be isolated from the 1.5 V or 1.35 V power by using an EMI bead, and a 2.2 µF capacitor needs to be placed closed to the chip pin.

2.1.3 PLL Power

- The AVDD09_PLL and the DVDD core power are isolated by using an EMI bead (1 kilohm@100 MHz). See Figure 2-1 and Figure 2-2.

Figure 2-1 SCH design for the filtering circuit of AVDD09_PLL

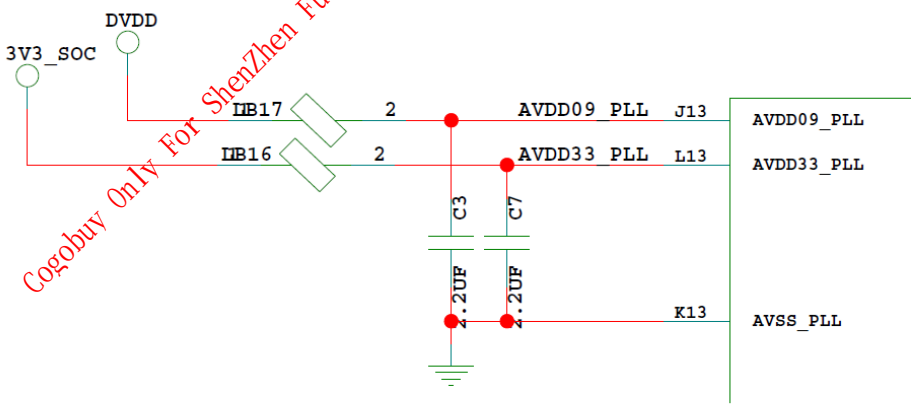

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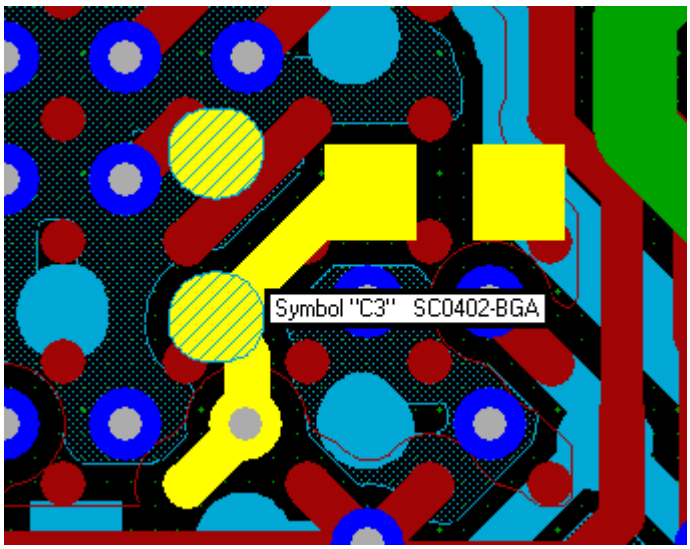
Figure 2-2 PCB design for the filtering circuit of AVDD09_PLL



- The AVDD33_PLL and the 3.3 V digital power are isolated by using an EMI bead (1 kilohm@100 MHz). See Figure 2-3 and Figure 2-4.

Figure 2-3 SCH design for the filtering circuit of AVDD33_PLL

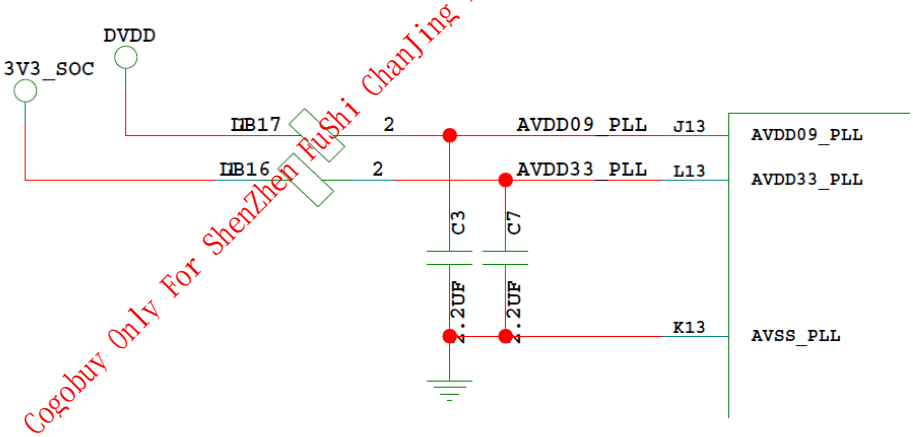


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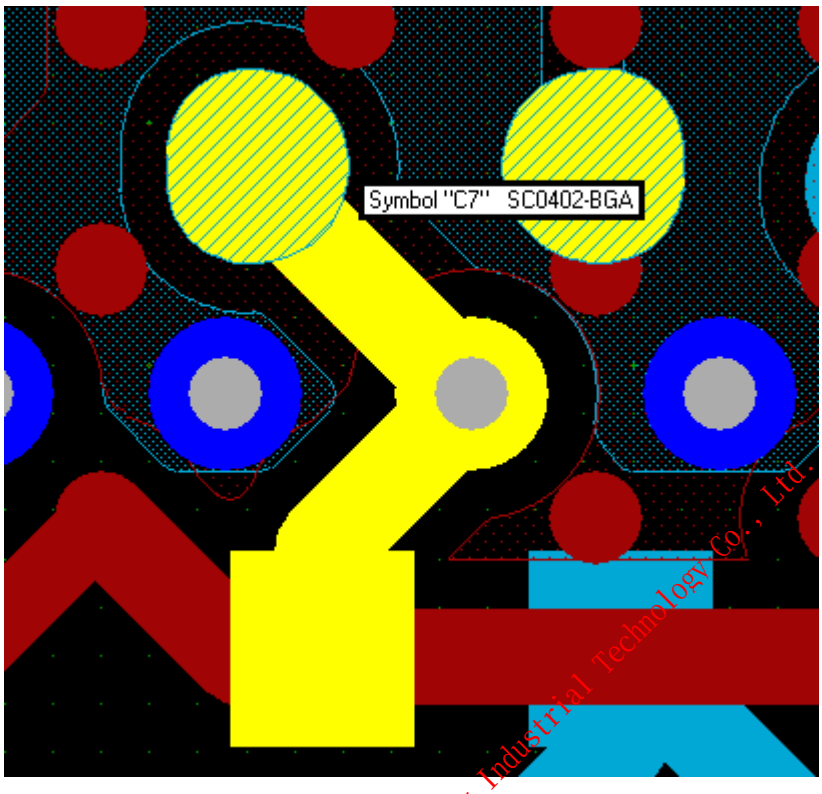
Figure 2-4 PCB design for the filtering circuit of AVDD33_PLL



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- The AVDD33_DDR_PLL_AC/DQ and the 3.3 V digital power are isolated by using an EMI bead (1 kilohm@100 MHz). See Figure 2-5 and Figure 2-6.

Figure 2-5 SCH design for the filtering circuit of AVDD33_DDR_PLL

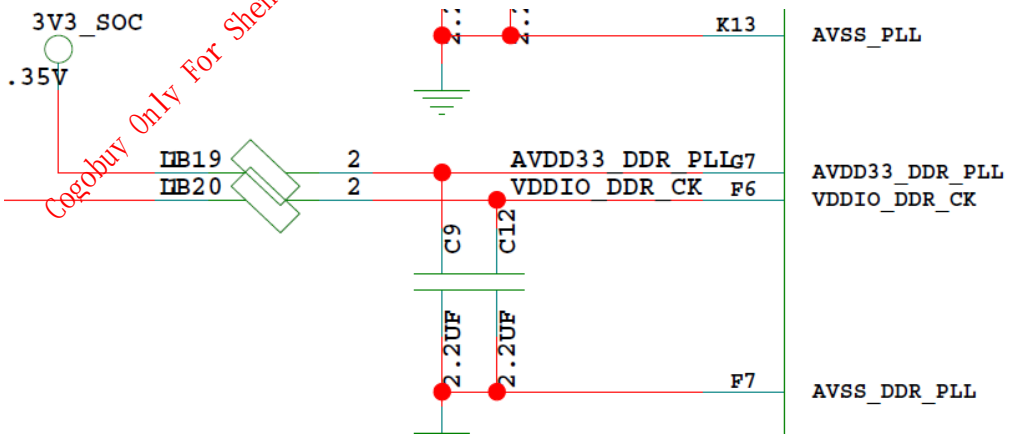

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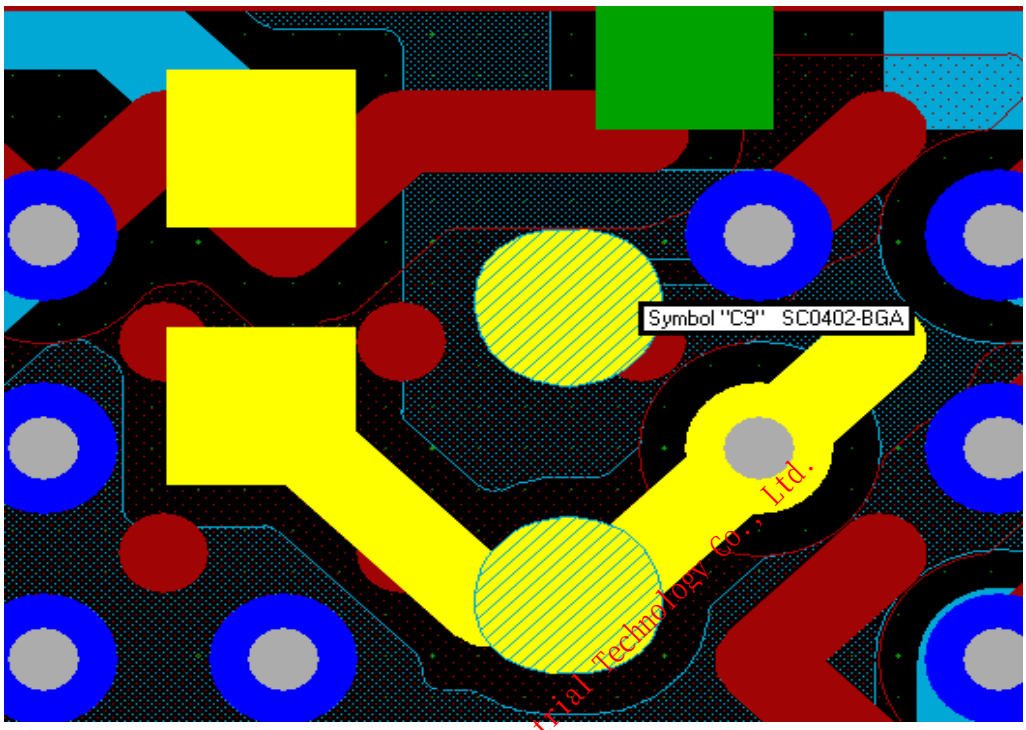
Figure 2-6 PCB design for the filtering circuit of AVDD33_DDR_PLL



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2.1.4 Analog Audio Power

AVDD33_AC is isolated from the 3.3 V digital power by using EMI beads, and at least one 2.2 µF capacitor is placed close to the chip pin.

2.2 Crystal Circuit

The traces of the crystal signals (Xin, Xout, RTC_XIN, and RTC_XOUT) must be surrounded with GND traces. The reference plane of the signal traces must be complete, and no high-speed signal can be routed under the crystal circuit.

2.3 DDR SDRAM Circuit

Hi3516C V500 connects to the 16-bit DDR3(L) SDRAM. For the 2-layer PCB design, completely follow the HI3516CV500DMEBLITE design. For the 4-layer PCB design, follow the HI3516CV500DMEB design.

Hi3516C V500 connects to the 16-bit DDR4 SDRAM. For the 4-layer PCB design, follow the HI3516CV500DMEB design.

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2.4 Flash Circuit

2.4.1 SPI Flash

The design requirements on the SPI flash signals are as follows:

- Avoid routing signal traces across power plane splits to maintain complete reference planes for signal traces.
- Ensure that the spacing between adjacent signal traces complies with the 3W rule.
- The trance length of SFC_CSN is used as the reference for that of SFC_CSN0/1, SFC_MOSI_IO0, SFC_MISO_IO1, SFC_WP_IO2, and SFC_HOLD_IO3, and the deviation should fall within ±1000 mils.
- The preceding length constraints are jointly controlled by the package and PCB design.

2.4.2 eMMC

The design requirements on the eMMC signals are as follows:

- Avoid routing signal traces across power plane splits to maintain complete reference planes for signal traces.
- Ensure that the spacing between adjacent signal traces complies with the 3W rule.
- The trace length of EMMC_DATA[0:3] and EMMC_CMD is based on that of EMMC_CLK, and the error should be within ±300 mils.
- The preceding length constraints are jointly controlled by the package and PCB design.

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2.5 RMII Signals

The design requirements on the RMII signals are as follows:

- Avoid routing signal traces across power plane splits to maintain complete reference planes for signal traces.
- Ensure that the spacing between adjacent signal traces complies with the 3W rule.
- The trace length of RMII_TXD[0:1] and RMII_TX_EN is based on that of RMII_CLK, and the error should be within ±500 mils.
  The trace length of RMII_RXD[0:1] and RMII_RX_DV is based on that of RMII_CLK, and the error should be within ±500 mils.
- For MDI0+, MDI0−, MDI1+, and MDI1 signals, the differential trace pair length deviation is ±5 mils, and the differential impedance is 100 ohms.
- The preceding length constraints are jointly controlled by the package and PCB design.

2.6 VI Signals

2.6.1 MIPI Rx

The design requirements on the MIPI/LVDS signals are as follows:

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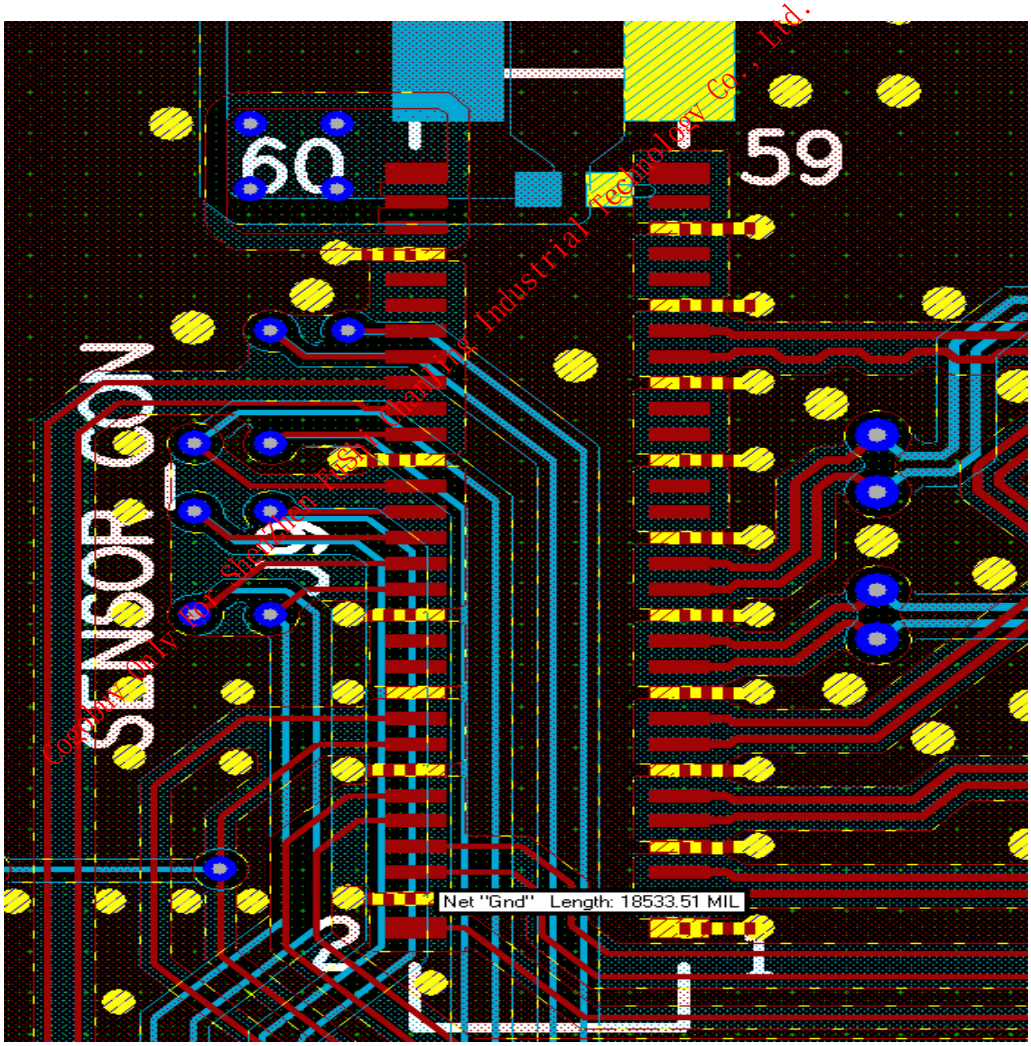
- Route differential signal traces by using the GND layer as the reference plane, and ensure that the reference plane is complete.
- It is recommended that the trace length of the PCB fall within 4 inches, the length deviation of the differential pair P/N fall within 5 mils, and the length deviation between differential trace pairs take sampling differential clocks as reference and fall within ±300 mils (jointly controlled by the package and PCB).
- The differential impedance for the MIPIRX differential trace pairs on the PCB must be 100 ohms±10%.
- Isolate the adjacent differential trace pairs from each other by using GND pins when the differential signals pass the connector. As shown in Figure 2-7, the yellow areas indicate the GND network, and the red areas indicate the differential signal trace pairs.
- The preceding length constraints are jointly controlled by the package and PCB design.

Figure 2-7 MIPI/LVDS differential signal pairs that are isolated from each other



2.6.2 Parallel CMOS

The design requirements on the parallel CMOS signals are as follows:

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- Avoid routing signal traces across power plane splits to maintain complete reference planes for signal traces.
- Ensure that the spacing between adjacent signal traces complies with the 3W rule.
- The trace length of VI_CLK is used as the reference for that of VI_DATA[0:15], VI_HS, and VI_VS, and the deviation should fall within ±500 mils.
- The preceding length constraints are jointly controlled by the package and PCB design.

2.7 VO Signals

The design requirements on the VO signals are as follows:

- Avoid routing signal traces across power plane splits to maintain complete reference planes for signal traces.
- Ensure that the spacing between adjacent signal traces complies with the 3W rule.
- The trace length of VOU_CLK is used as the reference for that of VOU_DATA[0:15], and the deviation should fall within ±500 mils.
- The preceding length constraints are jointly controlled by the package and PCB design.

2.8 Analog Audio Circuit

The design requirements on the analog audio circuit are as follows:

- Place the capacitor connected to the AC_VREF pin close to the master chip, and ensure that the spacing is less than or equal to 150 mils.
- Divide the AC_MICBIAS signal into two channels at the Hi3516C V500 end and use the signals as the bias level and the audio-left channel and audio-right channel respectively. This ensures the audio quality when the microphone (MIC) input is used. For details, see the latest schematic diagram of the HI3516CV500DMEB.
- Route the analog audio input/output signal and MICBIAS signal by using the GND layer as the reference plane, and ensure that the reference plane is complete.
- Surround the analog audio input/output signal and MICBIAS signal with GND traces, and evenly distribute the GND vias between adjacent signal traces. As shown in Figure 2-8.

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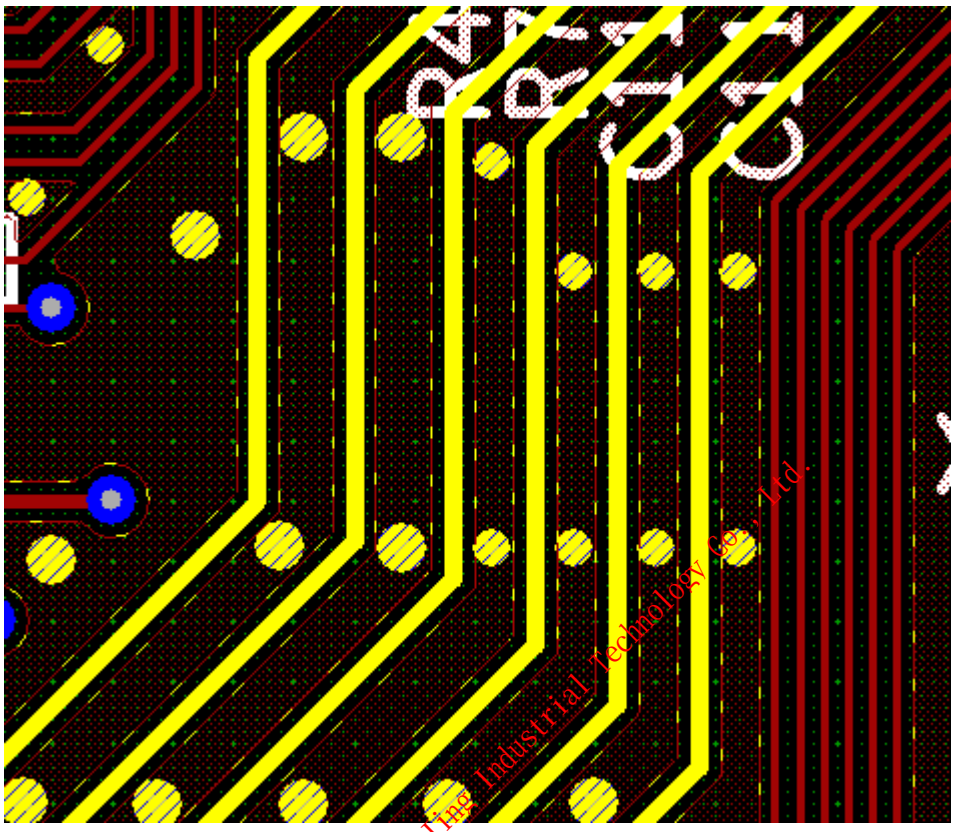
Figure 2-8 Analog audio signals surrounded with GND traces



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2.9 SDIO Signals

The design requirements on the SDIO signals are as follows:

- Ensure that the spacing between adjacent signal traces complies with the 3W rule.
- Design the trace length of SDIO0/1_CDATA[0:3] and SDIO0/1_CCMD based on that of SDIO0/1_CCLK_OUT, and ensure that the deviation falls within ±500 mils.
- Route the SDIO0 data signal traces by using the GND layer as the reference plane if the SDXC card needs to be supported, and ensure that the reference plane is complete.
- The preceding length constraints are jointly controlled by the package and PCB design.

2.10 USB 2.0 Signals

The design requirements on the USB 2.0 signals are as follows:

- Ensure that the length deviation for traces in a differential signal trace pair falls within ±5 mils, and the impedance of the differential trace is 90 ohms±10%.
- Route differential signal traces by using the GND layer as the reference plane, and ensure that the reference plane is complete.

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- When the USB 2.0 interface of Hi3516C V500 connects to an external socket, the trace length of the differential signals should be less than or equal to 5 inches, the number of vias cannot exceed 2, and the length of the external cables must fall within 1.5 m. When the USB 2.0 signals are used for board cascade testing, the trace length of differential signal lines should be less than or equal to 10 inches and the number of vias cannot exceed 2.

  Place a GND via near the via of USB 2.0 signals to obtain better signal quality.
- Keep the USB 2.0 differential traces away from other signal traces, and ensure that the spacing between the USB 2.0 differential traces and other signal traces is greater than 20 mils.
- Place the REXT resistor close to the master chip.
- It is recommended that the parasitic capacitors connected to the ESD components be less than 1 pF.
- The preceding length constraints are jointly controlled by the package and PCB design.

2.11 MIPI TX Signal Design

The design requirements on the MIPI TX signals are as follows:

- The differential impedance for the MIPITX differential trace pairs on the PCB must be 100 ohms±10%.
- Route differential signal traces by using the GND as the reference plane, and ensure that the reference plane is complete.
- If FPC connections are used, it is recommended that the total length of PCB and FPC not exceed 9 inches.
- The length deviation of the differential pair P/N fall within 5 mils. The length deviation between differential trace pairs should fall within 100 mils compared with the CLK trace.
- Keep the differential traces away from other signal traces, and ensure that the spacing between the differential traces and other signal traces is greater than 20 mils.
- The preceding length constraints are jointly controlled by the package and PCB design.

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3 ESD Design of the Entire System

3.1 Background

As the chip performs better and the clock frequency become higher, the entire system is more sensitive to external interference. Therefore, you need to pay special attention to the electrostatic discharge (ESD) part of the entire system design.

The ESD tests of Hi3516C V500 are conducted complying with the JEDEC standard. Hi3516C V500 has passed the ±2000 V test, which meets the industrial standards. However, you need to evaluate the board hardware design and entire system design based on your ESD test standards. This document provides the design recommendations and workarounds based on ESD design risks during the entire system design.

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3.2 ESD Design of the Entire System

- When designing the 24 MHz system clock, use the 4-pin surface mount device (SMD) crystal oscillator, and ensure that its two GND pins and the board GND are completely in contact to improve the anti-interference capability. Route other traces far away from the crystal oscillator area, that is, never route traces under the crystal oscillator.
- Keep the small system away from the metal interfaces during the PCB component layout design. The farther the small system is away from the metal interfaces, the better the ESD performance of the entire system.
- Add ESD protective components for the peripheral interfaces (such as the audio/video I/O interfaces, USB port, and Ethernet port) to improve their anti-interference capability.
- When the entire system is designed as a floating ground device, never use GND plane splits for the metal interfaces on the board.
- Use metal vias as the positioning holes of the board and connect them to the board GND. Ensure that the board GND is fully connected to the metal cover through the screw holes.
- When the entire system is designed as a grounding device, connect the metal cover to the earth, and connect the protective GND splits to the board digital GND in single-point mode. Ensure that the single point is far away from the circuits of the small system and close to the power connector of the entire system.
- Use the metal cover for the interface connectors (such as the USB port with positioning screws or the RJ45 connector with a tab), and ensure that the connectors and the metal cover of the entire system are completely in contact (using the conductive pillar or conductive gasket if necessary).

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You need to evaluate the preceding recommendations based on your standards and project experience.

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4 Design Recommendations for Chip Heat Dissipation

4.1 Maximum Power Consumption

The maximum power consumption of Hi3516C V500 is estimated to be 1.5 W based on the simulation result, which is for reference only. The final power consumption data is subject to the latest *Hi3516C V500 Power Consumption Test Report*.

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