Hi3516D V300 DDR3 Configuration Guide

Issue 00B02

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About This Document

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3516D	V300

Intended Audience

This document is intended for:

- Technical support engineers
- Software development engineers

Change History

Changes between document issues are cumulative. The latest document issue contains all the changes made in earlier issues.

Issue 00B03 (2019--)

This issue is the third draft release, which incorporates the following changes:

Section 3.1 is modified.

Sections 3.2 and 3.3 are added.

Issue 00B02 (2019-03-12)

This issue is the second draft release.

Issue 00B01 (2019-01-15)

This issue is the first draft release.

Contents

1 DDR3 Driver Configuration

1.1 CLK/AC Driver Configuration

- Register address
  DDR PHY: 0x1206d018
- Register description
  - Bit[25:23]: CK driver
  - Bit[22:20]: 2T driver
  - Bit[19:17]: 1T driver
- Drive strength
  - 000: disabled
  - 001: 240 ohms
  - 010: 120 ohms
  - 011: 80 ohms
  - 100: 60 ohms
  - 101: 48 ohms
  - 110: 40 ohms
  - 111: 34 ohms

NOTE
The 1T signals refer to CKE, CSN, ODT, and RESET signals, while the 2T signals refer to the AC signals except 1T signals.

1.2 DQS/DQ Driver Configuration in the Write Direction

- Register address
  DDR PHY: 0x1206d204 (bytes 0–1) and 0x1206d304 (bytes 2–3)
- Register description
  - Bit[16:14]: DQS driver in the write direction
  - Bit[13:11]: DQ driver in the write direction
- Drive strength
  - 000: disabled

- 001: 240 ohms
- 010: 120 ohms
- 011: 80 ohms
- 100: 60 ohms
- 101: 48 ohms
- 110: 40 ohms
- 111: 34 ohms

1.3 DQS/DQ Driver Configuration in the Read Direction

- Register address
  DDR PHY: 0x1206c064
- Register description
  Bit[21] and bit[17]: DQS/DQ driver in the read direction
- Drive strength
  - 00: 40 ohms
  - 01: 34 ohms
  - 10: reserved
  - 11: reserved

2 DDR3 ODT Configuration

2.1 DQS/DQ ODT Configuration in the Write Direction

2.1.1 ODT Enable in the Write Direction

- Register address
  DDRC: 0x120680a0
- Register description
  - Bit[0] = 0: ODT disabled in the write direction
  - Bit[0] = 1: ODT enabled in the write direction

2.1.2 ODT in the Write Direction

- Register address
  DDR PHY: 0x1206c064
- Register description
  - Bit[25], bit[22], and bit[18]: DQS/DQ ODT configuration in the write direction
- ODT values in the write direction
  - 000: ODT disabled
  - 001: 60 ohms
  - 010: 120 ohms
  - 011: 40 ohms

NOTICE

The ODT configuration in the write direction takes effect for both DQS and DQ signals.

2.2 DQS/DQ ODT Configuration in the Read Direction

2.2.1 ODT Enable in the Read Direction

- Register address

  DDR PHY: 0x1206d248 (bytes 0–1) and 0x1206d348 (bytes 2–3)
- Register description
  - Bit[3] = 0: ODT enabled in the read direction
  - Bit[3] = 1: ODT disabled in the read direction

2.2.2 ODT Values in the Read Direction

- Register address

  DDR PHY: 0x1206d204 (bytes 0–1) and 0x1206d304 (bytes 2–3)
- Register description
  - Bit[31:29]: DQS ODT in the read direction
  - Bit[28:26]: DQ ODT in the read direction
- ODT values in the read direction
  - 000: disabled
  - 001: 120 ohms
  - 010: 60 ohms
  - 011: 40 ohms
  - 100: 30 ohms
  - 101: 24 ohms
  - 110: 20 ohms
  - 111: 17 ohms

3 DDR3 Capacity Configuration

3.1 U-Boot Table Overview

The Hi3516D V300 memory interface can connect to a DDR3 DRAM with a maximum data bit width of 32 bits in single-channel mode. The DDR configuration is implemented in the U-Boot table. Hi3516D V300 provides two DDR3 U-Boot tables, corresponding to the DDR3 design schemes of DMEB and DMEPRO.

- DMEB U-Boot table: *Hi3516DV300-DMEB_4L_FLYBY-DDR3_1800M_512MB_16bitx2-A7_900M-SYSBUS_300M*
- DMEBPRO U-Boot table: *Hi3516DV300-DMEBPRO_6L_T-DDR3_1800M_1GB_16bitx2-A7_900M-SYSBUS_300M*

Table 3-1 lists the DDR specifications supported by the U-Boot tables.

Table 3-1 DDR specifications supported by the U-Boot tables

U-Boot Table	Total Capacity/Total Bit Width	Channel	DDR Type	DDR Rate (Mbit/s)	Rank Count	DDR Bit Width (Bit Width/PCS x Count)	Capacity/PCS
DMEB U-Boot table	512 MB/32 bits	Channel 0	DDR3	1800	1	16 bits x 2	2 Gbits
DMEBPRO U-Boot table	512 MB/32 bits or 1 GB/32 bits	Channel 0	DDR3	1800	1	16 bits x 2	2 Gbits or 4 Gbits

NOTE

Based on one DDR table, if the capacity of each DDR memory is reduced and the capacities of all DDR memories are the same, the table configuration does not need to be modified.

3.2 DMEB Capacity Modification

The default DMEB U-Boot table supports a bit width up to 32 bits in single channel mode and a total capacity of 512 MB with 2 Gbits each. If the DDR capacity changes, you need to

modify the U-Boot table accordingly. Table 3-2 lists the common capacity design solutions and configuration changes.

Table 3-2 DMEB capacity solutions

DMEB Capacity Solution	Total Capacity/Total Bit Width	Channel	DDR Type	DDR Rate (Mbit/s)	Rank Count	DDR Bit Width (Bit Width/PCS x PCS Count)	DDR Capacity/PCS
Solution 1	1 GB/32 bits	Channel 0	DDR3	1800	1	16 bits x 2	4 Gbits
Solution 2	256 MB/16 bits	Channel 0	DDR3	1800	1	16 bits x 1	2 Gbits
Solution 3	512 MB/16 bits	Channel 0	DDR3	1800	1	16 bits x 1	4 Gbits

3.2.1 DMEB Capacity Solution 1

Make the following modifications for the design of DMEB solution 1 based on the default U-Boot table.

Modification on the Address Mapping Space

Original DDRC configuration in the U-Boot table:

AXI_REGION_MAP	0x0100	0x1580	0	write	31	0	0x0000000FD

Modify the configuration as follows:

AXI_REGION_MAP	0x0100	0x1680	0	write	31	0	0x0000000FD

Capacity Modification

Original DDRC configuration in the U-Boot table:

DMC0_CFG_RNKVOL	0x8060	0x132	0	write	31	0	0x0000000FD

Modify the configuration as follows:

DMC0_CFG_RNKVOL	0x8060	0x142	0	write	31	0	0x0000000FD

tRFC Parameter Modification

Original DDRC configuration in the U-Boot table:

DMC0_CFG_TIMING8	0x8120	0x2592c07	0	write	31	0	0x0000000FD

Modify the configuration as follows:

DMC0_CFG_TIMING8	0x8120	0x4623007	0	write	31	0	0x0000000FD

3.2.2 DMEB Capacity Solution 2

Make the following modifications for the design of DMEB solution 2 based on the default U-Boot table.

Bit Width Modification

Original DDRC configuration in the U-Boot table:

DMC0_CFG_DDRMODE	0x8050	0xC10226	0	write	31	0	0x0000000FD

Modify the configuration as follows:

DMC0_CFG_DDRMODE	0x8050	0xC10216	0	write	31	0	0x0000000FD

Disable of Upper 16 Bits

Original DDRPHY0 configuration in the U-Boot table:

DXCTRL(BYTE2)	0xc308	0xf80000	0	write	31	0	0x0000000FD
DXCTRL(BYTE3)	0xc388	0xf80000	0	write	31	0	0x0000000FD
DXNBISTCTRL	0xc300	0x2501FF01	0	write	31	0	0x0000000FD
DXNBISTCTRL	0xc380	0x2501FF01	0	write	31	0	0x0000000FD

Modify the configuration as follows:

DXCTRL(BYTE2)	0xc308	0xf80003	0	write	31	0	0x0000000FD
DXCTRL(BYTE3)	0xc388	0xf80003	0	write	31	0	0x0000000FD
DXNBISTCTRL	0xc300	0x0	0	write	31	0	0x0000000FD
DXNBISTCTRL	0xc380	0x0	0	write	31	0	0x0000000FD

3.2.3 DMEB Capacity Solution 3

Combine the modifications of DMEB solutions 1 and 2 for the design of solution 3 based on the default U-Boot table.

3.3 DMEBPRO Capacity Modification

The default DMEBPRO U-Boot table supports a bit width up to 32 bits in single channel mode and a total capacity of 1 GB or 512 MB with 4 Gbits or 2 Gbits each. If the DDR capacity changes, you need to modify the U-Boot table accordingly. Table 3-3 lists the common capacity design solutions and configuration changes.

Table 3-3 DMEBPRO capacity solutions

DMEBPRO Capacity Solution	Total Capacity/Total Bit Width	Channel	DDR Type	DDR Rate (Mbit/s)	Rank Count	DDR Bit Width (Bit Width/PCS x PCS Count)	DDR Capacity/PCS
Solution 1	512 MB/16 bits or 256 MB/16 bits	Channel 0	DDR3	1800	1	16 bits x 1	4 Gbits or 2 Gbits

3.3.1 DMEBPRO Capacity Solution 1

Make the following modifications for the design of DMEBPRO solution 1 based on the default U-Boot table.

Bit Width Modification

Original DDRC configuration in the U-Boot table:

DMC0_CFG_DDRMODE	0x8050	0xC10226	0	write	31	0	0x0000000FD

Modify the configuration as follows:

DMC0_CFG_DDRMODE	0x8050	0xC10216	0	write	31	0	0x0000000FD

Disable of Upper 16 Bits

Original DDRPHY0 configuration in the U-Boot table:

DXCTRL(BYTE2)	0xc308	0xf80000	0	write	31	0	0x0000000FD

DXCTRL(BYTE3)	0xc388	0xf80000	0	write	31	0	0x0000000FD
DXNBISTCTRL	0xc300	0x2501FF01	0	write	31	0	0x0000000FD
DXNBISTCTRL	0xc380	0x2501FF01	0	write	31	0	0x0000000FD

Modify the configuration as follows:

DXCTRL(BYTE2)	0xc308	0xf80003	0	write	31	0	0x0000000FD
DXCTRL(BYTE3)	0xc388	0xf80003	0	write	31	0	0x0000000FD
DXNBISTCTRL	0xc300	0x0	0	write	31	0	0x0000000FD
DXNBISTCTRL	0xc380	0x0	0	write	31	0	0x0000000FD