



Pharos University in Alexandria
Faculty of Engineering
Computer Engineering Department
EE232&E232!! :Electronics

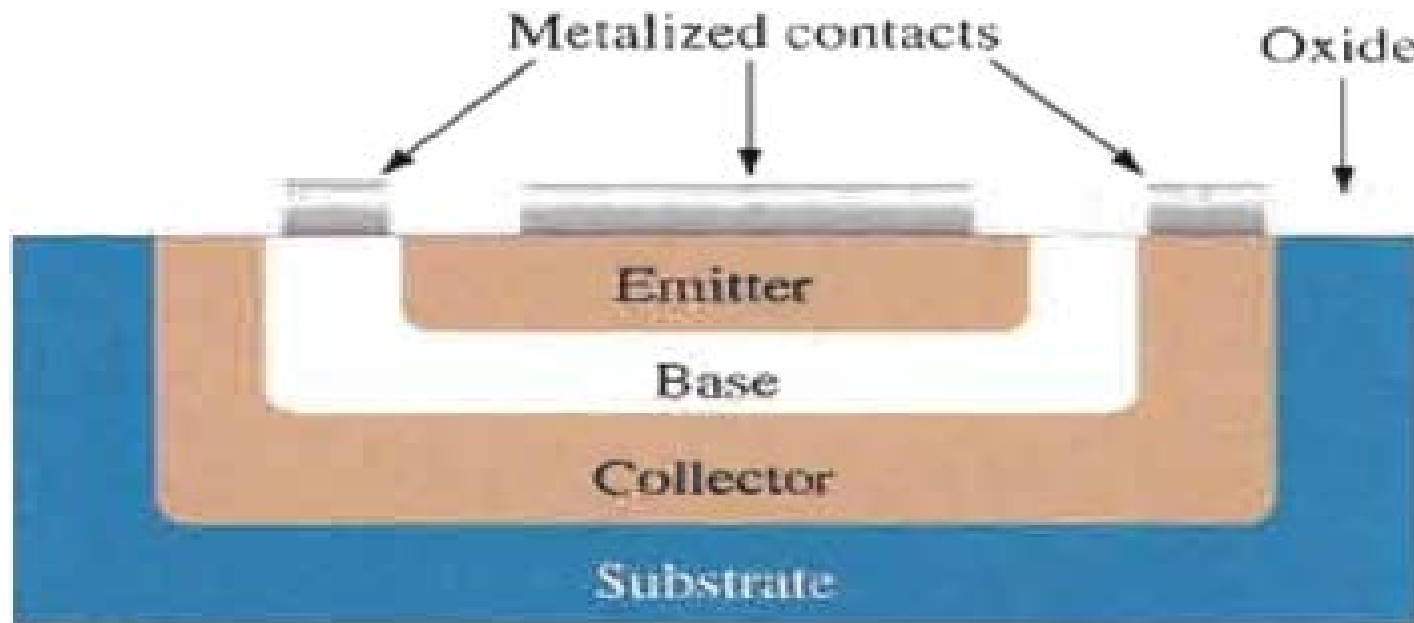
Chapter 5

Bipolar Junction Transistors

Lecture 9

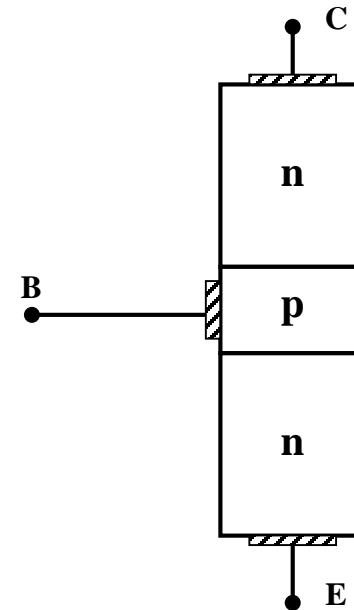
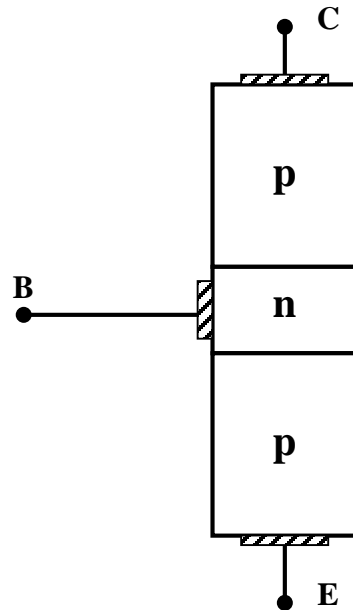
Transistor Structure:

The Bipolar Junction Transistor (BJT) is constructed with three doped semiconductor regions separated by two PN junctions. The three regions are called emitter, base, and collector

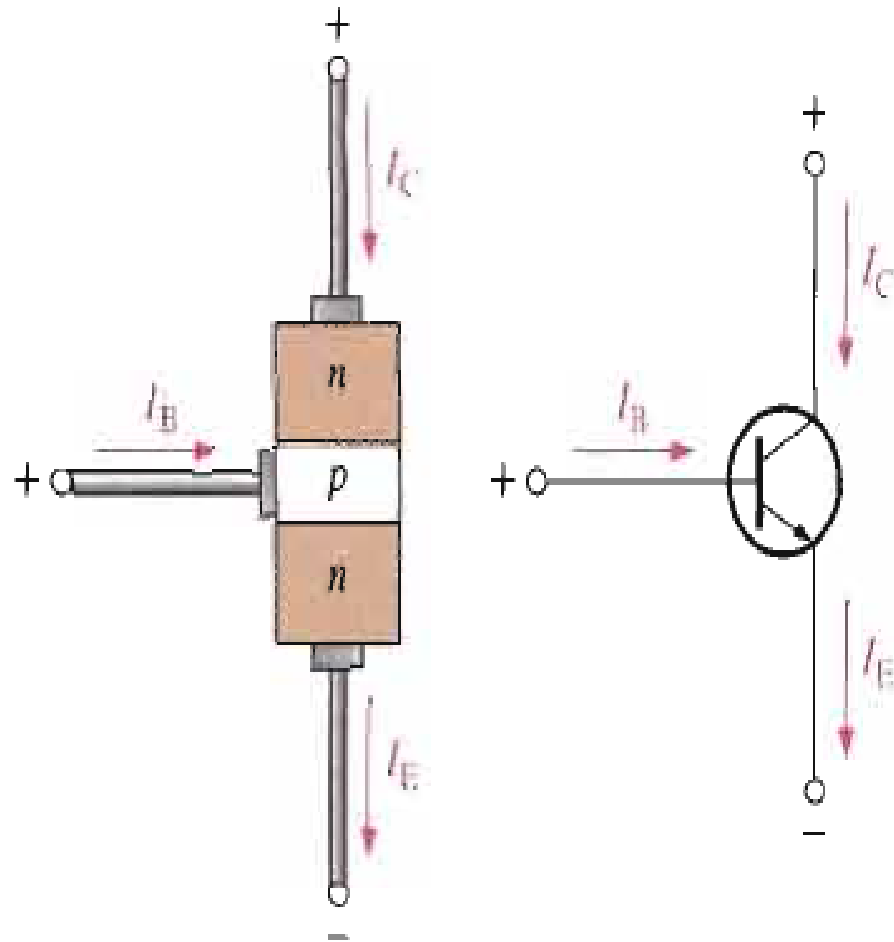


Two Types of BJTs:

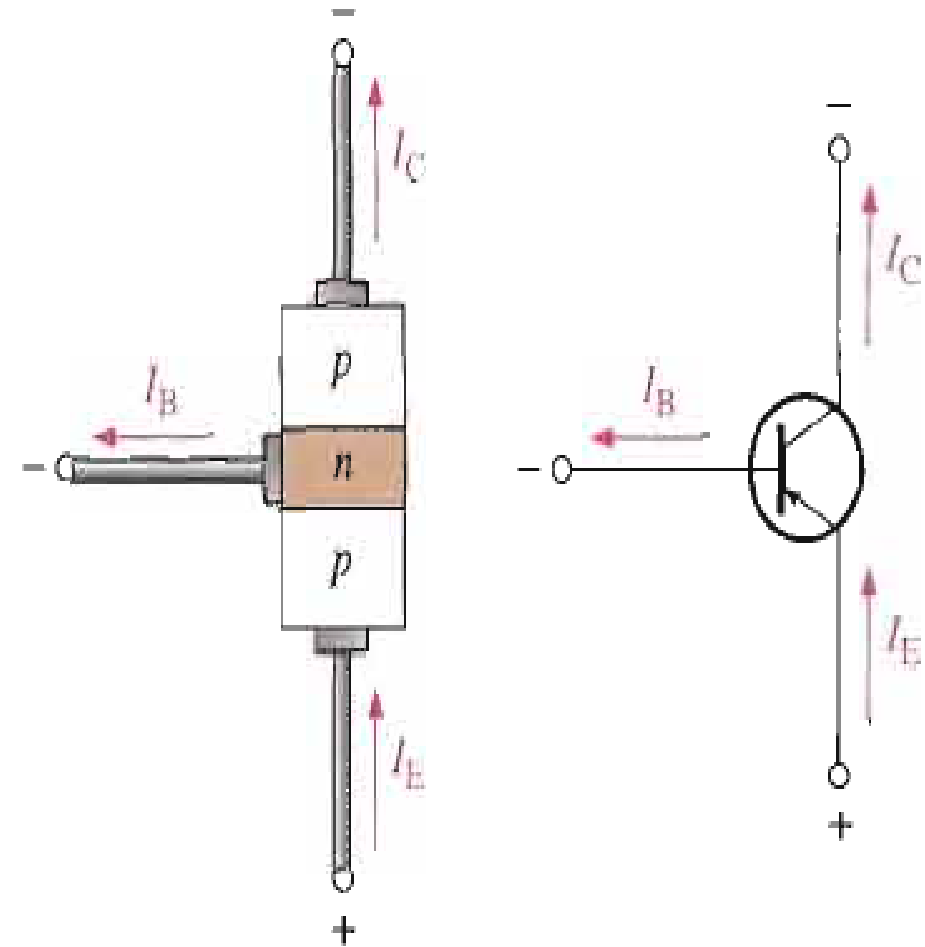
1. NPN consists of two n regions separated by a p region
2. PNP consists of two p regions separated by a n region



Standard BJT Symbols



(a) *npn*

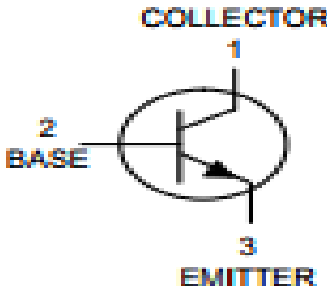


(b) *pnp*

BJT Data Sheets

Amplifier Transistors

NPN Silicon



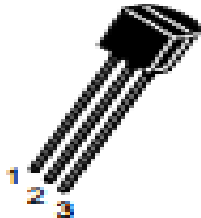
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CBO}	75	Vdc
Emitter–Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous	I_C	600	mA dc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

P2N2222A



CASE 29-04, STYLE 17
TO-92 (TO-226AA)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

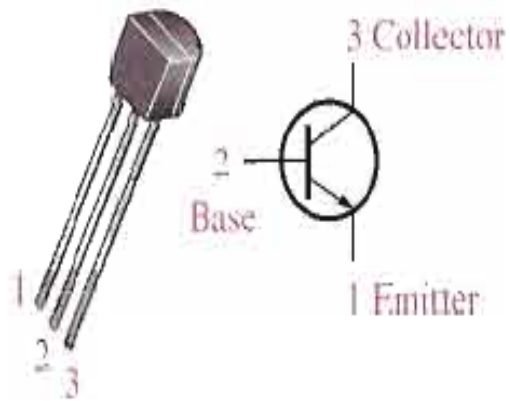
Collector–Emitter Breakdown Voltage ($I_C = 10\text{ mA}_{dc}$, $I_B = 0$)	$V_{(BR)CEO}$	40	—	V _{dc}
Collector–Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}_{dc}$, $I_E = 0$)	$V_{(BR)CBO}$	75	—	V _{dc}
Emitter–Base Breakdown Voltage ($I_E = 10\text{ }\mu\text{A}_{dc}$, $I_C = 0$)	$V_{(BR)EBO}$	6.0	—	V _{dc}
Collector Cutoff Current ($V_{CE} = 60\text{ V}_{dc}$, $V_{EB(off)} = 3.0\text{ V}_{dc}$)	I_{CEX}	—	10	nA _{dc}
Collector Cutoff Current ($V_{CB} = 60\text{ V}_{dc}$, $I_E = 0$) ($V_{CB} = 60\text{ V}_{dc}$, $I_E = 0$, $T_A = 150^\circ\text{C}$)	I_{CBO}	— —	0.01 10	μA_{dc}
Emitter Cutoff Current ($V_{EB} = 3.0\text{ V}_{dc}$, $I_C = 0$)	I_{EBO}	—	10	nA _{dc}
Collector Cutoff Current ($V_{CE} = 10\text{ V}$)	I_{CEO}	—	10	nA _{dc}
Base Cutoff Current ($V_{CE} = 60\text{ V}_{dc}$, $V_{EB(off)} = 3.0\text{ V}_{dc}$)	I_{BEX}	—	20	nA _{dc}

Transistor casing terminal identification

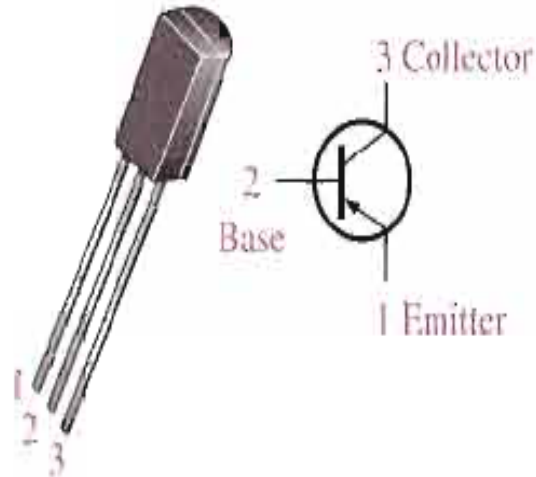
Gold , Aluminum, Nical, Plastic case

Types

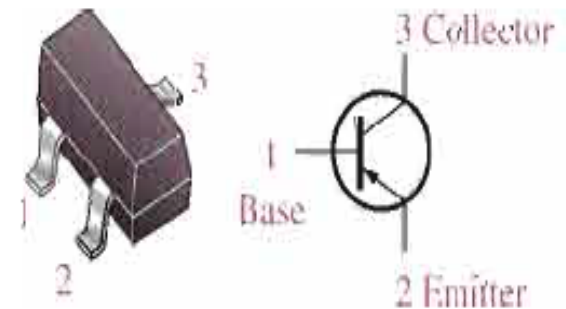
Plastic Cases for Small Signal Tr



(a) TO-92 or TO-226AA

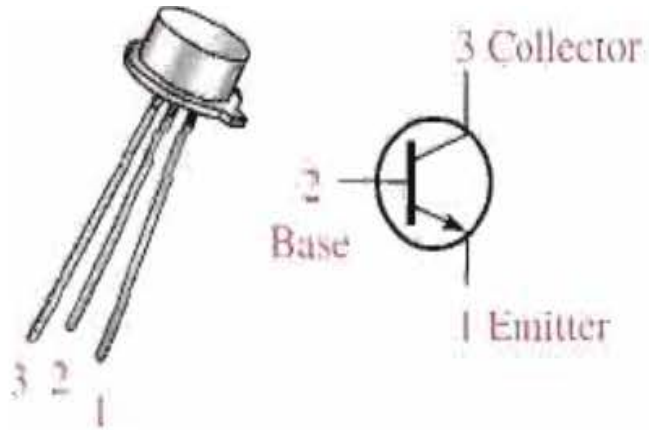


(b) TO-92 or TO-226AE

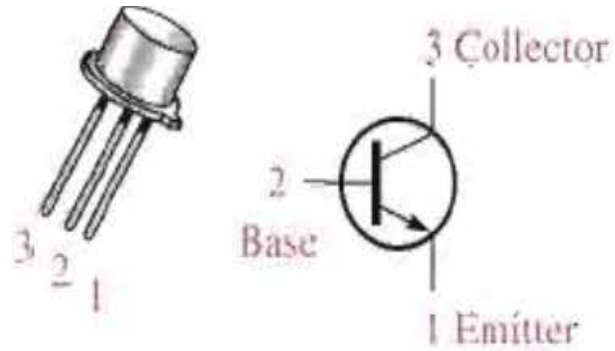


(c) SOT-23 or TO-236AB

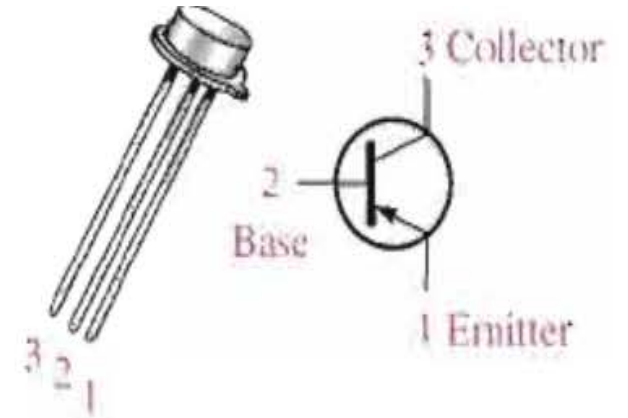
Metal Cases for Small Signal Tr



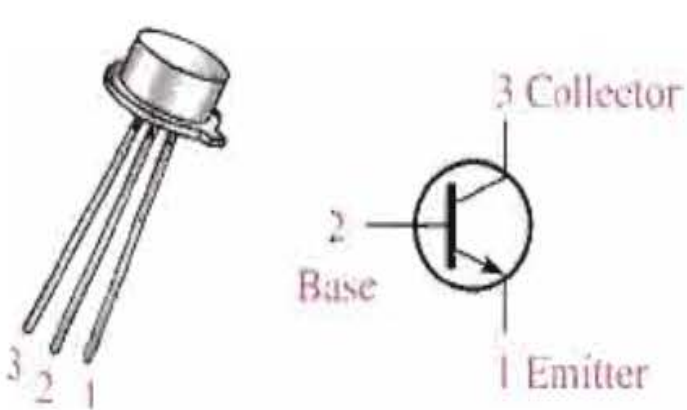
(a) TO-18 or TO-206AA



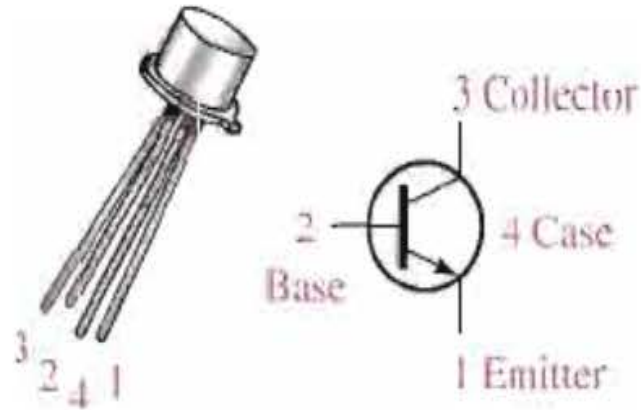
(b) TO-39 or TO-205AD



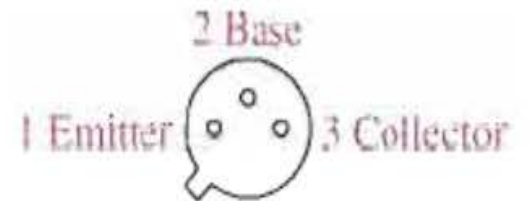
(c) TO-46 or TO-206AB



(d) TO-52 or TO-206AC

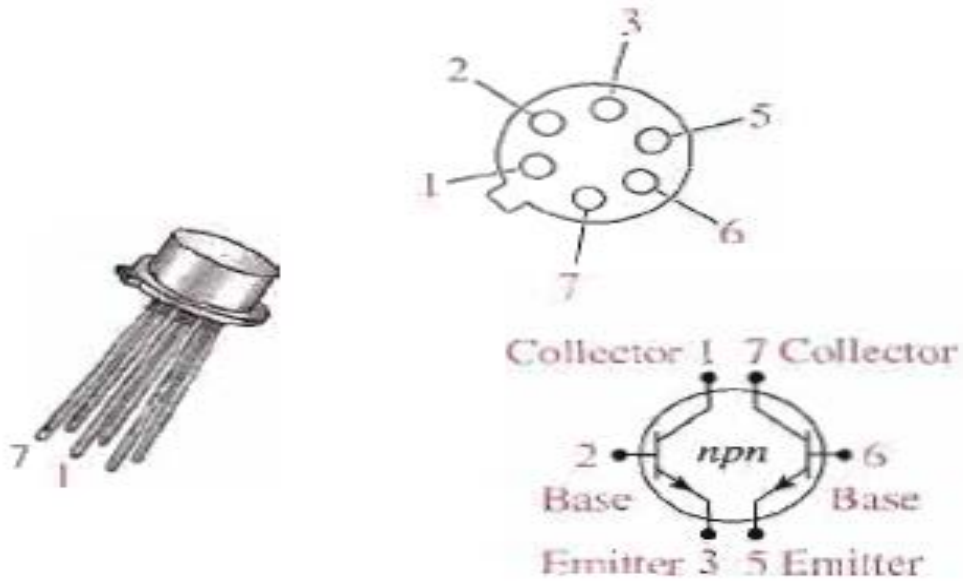


(e) TO-72 or TO-206AF

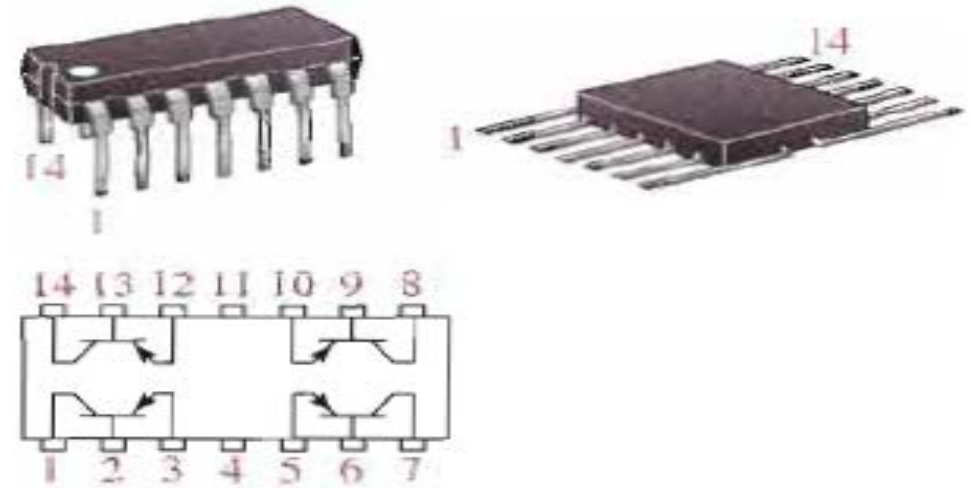


(f) Pin configuration (bottom view).
Emitter is closest to tab.

Typical Multiple Transistor Packages



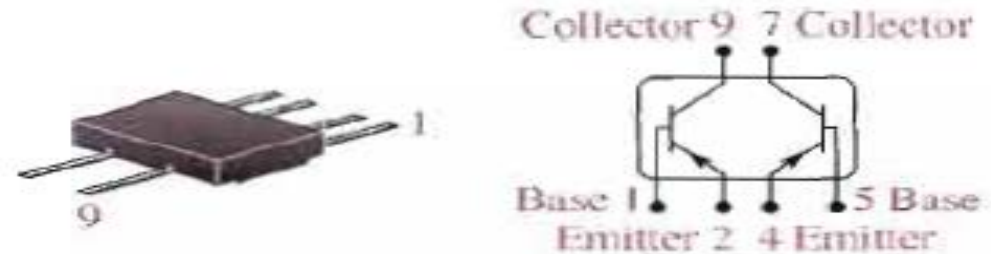
(a) Dual metal can



(b) Quad dual in-line (DIP) and quad flat-pack. Dot indicates pin 1.



(c) Quad small outline (SO) package for surface-mount technology

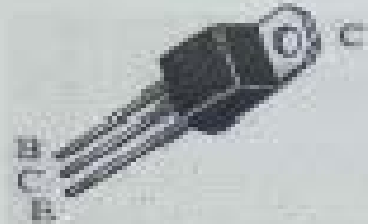


(d) Dual ceramic flat-pack

Typical Power Transistor



(a) TO-3 or TO-204AE



(b) TO-218



(c) TO-218AC



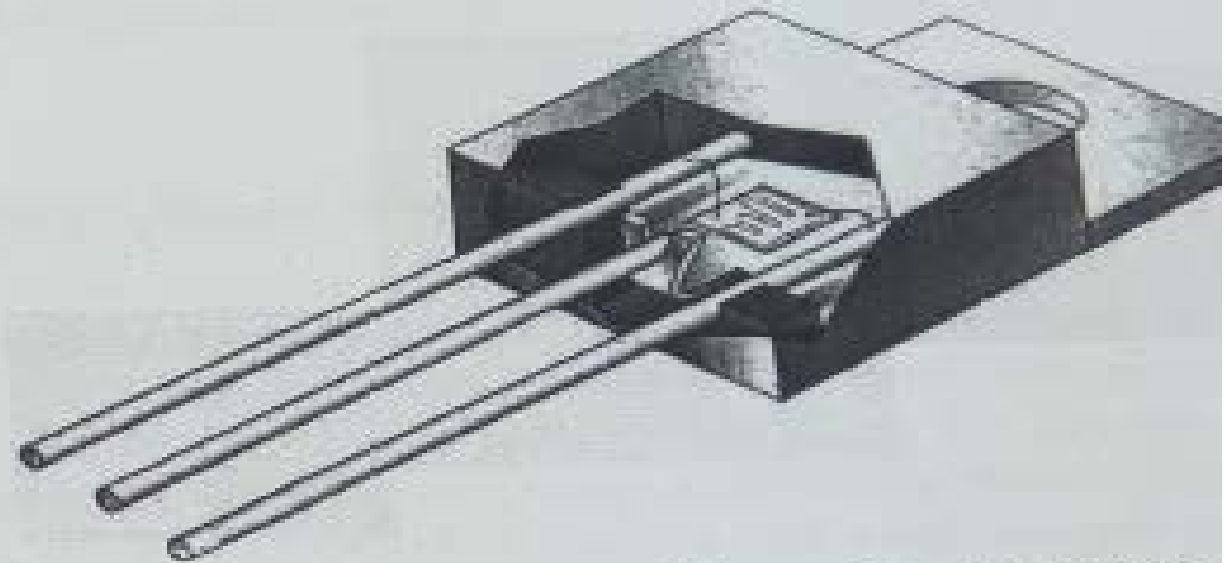
(d) TO-220AB



(e) TO-225AA

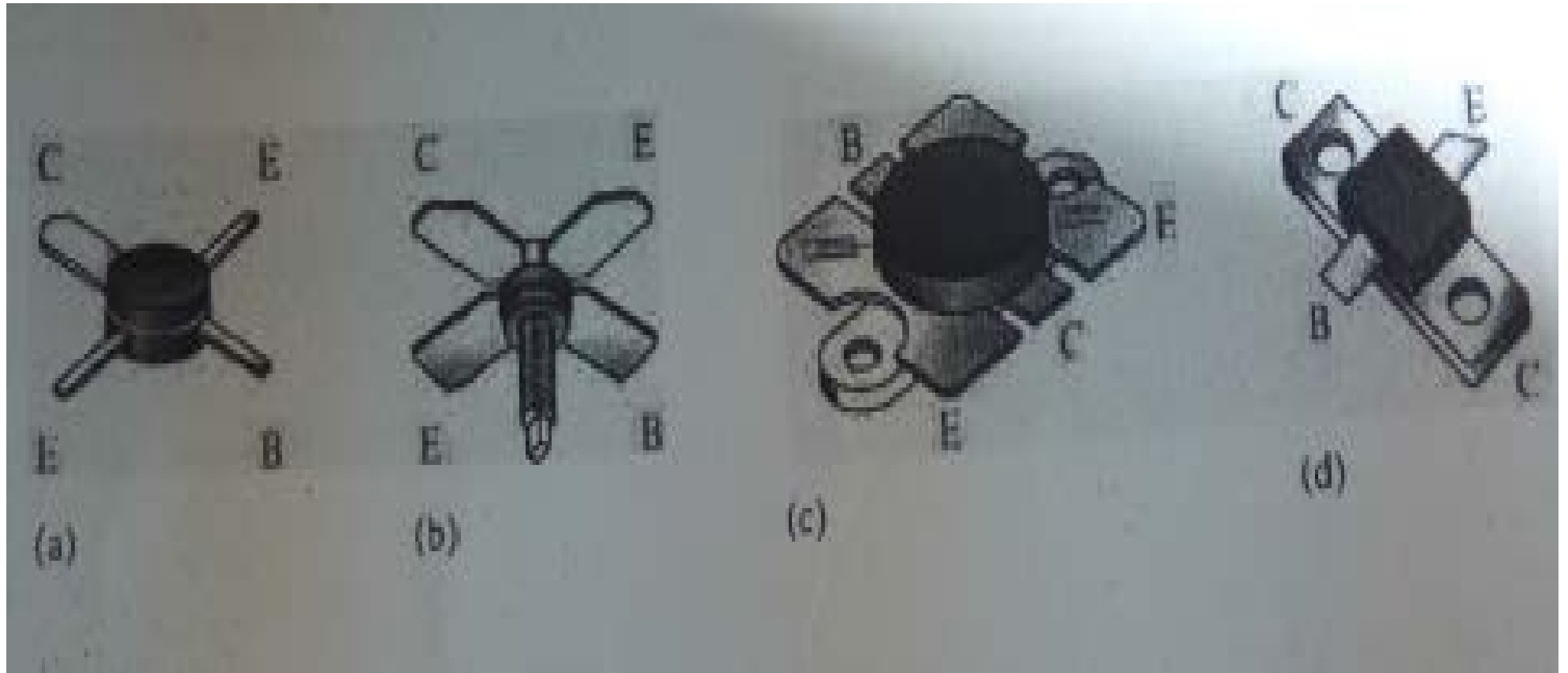


(f) Surface-mount technology



(g) Greatly enlarged cutaway view of tiny transistor chip mounted in encapsulated package

Typical RF Transistor



Transistor testing :

- ① Curve tracer
- ② digital meter
- ③ Ohmmeter

→ digital meter

For npn
Collector open, B-E Junction → F.B → Forward bias
+ve connect base, -ve connect to emitter

$$V_{BE} = 0.7V \text{ (0.5V} \rightarrow 0.9V)$$

$0.3 \rightarrow \text{Ge}$
 $1.2 \rightarrow \text{GaAs}$

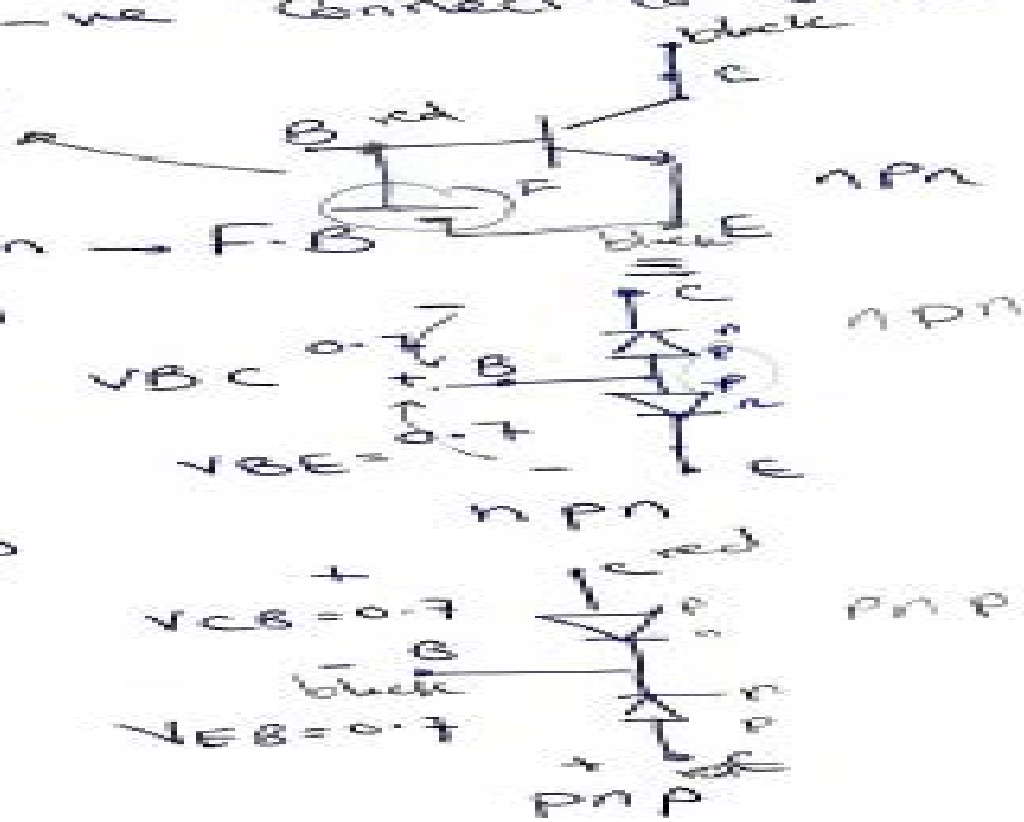
Emitter open, B-C Junction → F.B → Forward bias
+ve → base -ve → collector

$$V_{BC} = 0.7 \text{ (0.5V} \rightarrow 0.9V)$$



Reverse

Same Concept for pnp



if npn

(10)

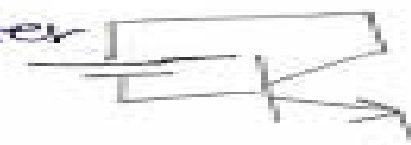
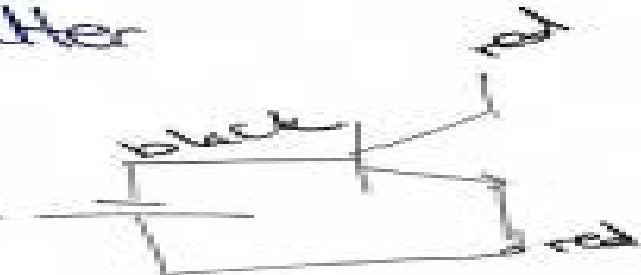
FOR R.B \rightarrow BE

-ve \rightarrow base, +ve \rightarrow Emitter
 $V_{BE} \rightarrow 2.6V$

R.B \rightarrow BC

-ve \rightarrow Base, +ve \rightarrow Collector

$V_{BC} = 2.6$



سليم

کرتہ نتائج آن T_r
مقی نقول T_r باب

if F.B, R.B

$V_{BE} = V_{BC} = 2.6$
OR $V_{BE} = V_{BC} = \text{Zero}$
میں سے

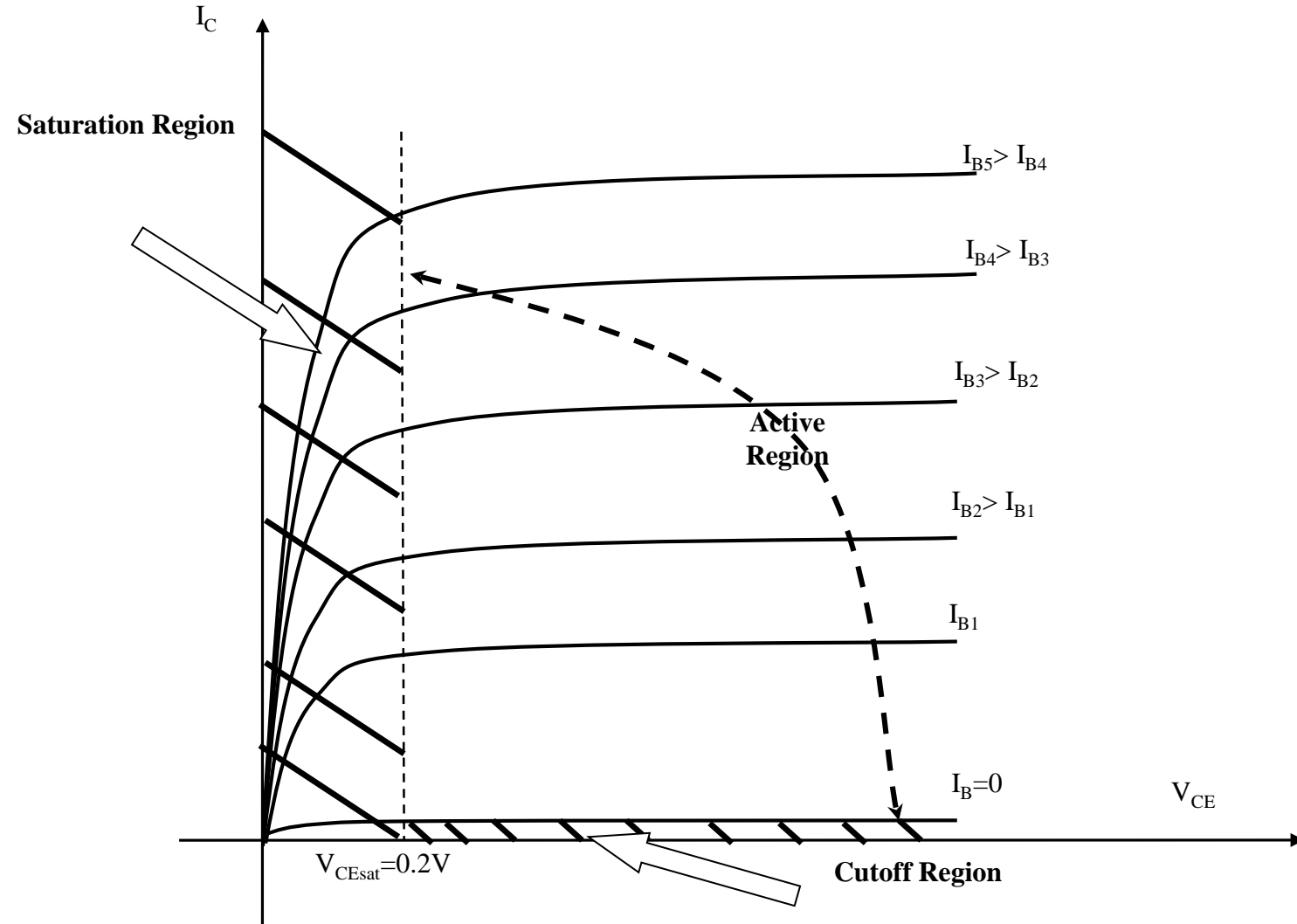
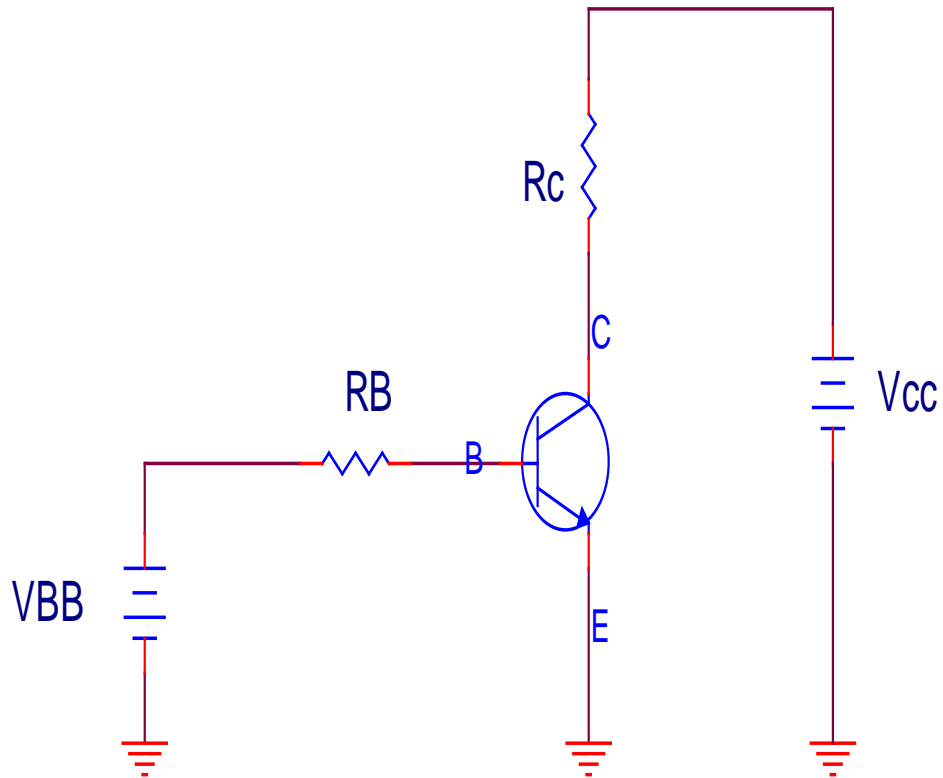
\rightarrow Ohmmeter

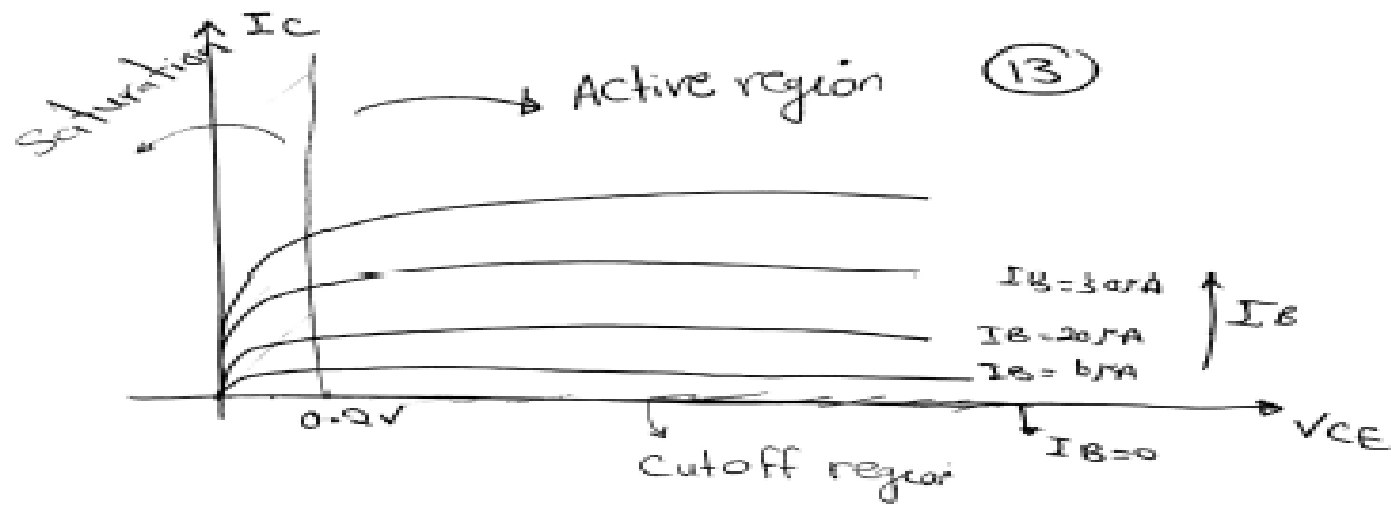
F.B \rightarrow low resistance \equiv 100 Ω to few kilohms
R.B \rightarrow high resistance $>$ 100k Ω

Transistor Under Bias

E-B	B-C	Mode of operation	Application
Forward	Reverse	Active mode	Amplifier
Forward	Forward	Saturation mode	Switch on (short circuit)
Reverse	Reverse	Cut- off mode	Switch off (open circuit)
Reverse	Forward	No use	No use

BJT O/P Characteristics and its Modes of Operation:





③ Cut off region

(14)

$$I_B = 0$$

$$I_C = I_E = 0 \quad \text{No Current}$$

① Active region

used as amplifier

$$V_{CE} > 0.2V \quad I_B > 0 \quad V_{BE} = 0.7V$$

$$I_C \approx I_E \approx \beta I_B, \quad \beta = \frac{\alpha}{1-\alpha}$$

② Saturation region

$$V_{CE} \leq 0.2$$

$$V_{CEsat} \approx 0.2V$$

$$V_{BEsat} = 0.7V$$

$$I_{Csat} \leq I_{Esat} \neq \beta I_B$$

↳ (Constant for different I_B value)

BJT as amplifier: 15

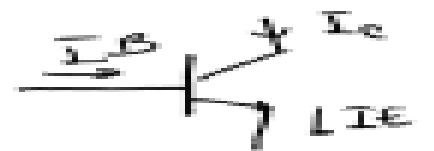
E-B Junction F
B-C Junction R

$$I_C = \alpha I_E$$

α : Current transfer ratio
usually $\alpha = 1$



$$I_C \approx I_E$$



β : amplification factor
depend on the operating temperature
its value increases with increasing temperature

$$I_C = \beta I_B$$

$$\alpha = \frac{\beta}{1 + \beta}$$

$$50 \leq \beta \leq 400$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

If not given put $\beta = 100$

$$I_E = I_C + I_B = (1 + \beta) I_B \approx R T_D$$

DC Solution & operating point (18)

Steps

- ① All Capacitors must be open circuit (o.c)
- ② Assume that BJT in active mode (F-R) (Amplifier)
 $V_{BE} = 0.7$ $I_C \approx I_E \approx \beta I_B$ $\beta = \frac{\alpha}{1-\alpha}$
 $\alpha = \frac{\beta}{1+\beta}$

③ We have 2 loops

④ Base - Emitter loop (B-E)

to get I_B

$$I_C \approx I_E \approx \beta I_B - \checkmark$$



⑤ Collector - Emitter loop (C-E)

get $V_{CE} = \checkmark$

if $V_{CE} > 0.2V$
our assumption
Correct
Active

$V_{CE} \leq 0.2V$

our assumption wrong
BJT in Saturation

Steps

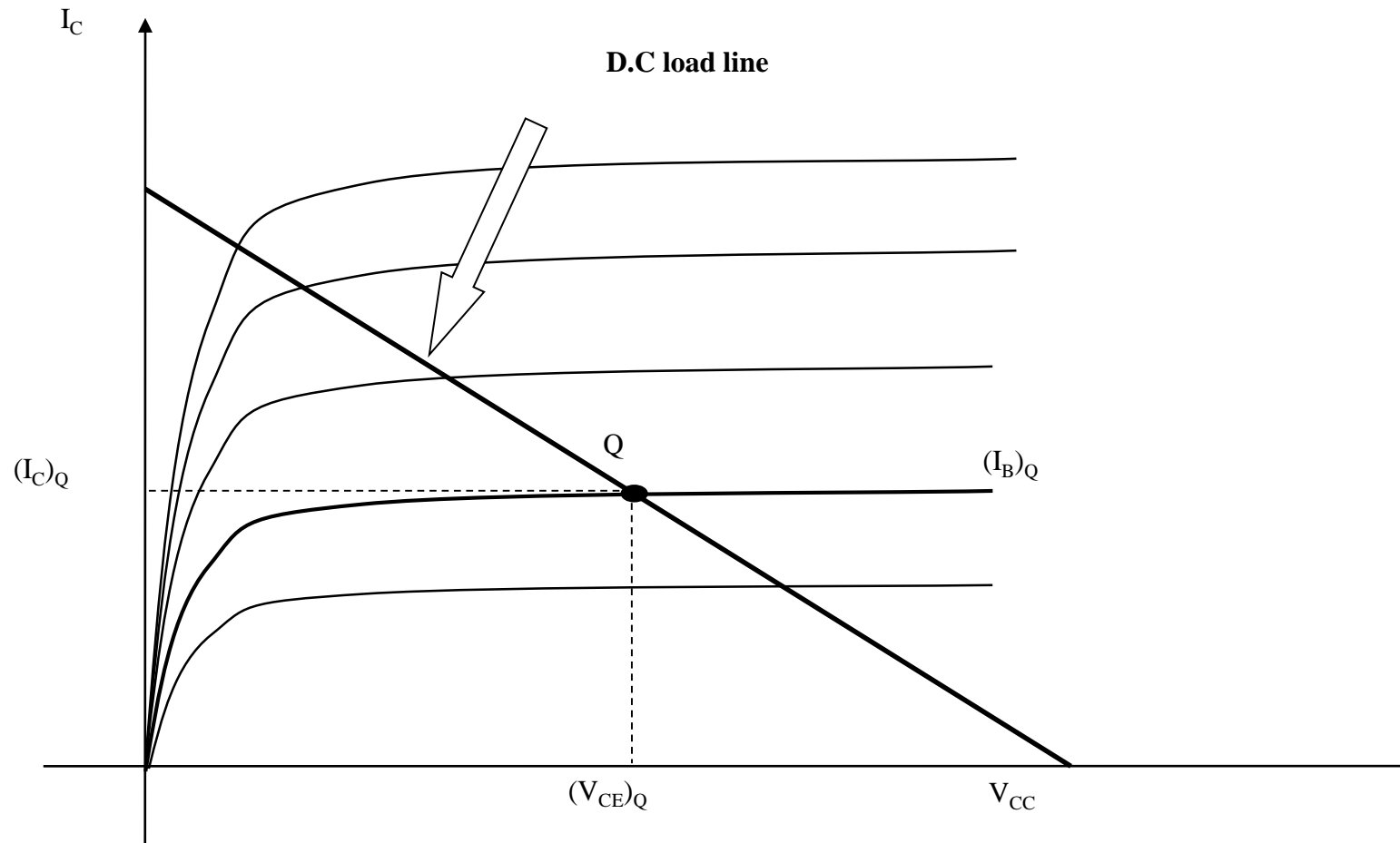
① E - C loop

$$V_{CE_{sat}} = 0.2V \rightarrow I_{C_{sat}} = I_E$$

② B - E loop

$$\rightarrow I_B$$

The DC Operating Point (Q-point):



BJT Amplifier Configurations:

The BJT amplifier has three circuit configurations:

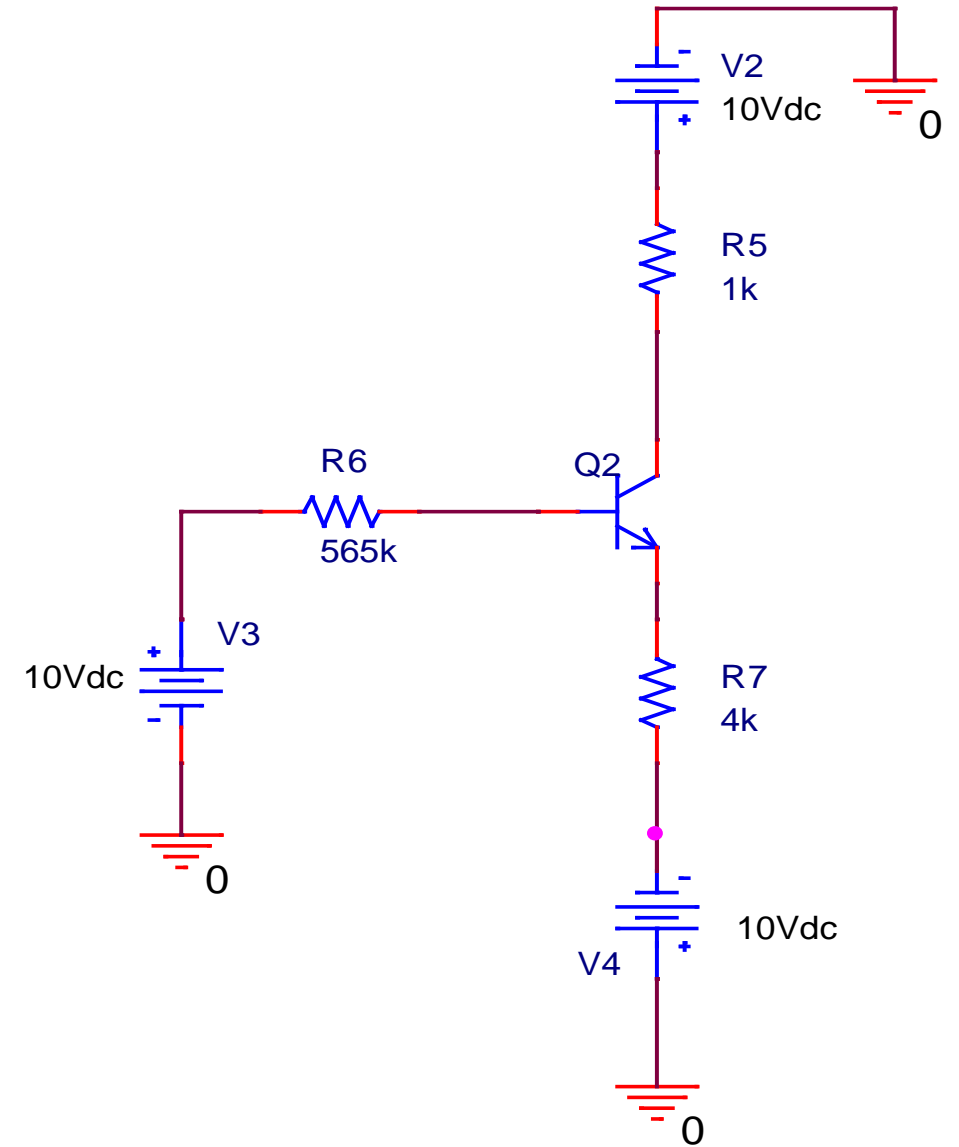
- a. **Common Emitter (CE):** The emitter is connected to the ground, the i/p signal is applied to the base and the o/p signal is on the collector.
- b. **Common Base (CB):** The base is connected to the ground, the i/p signal is applied to the emitter and the o/p signal is on the collector.
- c. **Common Collector (CC):** The collector is connected to the ground, the i/p signal is applied to the base and the o/p signal is on the emitter.

Example

$$\beta = 100$$

For the shown circuit,

- Find I_B , I_E , I_C , and sketch the DC load line and locate the operating point
- Repeat if $R_C = 11 \text{ k}\Omega$



Sol

KVL at B-E loop

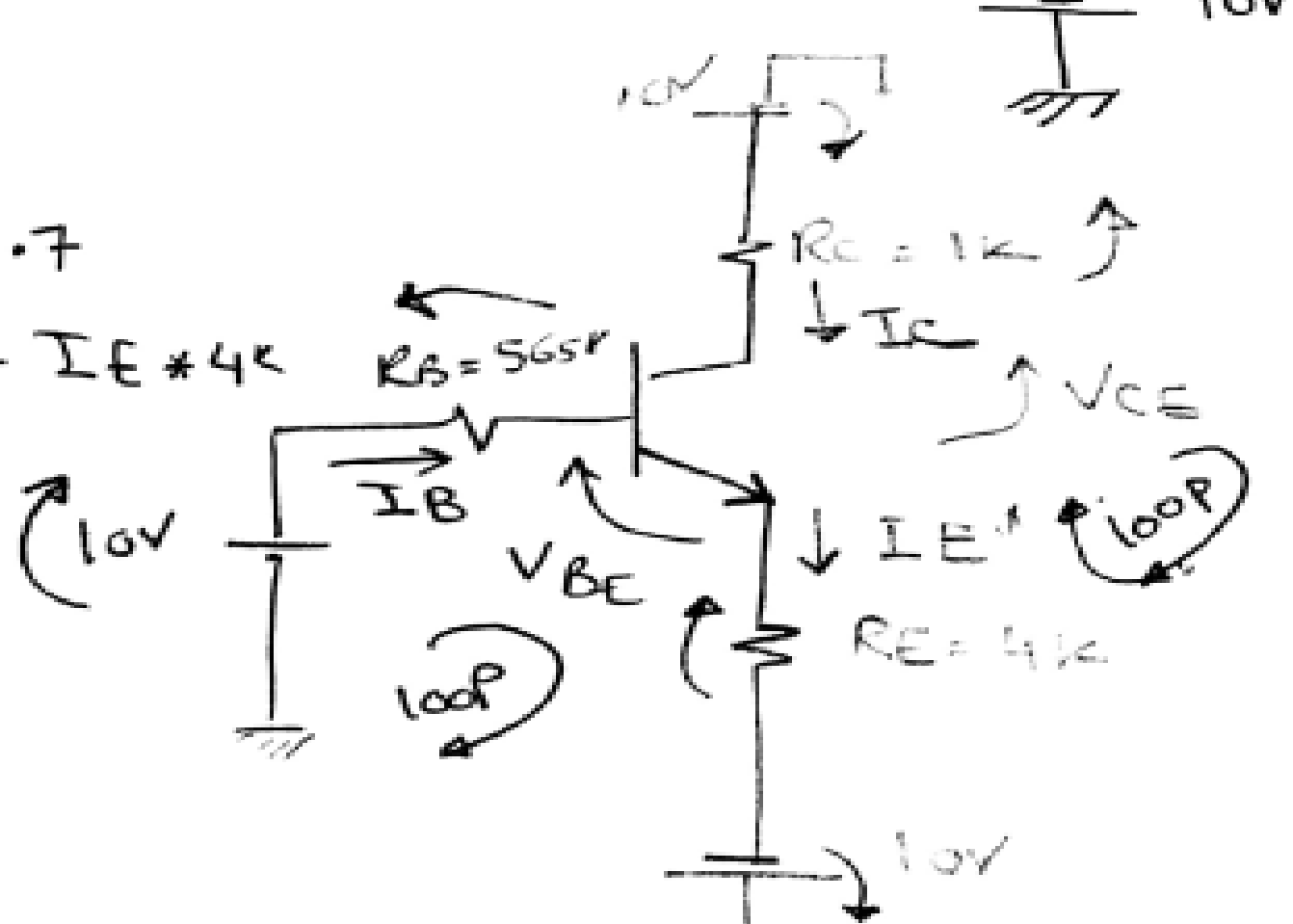
$$10 - I_B * 565^k - \overset{0.7}{V_{BE}} - I_E * 4^k + 10 = 0$$

$$I_E = \underset{100}{\beta} I_B$$

$$10 - I_B * 565^k - 0.7 - 100 * I_B * 4^k + 10 = 0$$

$$I_B = 0.02 \text{ mA}$$

$$I_C \approx I_E = \beta I_B = 2 \text{ mA}$$



KVL at EC loop ☺

$$-10 + I_C \times 1^k + V_{CE} + I_E \times 4^k - 10 = 0$$

$$I_C \approx I_E$$

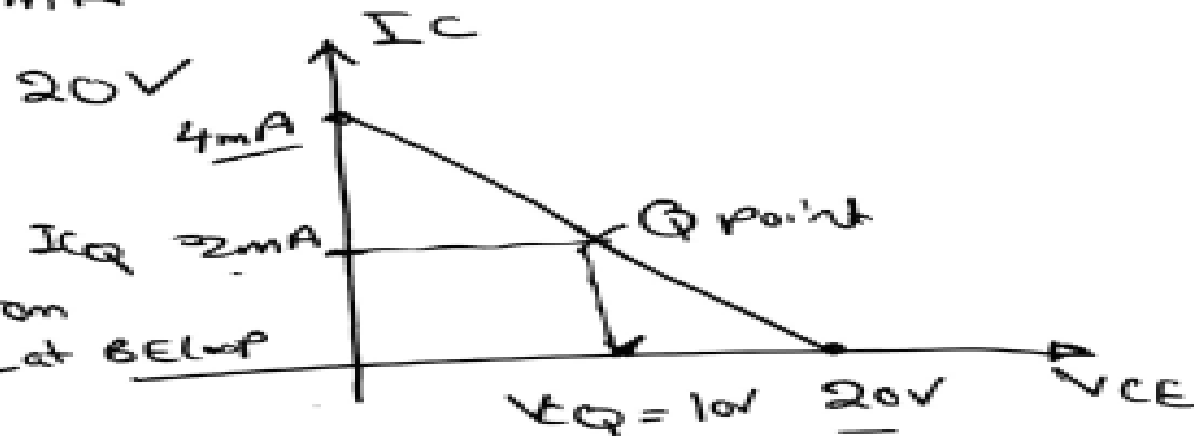
$$V_{CE} + 5^k I_C = 20 \quad | \text{ load line equation}$$

$$\text{if } V_{CE} = 0 \rightarrow I_C = 4 \text{ mA}$$

$$\text{if } I_C = 0 \rightarrow V_{CE} = 20 \text{ V}$$

to get Q-point

$$I_{CQ} \approx I_E = \beta I_B = 2 \text{ mA} \quad \text{from KVL at BE loop}$$



$$V_{CEQ} + 5^k \underbrace{I_{CQ}}_{2 \text{ mA}} = 20$$

$$V_{CEQ} = 10 \text{ V} > 0.2$$

Correct assumption
Active region

(22)
② if $R_C = 11k\Omega$

B-E loop \rightarrow No change from ① $I_B = 0.02mA$
 $I_C = I_E = 2mA$

E-C loop
 $R_C = 11k\Omega$

$$-10 + I_C \times 11k + V_{CE} + I_E \times 4k - 10 = 0$$

$$\boxed{V_{CE} + 15I_C = 20} \quad \text{load line}$$

to get Q-Point

$$I_{CQ} = 2mA \rightarrow V_{CEQ} = 10V < 0.2V$$

\therefore Assumption wrong

BJT in Saturation

E-C loop

$$V_{CEsat} = 0.2V$$

$$V_{CEsat} + 15I_{Csat} = 20$$

\downarrow
 $0.2V$

$$\boxed{I_{Csat} = 1.32mA}$$

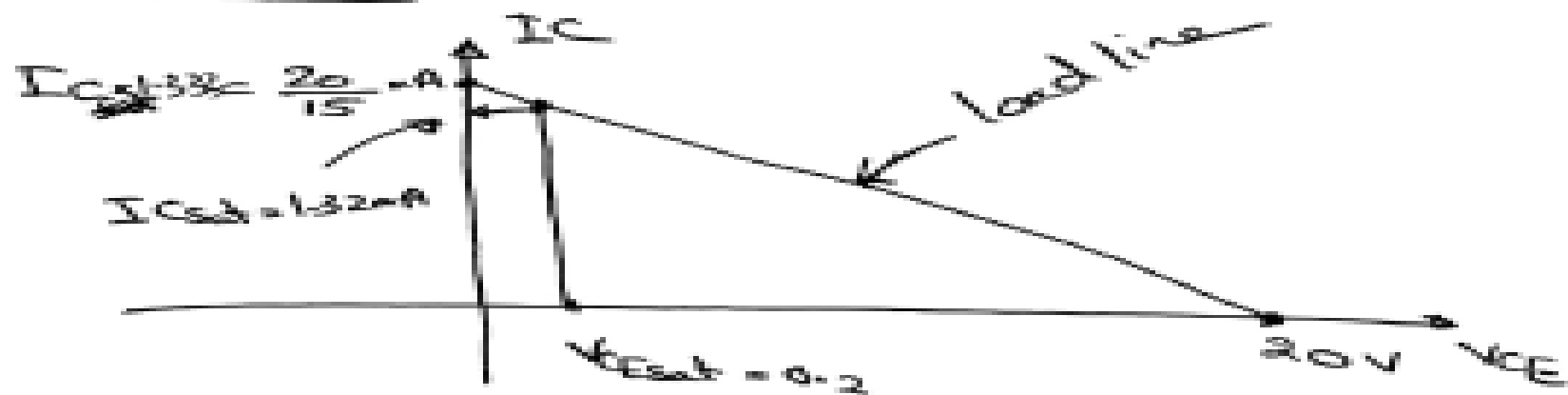
B-E loop

(23)

$$10 - I_{B_{sat}} \times 565k - V_{BE_{sat}} - I_{E_{sat}} \times 4k + 10 = 0$$

\downarrow \downarrow
 0.7 $I_{C_{sat}} = 1.32mA$

$I_{B_{sat}} = 0.0248mA$



$V_{CE} + 15k I_C = 20$

if $I_C = 0 \longrightarrow V_{CE} = 20$

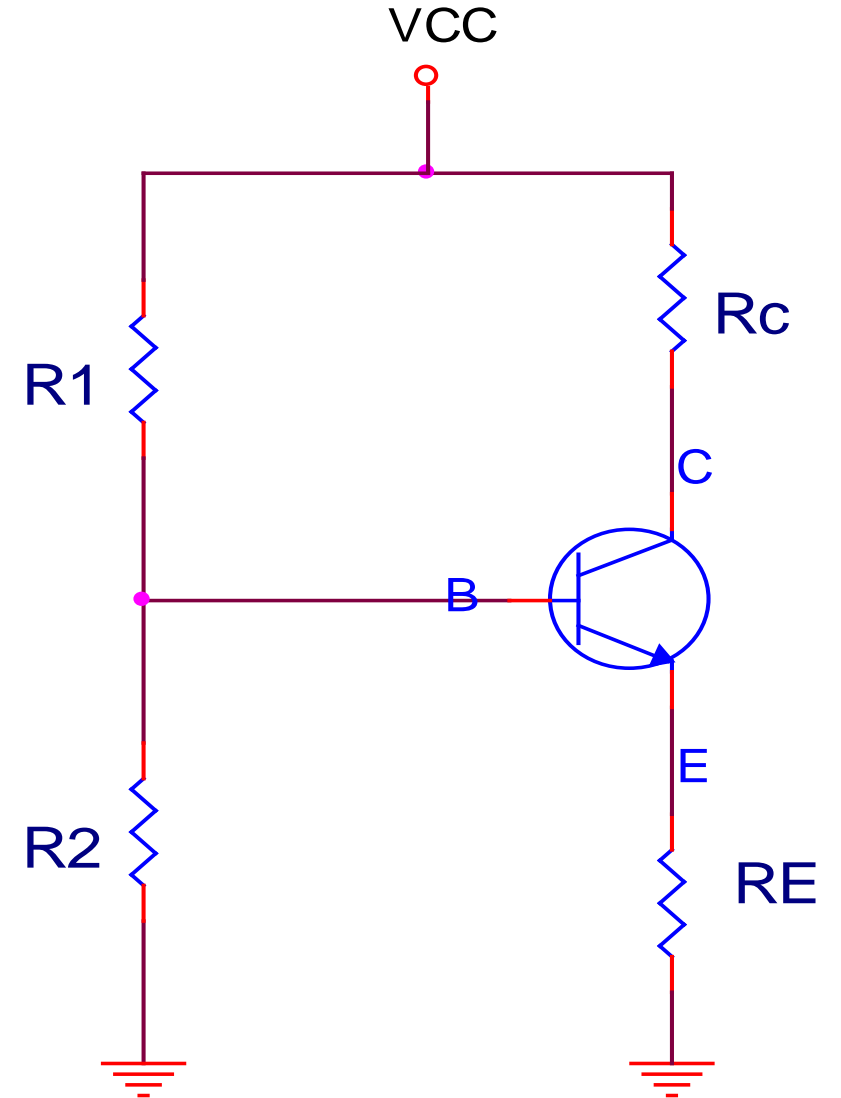
if $V_{CE} = 0 \longrightarrow I_C = \frac{20}{15}$

Example

In the following fig, $V_{CC} = 22\text{V}$, $R_1 = 39\text{ k}\Omega$,
 $R_2 = 3.9\text{ k}\Omega$, $R_E = 1.5\text{ k}\Omega$, $R_C = 10\text{ k}\Omega$,
 $\beta = 100$.

Determine the dc bias voltage V_{CE} and I_C
for voltage divider configuration

Solved in lecture



Example 2 of voltage divider bias Configuration 11 (24)

Determine the dc bias

Voltage V_{CE} and I_C

For voltage divider Configuration.

Sol

must make the V_{BE} in

$$V_{TH} = V_{CC} \frac{R_2}{R_1 + R_2}$$

$$V_{TH} = 22 \times \frac{3.9k}{3.9 + 39} = \boxed{2V}$$

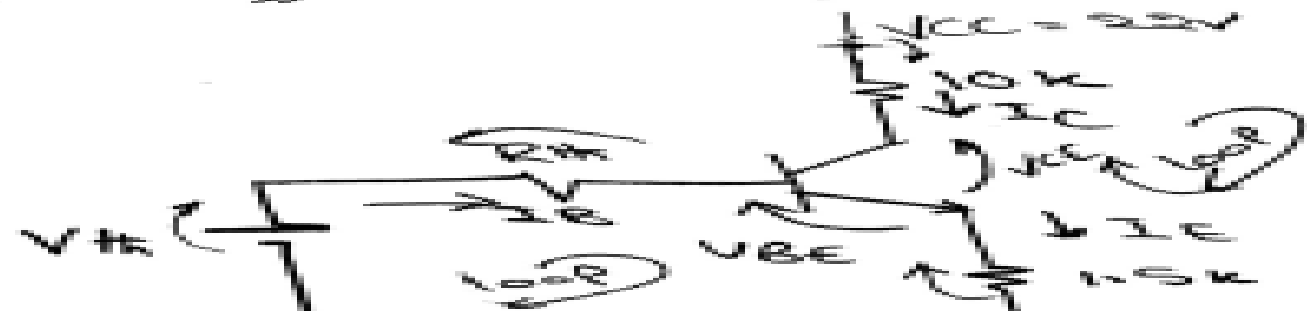
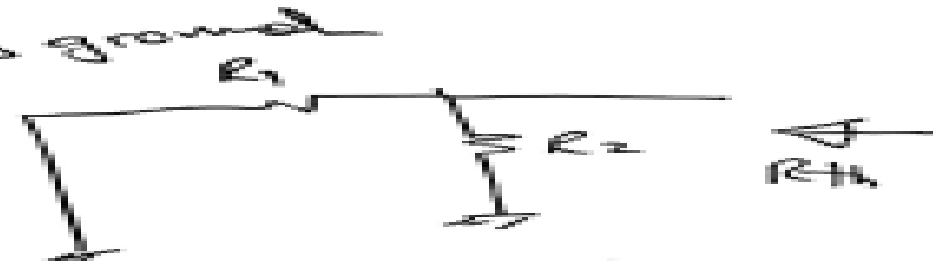
voltage divider rule



all dc sources ground

$$R_{TH} = R_1 \parallel R_2$$

$$\boxed{R_{TH} = 3.55k\Omega}$$



KVL at B-E loop

$$V_{B1} - I_B R_{B1} - V_{BE} - I_E R_E = 0$$

$\begin{matrix} \swarrow 2 & \searrow 3.55 & \swarrow 0.7 & \searrow 1.5k \\ & & & \text{BIB} \end{matrix}$

$$I_B = \boxed{8.38 \mu A}$$

$$I_C = I_E = \beta I_B = \boxed{0.84 mA}$$

KVL E-C loop

$$-V_{CC} + I_C \times 10^k + V_{CE} + I_E \times 1.5^k = 0$$

$\begin{matrix} \swarrow 22 & \searrow 0.84 & \swarrow I_C = 0.84 \end{matrix}$

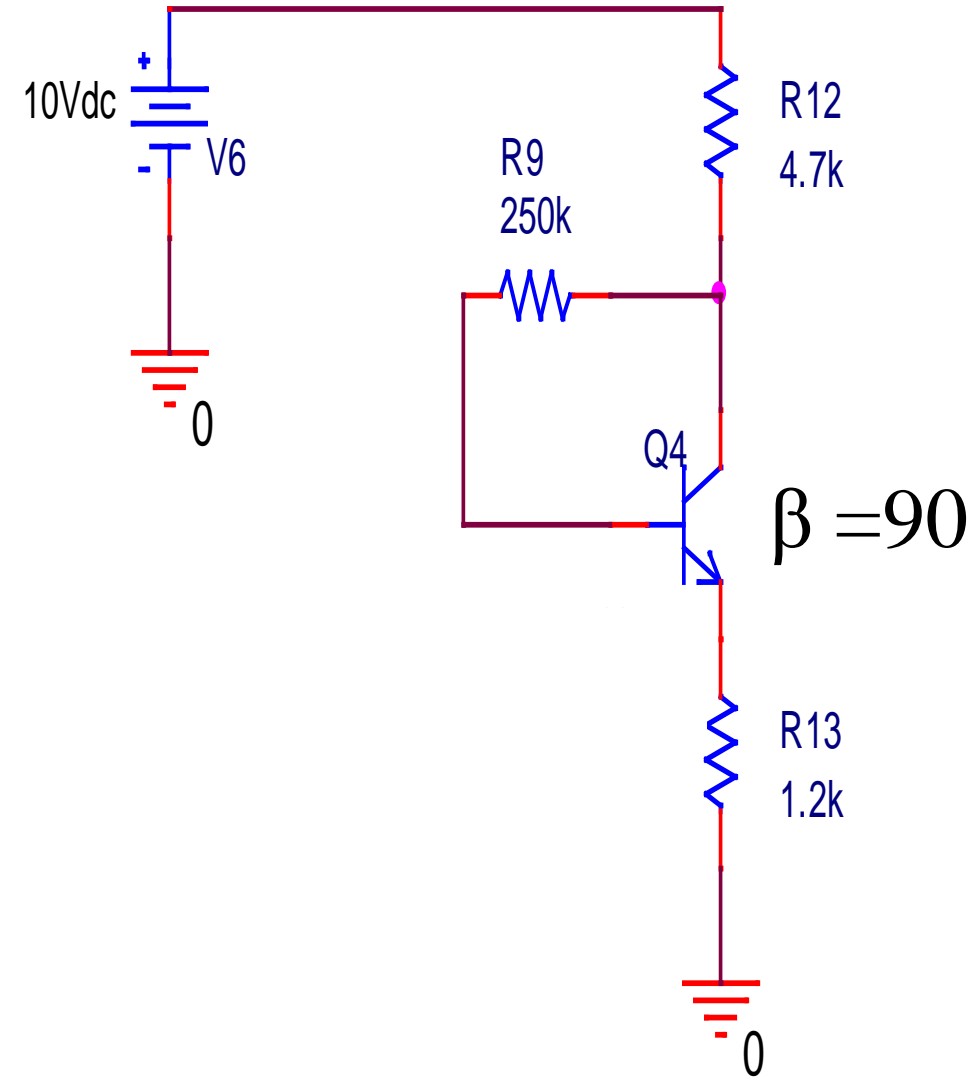
$$V_{CE} = 12.34 V > 0.2 \quad \text{Active Region}$$

Correct assumption

Example

Determine the following for
feed back configuration I_{CQ}
and V_{CEQ}

Solved in lecture



Example 11 (feedback configuration)

27

Determine the I_{CQ} , V_{CEQ}

KVL ~~loop~~ loop 1

$$10 - 4.7k I_B - I_B \times 250k - V_{BE} - I_E \times 1.2k = 0$$

$$I = I_B + I_E = (1 + \beta) I_B$$

1 choice

$$I \approx \beta I_B$$

$$I_B = 11.91 \mu A$$

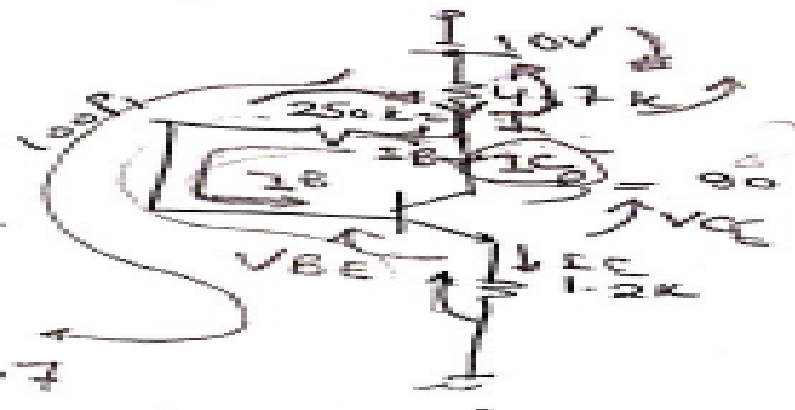
$$I_{CQ} = \beta I_B = 1.07 mA$$

KVL E-C loop

$$-10 + 4.7k I_{CQ} + V_{CEQ} + I_E \times 1.2 = 0$$

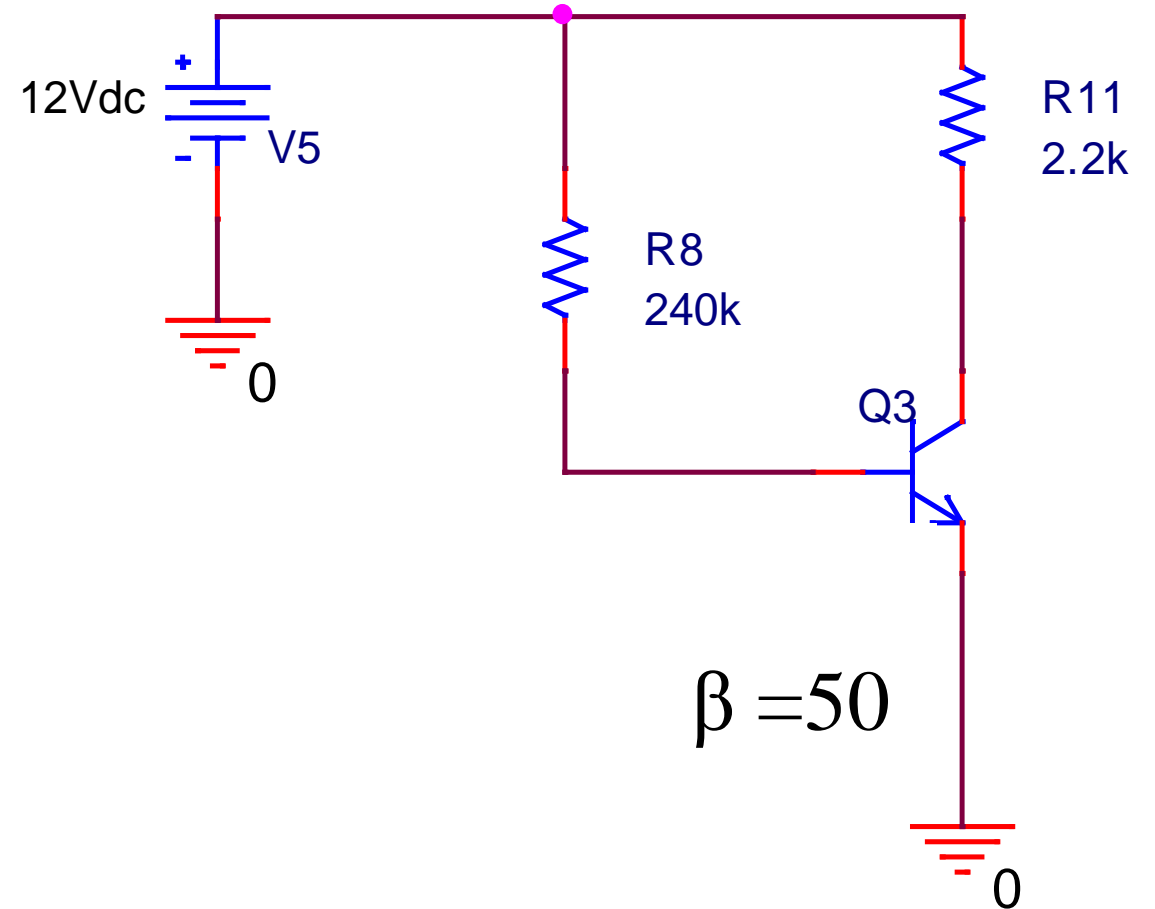
$I_{CQ} \approx I_E$

$$V_{CEQ} = 3.69 V$$



Example

Determine the following for fixed bias configuration I_{BQ} , I_{CQ} , V_{CEQ} , V_B , V_C and V_{BC}



B-E loop

$$12 - I_B \times 240^k - V_{BE} = 0$$

$$I_{BQ} = 47.08 \mu A$$

$$I_{CQ} = \beta I_{BQ} = (50)(47.08 \mu A)$$

$$I_{CQ} = 2.35 \text{ mA}$$

C-E loop

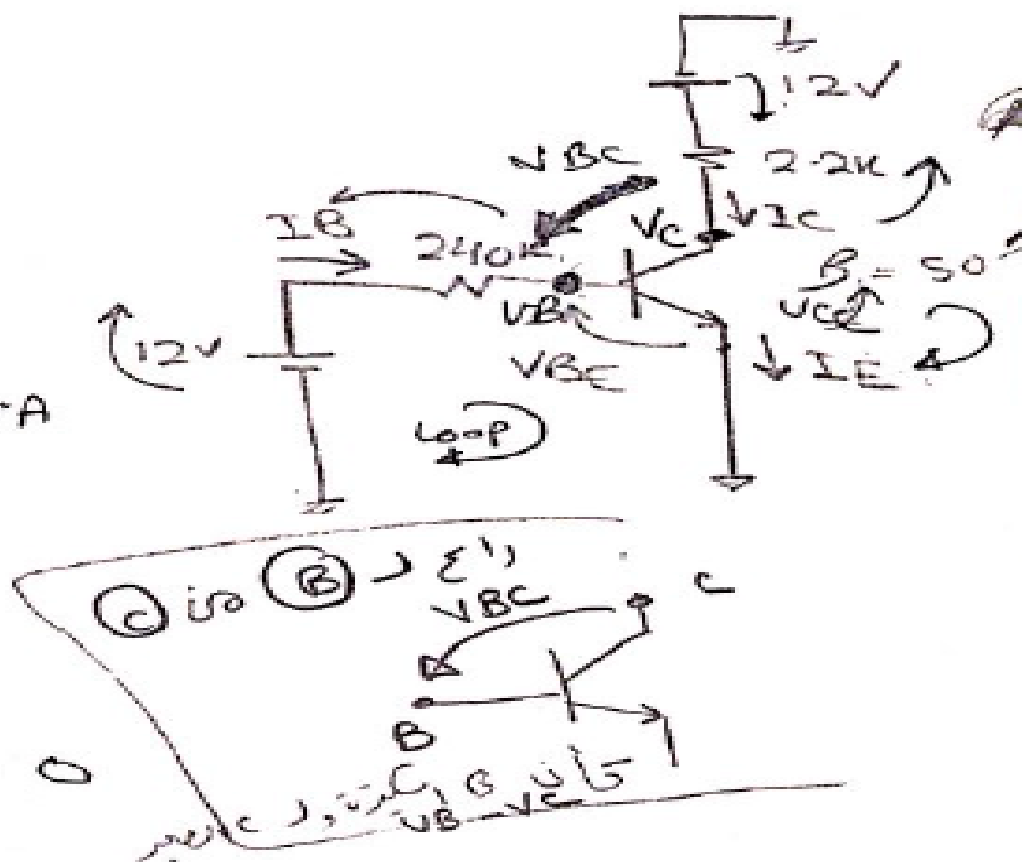
$$-12 + I_{CQ} \times 2.2^k + V_{CEQ} = 0$$

$$V_{CEQ} = 6.83 \text{ V} > 0.2 \text{ Active mode}$$

$$V_C = V_{CE} = 6.83 \text{ V}$$

$$V_B = V_{BE} = 0.7 \text{ V}$$

$$V_{BC} = V_B - V_C = -6.13 \text{ V}$$

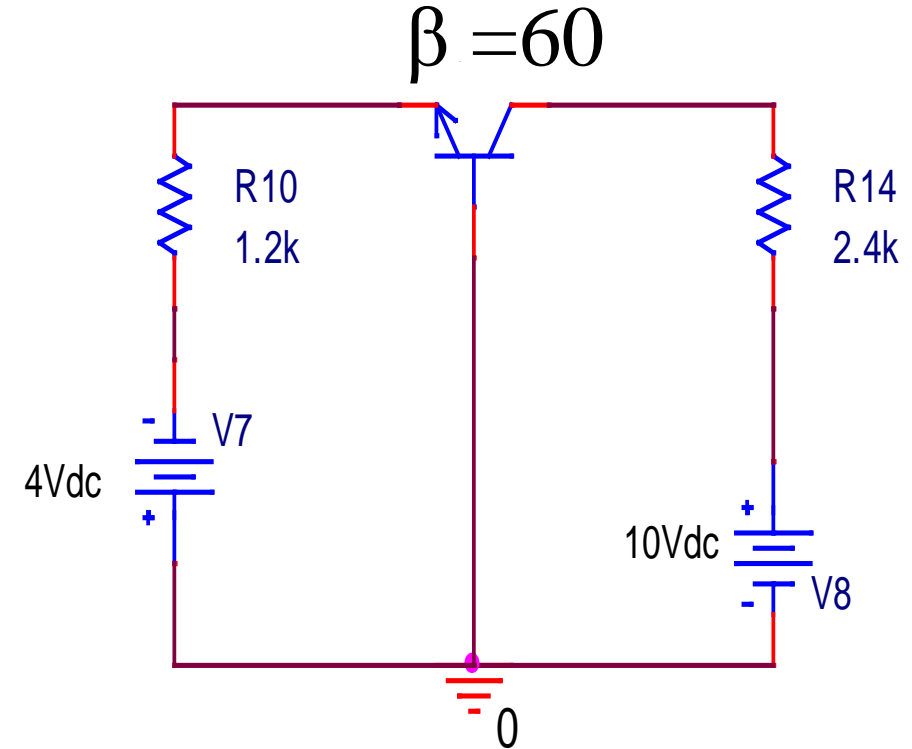


Active mode
Amplifier
BE \rightarrow F.B
BC \rightarrow R.B

Example

Determine the following for common base configuration
 I_E , I_B , V_B , V_{CE} and V_{CB}

Solved in lecture



Example 5 Common-Base Configuration Base Connected to 8

Determine I_E, I_B, V_{CE}, V_{CB}

For Common-base Configuration



KVL E-B loop

$$-4 + I_E \times 1.2k + V_{BE} = 0$$

$\downarrow 0.7$

$$I_E = 2.75 \text{ mA}$$

$$I_C = I_E = 2.75 \text{ mA}$$

$$I_C = \beta I_B$$

$$I_B = \frac{I_C}{\beta} = \frac{2.75 \text{ mA}}{60} = 0.045833 \text{ mA}$$



KVL E-C loop 1

$$-4 + I_E \times 1.2k + V_{CE} + I_C \times 2.4k - V_{CC} = 0$$

$\downarrow 2.75 \quad \downarrow 1.2k \quad \downarrow 2.75 \quad \downarrow 2.4k \quad \downarrow 4$



$$\boxed{V_{CE} = 4.1 \text{ V}}$$

KVL loop 2

2.75

$$V_{CB} + I_E \times 2.4k - V_{CE} = 0$$

$\downarrow 2.75 \quad \downarrow 2.4k \quad \downarrow 4.1$

$$V_{CB} = 3.51 \text{ V}$$