SOC Design Lab3 Report

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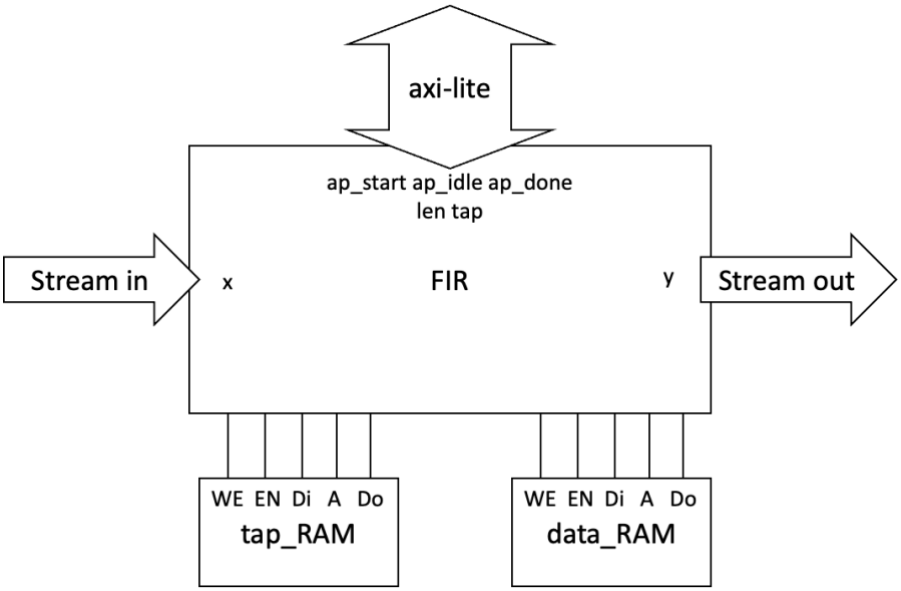
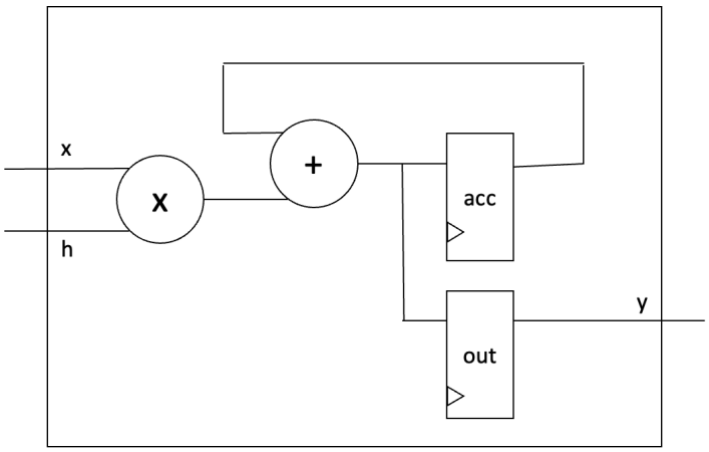
1. Architecture Design

1.1 Block diagram

1.1.1 System overview



1.1.2 FIR engine



1.1.3

1.2 Control signal

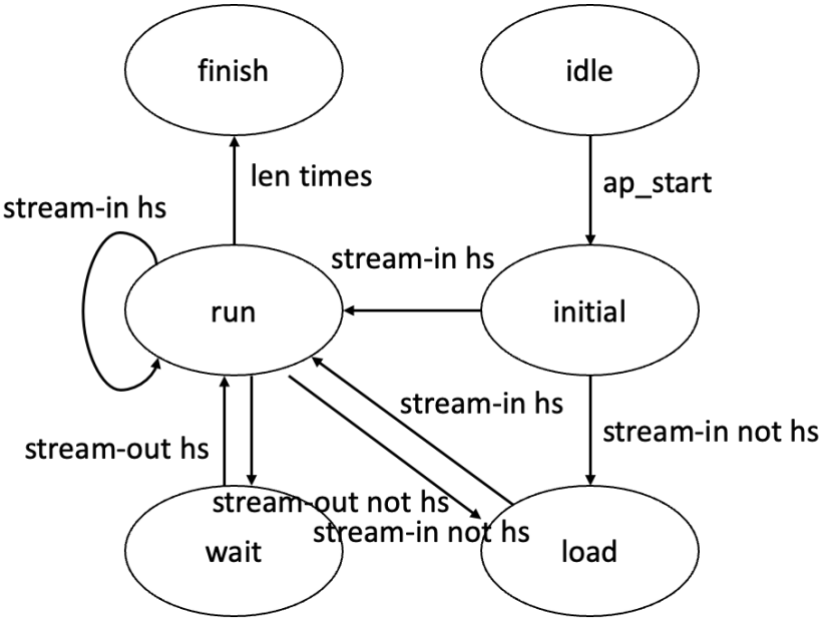
1.2.1 State diagram

Initial: reset data ram

Run: run FIR engine

Load: wait for stream-in data

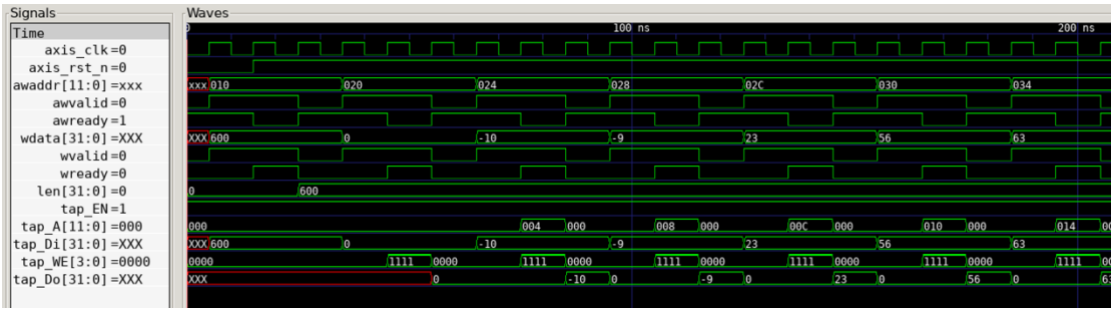
Wait: wait for stream-out data

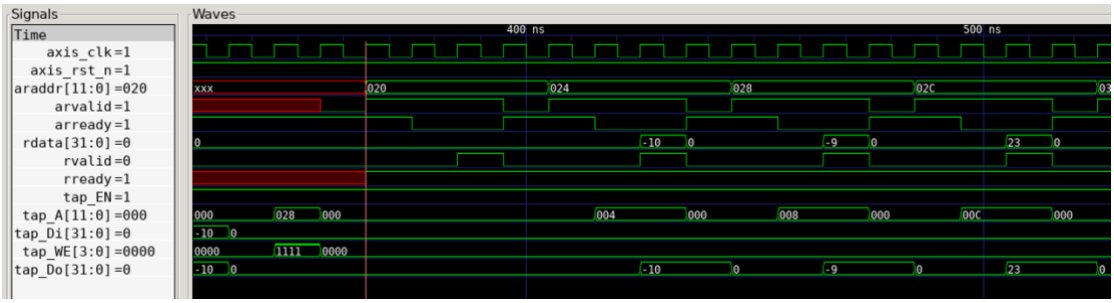


2. Verification and Synthesis

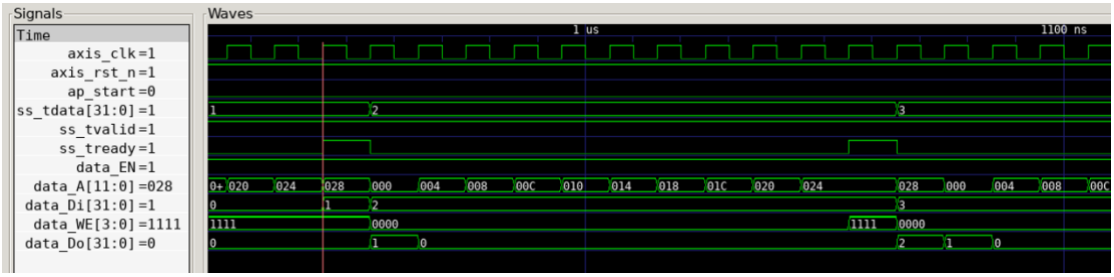
2.1 Simulation waveform

2.1.1 Coefficient program and read back

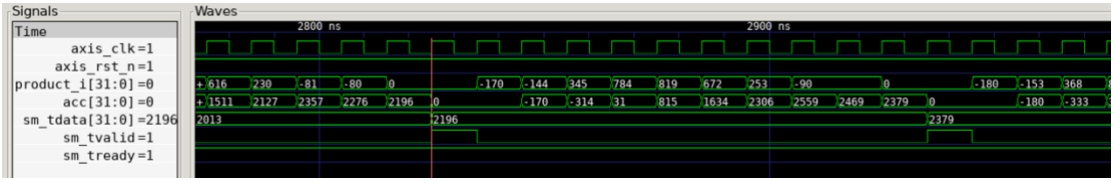




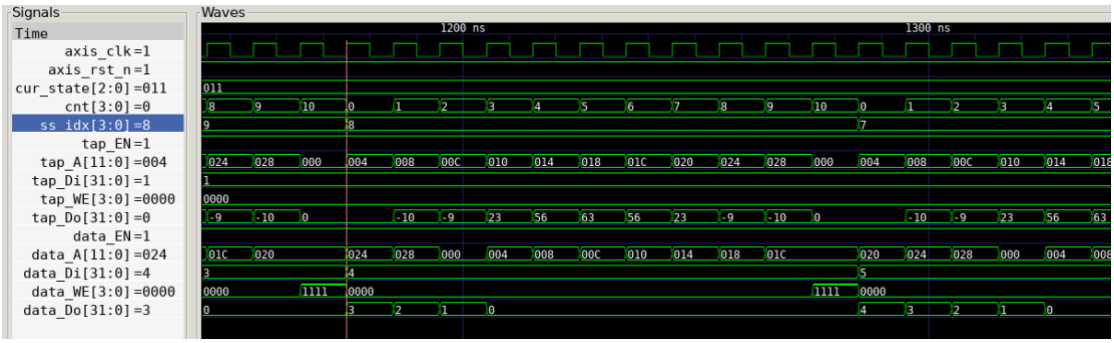
2.1.2 Data-in stream in



2.1.3 Data-out stream out



2.1.4 Bram access control



2.2 Synthesis

2.2.1 Timing report summary

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File
1	axis_clk	10.000	0.000	5.000	☐	[get_ports axis_clk]	constraints.xdc

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.558 ns	Worst Hold Slack (WHS):	0.137 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	258	Total Number of Endpoints:	258	Total Number of Endpoints:	171

All user specified timing constraints are met.

2.2.2 Critical path

Summary

Name	Path 1
Slack	3.558ns
Source	len_reg[4]/C (rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	cur_state_reg[2]/D (rising edge-triggered cell FDCE clocked by axis_clk {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	axis_clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns (axis_clk rise@10.000ns - axis_clk rise@0.000ns)
Data Path Delay	6.306ns (logic 3.319ns (52.632%) route 2.987ns (47.368%))
Logic Levels	12 (CARRY4=8 LUT1=1 LUT5=1 LUT6=2)
Clock Path Skew	-0.145ns
Clock Un...rtainty	0.035ns