SmartSpiceRF

Switched-Capacitor Filter Simulation

Tutorial

Introduction

Information presented in this Tutorial is based on the assumption that the user is familiar with the following:

- Basics of the computer operating system and hardware employed
- Basic terminology of semiconductor process and device operation
- Circuit design, schematic capture, and simulation

The simulation flow described in Tutorial uses Silvaco Process Design Kit (PDK) based on a fictional process called SBCD (Silvaco Bipolar Cmos Dmos). SBCD process includes the following devices: two low-voltage Cmos, two high-voltage Dmos, four resistors, capacitor, and inductor. SBCD libraries provide all the data needed to demonstrate a real design flow.

This Tutorial presents front end design flow of Switched-Capacitor Filter (SC) circuit and guides you through the following circuit design steps:

- Schematic Capture with Gateway
- Simulation with SmartSpiceRF
- Results postprocessing with SmartView

The following Silvaco EDA tools are needed to work with Tutorial:

- GATEWAY
- SMARTSPICERF
- SMARTVIEW

1: GATEWAY Schematic Capture

Start `Gateway` and load the workspace file `SC.workspace` by selecting **File→Open→Workspace.** When the browser window appears, navigate to the directory where `RF Demo PDK Examples` were installed, descent into `./SC` directory, and select `SC.workspace` file.

1.1: Loading SCF Schematic

This Tutorial presents the first order low pass switched-capacitor filter (SCF) simulation.

SCF and OP Amplifier circuit schematics, shown on Figure 1 and Figure 2 accordingly, were used to create two testbench circuits.

To load these files, select **File→Open→ Schematic**. When the file browser appears, navigate to the `./libraries/symbols/sc`. directory and select `SC_test.schlr`, then `OpAmp.schlr`.

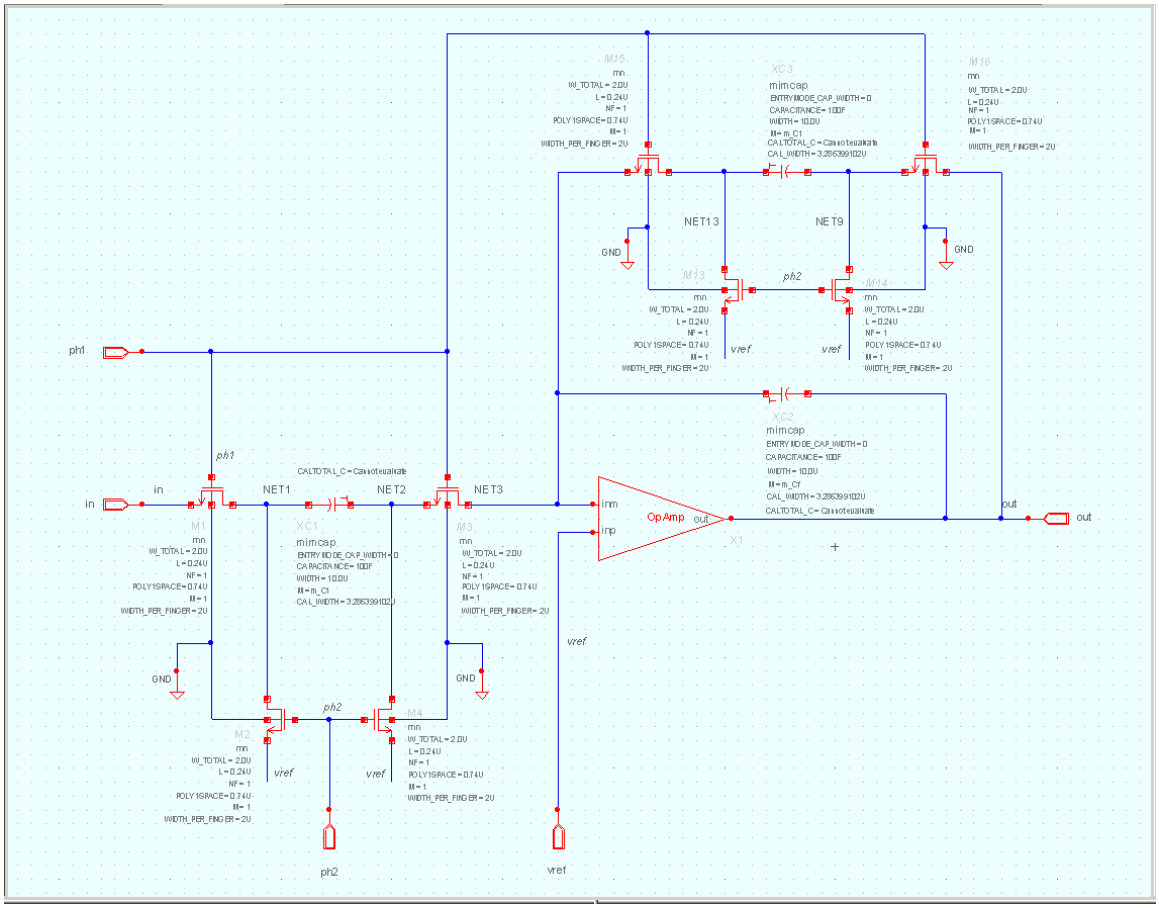

Figure 1: Switched-Capacitor Filter Schematic

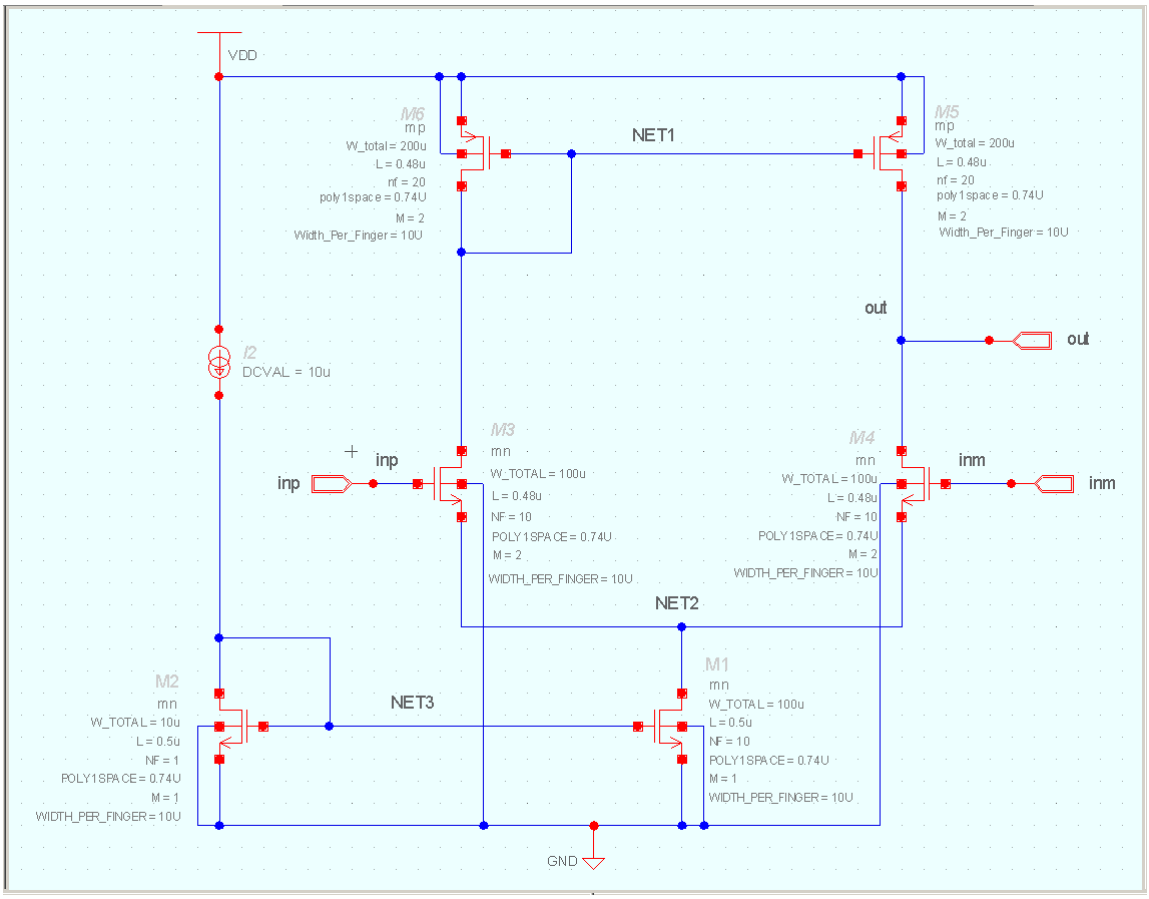

Figure 2: OP Amplifier Schematic

1.2: Simulator Setup

Check GATEWAY that your preferred simulator is set to SMARTSPICERF. In GATEWAY click on **Edit -> Preferences** to open the preferences setup window (Figure 3). Choose **Tools-> Simulato**r and set (check) Simulator to SMARTSPICERF. Version number is set to Default (the latest installed version) in **Version** window. You can define any specific version too.

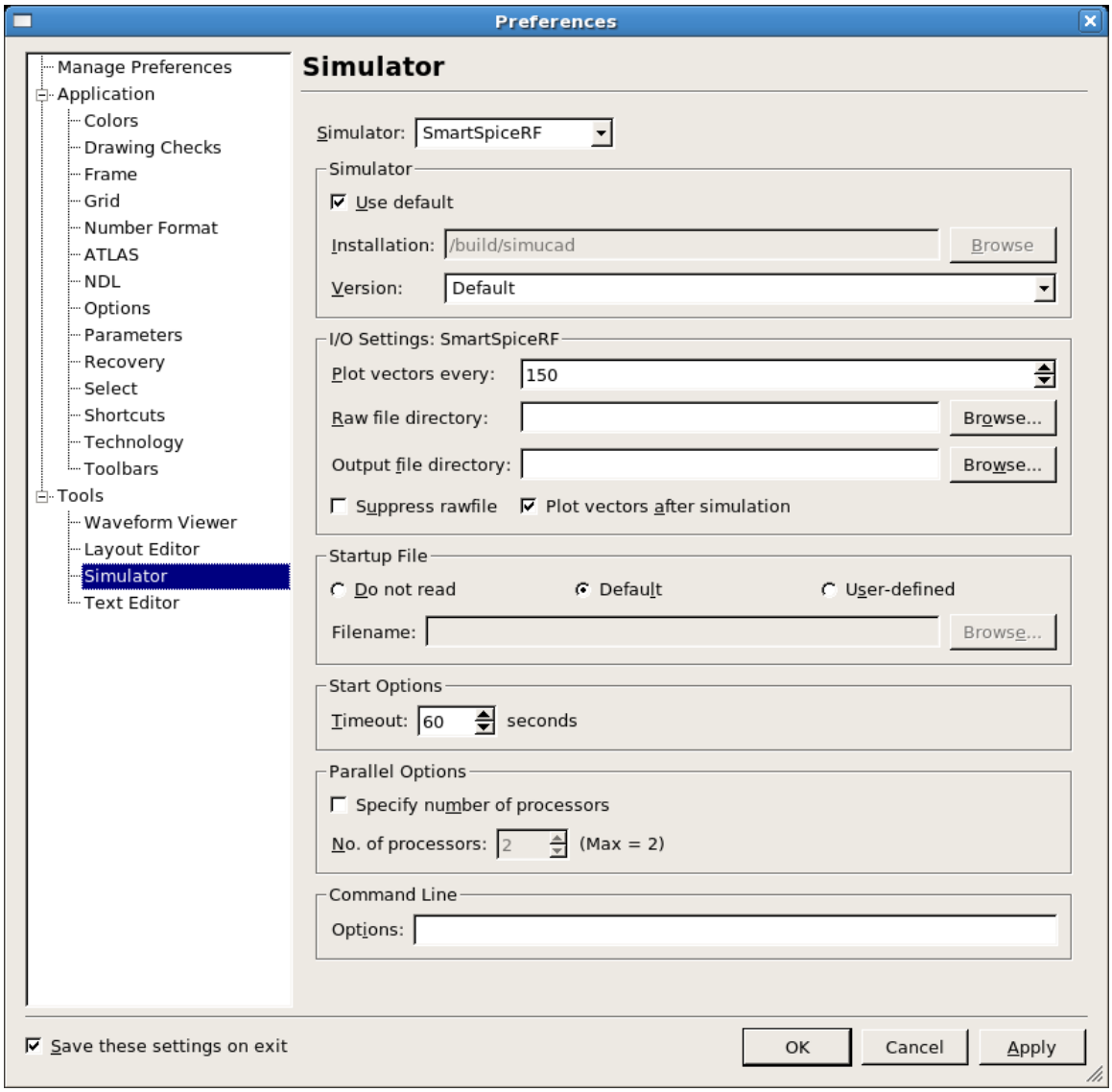

Figure 3: Simulator Preferences Window

2: SmartSpiceRF Simulations

This Tutorial illustrates how SmartSpiceRF can simulate switched-capacitor filter circuits and provide basic measurements.

2.1: Transient Analysis

Transient analysis is provided with testbench file `TB_SC_test.schlr`.

2.1.1: Loading Testbench Schematic

To load the first testbench schematic, select **File→Open→ Schematic**. When the file browser appears, navigate to the `./SC` directory and select the file `TB_SC_test.schlr.` The SCF testbench circuit schematic will appear in the window (Figure 4).

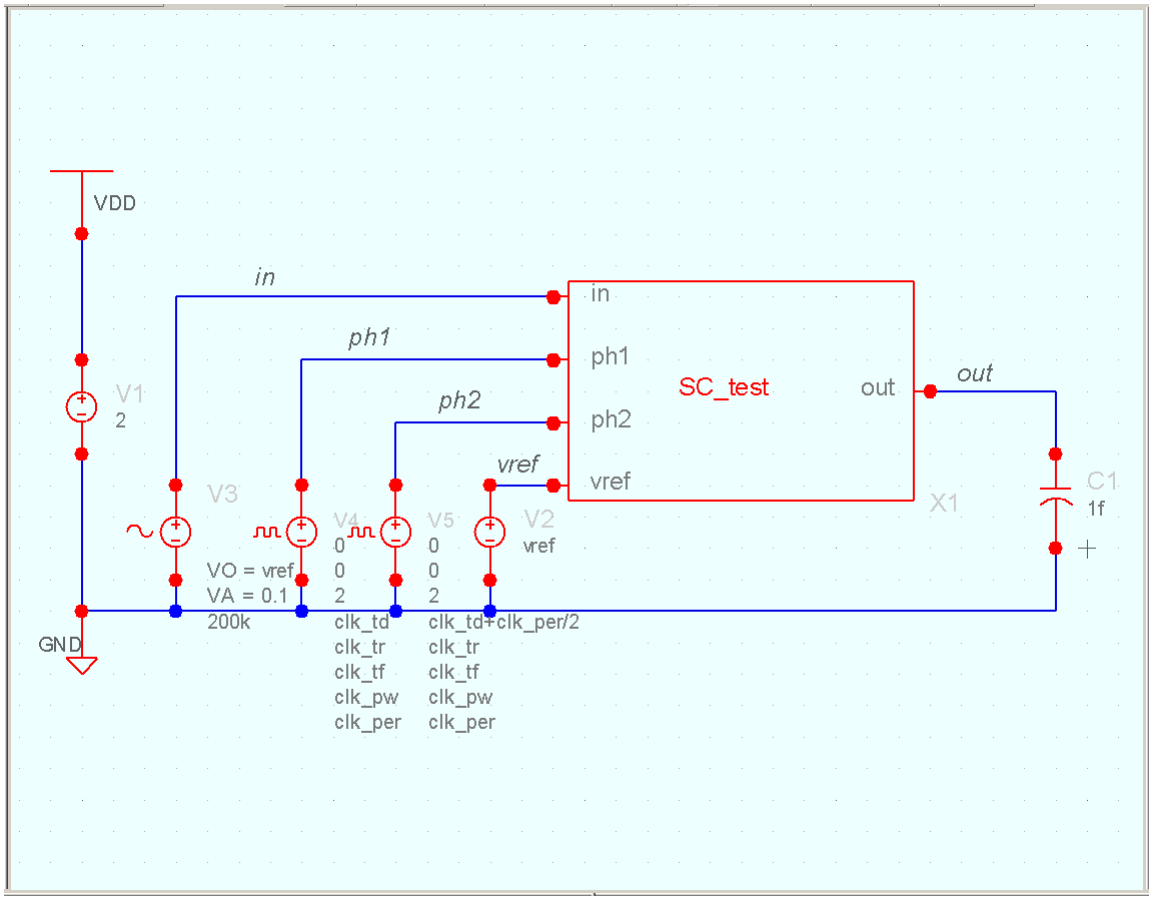

Figure 4: Testbench of Switched-Capacitor Filter for Transient Analysis

2.1.2: Generating Netlists

Netlists are the text files used to describe device connectivity and element properties of the circuit. GATEWAY can create two different netlist formats: SMARTSPICE for circuit simulation, or GUARDIAN for layout design. See the GATEWAY USER'S MANUAL for more information on these formats.

To generate netlist in SMARTSPICE format, either select **Simulation→Create Netlist,** or click on **SmartSpice Netlist** icon (Figure 5) in **Tool Bar**.

Figure 5: Create Netlist Icon

SMARTSPICE netlist then will appear in a new window:

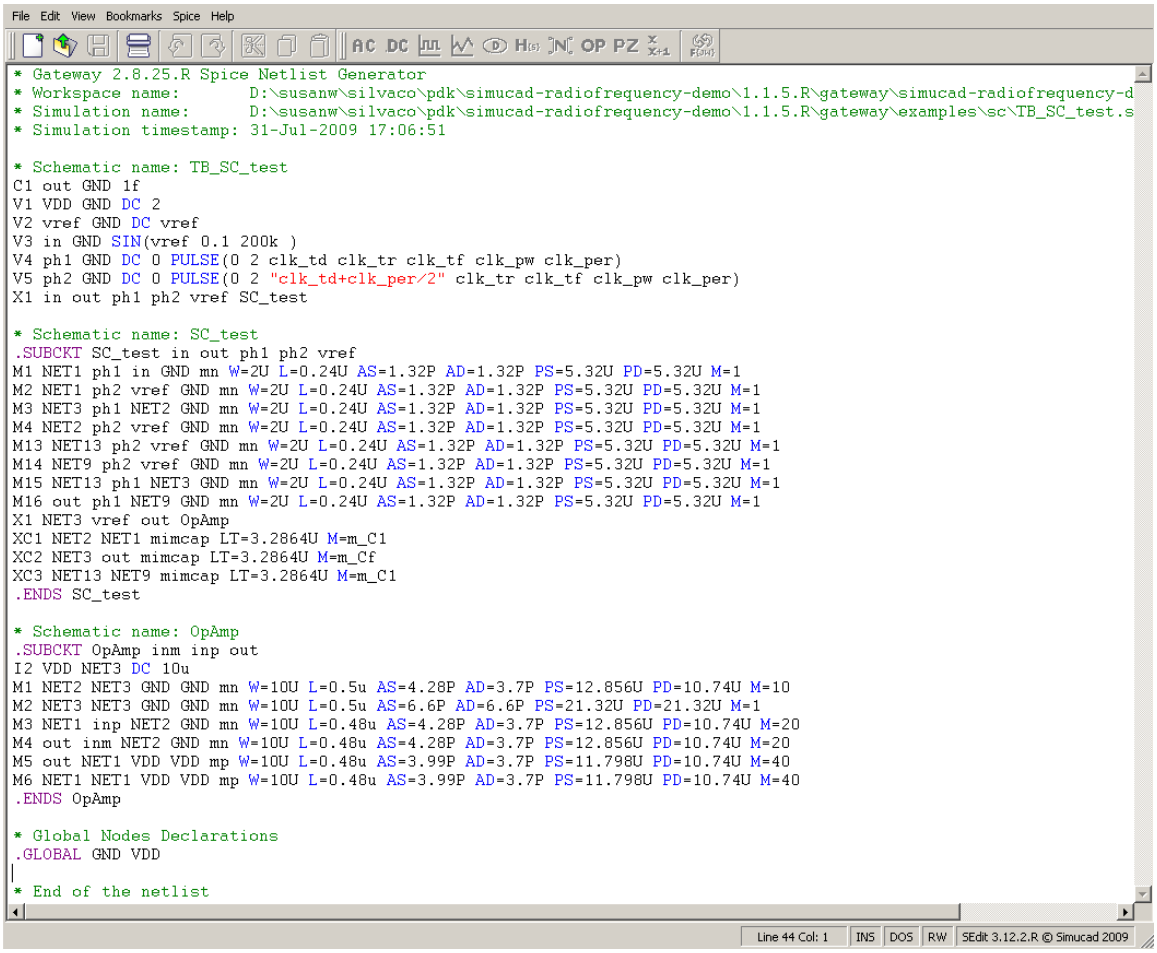

Figure 6: SCF Testbench Netlist

2.1.3: Control File

SMARTSPICERF needs more than just a circuit netlist to perform a meaningful simulation. It needs Circuit Netlist, Voltage or Current stimulus, Options, Analysis Statements, and active device Model parameters or Libraries. All this information comes together in the form of an Input Deck file (*.in, *.inp, *.cir, *.sp, *.sm, *.scs, etc.), which provides SMARTSPICERF with all needed information to run simulation and generate output data.

Click on the simulation **Tool Bar** icon **Edit Control File** (Figure 7):

Figure 7: Edit Control File Icon

The control file will be opened in the text editor `Sedit` window. The control file `TB_SC_test.ctr` (Figure 8) consists of path to SILVACO RF Demo PDK model library file as well as SMARTSPICERF .OP and .TRAN Analyses statements. The control file combined with the circuit netlist and list of vectors to be saved creates an Input Deck for SMARTSPICERF.

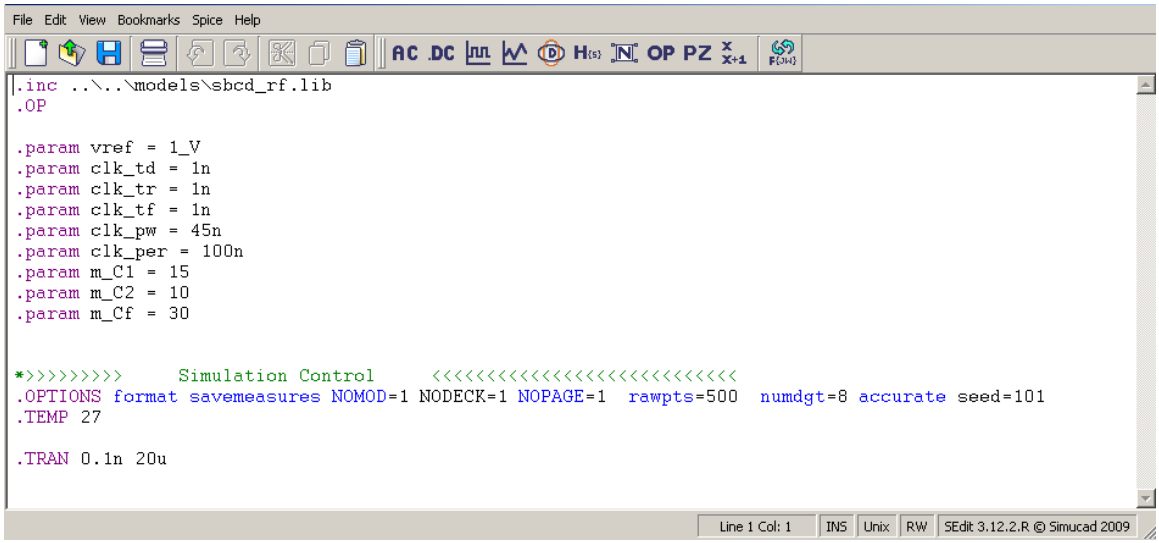

Figure 8: TB_SC Control File

Transient analysis statement is shown as follows:

```
****************************************
.TRAN 0.1n 20u
****************************************
```

Click on  (**Gateway -> Simulation -> Run**) to begin the SMARTSPICERF simulation.

2.1.4: Simulation Results

Simulation results in form of plots will be loaded into SMARTVIEW, and SMARTVIEW **Data Browser** window will be open.

Open plot `tran1`, then select vector `v(out)` and click **Plot**. The waveform plot is shown on Figure 9.

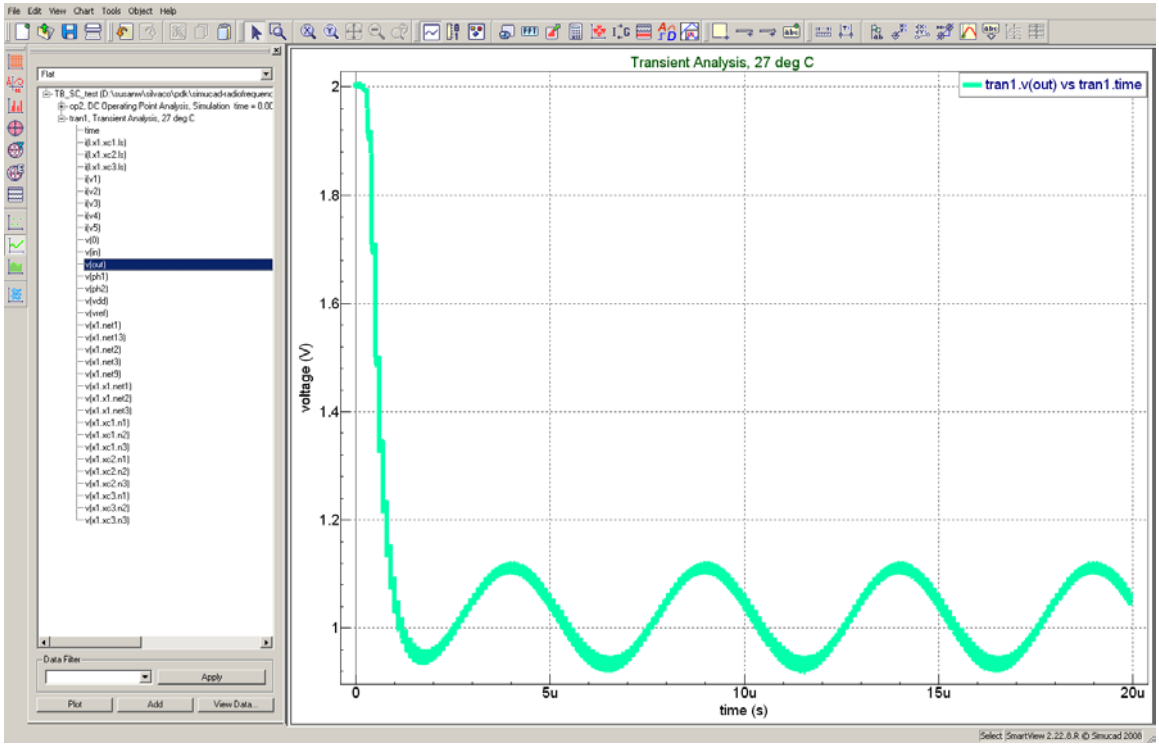

Figure 9: Waveform v(out) Plot

2.2: Transfer Function and Noise Analyses

Transient analysis is provided with testbench file `TB_SC_test_PSS.schlr`.

2.2.1: Loading Testbench Schematic

To load testbench schematic, select **File→Open→ Schematic**. When the file browser appears, navigate to the `./SC` directory and select the file `TB_SC_test_PSS.schlr.` The SCF testbench circuit schematic will appear in the window (Figure 10).

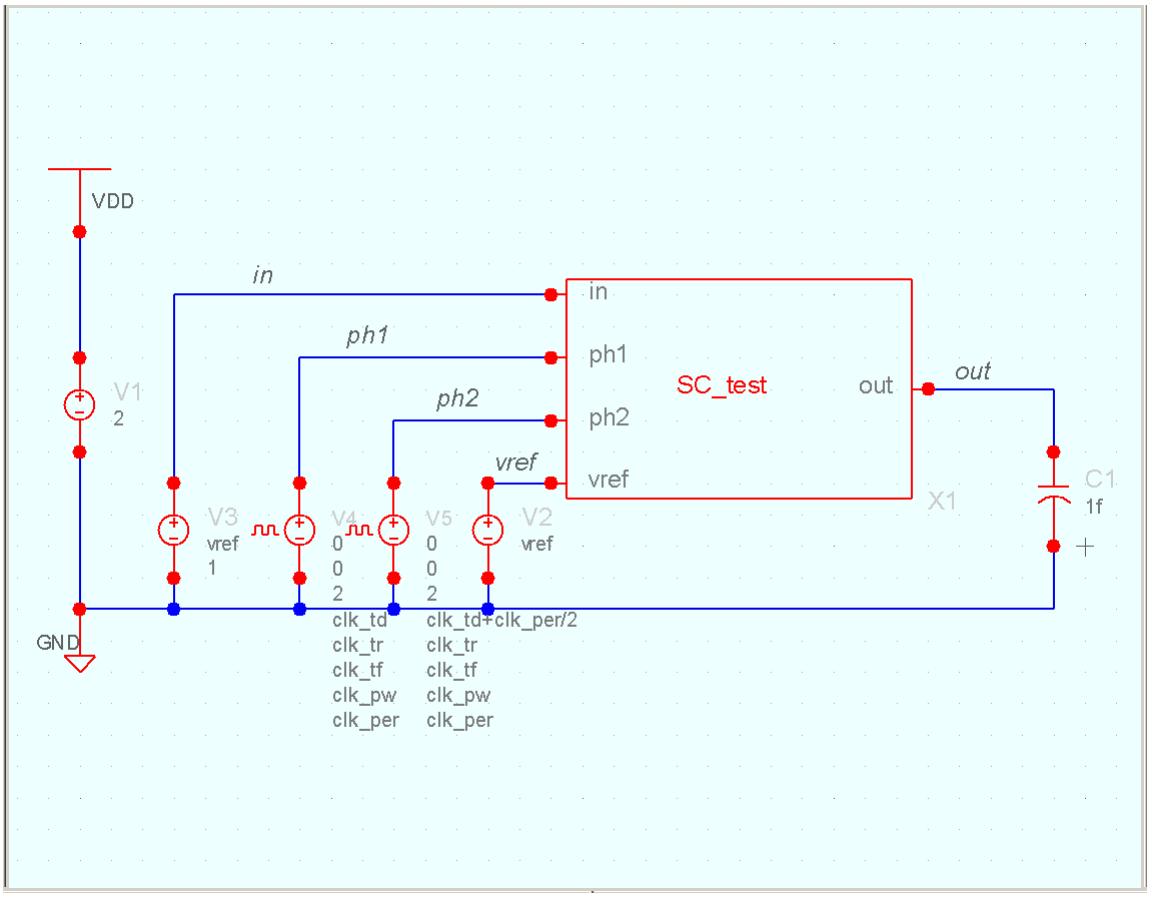

Figure 10: Testbench of Switched-Capacitor Filter for RF Analyses

2.2.2: Generating Netlists

To generate netlist in SMARTSPICE format, either select **Simulation→Create Netlist,** or click on **SmartSpice Netlist** icon (Figure 5) in **Tool Bar**.

SMARTSPICE netlist then will appear in a new window:

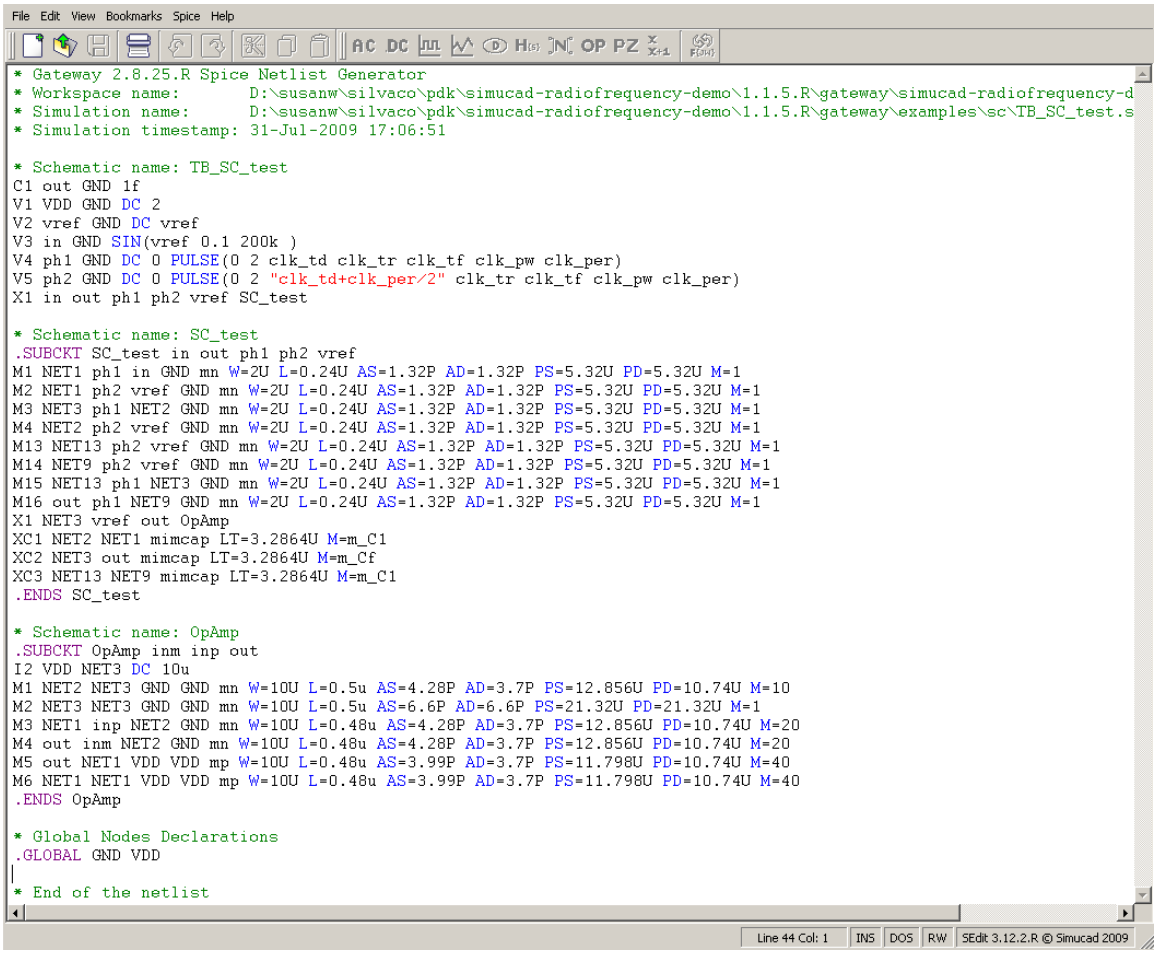

Figure 11: SCF RF Testbench Netlist

2.2.3: Control File

Click on the simulation **Tool Bar** icon **Edit Control File** (Figure 7):

The control file will be opened in the text editor `Sedit` window. The control file `TB_SC_test_PSS.ctr` (Figure 12) consists of path to SILVACO RF Demo PDK model library file as well as SMARTSPICERF .OP, .HAC, and HNOISE Analysis statements. The control file combined with the circuit netlist and list of vectors to be saved creates an Input Deck for SMARTSPICERF.

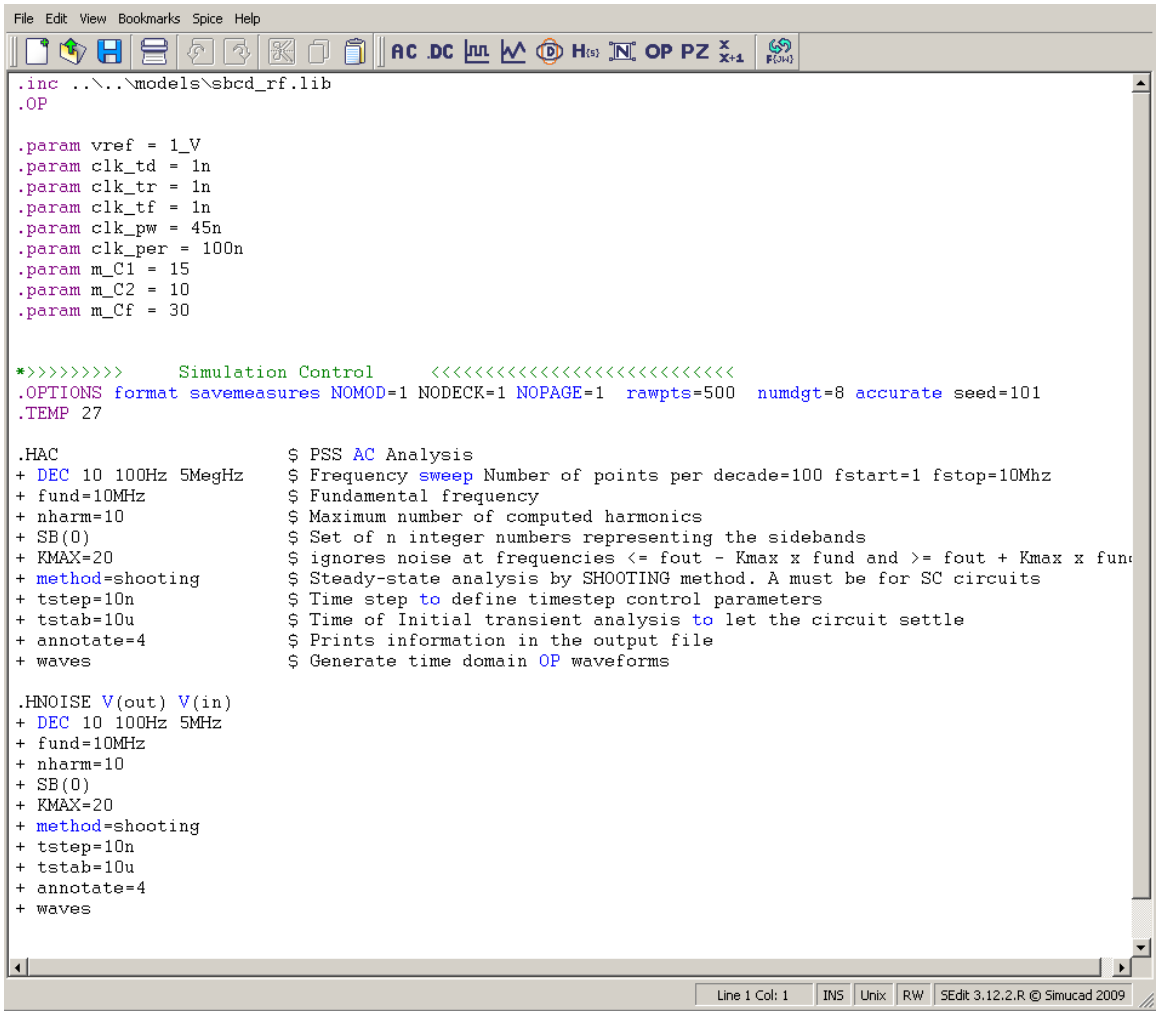

Figure 12: SCF RF Testbench Control File

Transfer function analysis statements are shown as follows.

```
**************************************
.HAC
+ DEC 10 100Hz 5MegHz
+ fund=10MHz
+ nharm=10
+ SB(0)
+ KMAX=20
+ method=shooting
+ tstep=10n
+ tstab=10u
+ annotate=4
+ waves
**************************************
```

.HNOISE analysis statement to calculate output noise is shown as follows.

```
*************************
.HNOISE V(out) V(in)
+ DEC 10 100Hz 5MHz
+ fund=10MHz
+ nharm=10
+ SB(0)
+ KMAX=20
+ method=shooting
+ tstep=10n
+ tstab=10u
+ annotate=4
+ waves
*************************
```

Click on  (**Gateway -> Simulation -> Run**) to begin the SMARTSPICERF simulation.

2.2.4: Simulation Results

SmartSpiceRF outputs simulation results of Large-Signal PSS, Small-Signal HAC and NOISE analyses, and statistic information into Output window and creates number of plots with Waveforms, Spectra, Measurement results, etc. Simulation results in form of plots will be loaded into SMARTVIEW, and SMARTVIEW **Data Browser** window will be open.

Open plot `hac1`, then select vector `v(out)`, and click **Plot**.

The transfer function is shown in Figure 13.

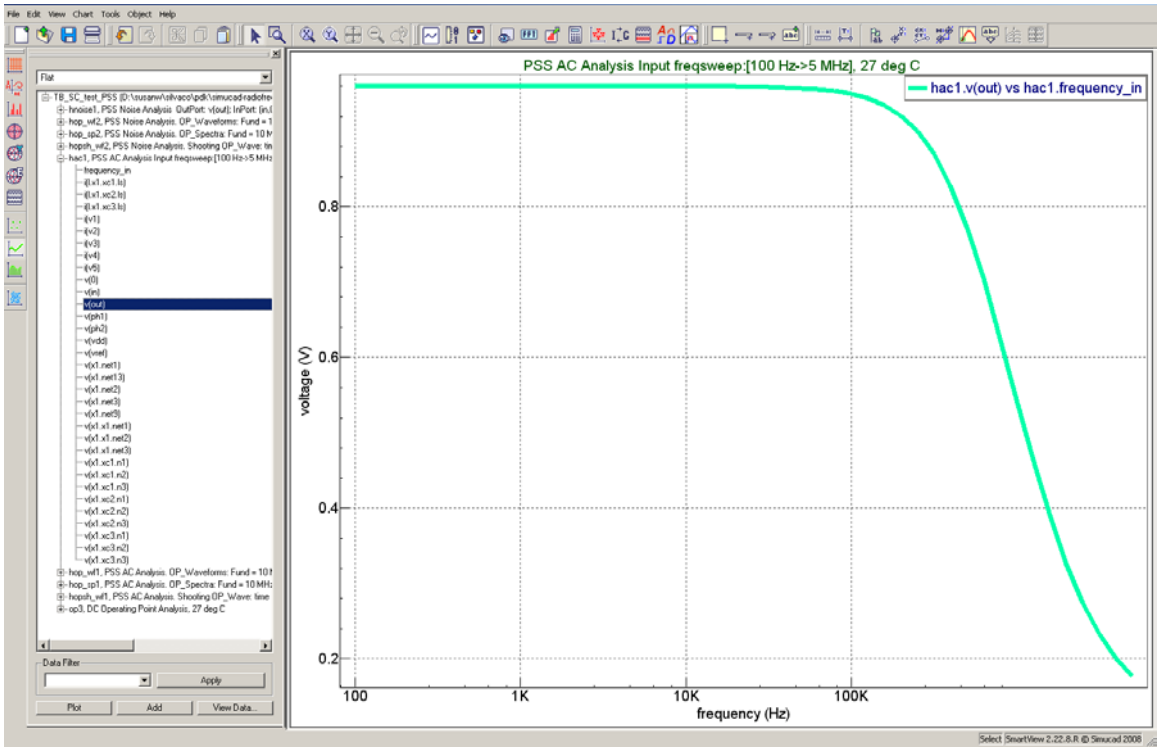

Figure 13: Transfer Function Plot

Open plot `hnoise1`, then select vector `onoise_s`, and click **Plot**.

The output noise plot is shown in Figure 14.

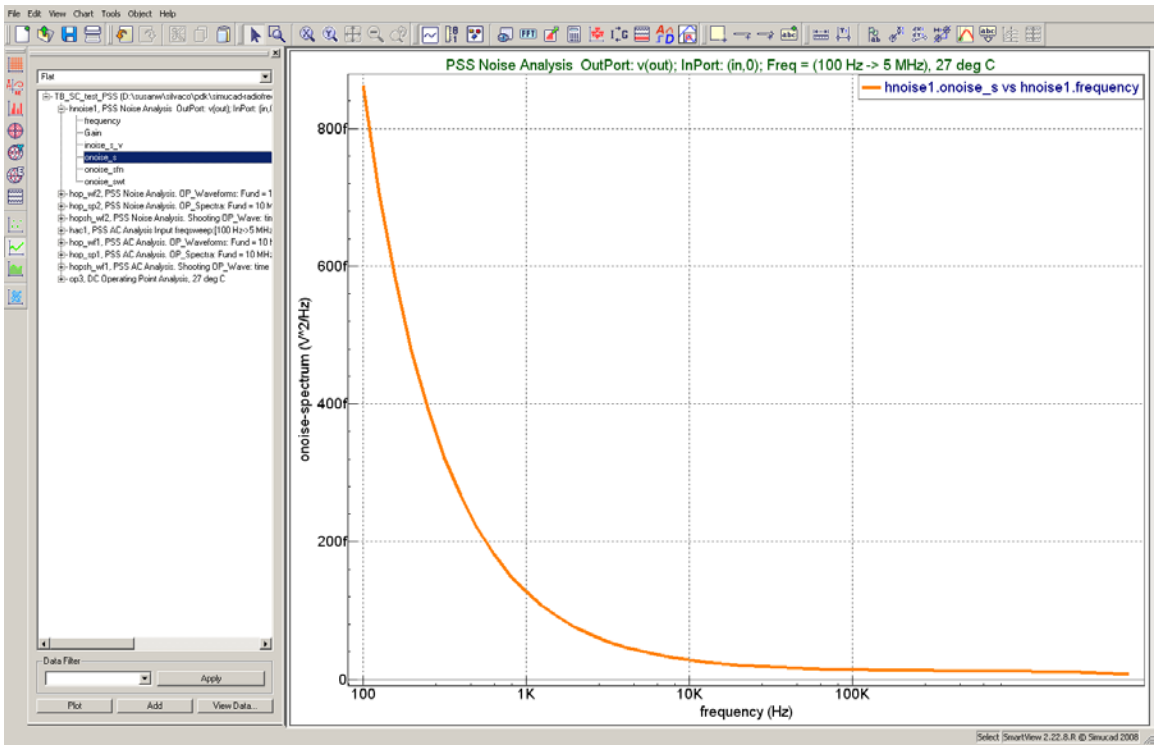

Figure 14: Output Noise Plot