hipex_ex04 : Hipex Parasitic RC Extraction Example (Hipex-RC)

Requires: Expert, Hipex
Minimum Versions: Expert 4.8.8.R, Hipex 3.4.7.R.

This example demonstrates running Hipex Parasitic RC Extraction on a layout in the Expert interactive layout environment

1: Setting up Hipex-RC in Expert

First start the Expert layout editor program, either with the command **expert** or by clicking the expert icon. From the main menu bar at the top, click **File → Open** to pop up the *Load Project* menu, navigate to the directory into which the ***hipex_ex04.eld*** design database file was downloaded and **Open** it. This will call up the *Open Cell(s)* menus, and here double-click ***mux4***, the top-level cell. By default this shows the hierarchical view of the design; you can see the full details by clicking **View → Cell View → Flat**. (*Figure1)*

The next step is to load the required Hipex technology files and change any settings to customize the extraction. From the main Expert menu, click **Verification → Extraction → Setup**; this pops up the *Layout Parameter Extraction Setup* panel. The pages within this panel are accessed using the menu on the left. (*Figure2* *Technology* page shown)

The first page *Layout* shows the Database file and Top cell; by default these are set to the currently open database and cell. The second page, *Node Names*, controls how instance and net names are derived. Specifying Global node names (eg, VSS for Ground) will cause those names to be declared as *.GLOBAL in the extracted netlist.

The fourth page, *Cell Explosion*, controls the extraction of the design hierarchy. The default is to EXPLODE all cells, which has the effect of producing a flat netlist in this simple example; to create a fully hierarchical netlist, click **Set all → Hcell.**

The fifth page, Netlisting, controls the details of the extracted netlists and parasitic files which will be generated. Default filenames for all the possible types of output are generated based of the current design/cell; you can change these and/or set options, for example to output the source/drain areas/perimeter or set a threshold on parasitic capacitances to be shown. Note that this page only controls the details of the output; if does not enable or initiate the actual generation of the output files; this is done at a later stage.

The sixth page, *Technology*, is where you need to specify the technology files for the extractions. For *Derived layer generation*, select *Use external script* and use the file browser to specify the ***hipex_ex04_lvs.dsf*** file previously downloaded. This file controls the generation of device recognition layers from the drawn/mask layers.
For a parasitic RC extraction, you must select *Use external LISA script* in the *Parasitic capacitance technology* and *Parasitic resistance technology* sections and use the file browser to specify, respectively, the ***hipex_ex04_c.lisa*** and ***hipex_ex04_r.lisa*** files previously downloaded.

The seventh page, *Parasitic Extraction*, provides more advanced settings. For parasitic resistance extraction it allows you to specify a resistance threshold to prevent the generation of tiny resistors in the netlist, and to specify that parasitic resistors are not generated for power nets (Ignore power node)

When you have completed all required pages, click OK in the *Layout Parameter Extraction Setup* Panel

2: Hipex Parasitic RC Extraction

The netlist extraction can now be run, with **Verification → Extraction → Hipex-Net → Run** from the main Expert window. This step is necessary even if only the parasitics are required, because the full connectivity must first be extracted to identify all the nodes.

After the netlist extraction has been done, it is now possible to continue to parasitic RC extraction. This is run in almost exactly the same way as the Hipex-Net extraction with the commands from the main Expert window: **Verification → Extraction → Hipex-RC → Run**

When the netlist extraction has completed a window will popup, inviting you to *Close*, *Open Netlist* or *Show Detail* (ie. Show the run log). The *Open Netlist* editor window shows both the text netlist (on the left) and a hierarchy display (on the right). These are linked; clicking on a device in the hierarchy display will highlight the corresponding item in the text netlist. It is also linked to the layout, so clicking on the item in the hierarchy display will also jump to the relevant cell in the Expert layout editor**. (***Figure3*)

As with the plain netlist extraction, you can go back into the Verification → Extraction → Netlister menu and create other types of netlists, including flat netlists from the hierarchical databases: Verification → Extraction → Netlister → RC Flat Spice Netlist (*Figure4*)

Another option is to select *Output parasitic net models* in the *Netlisting* control page. This causes the parasitics to be output as separate subcircuits in separate files, which can improve the readability of the netlists for large circuits with a lot of parasitics (Figure5).