

## hipex\_ex05 : Hipex DSPF/SPEF Parasitic Extraction

Requires: Expert, Hipex

Minimum Versions: Expert 4.8.8.R, Hipex 3.4.7.R.

This example demonstrates running Hipex Parasitic Extraction on a layout in the Expert interactive layout environment, with output in DSPF/SPEF format

### 1: Setting up Parasitic Extraction in Expert

First start the Expert layout editor program, either with the command **expert** or by clicking the expert icon. From the main menu bar at the top, click **File** → **Open** to pop up the *Load Project* menu, navigate to the directory into which the [hipex\\_ex05.eld](#) design database file was downloaded and **Open** it. This will call up the *Open Cell(s)* menus, and here double-click **mux4**, the top-level cell. By default this shows the hierarchical view of the design; you can see the full details by clicking **View** → **Cell View** → **Flat**. ([Figure1](#))

The next step is to load the required Hipex technology files and change any settings to customize the extraction. From the main Expert menu, click **Verification** → **Extraction** → **Setup**; this pops up the *Layout Parameter Extraction Setup* panel. The pages within this panel are accessed using the menu on the left. ([Figure2](#) *Netlisting* page shown)

The first page *Layout* shows the Database file and Top cell; by default these are set to the currently open database and cell. The second page, *Node Names*, controls how instance and net names are derived. Specifying Global node names (eg, VSS for Ground) will cause those names to be declared as \*.GLOBAL in the extracted netlist.

The fourth page, *Cell Explosion*, controls the extraction of the design hierarchy. The default is to EXPLODE all cells, which has the effect of producing a flat netlist in this simple example; to create a fully hierarchical netlist, click **Set all** → **Hcell**.

The fifth page, *Netlisting*, controls the details of the extracted netlists and parasitic files which will be generated. Default filenames for all the possible types of output are generated based of the current design/cell. In the final section for *Parasitic RC netlist* you can select the output netlist format; the standard SPICE format is enabled by default, but you can also enable **DSPF** and **SPEF** formats for digital timing or STA back-annotation. You may select any of the formats simultaneously.

The sixth page, *Technology*, is where you need to specify the technology files for the extractions. For *Derived layer generation*, select *Use external script* and use the file browser to specify the [hipex\\_ex05\\_lvs.dsf](#) file previously downloaded. This file controls the generation of device recognition layers from the drawn/mask layers. To do a parasitic capacitance or RC extraction, you must select *Use external LISA script* in the *Parasitic capacitance technology* section and use the file browser to specify the [hipex\\_ex05\\_c.lisa](#) file previously downloaded. To do a parasitic resistance or RC extraction, you must select *Use external LISA script* in the *Parasitic resistance technology* section and use the file browser to specify the [hipex\\_ex05\\_r.lisa](#) file previously downloaded.

The seventh page, *Parasitic Extraction*, provides more advanced settings. For parasitic resistance extraction it allows you to specify a resistance threshold to prevent the generation of tiny resistors in the netlist, and to specify that parasitic resistors are not generated for power nets (Ignore power node).

When you have completed all required pages, click OK in the *Layout Parameter Extraction Setup* Panel

## 2: Parasitic Extraction

The netlist extraction can now be run, with **Verification → Extraction → Hipex-Net → Run** from the main Expert window. This step is necessary even if only the parasitics are required, because the full connectivity must first be extracted to identify all the nodes.

After the netlist extraction has been done, it is now possible to continue to parasitic (R, C, or RC) extraction. These are run in almost exactly the same way as the Hipex-Net extraction with the commands from the main Expert window.

For parasitic capacitance extraction: **Verification → Extraction → Hipex-C → Run**

For parasitic resistance extraction: **Verification → Extraction → Hipex-R → Run**

For parasitic distributed RC extraction: **Verification → Extraction → Hipex-RC → Run**

The progress panel, which these runs pop up, give you the option to open the netlist in the interactive Netlist Editor: This is only relevant to the spice netlist format; the DSPF/SPEF formats are only parasitic netlists and cannot support probing of the normal devices. The DSPF/SPEF netlists can instead be viewed from a separate menu entry, eg. **Verification → Extraction → Hipex-RC → View DSFP Netlist**. ([Figure3](#)) The DSPF/SPEF netlists will be placed in an SPF subdirectory, or as set in the *Netlisting* setup page.

Note that the normal mode for DSPF/SPEF file generation is full RC (as opposed to R or C). However it is also possible to generate an R-only or C-only DSPF/SPEF file. To do this, you must delete any RC databases; the simplest way to do this is to delete the while .xwd directory. Then run **Hipex-C or Hipex-R**, and finally run the DSPF and/or SPEF netlister **Verification → Extraction → Netlister → DSPF Netlist** or **Verification → Extraction → Netlister → SPEF Netlist**. ([Figure4](#))