SmartSpiceRF

Voltage Controlled Oscillator Simulation

Tutorial

Introduction

Information presented in this Tutorial is based on the assumption that the user is familiar with the following:

- Basics of the computer operating system and hardware employed
- Basic terminology of semiconductor process and device operation
- Circuit design, schematic capture, and simulation

The simulation flow described in Tutorial uses Silvaco Process Design Kit (PDK) based on a fictional process called SBCD (Silvaco Bipolar Cmos Dmos). SBCD process includes the following devices: two low-voltage Cmos, two high-voltage Dmos, four resistors, capacitor, and inductor. SBCD libraries provide all the data needed to demonstrate a real design flow.

This Tutorial presents front end design flow of Voltage Controlled Oscillator (VCO) and guides you through the following circuit design steps:

- Schematic Capture with Gateway
- Simulation with SmartSpiceRF
- Results postprocessing with SmartView

The following Silvaco EDA tools are needed to work with Tutorial:

- GATEWAY
- SMARTSPICERF
- SMARTVIEW

1: GATEWAY Schematic Capture

Start `Gateway` and load the workspace file `VCO.workspace` by selecting **File→Open→Workspace.** When the browser window appears, navigate to the directory where `RF Demo PDK Examples` were installed, descent into `./VCO` directory, and select `VCO.workspace` file.

1.1: Loading VCO Schematic

To load VCO example circuit schematic, select **File→Open→ Schematic**. When the file browser appears, navigate to the `./VCO` directory and select the file `VCO.schlr`. The VCO example circuit schematic will appear in the window (Figure 1).

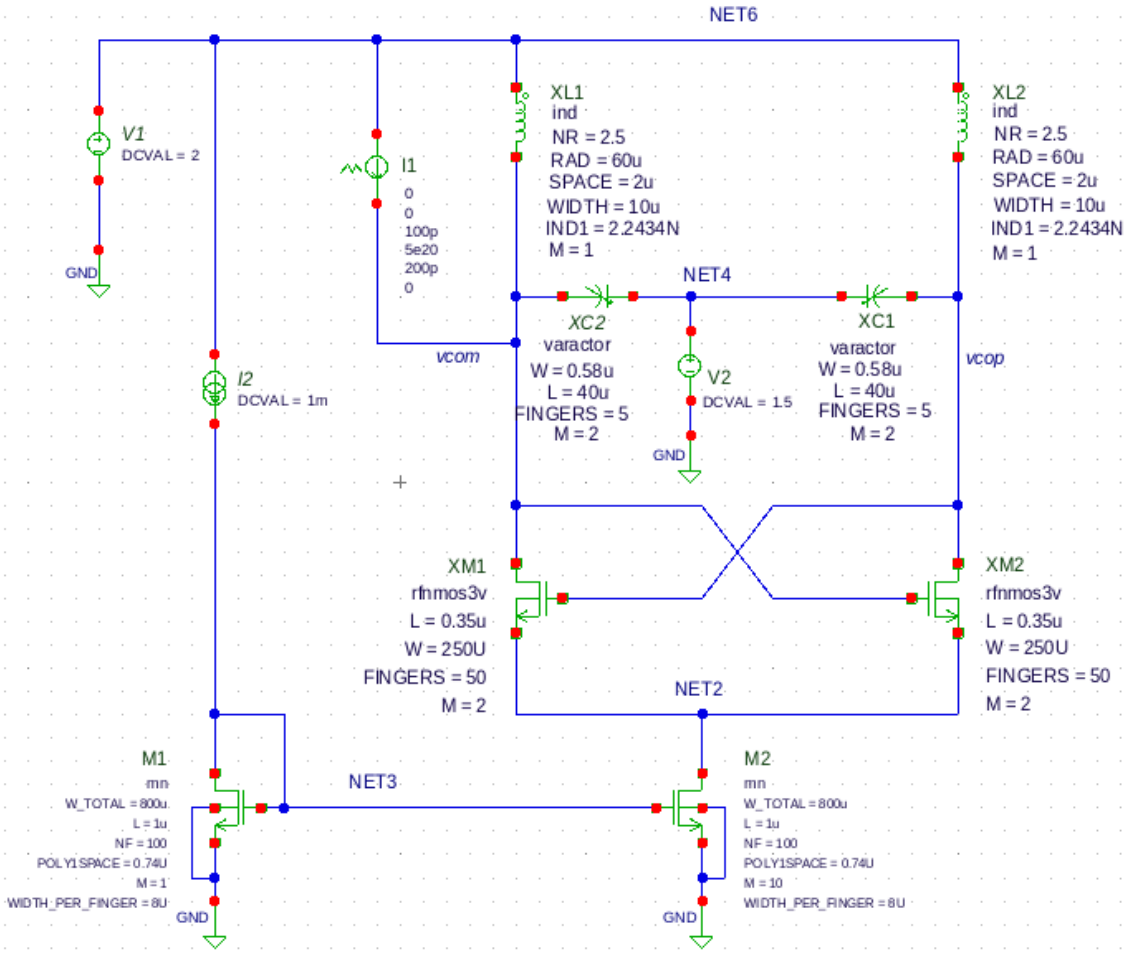

Figure 1: VCO Schematic

1.2: Editing Circuit Schematic

Edit VCO schematic shown in Figure 1. Double click on schematic symbol of Voltage source V2 to open Attributes Instance window (Figure 2). Set the DC voltage DCVAL = 0.5.

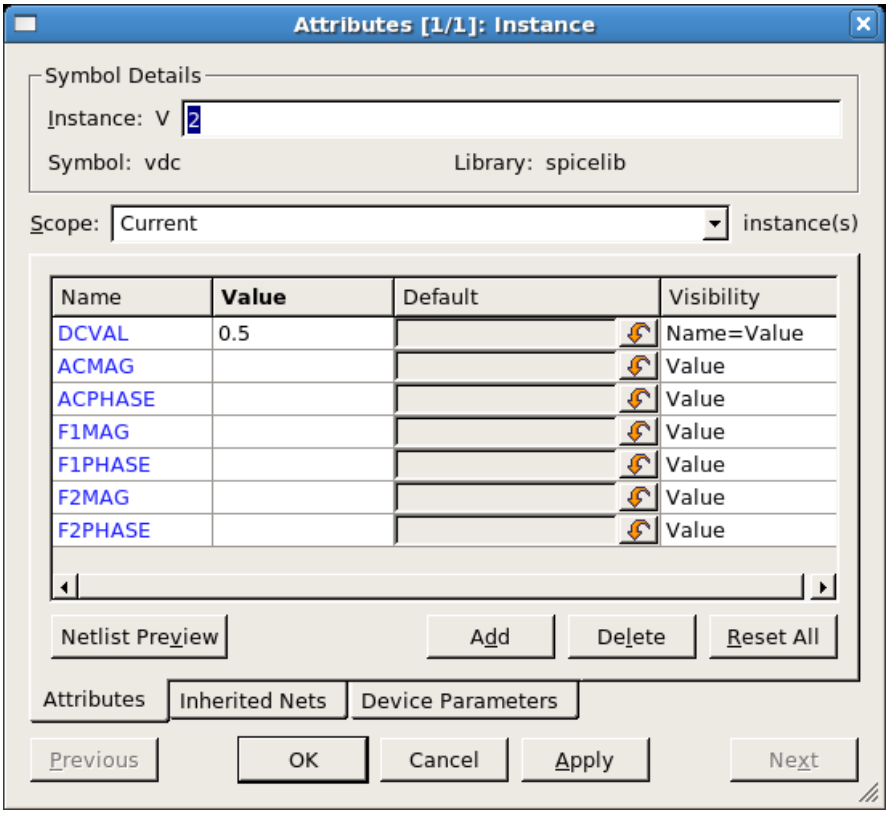

Figure 2: V2 Instance Attributes Window

1.3: Generating Netlists

Netlists are ASCII files used to describe device connectivity and element properties of the circuit. GATEWAY can create two different netlist formats: SMARTSPICE for circuit simulation, or GUARDIAN for layout design. See the GATEWAY USER'S MANUAL for more information on these formats.

To generate a netlist in SMARTSPICE format, either select **Simulation→Create Netlist,** or click on **SmartSpice Netlist** icon (Figure 3) in **Tool Bar**.

Figure 3: Create Netlist Icon

SMARTSPICE netlist then will appear in a new window:

```
1 * Gateway 2.10.5.A Spice Netlist Generator
2 * Workspace name:       U:\SmartSpice_RF\RF_Demo_PDK\gateway\simucad-radiofrequency-demo_sbcd.workspace
3 * Simulation name:      U:\SmartSpice_RF\RF_Demo_PDK\gateway\examples\VCO\VCO.schlr
4 * Simulation timestamp: 03-Dec-2009 11:18:27
5
6 * Schematic name: VCO
7 I1 NET6 vcom PWL(0 0 100p 5e20 200p 0 )
8 I2 NET6 NET3 DC 1m
9 M1 NET3 NET3 GND GND mn W=8U L=1u AS=3.0064P AD=2.96P PS=8.9116U PD=8.74U M=100
10 M2 NET2 NET3 GND GND mn W=8U L=1u AS=3.0064P AD=2.96P PS=8.9116U PD=8.74U M=1K
11 V1 NET6 GND DC 2
12 V2 NET4 GND DC 0.5
13 XC1 NET4 vcop varactor L=40u W=0.58u N=5 M=2
14 XC2 NET4 vcom varactor L=40u W=0.58u N=5 M=2
15 XL1 NET6 vcom ind WIDTH=10u RAD=60u SPACE=2u NR=2.5 M=1
16 XL2 NET6 vcop ind WIDTH=10u RAD=60u SPACE=2u NR=2.5 M=1
17 XM1 vcom vcop NET2 NET2 rfnmos3v LR=350N WR=5U NR=50 M=2
18 XM2 vcop vcom NET2 NET2 rfnmos3v LR=350N WR=5U NR=50 M=2
19
20 * End of the netlist
21
```

Figure 4: VCO Netlist

1.4: Simulator Setup

Check GATEWAY that your preferred simulator is set to SMARTSPICERF. In GATEWAY click on **Edit -> Preferences** to open the preferences setup window (Figure 5). Choose **Tools > Simulato**r and set (check) Simulator to SMARTSPICERF. Version number is set to Default (the latest installed version) in **Version** window. You can define any specific version too.

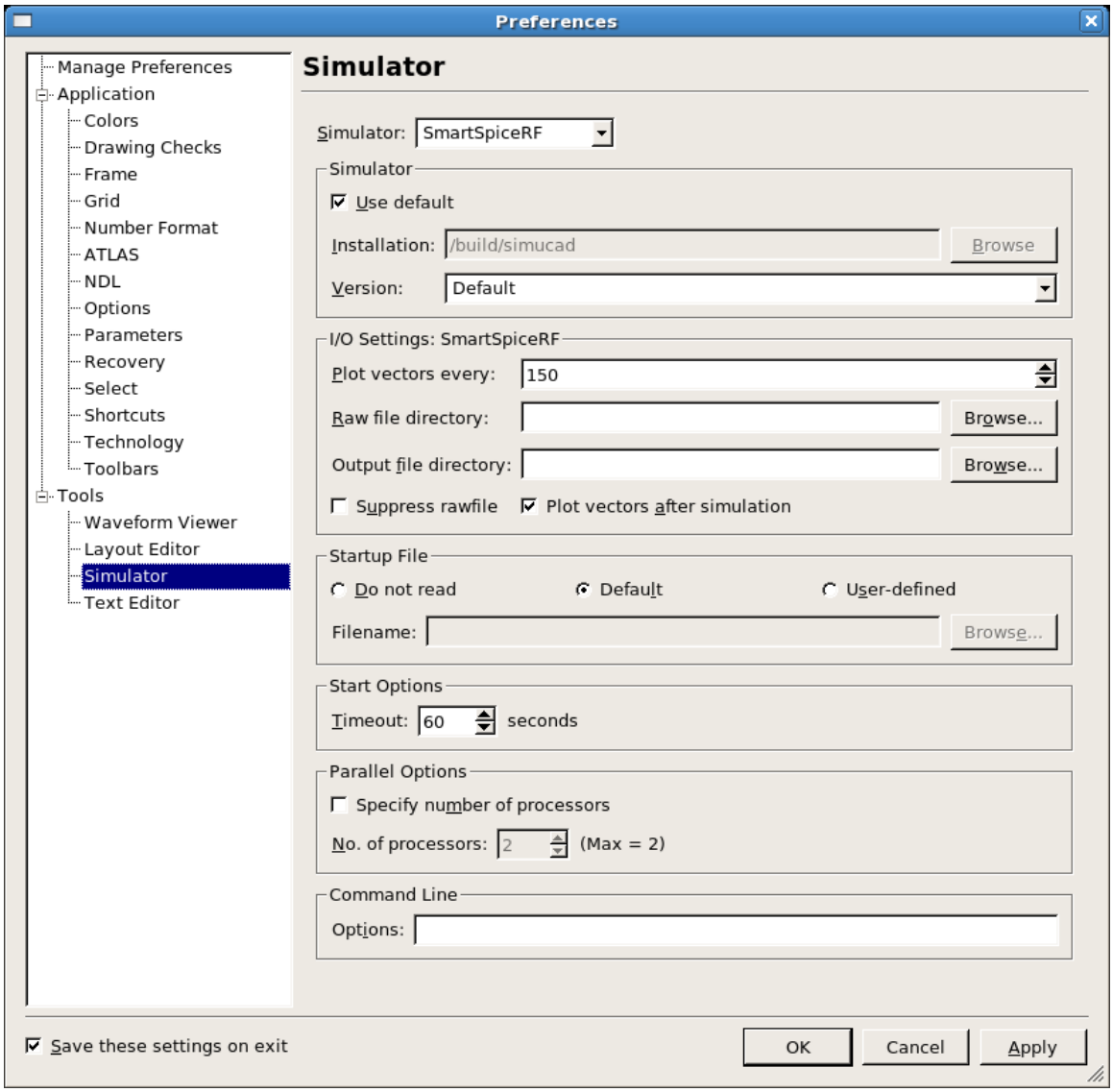

Figure 5: Simulator Preferences Window

1.5: Control File

SMARTSPICERF needs more than just a circuit netlist perform a meaningful simulations. It needs Circuit Netlist, Voltage or Current stimulus, set of Options, Analysis Statements, and active devices Model parameters or Libraries. All this information comes together in the form of Input Deck file (*.in, *.inp, *.cir, *.sp, *.sm, *.scs, etc.), which provides SMARTSPICERF with all needed information to run simulation and generate output data.

Click on the simulation **Tool Bar** icon **Edit Control File** (Figure 6):

Figure 6: Edit Control File Icon

The control file will be opened in the text editor `Sedit` window. The control file `VCO.ctr` (Figure 7) consists of path to SILVACO RF Demo PDK model library file as well as SMARTSPICERF .OP and .HNOISE Analyses statements. The control file combined with the circuit netlist and list of vectors to be saved creates an Input Deck for SMARTSPICERF.

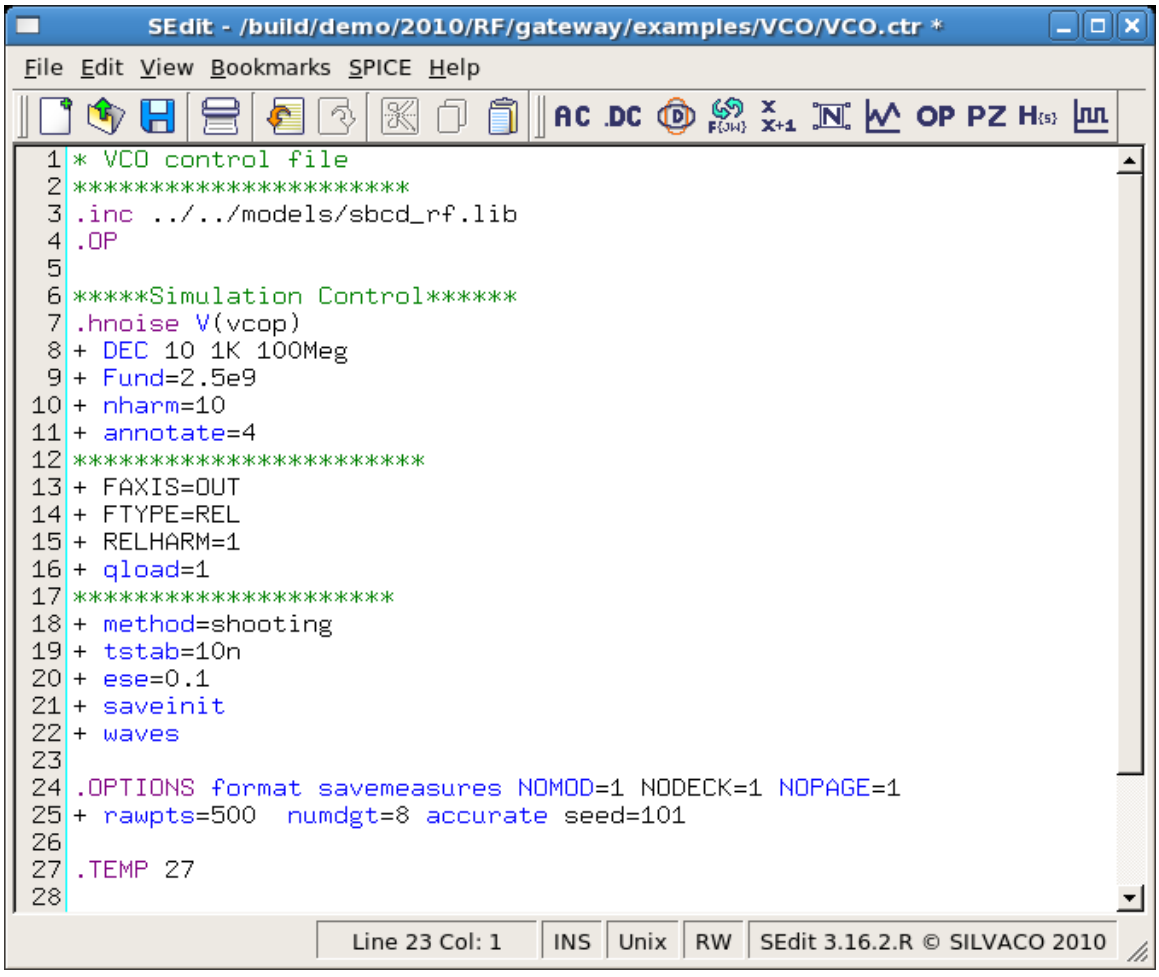

Figure 7: VCO Circuit Control File

1.6: VCO Noise Analysis Setup

Oscillator Noise Analysis is a two-stage process:

- Periodic Steady-State analysis is provided to find out Frequency of Oscillation, Amplitude of the Carrier, and Shape of the Output signal
- The following Small-Signal analysis is provided to compute Noise PSD and Phase Noise at the Given Output over desired Frequency range, offset from the Frequency of Oscillation.

The completed VCO.in input deck was created from the vco.net netlist and the vco.ctr control file containins the following analysis statement.

```
.hnoise V(vcop)
+ DEC 10 1K 100Meg
**********************
+ FTYPE=REL
+ FAXIS=OUT
+ RELHARM=1
*********************
+ nharm=10
+ method=shooting
+ qload = 1
+ tstab=10n
+ annotate=4
************************
+ saveinit
+ waves
*********************************************************
```

The .HNOISE analysis performs a frequency sweep of (+1KHz -> +100MHz) relative to the defined Frequency of Oscillation. PSS is calculated by Shooting method.

2: SmartSpiceRF Simulation

Click on  (**Gateway -> Simulation -> Run**) to begin the SMARTSPICERF simulation.

After the simulation is finished, the oscillation frequency of 2.08 e+09 Hz is shown in the Simulation Output window.

2.1: SmartSpiceRF Noise Simulation Results

SmartSpiceRF outputs simulation results of Large-Signal PSS and Small-Signal Noise analyses and statistic information into Output window and creates number of plots with Waveforms, Spectra, Noise, Measurement results, etc. .HNOISE analysis outputs Large-signal steady-state waveforms and spectra any of circuit variables.

2.1.1: Output window

Output window, for example, may consist of the following information:

```
Frequency of Oscillation   Fosc  = 2.499878e+007 Hz
Carrier:       Total Power    Psig  = 1.719005e+000 Wt
   1st Harmonic's Power   Psig1 = 7.844351e-001 Wt
    Effective amplitude          Ac = 1.854187e+000 V
```

2.1.2: SmartSpiceRF Plots and Vectors

Simulation results in form of plots will be loaded into SMARTVIEW, and SMARTVIEW **Data Browser** window will be open.

.HNOISE analysis produces the number of plots:

• **hopsh_wf** plot consists of the periodic steady-state waveforms at the final Shooting iteration.
• **hop_sp** plot consists of the frequency-domain spectra. The results are calculated from hopsh_wf waveforms by Inverse Fourier Transform at the frequency points *k*fund*, where *fund* is the calculated fundamental frequency of oscillation, and *k=0, 1, ..., nharm.*
• **hop_wf** plot consist of the waveforms at unified time grid with the number of time points defined by a specified number of harmonics *nharm*. This plot is output, if keyword WAVES was specified in analysis statement. If not, only the spectra plot hop_sp will be output.
• **hinit_wf** plot consists of the initial transient analysis waveforms,, if the keyword SAVEITER was specified in analysis statement.
• **hiter_wf** plots consist of the shooting iteration time-domain waveforms, if the keyword SAVEITER was specified in analysis statement.

.PRINT, .PROBE, .SAVE and .MEASURE statements must use the analysis and/or specific plot names HOPSH_WF, HOP_WF, HOP_SP and so forth, to make any measurement and output separate results. The output statements without the analysis type name will output all types of results for all types of analysis.

3: SmartView Graphic Postprocessor

Number of plots and associated vectors depends on type of analyses provided and used methods. Open plot “hnoise2”, select vector “PhaseNoise2”, and click **Plot**. The Phase Noise plot is shown in the SMARTVIEW window. The oscillation frequency of 2.08 GHz is shown in the header The phase noise at 100kHz offset frequency is -97.2dBc/Hz (Figure 8).

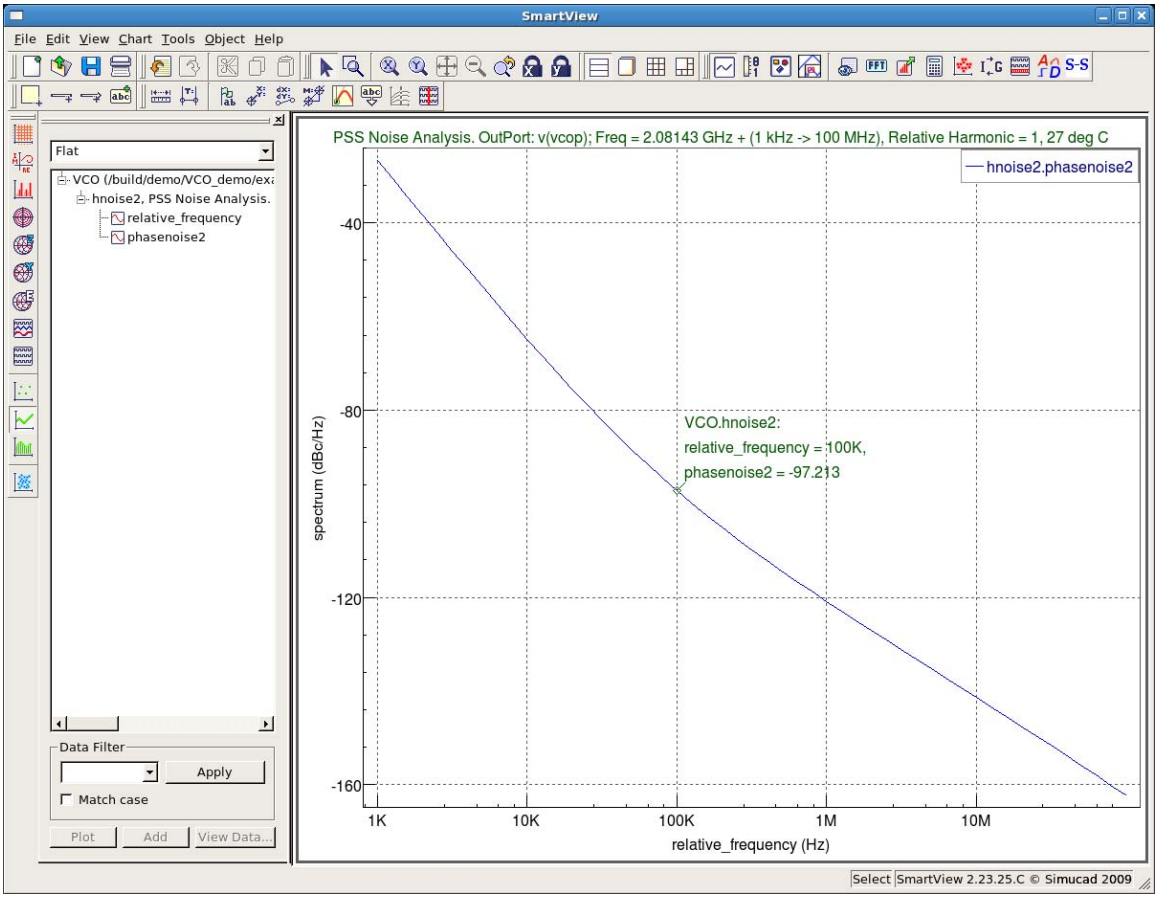

Figure 8: Phase Noise Plot for Tuning Voltage of 0.5 V

3.1: Return to GATEWAY schematic window and edit schematic shown in Figure 1. Set the DC voltage of V2 to DCVAL = 1.5 V. Click on GATEWAY **Tab**  to begin the second simulation.

3.2: After the simulation will finish, select vector "PhaseNoise" from "hnoise4" plot and click **Plot**. The oscillation frequency of 2.04558 GHz is shown in the header. The phase noise at 100kHz offset frequency is -96.953 dBc/Hz (Figure 9).

So the tuning range is 2.04 GHz to 2.08 GHz for the tuning voltage of 0.5 V to 1.5 V.

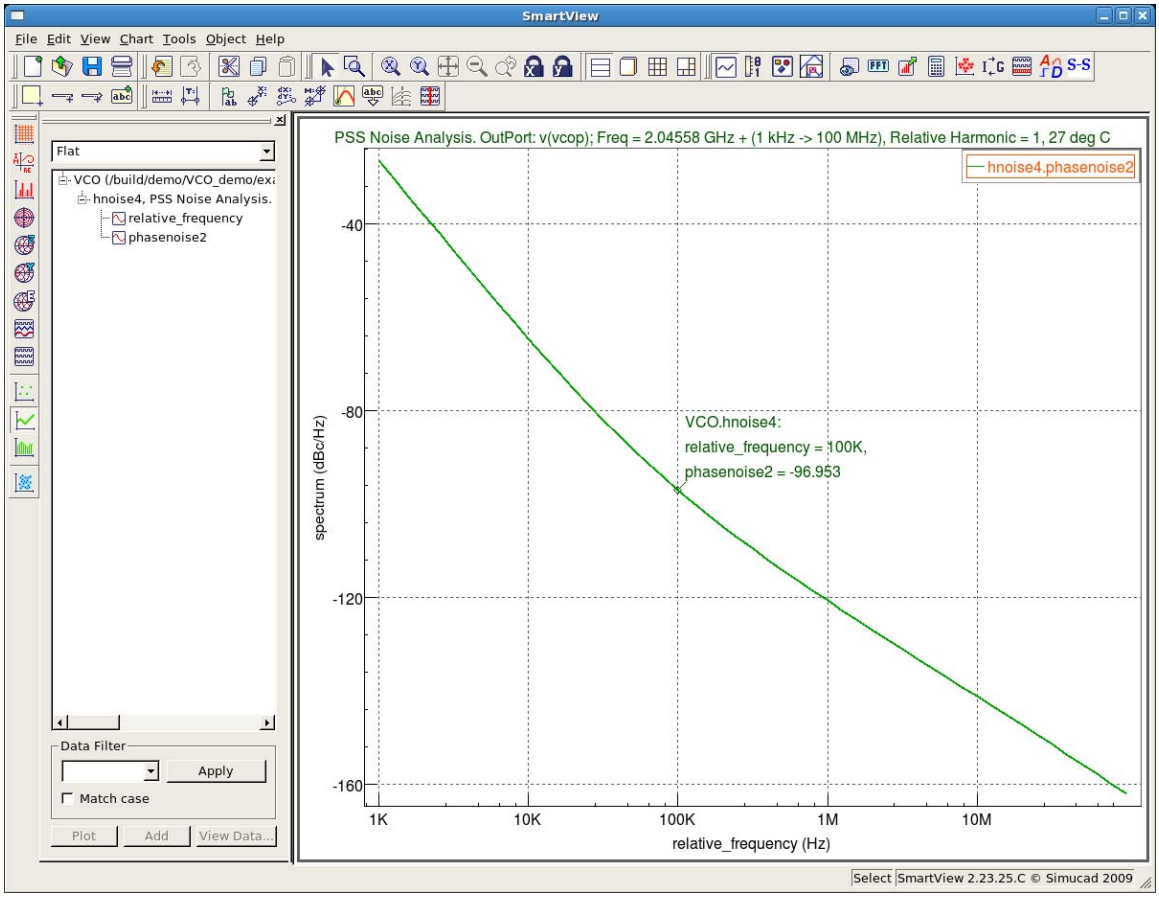

Figure 9: Phase Noise Plot for Tuning Voltage of 1.5 V

3.3: Remember we've added the "saveinit" flag into .HNOISE statement to save results of Initial Transient analysis of the Shooting method? OK so let's see what the start-up behavior of the oscillator looks like. In Data Browser Panel, select "hinit_wf2"plot, then select vector "V(vcop)" and click **Plot**. Figure 10 shows waveform at the oscillator node vcop for tuning voltage of 1.5V.

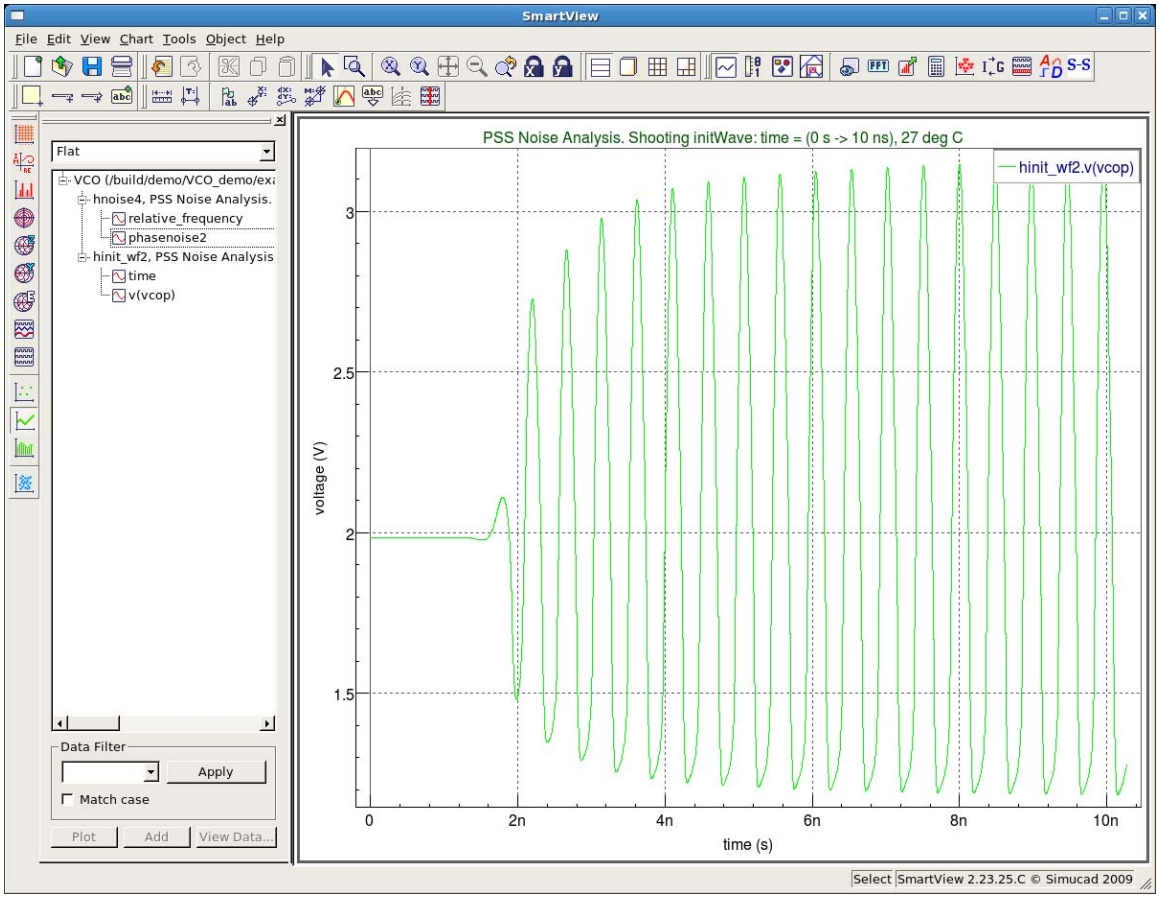

Figure 10: V(vcop) Waveform for Tuning Voltage of 1.5 V