

FPGA Innovation Design Contest AMD Track – FPT International Conference Design Report*

*Change your paper title

Anonymous Authors

Abstract—This paper presents a project developed for the 2025 National Undergraduate Embedded Chip and System Design Competition – FPGA Innovation Design Contest, AMD Track (Advanced Self-Selected Topic). The abstract should summarize the background, main contributions, technical approach, experimental results, and conclusion.

Index Terms—FPGA, hardware acceleration, embedded systems, parallel computing, AMD

I. INTRODUCTION AND RESEARCH BACKGROUND

A. Research Background

This section introduces the technical background and application domain of the project. It analyzes existing computing paradigms such as CPUs, FPGAs, GPUs, and ASICs, comparing their advantages and disadvantages. The section should identify the limitations of current technologies and the potential for innovation.

B. Main Contributions

The main contributions of this project are summarized as follows:

- 1) **Contribution 1:** [Detailed description]
- 2) **Contribution 2:** [Detailed description]
- 3) **Contribution 3:** [Detailed description]

C. Report Structure

This paper is organized as follows: Section II presents the design methodology and key technologies. Section III discusses experimental design and performance evaluation. Section IV provides comparative analysis. Section V outlines challenges, lessons learned, and future directions.

II. DESIGN METHODOLOGY AND KEY TECHNIQUES

A. Overall Design Concept

This section describes the overall design philosophy and methodology of the system.

B. Key Algorithm Design

The design and optimization of the core algorithms are elaborated here.

1) **Theoretical Foundations:** This part explains the mathematical principles underlying the proposed algorithms.

2) **Parallel Design:** Multi-level parallelization strategies are discussed in detail.

3) **Pipeline Design and Optimization:** This section describes the pipelined architecture and optimization techniques.

4) **Data Precision Analysis and Optimization:** An analysis of the impact of numerical precision on system performance and accuracy.

C. High-Performance Memory Design

1) **Memory Access Optimization:** Optimization techniques for memory access patterns are presented.

2) **Bandwidth Optimization:** This section discusses techniques to enhance memory bandwidth utilization.

D. Hardware-Software Interface Design

1) **High-Speed Communication Interfaces:** Design considerations for high-speed data transmission interfaces are detailed here.

III. EXPERIMENTAL DESIGN AND PERFORMANCE EVALUATION

A. Experimental Environment

1) Software Environment:

- **Operating System:** [Version information]
- **Development Tools:** [Vivado/Vitis version]
- **Programming Environment:** [Languages and libraries]

2) **Benchmark Comparison:** This section describes the baseline implementations used for performance comparison.

B. Functional Verification

1) **Unit Testing:** Detailed testing of each module is provided.

2) **Integration Testing:** System integration testing results are presented.

C. Performance Testing

1) **Latency Testing:** Detailed latency measurement results are presented.

2) **Accuracy Verification:** Verification of algorithmic accuracy is described.

D. Resource Utilization Analysis

TABLE I
FPGA RESOURCE UTILIZATION

Resource	Used	Available	Utilization	Evaluation
LUT	[num]	[total]	[%]	[evaluation]
FF	[num]	[total]	[%]	[evaluation]
BRAM	[num]	[total]	[%]	[evaluation]
DSP	[num]	[total]	[%]	[evaluation]

1) Logic Resource Usage:

2) *Memory Resource Efficiency*: A detailed analysis of memory resource utilization efficiency.

3) *Computation Resource Efficiency*: An analysis of DSP and LUT computational efficiency.

E. Performance Comparison and Analysis

1) Comparison with Existing Solutions:

- **Performance Comparison:** Comparative performance results between this work and existing solutions.
- **Advantage Analysis:** A detailed analysis of the advantages of this work.
- **Limitation Analysis:** A discussion of the current limitations of this work.

2) *Scalability Analysis*: Analysis of scalability and adaptability of the proposed design.

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APPENDIX A SYSTEM SOURCE CODE DIRECTORY TREE

```
project_root/
└── src/ : Source code directory
    ├── rtl/ : RTL code
    │   ├── top_module.v : Top-level module
    │   ├── accelerator/ : Accelerator core
    │   ├── interface/ : Interface modules
    │   └── utils/ : Utility modules
    ├── software/ : Software section
    │   ├── driver/ : Drivers
    │   ├── api/ : API interfaces
    │   └── app/ : Applications
    ├── constraints/ : Constraint files
    ├── testbench/ : Test files
    └── scripts/ : Build scripts
    └── docs/ : Documentation
    └── data/ : Test data
    └── results/ : Experimental results
    └── README.md : Project description
```

APPENDIX B KEY LLM INTERACTION RECORDS

A. Important Interaction 1:

- **User Question:** [Simplified question]
- **LLM Suggestion:** [Key suggestion summary]
- **Implementation Effect:** [Observed improvement]

B. Important Interaction 2:

- **User Question:** [Simplified question]
- **LLM Suggestion:** [Key suggestion summary]
- **Implementation Effect:** [Observed improvement]

C. Important Interaction 3:

- **User Question:** [Simplified question]
- **LLM Suggestion:** [Key suggestion summary]
- **Implementation Effect:** [Observed improvement]

APPENDIX C OTHER SUPPLEMENT CONTENTS