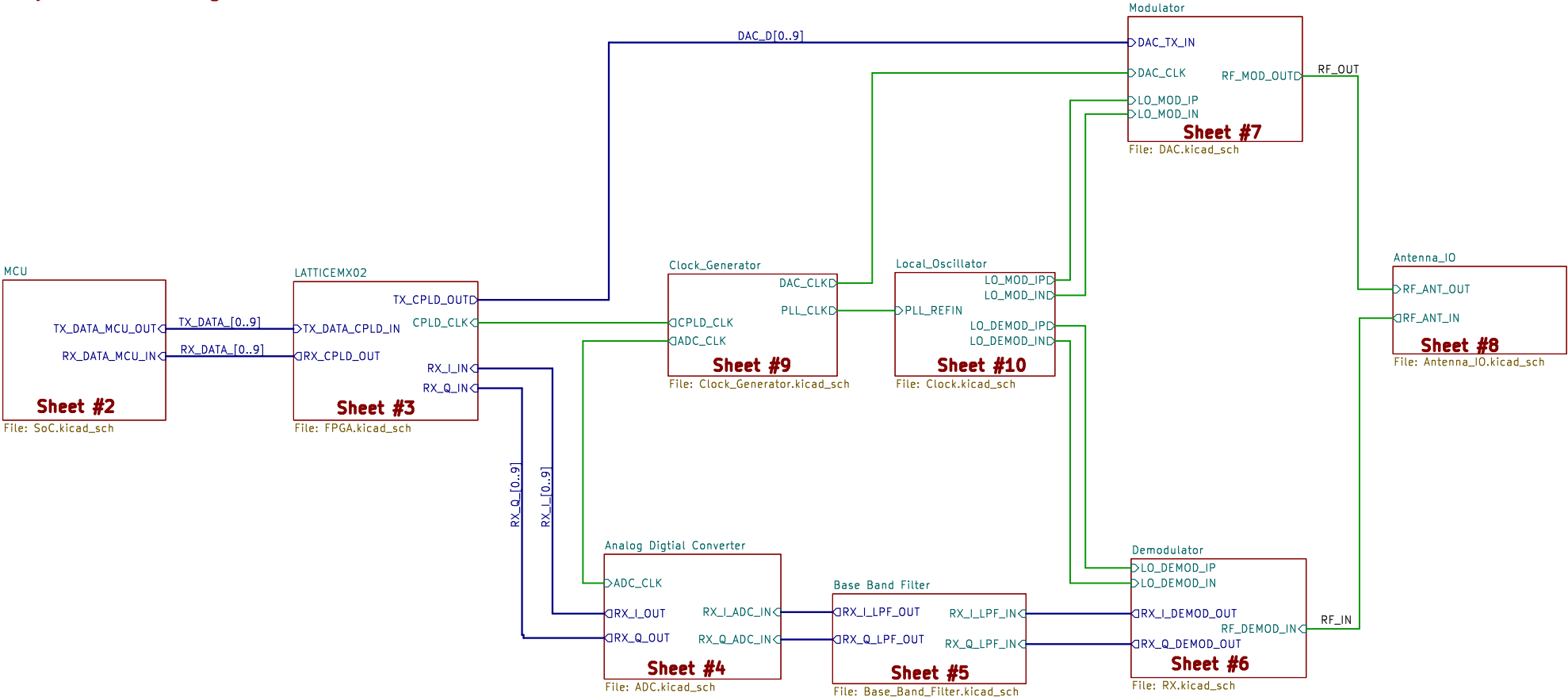


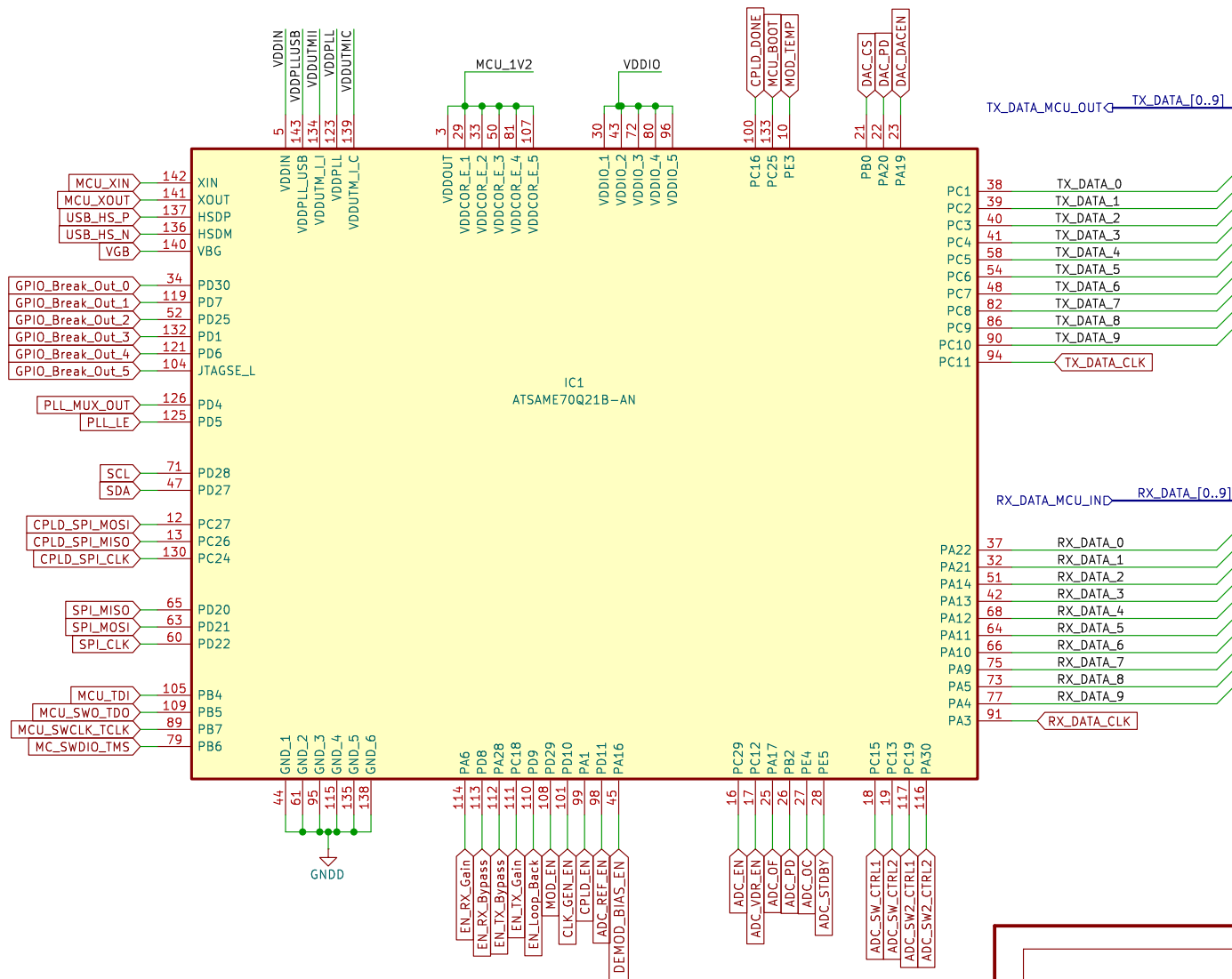
System Diagram



Power and Connectors

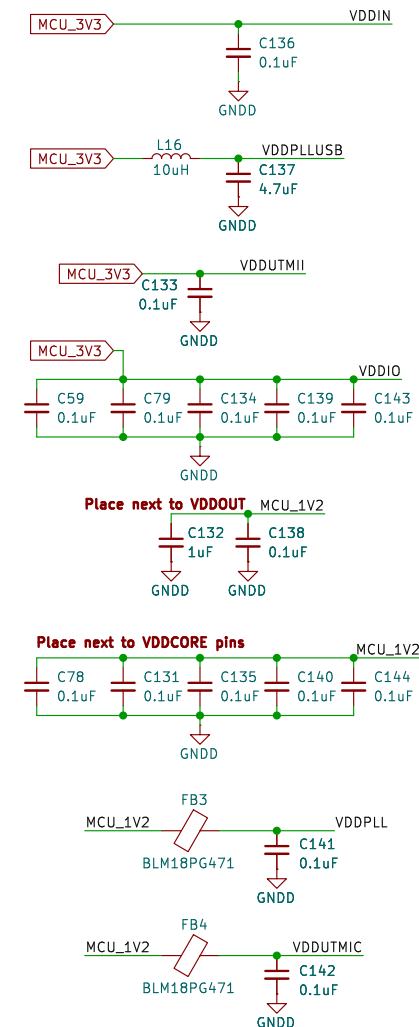


MCU, SAME70



VDDCORE, VDDPPL, and VDDUTMIC are powered through the embedded 1.2 V regulator through VDDOUT

MCU Power Filters



Sheet: /MCU/
File: SoC.kicad_sch

Title:

Size: A4
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Rev:

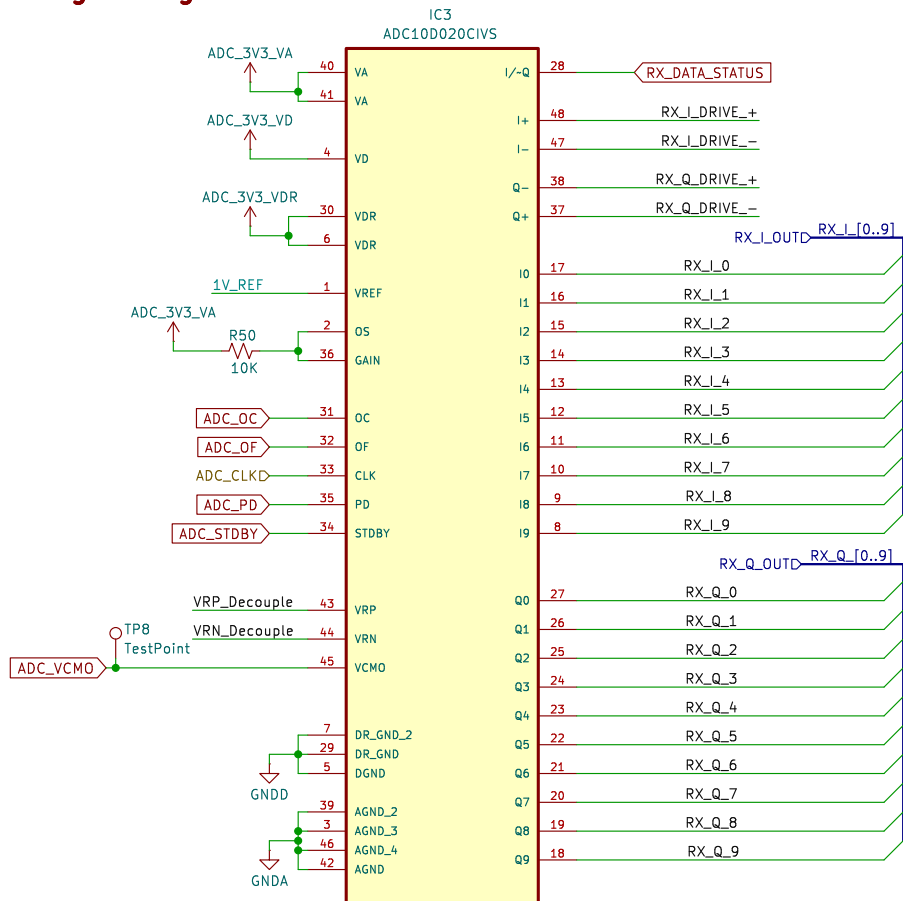
Id: 2/12

[illegible]

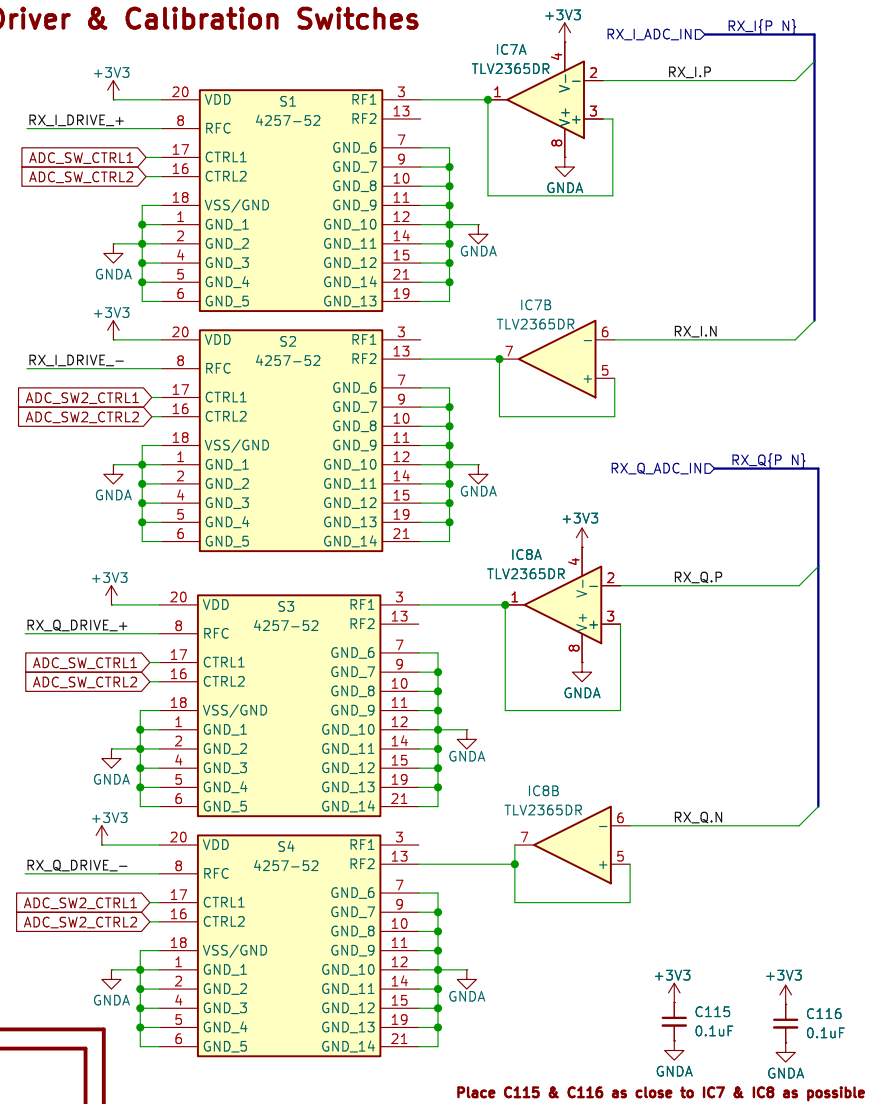
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File: FPGA.kicad_sch		
Title:		
Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.8		Id: 3/12

Place C120–C130 as close to each power pin as possible

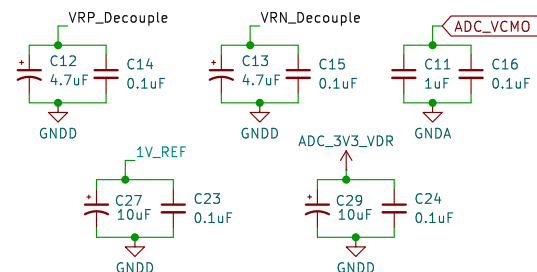
Analog To Digital Converter



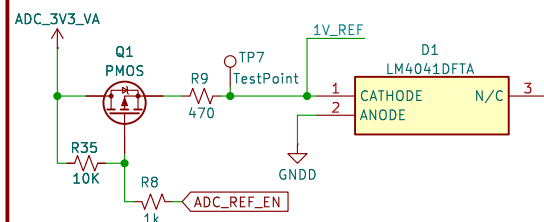
ADC Driver & Calibration Switches



ADC Decoupling Capacitors



1V Reference



Sheet: /Analog Digital Converter/
File: ADC.kicad_sch

Title:

Size: A4

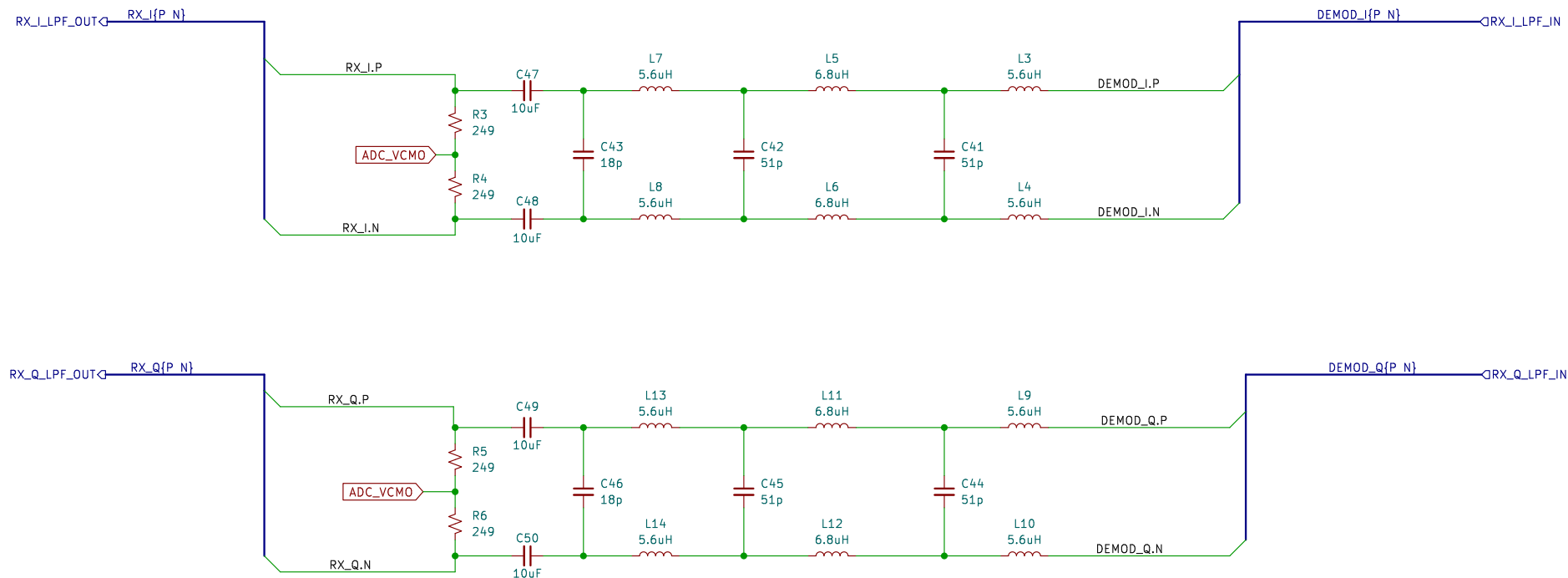
Date:

KiCad E.D.A. 8.0.8

Rev:

Id: 4/12

Base Band Low Pass Filter, 6th Order Chebyshev



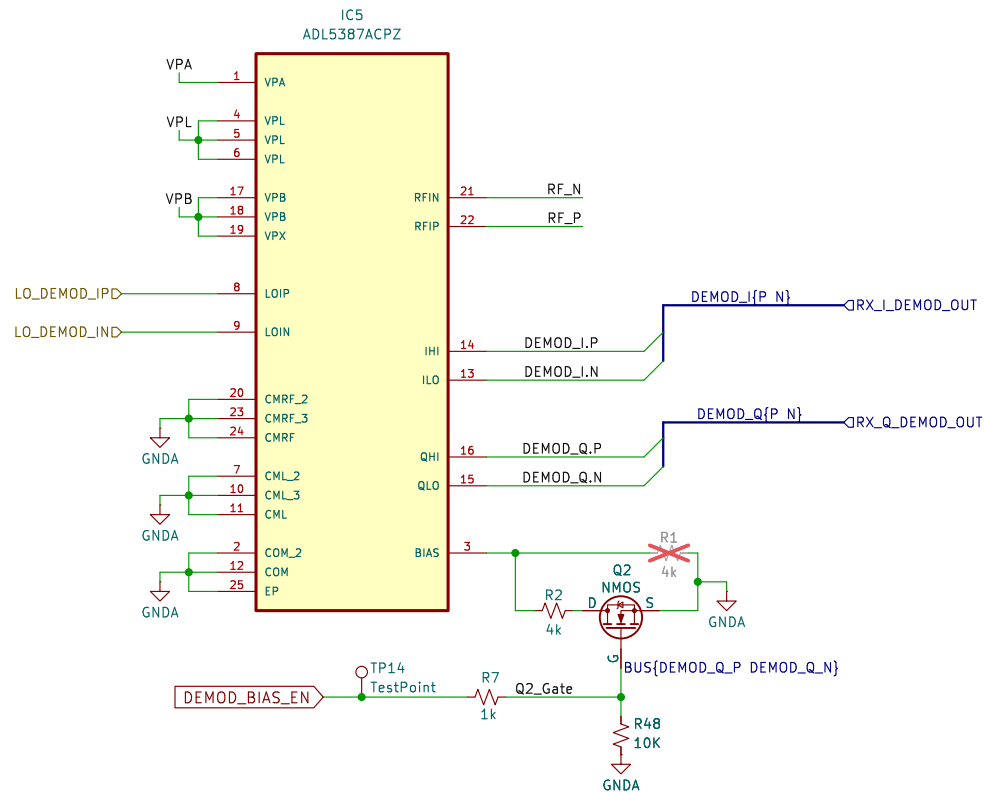
Notes:

The ADL5387 has an output bandwidth of 240 MHz. While the ADC12020 is capable of sampling at a rate of 20 MSPS. In order to prevent signal ailsining a differential low pass filter as been implemented on both the I and Q signals.

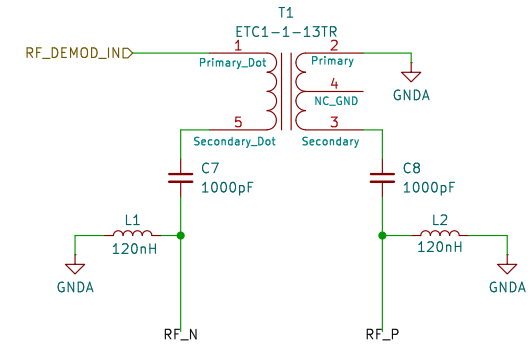
A Chebyshev typology was selected to maximize signal attenuation when all poles combine within the stop band. The filters were tuned to 10 MHz, despite the maximum 20 MHz bandwidth made availble through quadature sampling. This decsion was made based on data rate limitaiions with USB 2.0 operating at 480 Mbps.

Sheet: /Base Band Filter/ File: Base_Band_Filter.kicad_sch		
Title:		
Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.8	Id: 5/12	

Demodulator



BALUN Transformer



The BALUN transformer is used to generate a differential signal from the single ended RF Signal created by the antenna

Reccomened Inductance

For operation above 50 MHz $L1 = L2 = 120\text{nH}$, $C9 = C10 = 1000\text{ pF}$
For operation above to 30 MHz $L1 = L2 = 680\text{nH}$, $C9 = C10 = 0.01\text{ }\mu\text{F}$

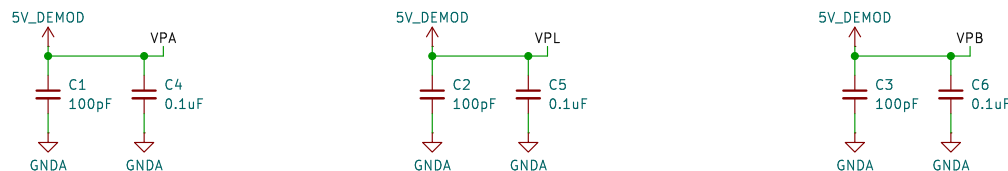
General Notes:

Differential Pairs RX_I_LO & RX_I_HI , RX_Q_LO & RX_Q_HI have a range of 2Vpp with a bias voltage of $V_{dd} - 2.8$. There for when $V_{dd} = 5$ Vbias = 2.2 V and the differential signals have a range of 1.2 to 3.2 V

When the BIAS pin is open, the mixer runs at maximum current and have the highest dynamic range. The mixer current can be reduce by placing a resistor to ground. By reducing the mixer current, the overall power consumption, noise figure, and IIP3 will also be reduced

Power pins are grouped to nearby pins, place power decoupling circuits as close to the demodulator as possible

RF Power Decoupling



Sheet: /Demodulator/
File: RX.kicad_sch

Title:

Size: A4
KiCad E.D.A. 8.0.8

Date:

Rev:
Id: 6/12

Digital to Analog Converter

The diagram illustrates the circuit for a Digital to Analog Converter (DAC) using the IC4 MAX5185. The circuit includes the following components and connections:

- Power Supply:** The DAC is powered by +3V3 and GND. The AVDD and DVDD pins are connected to +3V3 and GND through decoupling capacitors C34, C35, C36, and C37.
- Control Pins:** The DACEN, PD, CS, and CLK pins are connected to the DAC control signals.
- Digital Input:** The digital input is DAC_D[0..9], connected to the DAC_D0 through DAC_D9 pins.
- Reference Voltage:** The reference voltage is set by DAC_REF0, connected to the REF0 pin and TP9.
- Output Pins:** The output pins are OUT1P, OUT1N, OUT2P, and OUT2N, connected to the DAC_I+, DAC_I-, DAC_Q+, and DAC_Q- signals respectively.
- Grounding:** The AGND pin is connected to GND, and the REN pin is connected to GND. The NC pin is also connected to GND.

Modulator

The schematic diagram illustrates the Modulator section, centered around the IC6, ADL5385ACPZ-R7. The IC is represented by a yellow rectangle with pins 1 through 25. The connections are as follows:

- Power and Biasing:**
 - Pin 8 (VPS1) is connected to 5V_MOD, with a 0.1uF capacitor (C28) to GND.
 - Pin 11 (VPS2) is connected to 5V_MOD, with a 0.1uF capacitor (C30) to GND.
 - Pin 23 (VPS3) is connected to 5V_MOD, with a 0.1uF capacitor (C31) to GND.
 - Pin 24 (VPS3) is connected to 5V_MOD.
- TX Signals:**
 - Pin 13 (TX_L_HI) is connected to TX_L+.
 - Pin 14 (TX_L_LO) is connected to TX_L-.
 - Pin 18 (TX_Q_HI) is connected to TX_Q+.
 - Pin 17 (TX_Q_LO) is connected to TX_Q-.
- LO Signals:**
 - Pin 21 (LO_IN_HI) is connected to LO_MOD_IPD.
 - Pin 22 (LO_IN_LO) is connected to LO_MOD_IND.
- COM Signals:**
 - Pin 4 (COM1) is connected to COM1.
 - Pin 5 (COM1) is connected to COM1.
 - Pin 6 (COM1) is connected to COM1.
 - Pin 15 (COM2) is connected to COM2.
 - Pin 16 (COM2) is connected to COM2.
 - Pin 19 (COM3) is connected to COM3.
 - Pin 20 (COM3) is connected to COM3.
- Control and Output:**
 - Pin 10 (TEMP) is connected to MOD_TEMP.
 - Pin 12 (ENBL) is connected to MOD_EN.
 - Pin 7 (VOUT) is connected to RF_MOD_OUT.
 - Pin 25 (EP) is connected to GND.
 - Pin 3 (NC) is connected to GND.
 - Pin 2 (NC) is connected to GND.
 - Pin 1 (NC) is connected to GND.

DAC Driver

The DAC driver circuit consists of two stages. The first stage (left) uses two MCP6497 op-amp chips, IC9A and IC9B. IC9A is configured as a voltage follower with its non-inverting input (+) connected to DAC_I+ and its output (1) connected to TX_I+. IC9B is configured as an inverting amplifier with its non-inverting input (+) connected to DAC_I- and its output (7) connected to TX_I-. The second stage (right) uses two MCP6497 op-amp chips, IC10A and IC10B. IC10A is configured as a voltage follower with its non-inverting input (+) connected to DAC_Q- and its output (1) connected to TX_Q-. IC10B is configured as a voltage follower with its non-inverting input (+) connected to DAC_Q+ and its output (7) connected to TX_Q+. All op-amps are powered by +3V3 and GND. Resistors R18, R19, R20, R21, R22, R23, R24, and R25 are all 1.5K or 1K.

Notes

The following data listed is to provide insight into the behavior of the DAC Drivers:

- Full Scale output of DAC: 400mV
- Full Scale Input: 1V to 1.4V
- DC offset: 1.2V Internal DAC Reference
- Gain: 1.5
- Full Scale Output of DAC Driver: 1.5V to 2.1V

Sheet: /Modulator/ File: DAC.kicad_sch	
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Size: A4	Date:
KiCad E.D.A. 8.0.8	Rev: Id: 7/12

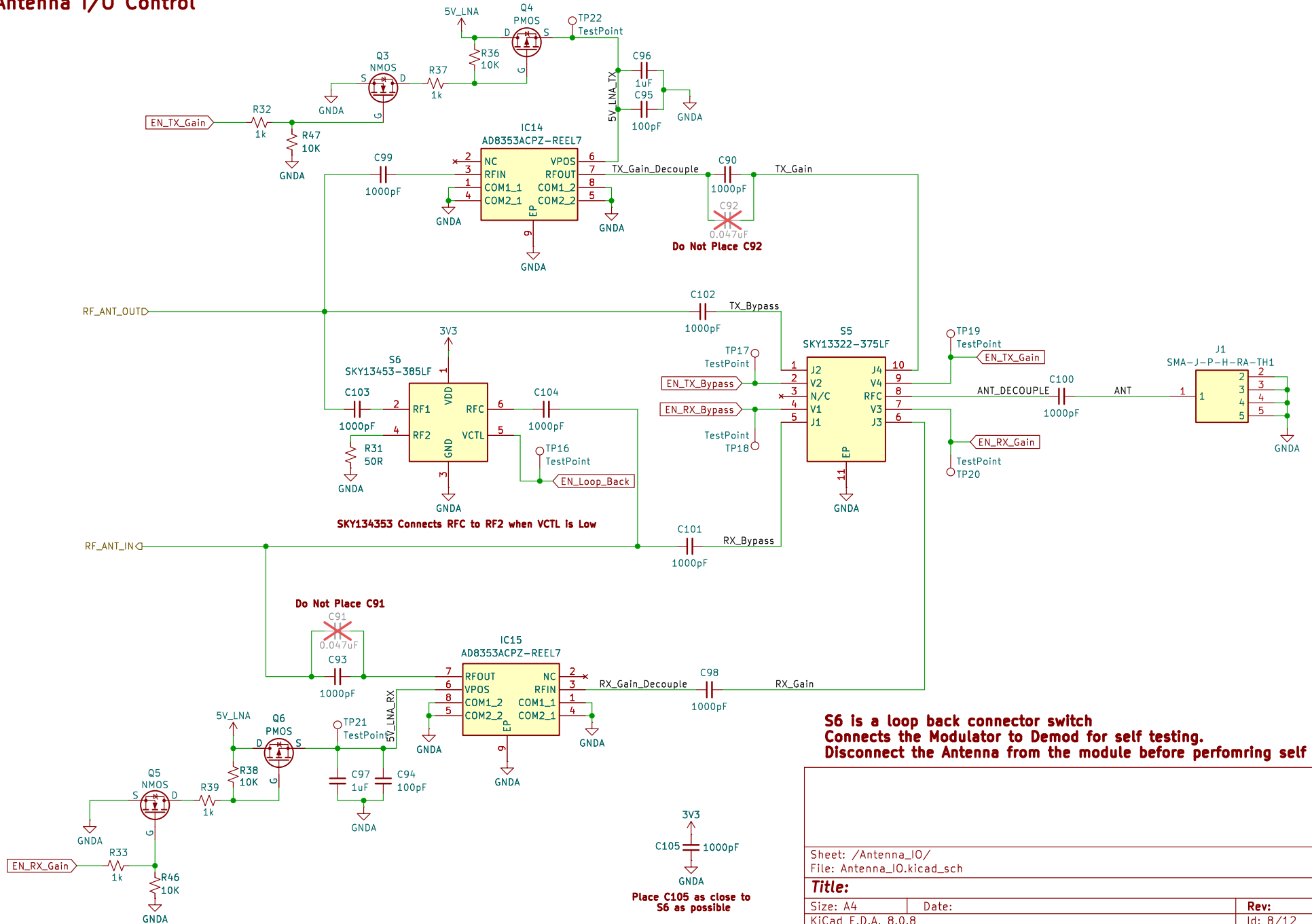
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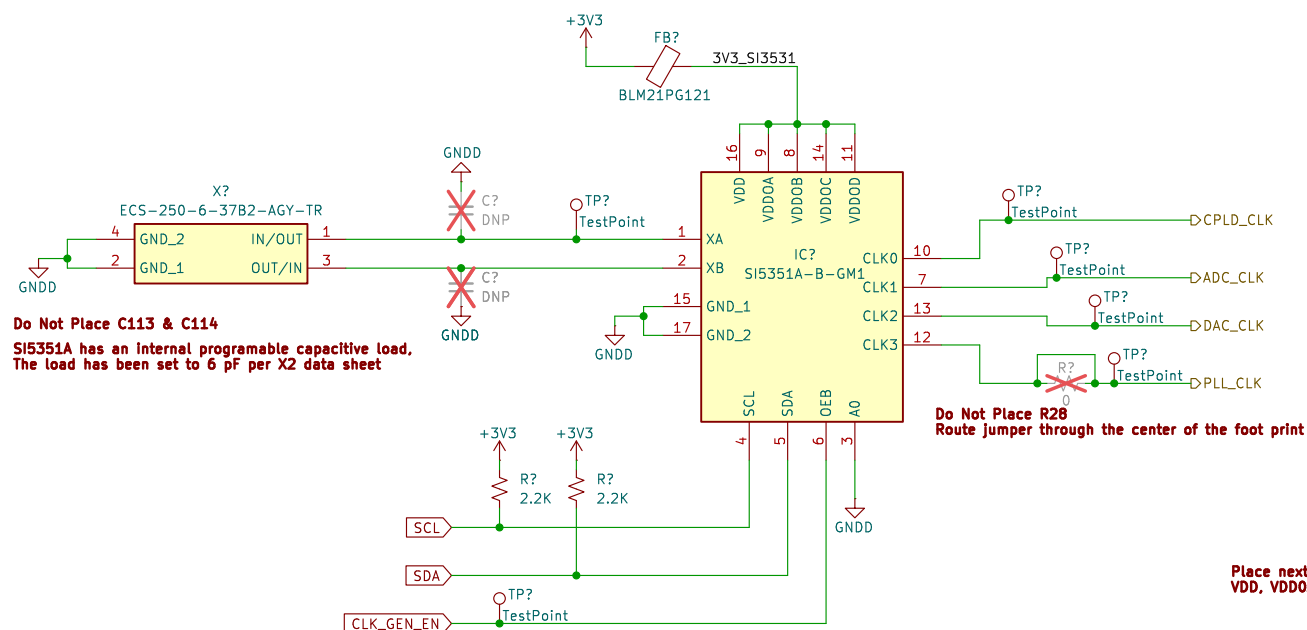
KiCad E.D.A. 8.0.8	Id: 7/12
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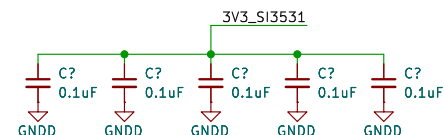
Antenna I/O Control



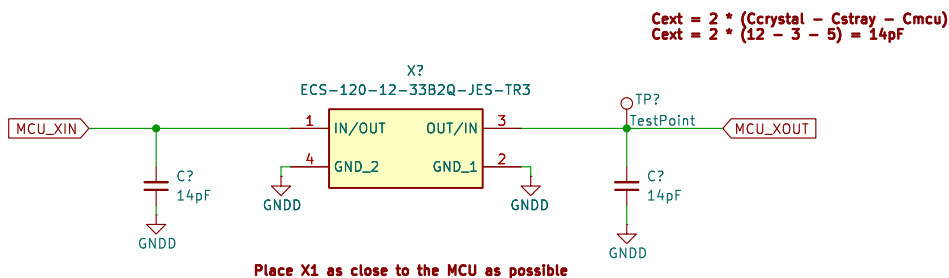
Clock Generator



Place next to each power supply pin:
VDD, VDD0A, VDD0B, VDD0C, and VDD0D



MCU Crystal



Notes:

IC13 Generates the clock signals for the FPGA, ADC, DAC, and the PLL for the Modulator and Demodulator

By default PLL is clocked by IC13, cut the jumper across R28 and populate R27 if you wish use clock the PLL using X2

OEB enables the output of IC13. The pin is Active Low, Pull High to disable outputs. All Output are enabled simultaneously.

Sheet: /Clock_Generator/
File: Clock_Generator.kicad_sch

Title:

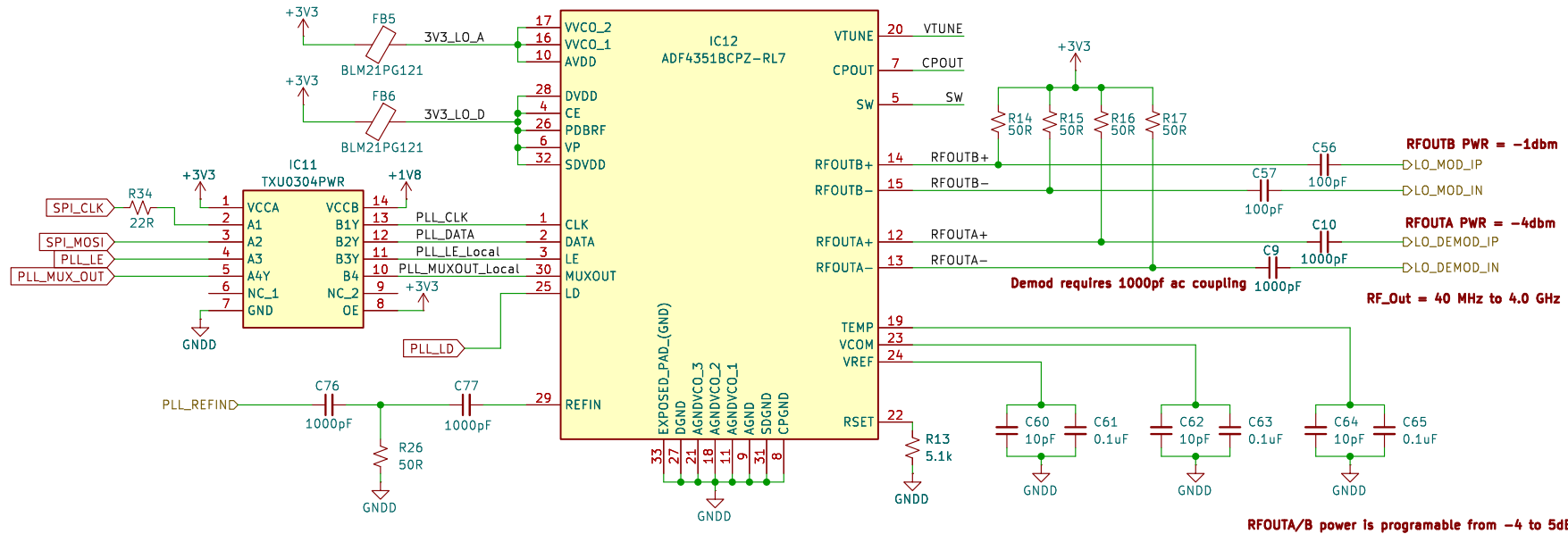
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KiCad E.D.A. 8.0.8	

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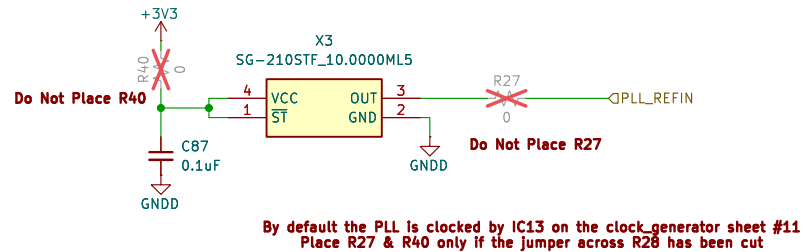
Rev:

Id: 9/12

Local Oscillator Clock Generator

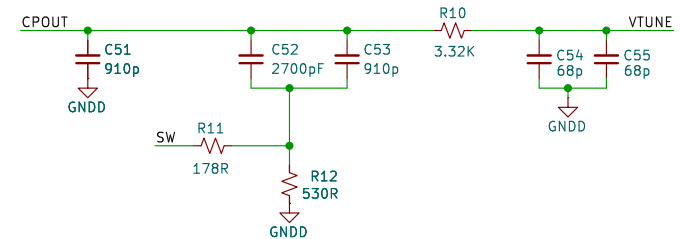


Crystal Oscillator



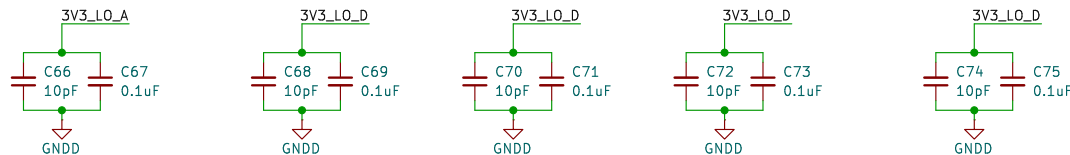
Loop Filter

Fast Lock Topology
 Loop Bandwidth: 50 KHz
 Phase Margin: 60.0 deg
 Time to Lock: 105 uS



PLL Power Decoupling

Place one Pair next to each power supply pin of IC12:
 DVDD, AVDD, PDBRF, VP, SDVDD



Sheet: /LocalOscillator/
 File: Clock.kicad_sch

Title:

Size: A4

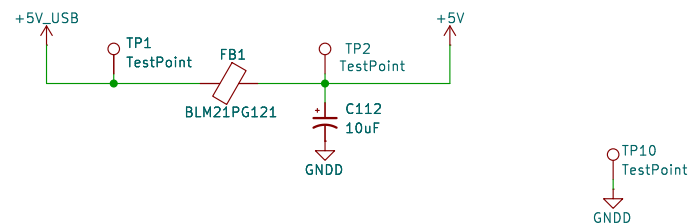
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Rev:

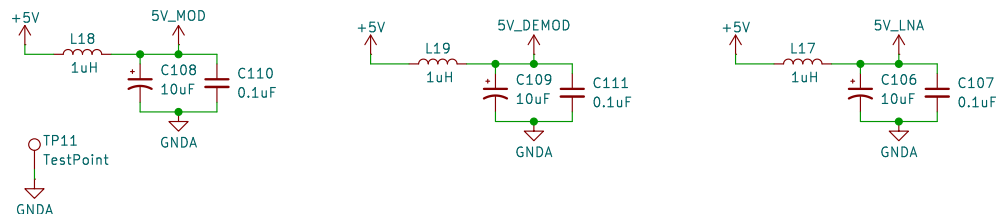
KiCad E.D.A. 8.0.8

Id: 10/12

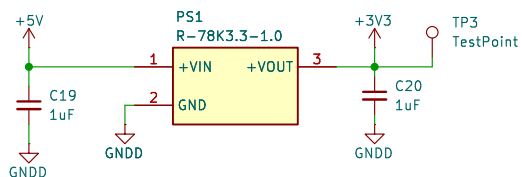
5V Power Input Filter



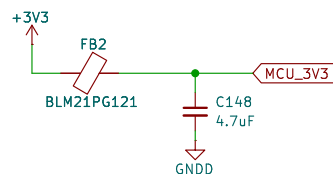
5V Analog Power Filters



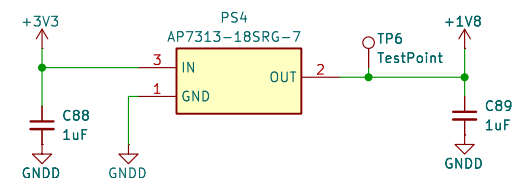
3V3 Power Supply



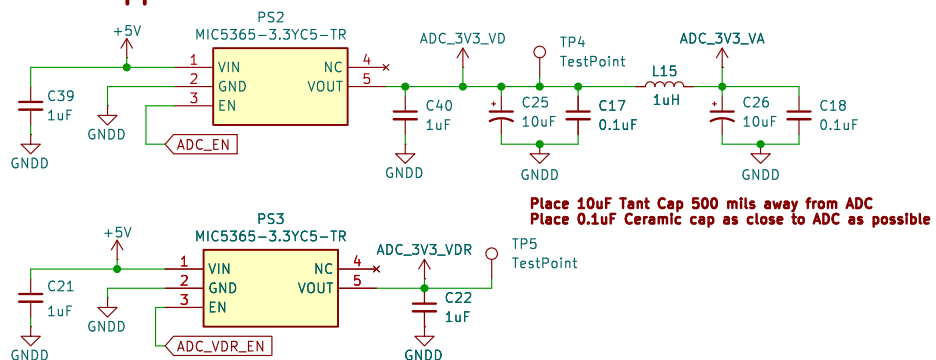
MCU Power Filter



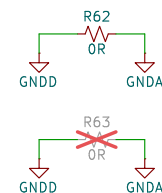
1V8 Power Supply



ADC Power Supplies



Analog & Digital Ground Jumper



Sheet: /Power/
File: Power.kicad_sch

Title:

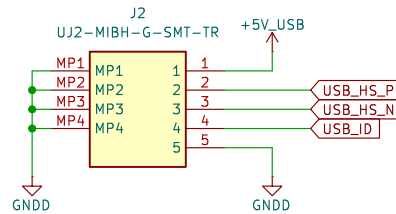
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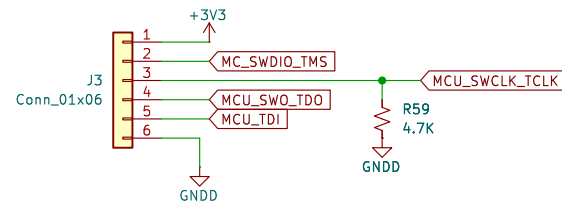
Rev:

Id: 11/12

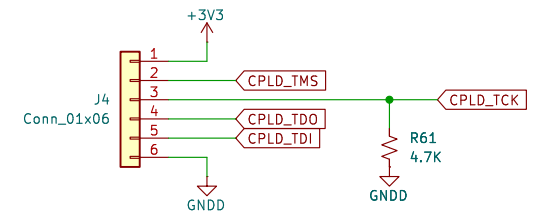
USB Connection



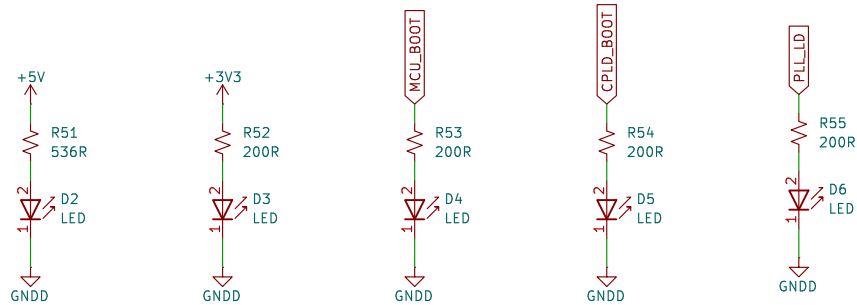
MCU Programing/JTAG



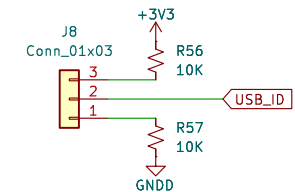
CPLD Programing/JTAG



Debuging LEDs

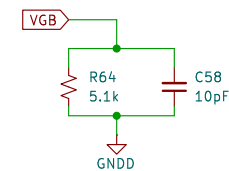


USB OTG Jumpers

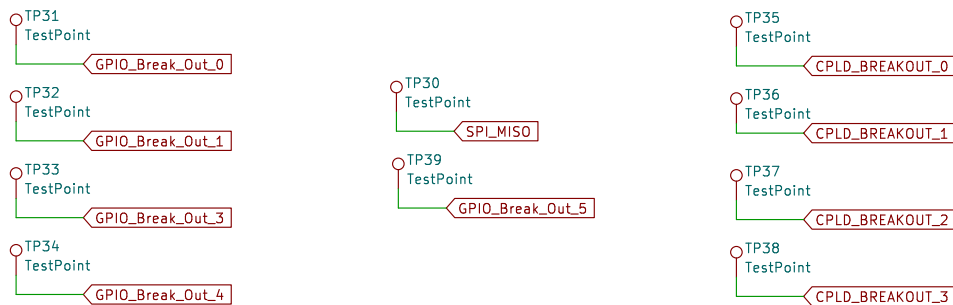


Leave Floating for USB Device/Generic Operation

For USB OTG:
Place Jumper across pins 1 and 2 for USB Device
Place Jumper across pins 2 and 3 for USB Host



Extra Pin Breakout



Sheet: /Connectors/
File: Connectors.kicad_sch

Title:

Size: A4

Date:

KiCad E.D.A. 8.0.8

Rev:

Id: 12/12