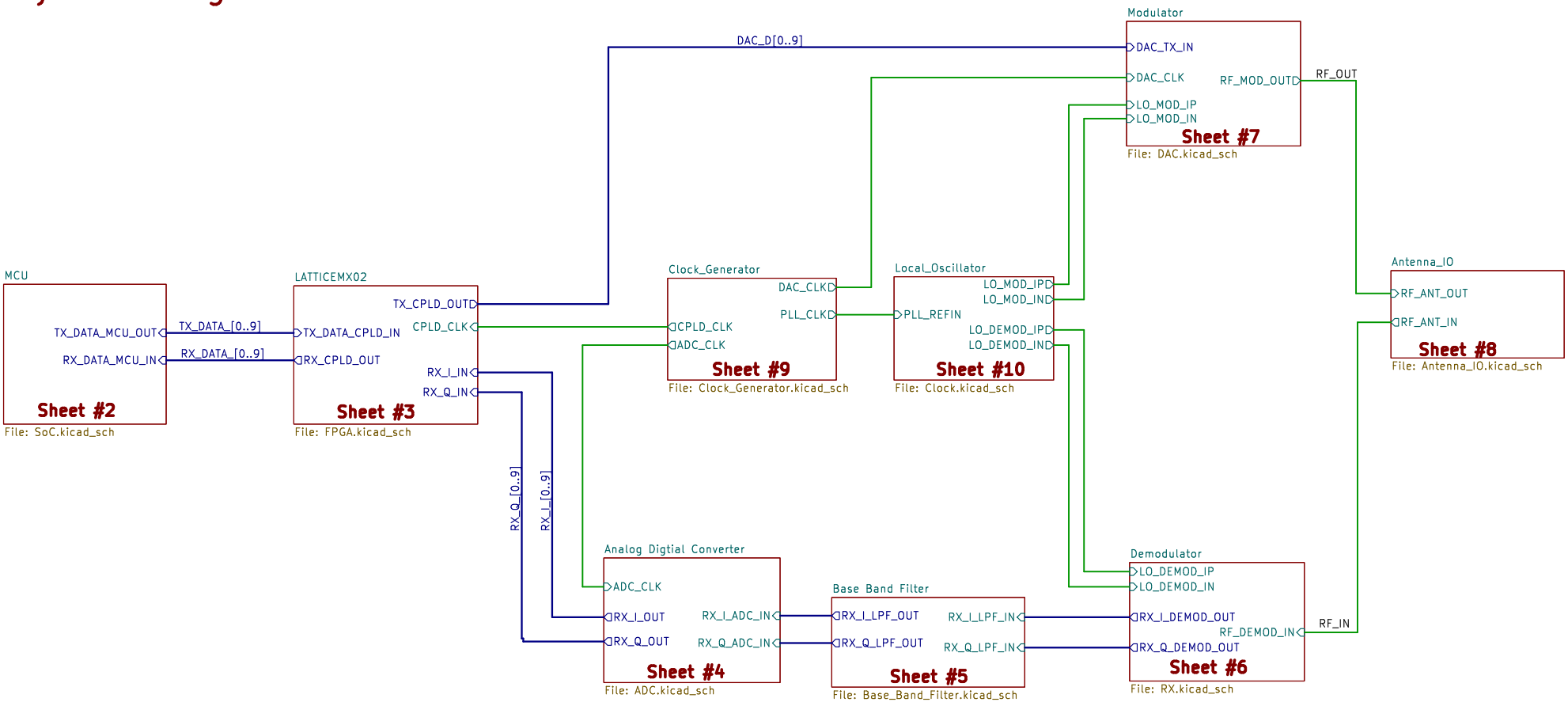
System Diagram



Power and Connectors

Power

Sheet #11

File: Power.kicad_sch

Connectors

Sheet #12

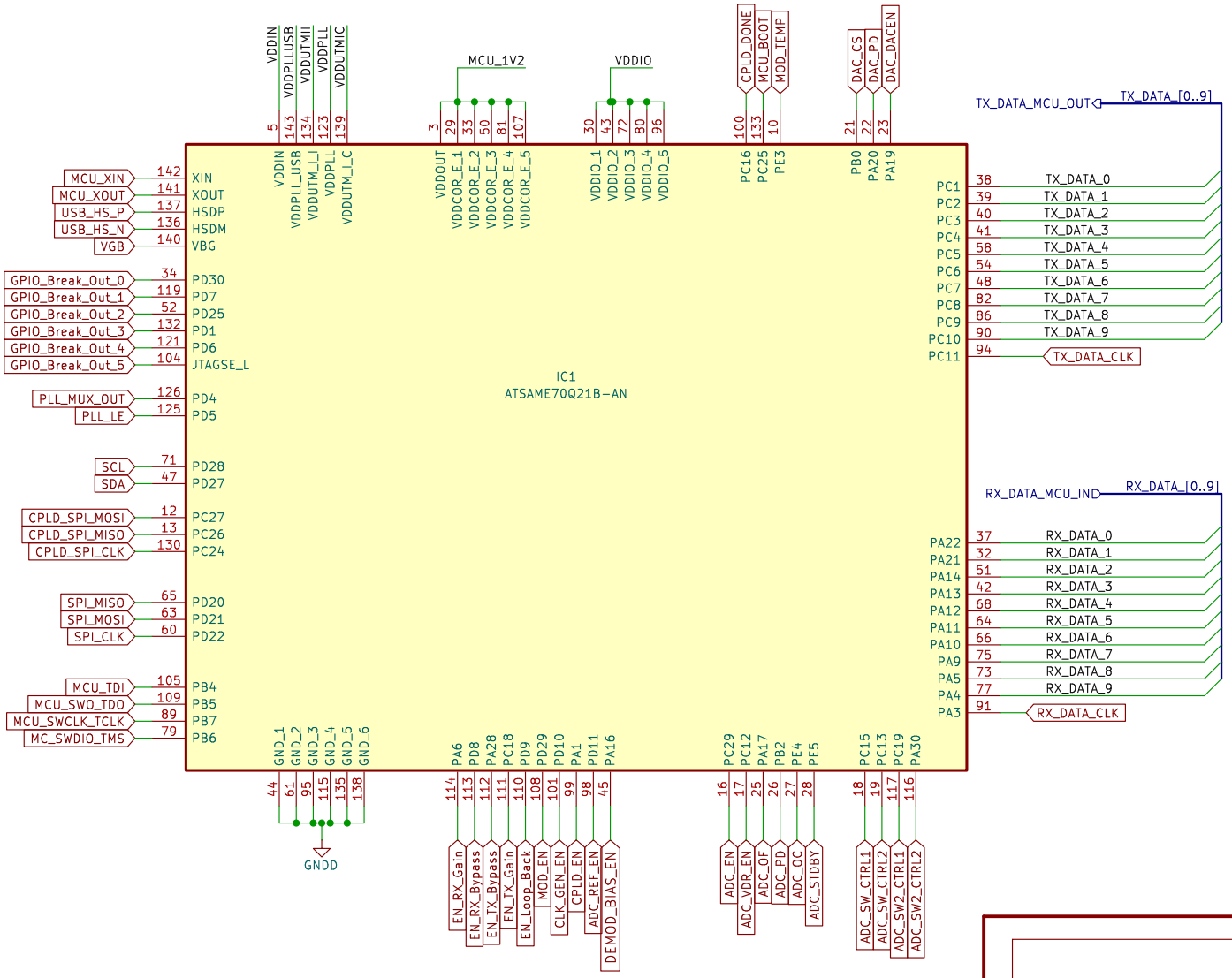
File: Connectors.kicad_sch

Sheet: /
File: SoftwareDefinedRadio.kicad_sch

Title:

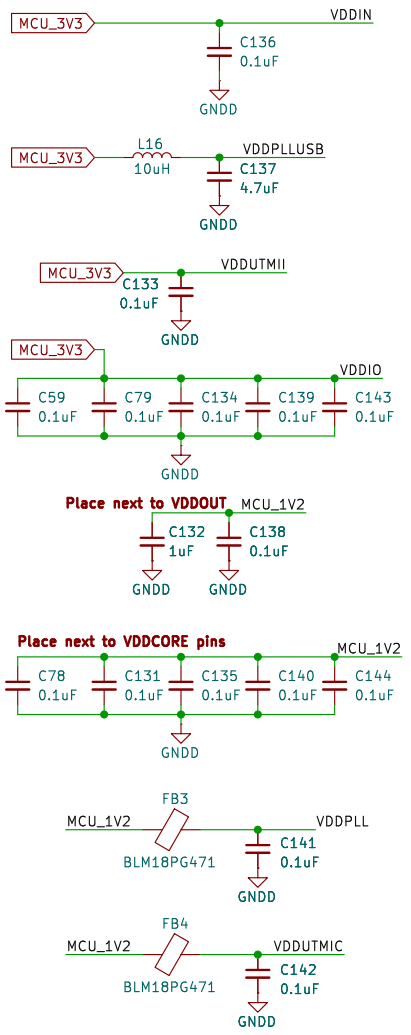
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 1/12

MCU, SAME70



VDDCORE, VDDPPL, and VDDUTMIC are powered through the embedded 1.2 V regulator through VDDOUT

MCU Power Filters

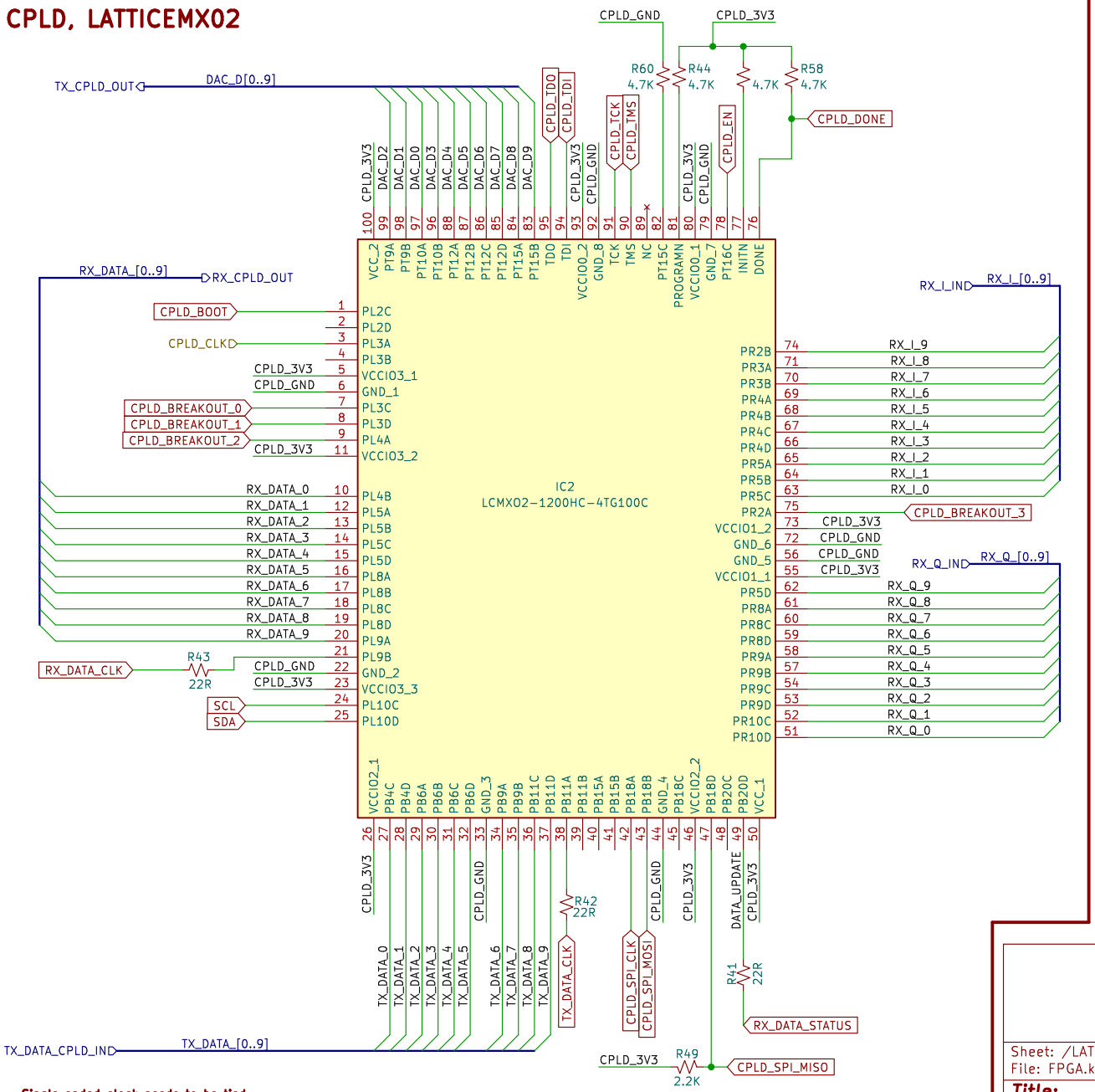


Sheet: /MCU/
File: SoC.kicad_sch

Title:

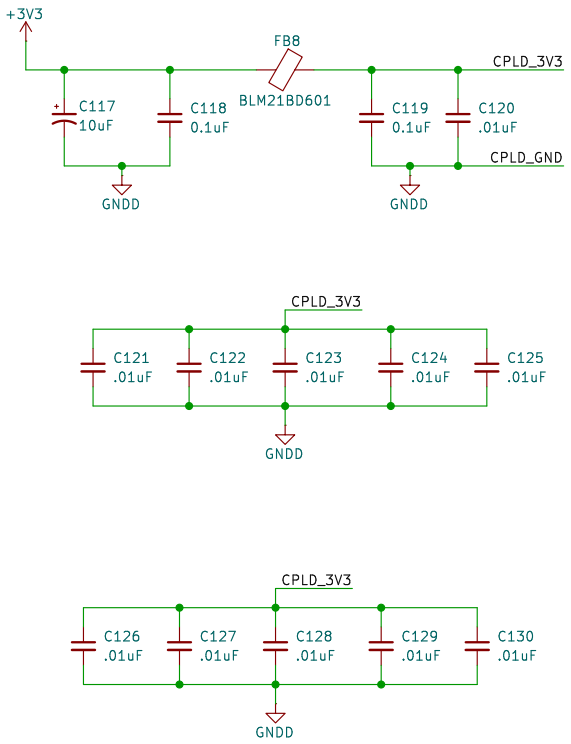
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 2/12

CPLD, LATTICEMX02



Single ended clock needs to be tied to a clock input marked "true" I.E. PL3A

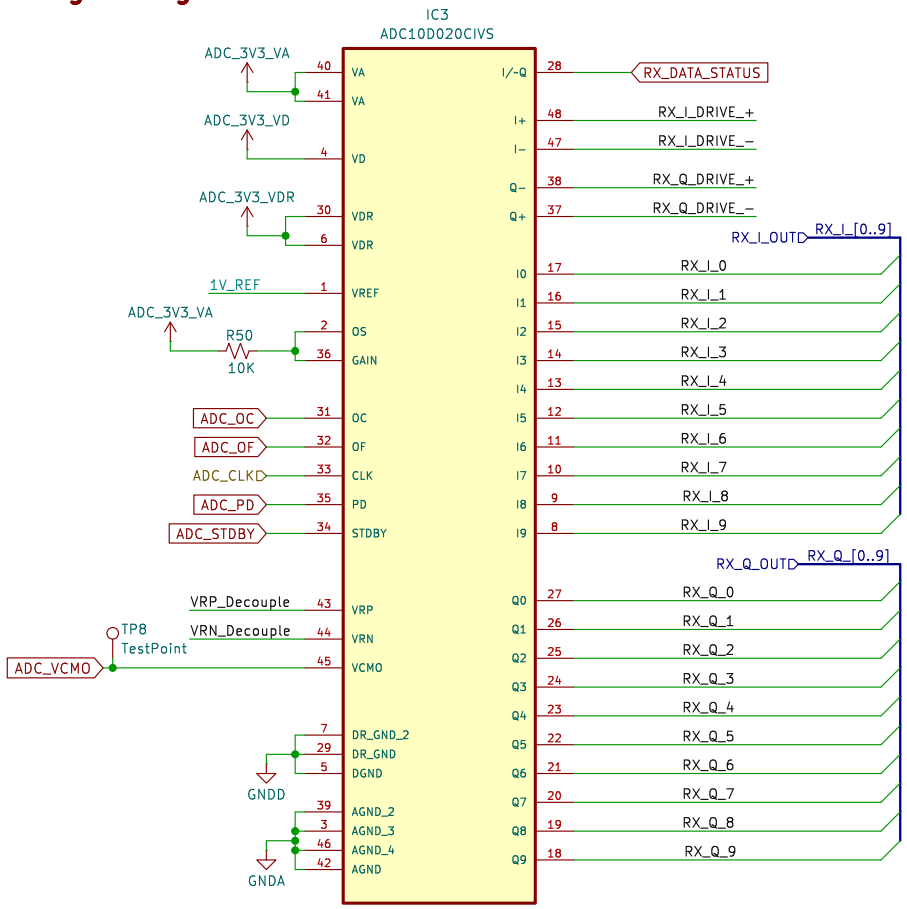
CPLD Power Filter



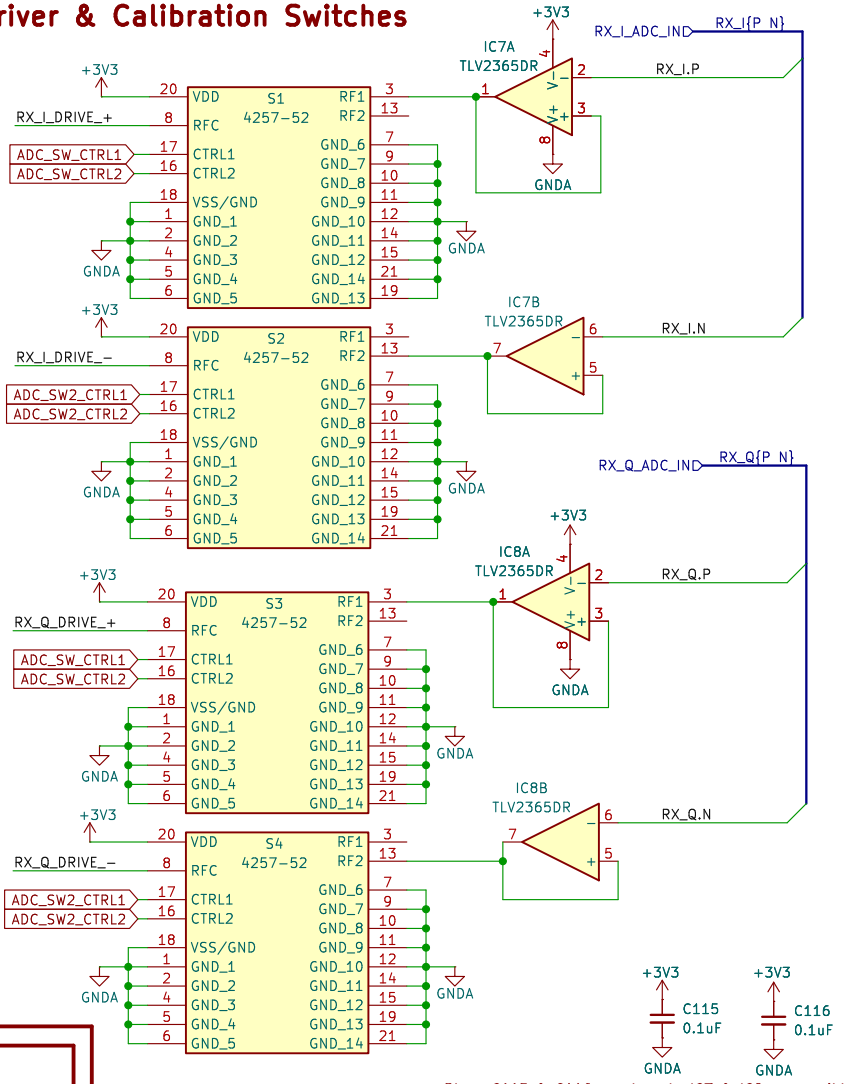
Place C120–C130 as close to each power pin as possible

Sheet: /LATTICEMX02/ File: FPGA.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 3/12

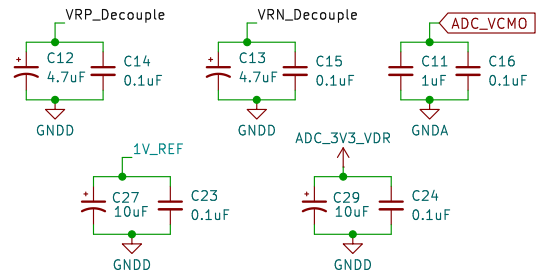
Analog To Digital Converter



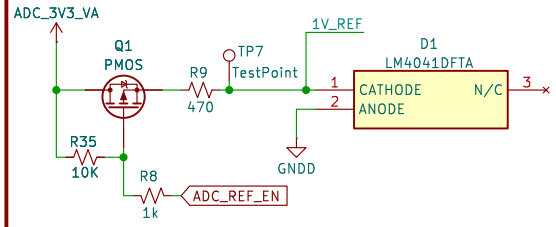
ADC Driver & Calibration Switches



ADC Decoupling Capacitors



1V Refrence

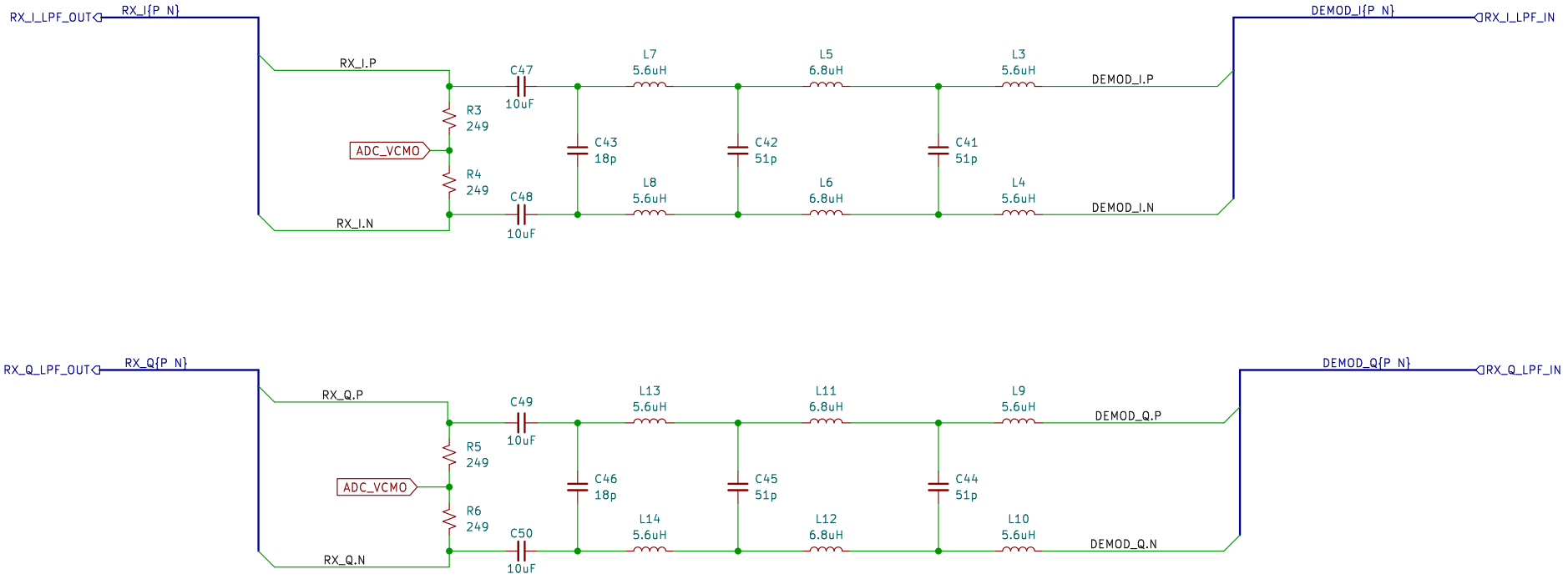


Sheet: /Analog Digtial Converter/
File: ADC.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 4/12

Base Band Low Pass Filter, 6th Order Chebyshev



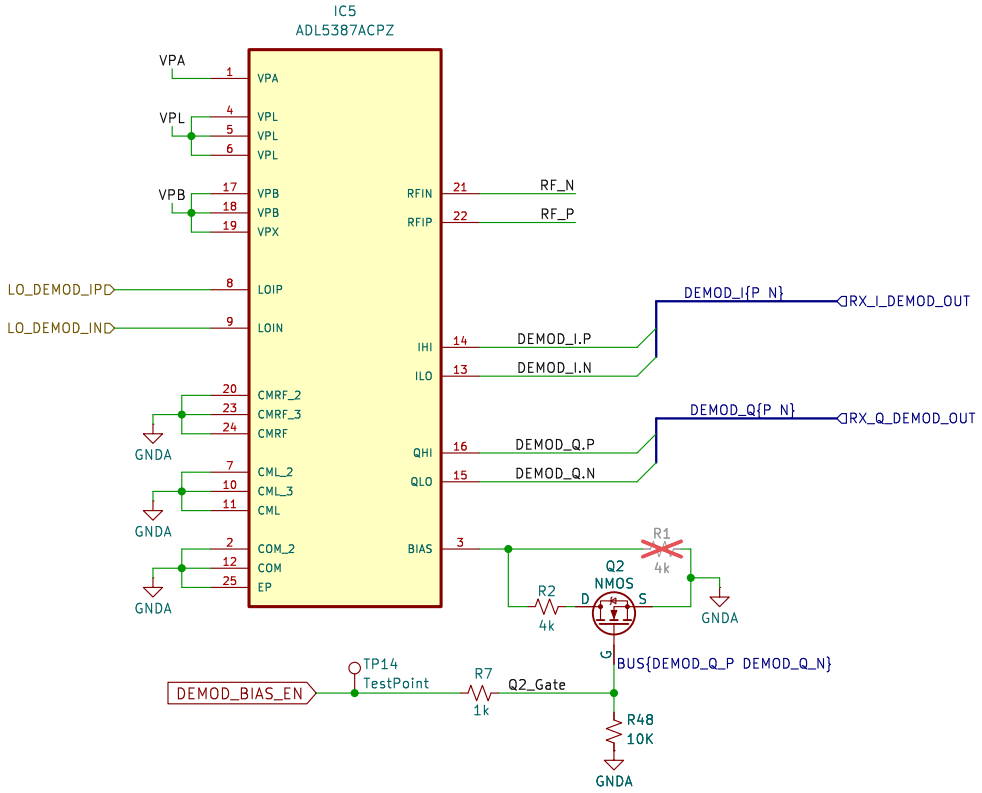
Notes:

The ADL5387 has an output bandwidth of 240 MHz. While the ADC12020 is capable of sampling at a rate of 20 MSPS. In order to prevent signal ailsining a differential low pass filter as been implemented on both the I and Q signals.

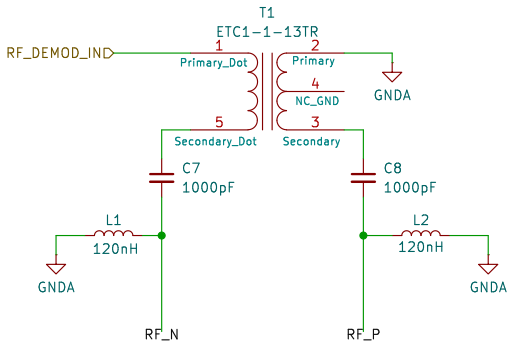
A Chebyshev typology was selected to maximize signal attenuation when all poles combine within the stop band. The filters were tuned to 10 MHz, despite the maximum 20 MHz bandwidth made availble through quadature sampling. This decsion was made based on data rate limitaions with USB 2.0 operating at 480 Mbps.

Sheet: /Base Band Filter/		
File: Base_Band_Filter.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 5/12

Demodulator



BALUN Transformer



The BALUN transformer is used to generate a differential signal from the single ended RF Signal created by the antenna

Reccomened Inductance
For operation above 50 MHz L1 = L2 = 120nH, C9 = C10 = 1000 pF
For operation above to 30 MHz L1 = L2 = 680nH, C9 = C10 = 0.01 µF

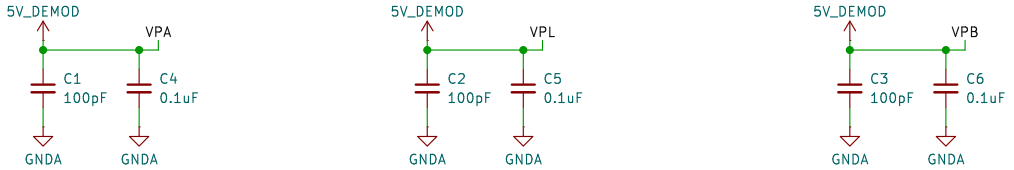
General Notes:

Differential Pairs RX_I_LO & RX_I_HI, RX_Q_LO & RX_Q_HI have a range of 2Vpp with a bias voltage of Vdd − 2.8. There for when Vdd = 5 Vbias = 2.2 V and the differential signals have a range of 1.2 to 3.2 V

When the BIAS pin is open, the mixer runs at maximum current and have the highest dynamic range. The mixer current can be reduce by placing a resistor to ground. By reducing the mixer current, the overall power consumption, noise figure, and IIP3 will also be reduced

Power pins are grouped to nearby pins, place power decoupling circuits as close to the demodulator as possible

RF Power Decoupling

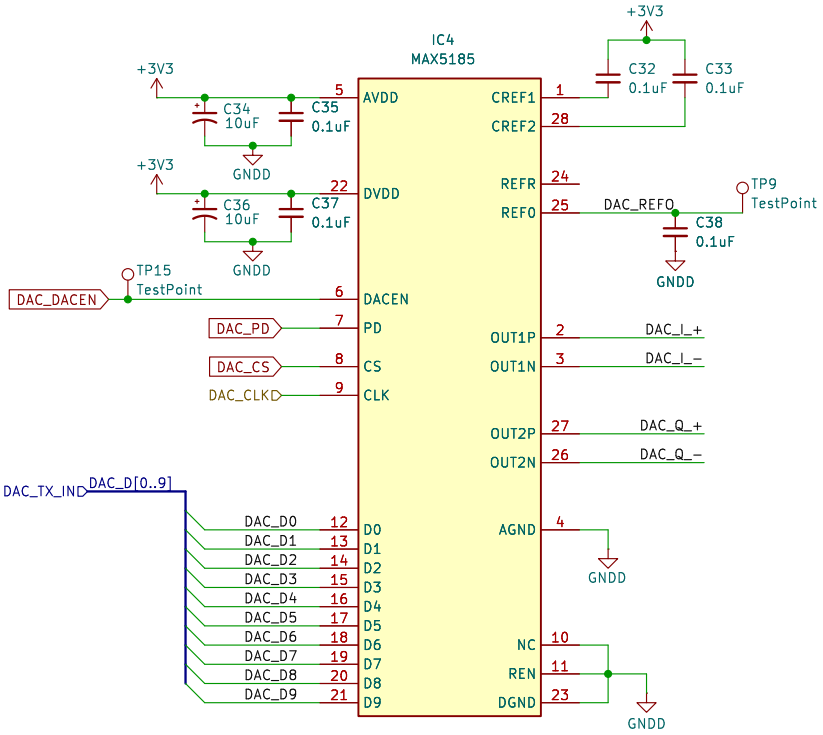


Sheet: /Demodulator/
File: RX.kicad_sch

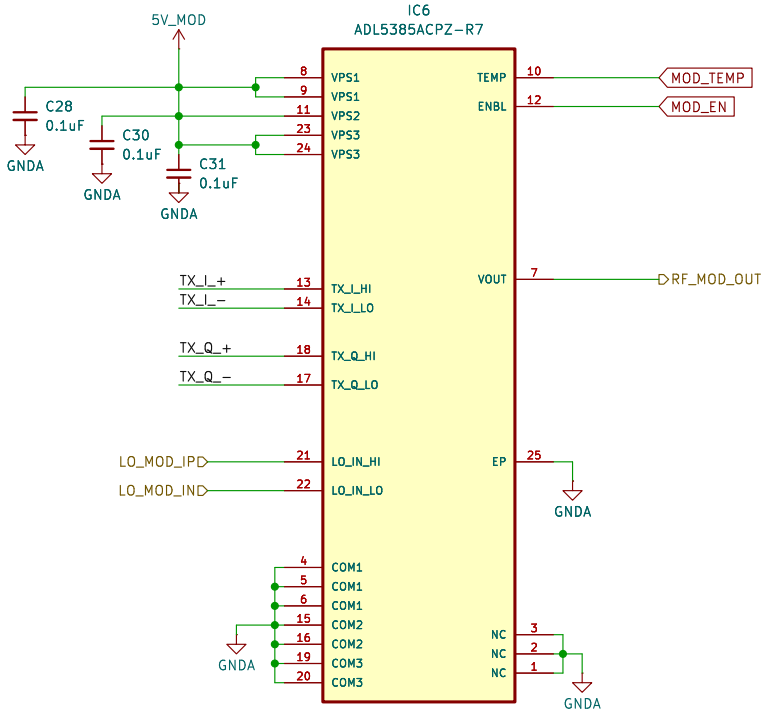
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 6/12

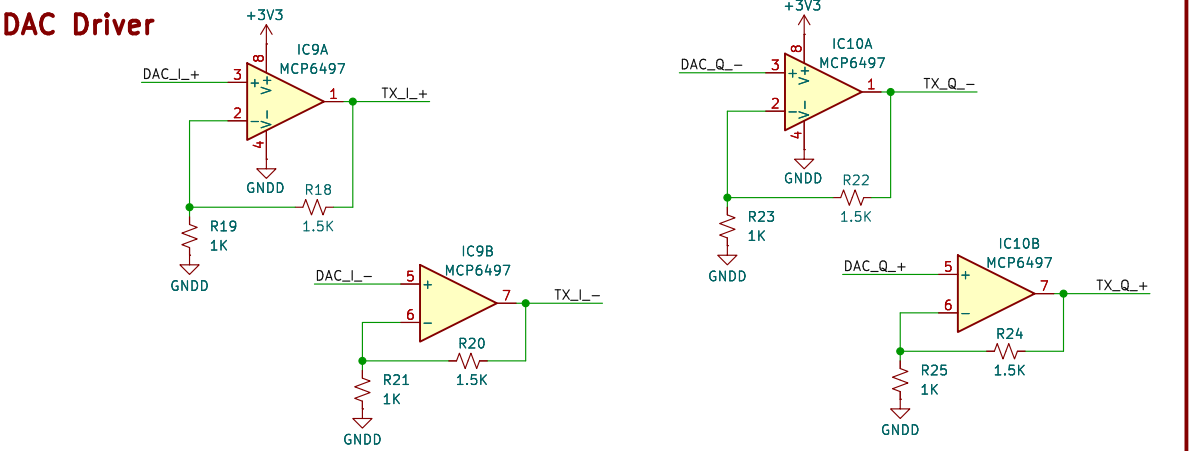
Digital to Analog Converter



Modulator



DAC Driver



Notes

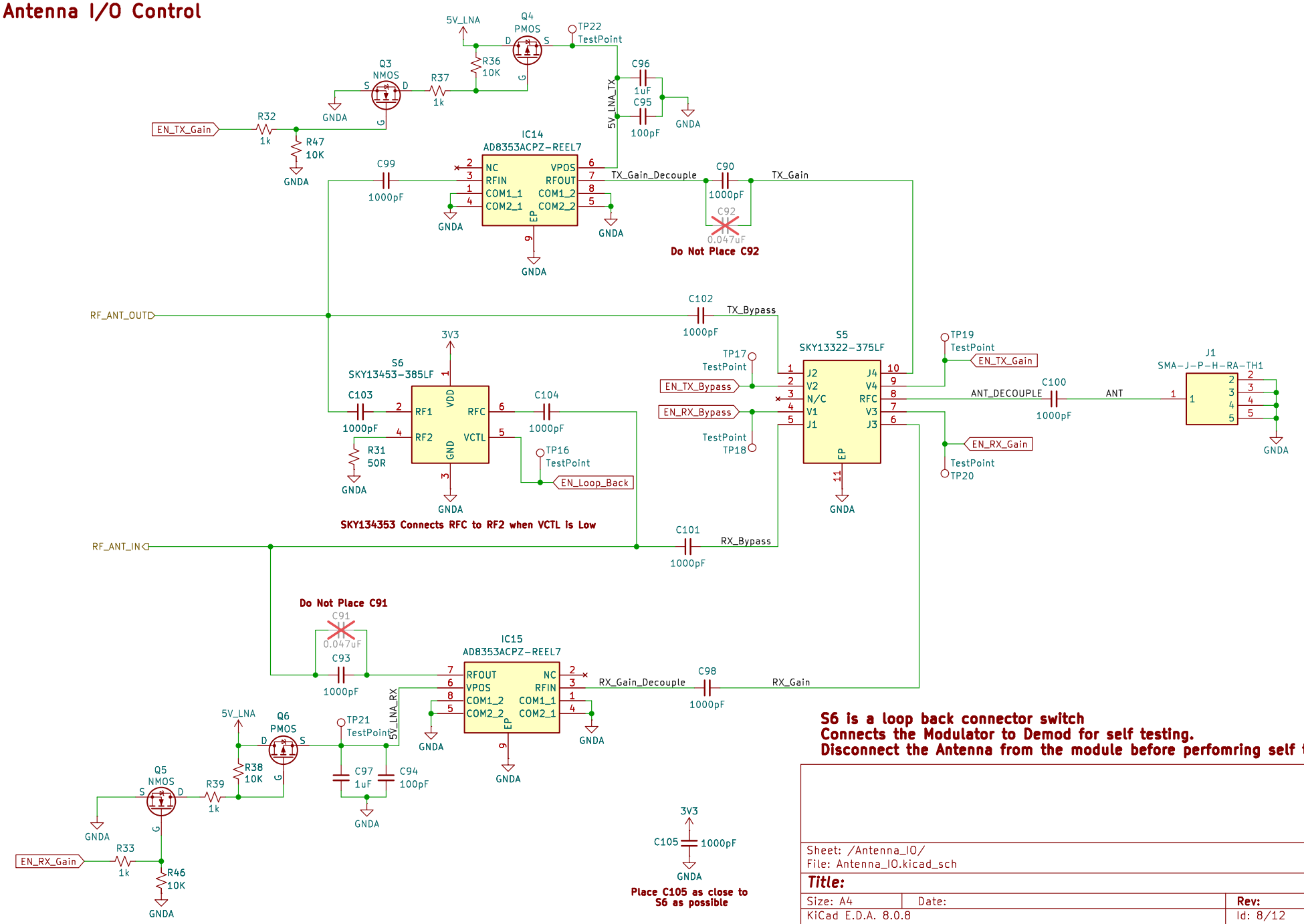
The following data listed is to provide insight into the behavior of the DAC Drivers:
−Full Sacle output of DAC: 400mV
−Full Scale Input: 1V to 1.4V
−DC offset: 1.2V interal DAC Refrence
−Gain: 1.5
−Full Scale Output of DAC Driver: 1.5V to 2.1V

Sheet: /Modulator/
File: DAC.kicad_sch

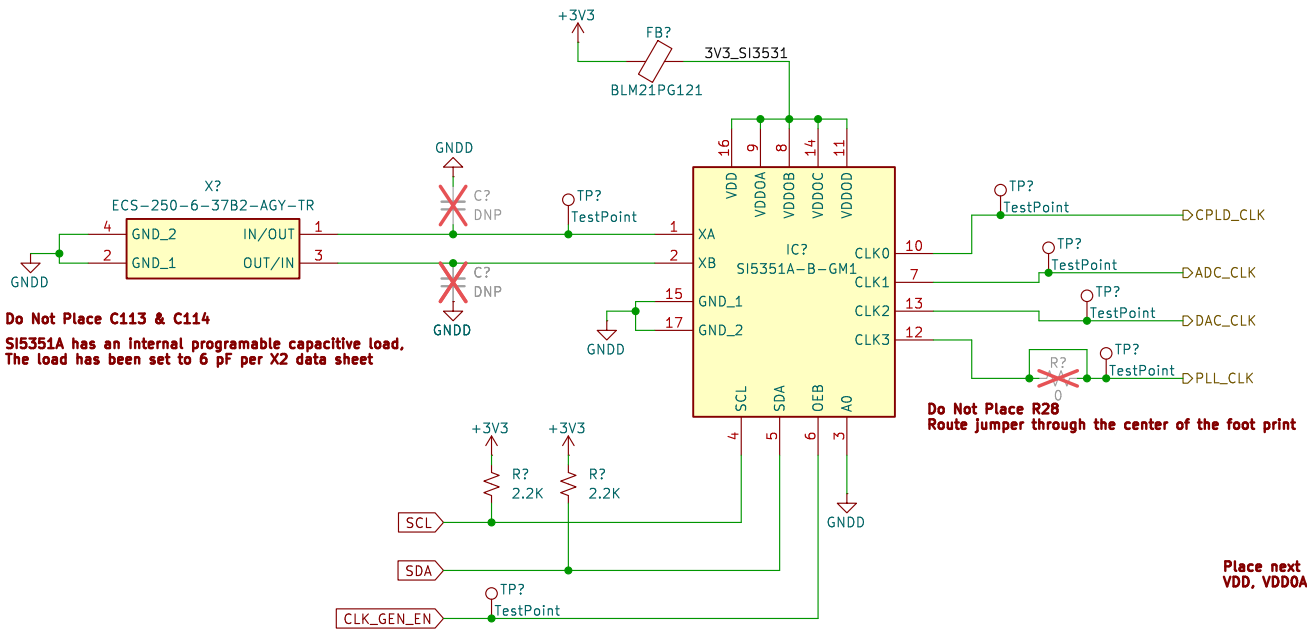
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 7/12

Antenna I/O Control



Clock Generator

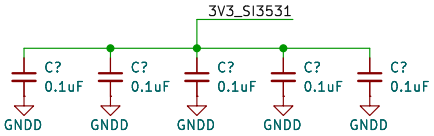


Do Not Place C113 & C114

SI5351A has an internal programable capacitive load, The load has been set to 6 pF per X2 data sheet

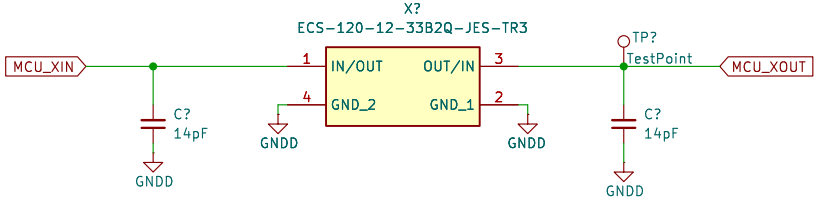
Do Not Place R28
Route jumper through the center of the foot print

Place next to each power supply pin: VDD, VDDOA, VDDOB, VDDOC, and VDDOD



MCU Crystal

Cext = 2 * (Ccrystal − Cstray − Cmcu)
Cext = 2 * (12 − 3 − 5) = 14pF



Place X1 as close to the MCU as possible

Notes:

IC13 Generates the clock signals for the FPGA, ADC, DAC, and the PLL for the Modulator and Demodulator

By default PLL is clocked by IC13, cut the jumper across R28 and populate R27 if you wish use clock the PLL using X2

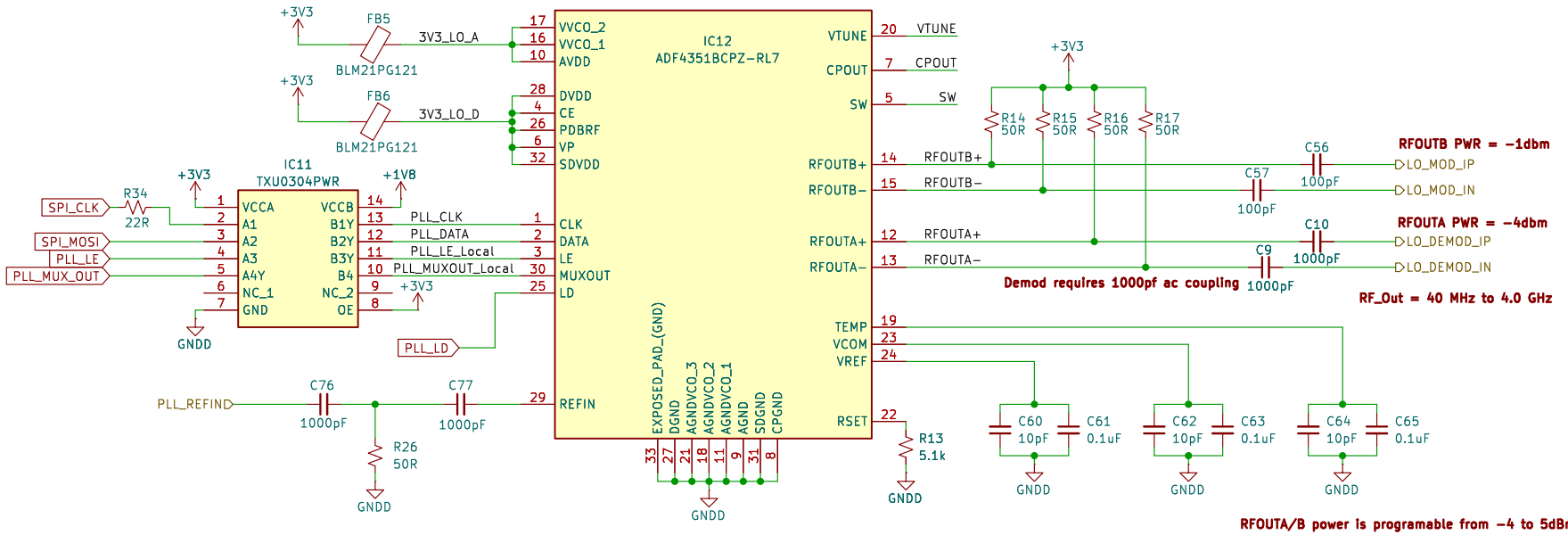
OEB enables the output of IC13. The pin is Active Low, Pull High to disable outputs. All Output are enabled simultaneously.

Sheet: /Clock_Generator/
File: Clock_Generator.kicad_sch

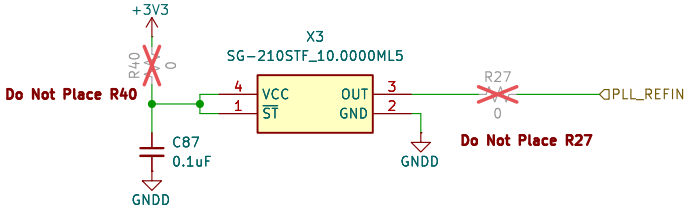
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 9/12

Local Oscillator Clock Generator

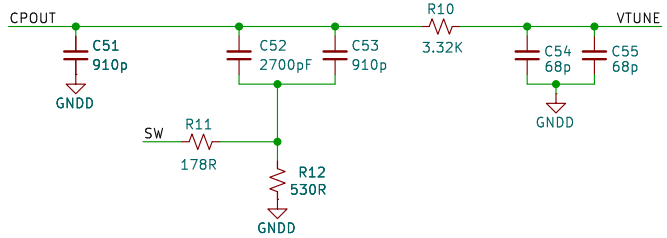


Crystal Oscillator



By default the PLL is clocked by IC13 on the clock_generator sheet #11
Place R27 & R40 only if the jumper across R28 has been cut

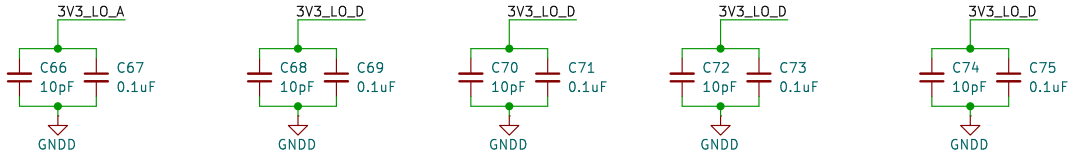
Loop Filter



Fast Lock Topology
Loop Bandwidth: 50 Khz
Phae Margin: 60.0 deg
Time to Lock: 105 uS

PLL Power Decoupling

Place one Pair next to each power supply pin of IC12:
DVDD, AVDD, PDBRF, VP, SDVDD

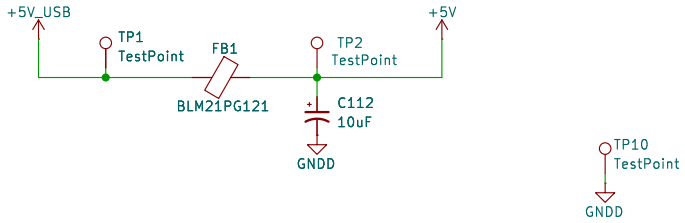


Sheet: /Local_Oscillator/
File: Clock.kicad_sch

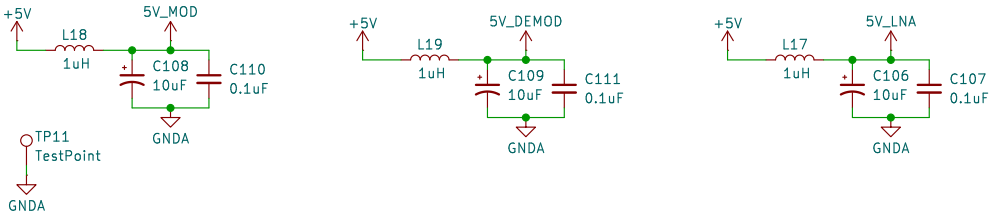
Title:

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.8		Id: 10/12

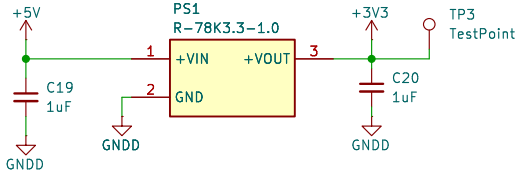
5V Power Input Filter



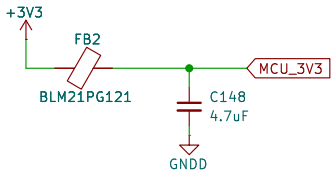
5V Analog Power Filters



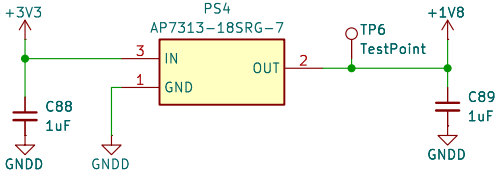
3V3 Power Supply



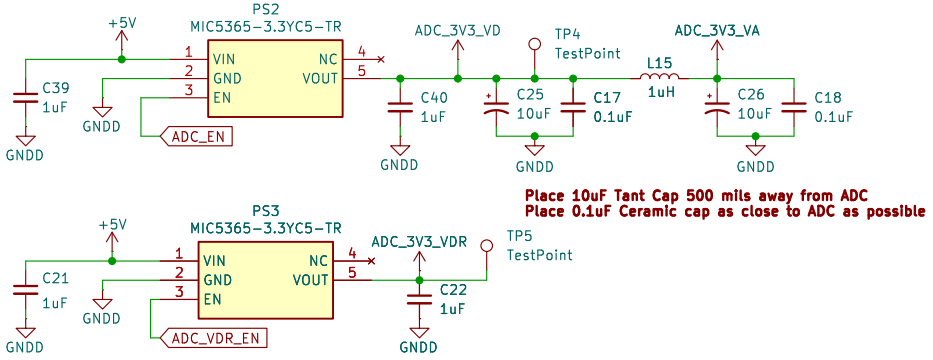
MCU Power Filter



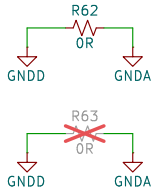
1V8 Power Supply



ADC Power Supplies

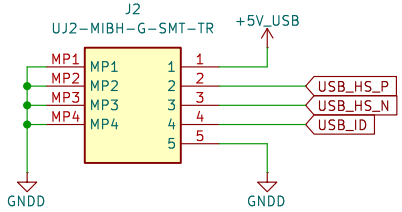


Analog & Digital Ground Jumper

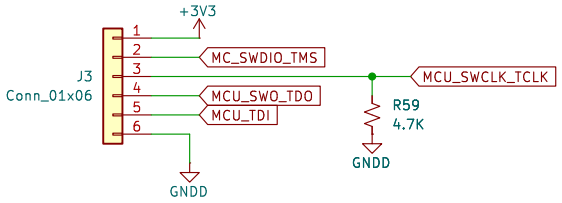


Sheet: /Power/ File: Power.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 11/12

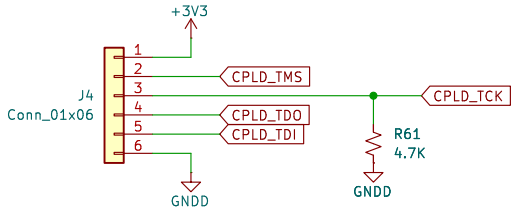
USB Connection



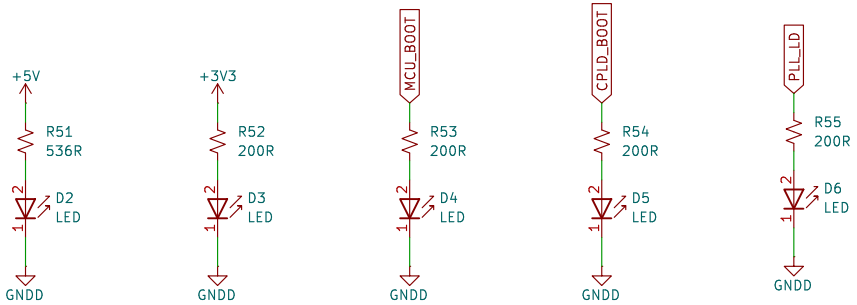
MCU Programing/JTAG



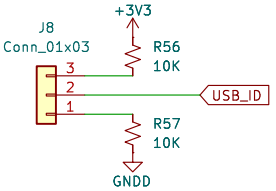
CPLD Programing/JTAG



Debuging LEDs

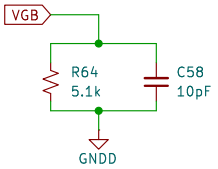


USB OTG Jumpers

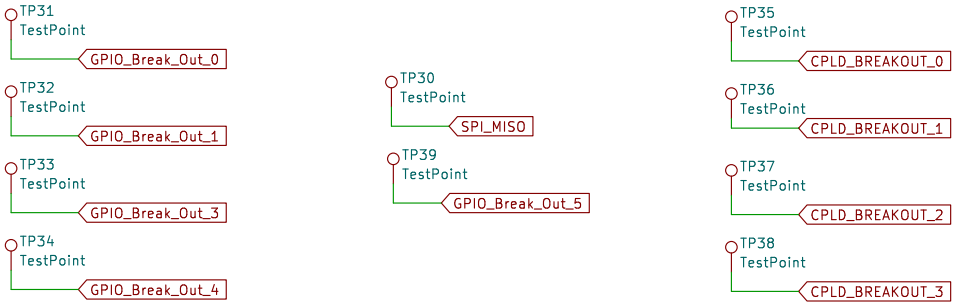


Leave Floating for USB Device/Generic Operation

For USB OTG:
Place Jumper across pins 1 and 2 for USB Device
Place Jumper across pins 2 and 3 for USB Host



Extra Pin Breakout



Sheet: /Connectors/
File: Connectors.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 12/12