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# Oxide-Based Electrolyte-Gated Transistors for Spatiotemporal Information Processing

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**Spiking neural networks (SNNs) sharing large similarity with biological nervous systems are promising to process spatiotemporal information and can provide highly time- and energy-efficient computational paradigms for the Internet-of-Things and edge computing. Nonvolatile electrolyte-gated transistors (EGTs) provide prominent analog switching performance, the most critical feature of synaptic element, and have been recently demonstrated as a promising synaptic device. However, high performance, large-scale EGT arrays, and EGT application for spatiotemporal information processing in an SNN are yet to be demonstrated. Here, an oxide-based EGT employing amorphous $Nb_2O_5$ and $Li_xSiO_2$ is introduced as the channel and electrolyte gate materials, respectively, and integrated into a 32 × 32 EGT array. The engineered EGTs show a quasi-linear update, good endurance ($10^6$) and retention, a high switching speed of 100 ns, ultralow readout conductance (<100 nS), and ultralow areal switching energy density (20 f) $\mu m^{-2}$). The prominent analog switching performance is leveraged for hardware implementation of an SNN with the capability of spatiotemporal information processing, where spike sequences with different timings are able to be efficiently learned and recognized by the EGT array. Finally, this EGT-based spatiotemporal information processing is deployed to detect moving orientation in a tactile sensing system. These results provide an insight into oxide-based EGT devices for energy-efficient neuromorphic computing to support edge application.**

The advent of the Internet-of-Things has led to an exponential growth of information and almost all of them are represented in space and time domain, imposing urgent requirements for time- and energy-efficient way to process these spatiotemporal information at where the data is generated, i.e., edge computing.[1,2] These issues can be addressed by the neuromorphic paradigm of computing inspired by biological sensory nervous systems, which can be integrated with terminal sensors to form intelligent sensory systems.[3–7] Information processing in biological sensory nervous systems involves billions of neurons interconnected through trillions of synapses, constituting immense neural networks.[8] Compared with traditional von Neumann-based computing architecture, neural networks greatly reduce time- and energy consumption by taking the advantage of co-location of logic and memory, hyper-connectivity, robustness, and massively parallel processing.[9] As the third-generation artificial neural network, spiking neural networks (SNNs) are inspired by biological nervous systems. They employ spiking neurons as computational units that process information with timing of spikes.[10] Therefore, SNNs provide the potential for spatiotemporal information processing with high time- and energy-efficiency. The learning and recognition functions aiming at spatiotemporal patterns have been demonstrated in SNN formed by resistive switching synaptic devices.[11] However, this synaptic device suffers from several performance limitations such as the discrete weight update, write variation, and high energy programing related to the filamentary switching mechanism.[12–17] Recently, He et al. use capacitively coupled multi-terminal neurotransistors for spatiotemporal information processing, where the neurotransistors mimic the dendritic discriminability of different spatiotemporal input sequences.[18] To physically emulate neural networks in hardware, large-scale crossbar

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arrays of nonvolatile memories with analog switching feature are highly demanded to implement the synaptic functions.[19,20]

Recently, three-terminal nonvolatile electrolyte-gated transistors (EGTs) have been proposed as synaptic devices to build artificial neural networks (ANNs) for multiply-and-accumulate acceleration in deep learning applications.[21–24] EGTs provide decoupled write/read operations, where the gate terminal is used for channel conductance modulation through driving ions (i.e., $H^+$, $Li^+$) in electrolyte and then injecting them into channel, and source/drain terminals for readout. The decoupling improves not only the precision of synaptic weights and programming energy but also the linearity of weight update, both of which are critical to the computing accuracy of ANN.[14,25] These features render EGT a promising candidate for high-performance neural network computing. However, the application of EGTs remains a challenge owing to constrains in following aspects. First, large-scale EGT arrays are still lacking, since most reported EGTs use organic or 2D material channels and organic or liquid electrolytes,[26–29] which incurs great challenge for fabricating large-area channel/electrolyte thin films and patterning them by conventional lithography techniques. Second, despite the EGTs with inorganic channel/electrolyte materials, such as $W/WO_3$,[30] $LiCoO_2/LiPON$,[31] $ZnO/Ta_2O_5$,[32] show potential for large-area preparation, they usually suffer from the high channel conductance values (10–1000 μS), leading to a higher demand for current capacity, unacceptable voltage drops, and excessive power dissipation on wires as array dimensions increase. For an instance, to reach 1000 × 1000 array size, device currents must drop below 10 nA and the resistance per cell has to approach 100 MΩ.[22] Note that some EGTs with oxide channels and proton doped $SiO_2$ electrolytes show channel conductance modulation in a low value range.[33] However, the retention properties of these devices are usually too short to meet the requirement of neural networks for learning. Third, concerning ion movement during the synaptic weight update, the operation speeds of EGTs (≈μs) are still uncompetitive compared with two-terminal memristive devices (<100 ns).[12,22] Besides, high endurance, long retention time, and low energy consumption are also needed to be improved further to satisfy computational accuracy and energy efficiency demands (see **Table 1**).

In this work, we introduce an oxide-based EGT array (32 × 32) where amorphous niobium pentoxide ($\alpha$-$Nb_2O_5$) is used as the channel and amorphous Li-doped $SiO_2$ ($Li_xSiO_2$) as the gate dielectric. First, $Nb_2O_5$ is thermodynamically stable and CMOS compatible material with wide bandgap ≈3.4 eV and thus ultralow intrinsic conductivity.[34] It has been widely studied in the field of energy devices such as Li-ion batteries[35] and supercapacitors.[36] Compared to most transition metal oxides, the $Nb_2O_5$ surprisingly features the high-rate reversible intercalation of Li-ions despite its insulating character.[37] In fact, analog switching induced by the continuum Li-ion intercalation and extraction has been observed in lithium niobite, showing great potential for two-terminal memristive applications.[38,39] Therefore, $Nb_2O_5$ has been endowed with the promising characteristics to be used as the EGT channel. Second, the high insulating $Li_xSiO_2$ which acts as Li-ion electrolyte in EGTs benefits the reduction of the gate leakage current.[40,41] Although Li volatility is a concern for compatibility with semiconductor fabrication processes, this issue has been actively addressed by new technologies, such as Li diffusion barriers.[42,43] Furthermore, many fabs are developing unconventional/special processing (e.g., Pb, CNTs) to meet the demand of novel electronics.[44] Therefore, we believe that the CMOS compatibility of our device will be further improved in the foreseeable future. With the engineered EGTs, analog channel conductance modulation with quasi-linear update, low variation, high switching speed, high endurance, low readout weight, and low energy consumption have been demonstrated. Owing to these superiorities, the developed EGT array is leveraged as synapses to realize learning and recognition of spatiotemporal spike sequences in a SNN. Further implementation of moving object detection proves the practical function of spatiotemporal information processing in sensing system, illustrating the promising application of the oxide-based EGTs in intelligent sensory system with time- and energy-efficient neuromorphic computing.

The structure of EGT is similar to that of the traditional field effect transistors (FETs). The differences are that the gate dielectric is replaced by electrolytes with mobile ions (e.g., $H^+$, $Li^+$) and the semiconductor channel is replaced by ion-permeable materials (e.g., layered oxides and organics).[23,26,27,31] **Figure 1**a–c illustrates the structure of as-prepared EGT array, individual EGT unit and the electrical measurement setup. The titanium nitride (TiN) thin film with a thickness of 40 nm is deposited by ion-beam sputtering and patterned by standard lithography and etching procedures to serve as source and drain electrodes. 20 nm $\alpha$-$Nb_2O_5$ and 80 nm $Li_xSiO_2$ thin films are prepared as gate electrolyte and channel, respectively, by standard lithography process and magnetron sputtering at room temperature. The detailed process of device fabrication and characterization are described in the Experimental Section and Figures S1 and S2 (Supporting Information). Figure 1d shows the transfer curves ($I_d$–$V_g$) at different sweep rates, where the corresponding $I_d$ is monitored by applying a small dc voltage $V_d$ = 0.1 V between the source and drain electrodes. With the $V_g$ sweeping from –5 to 5 V, a clear counterclockwise loop can be observed with a large high/low current ratio at $V_g$ = 0 V indicating a nonvolatile change of channel conductance ($G$) which is essential for the emulation of synaptic function. Another feature of the transfer curve of our device is the tunable memory window and on/off ratio at 0 V depending on the $V_g$ sweep rate (Figure 1e). This feature indicates that our device can vary its storage status under different measurement conditions. This allows our device to have analog switching capability so that $I_d$ can be modulated by the amplitude, duration, and frequency of $V_g$ pulses, which corresponds to the electric field change around the channel material. The gate leakage current ($I_g$) of the EGT at different sweep rates are simultaneously measured, as shown in Figure 1f. The maximum $I_g$, achieved at 278 mV $s^{-1}$, is less than 300 pA, indicating a good insulating property of the $Li_xSiO_2$ electrolyte. Note that sweep-rate dependent oxidation and reduction peaks appear separately in the positive and negative voltage region. The large $I_d$–$V_g$ hysteresis as well as the concomitant broad peaks in $I_g$–$V_g$ can be interpreted as the $Li^+$ intercalation into (extraction out of) the $\alpha$-$Nb_2O_5$ channel when applying positive (negative) bias to the gate, as schematically shown in inset of Figure 1f. This process can be described by the following reaction[37]

$$x\mathrm{Li}^+ + x\mathrm{e}^- + \mathrm{Nb_2O_5} \leftrightarrow \mathrm{Li}_x\mathrm{Nb_2O_5} \quad (1)$$

**Table 1.** Comparison of the various reported EGTs.

| Channel material | Electrolyte | Nonvolatility | Conductance [$G$][a] | Variation [$\sigma/\Delta G$] | Array size | Programming symmetry | Nonlinearity [$\nu$][b] | Write pulse width | Programing energy | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|
| p-Si | $RbAg_4I_5$/ MEH-PPV | Low | ≈130 nS | – | Single | – | – | 1 ms | ≈10 pJ | [64] |
| $SmNiO_3$ | Ionic liquid | High | – | Low | Single | Asymmetric | Middle | 10 ms | – | [65] |
| CNTs | PEG | Low | ≈45 nS | – | Single | – | – | 1 ms | ≈7.5 pJ | [66] |
| IZO | $SiO_2$ | Low | ≈26 nS | – | Single | – | – | 10 ms | ≈45 pJ | [33] |
| PEDOT:PSS | KCl | Middle | ≈600 µS | – | Single | – | – | ≥1 ms | ≈150 nJ | [67] |
| IZO | Chitosan | Low | ≈85 µS | – | Single | – | – | 10 ms | ≈3.9 pJ | [68] |
| PEO/P3HT | Ion gel | Low | ≈10 nS | – | Single | Asymmetric | Middle | 50 ms | ≈1.23 fJ | [69] |
| IZO | Methylcellulose | Low | ≈2 µS | – | Single | – | – | 40 ms | ≈800 pJ | [70] |
| IZO | Graphene oxide | Low | ≈1.2 µS | – | Single | – | – | 10 ms | ≈120 pJ | [71] |
| IGZO | Aqueous solutions | Low | ≈4 µS | – | Single | – | – | 10 ms | ≈800 pJ | [72] |
| $\alpha$-$MoO_3$ | Ionic liquid | Middle | ≈160 nS | Low | Single | Asymmetric | Middle | 1 ms | ≈9.6 pJ | [27] |
| PEDOT:PSS/PEI | KCl | High | ≈2.75 mS | Low | Single | Asymmetric | Middle | ≥6 ms | ≈10 pJ | [26] |
| $Li_{1-x}CoO_2$ | LiPON | High | ≈290 µS | Low (≈11%) | Single | Asymmetric | Middle | ≈2 s | Projection: ≈10 aJ ($200 \times 200$ nm$^2$) | [31] |
| ZnO | $Ta_2O_5$ | High | ≈50 µS | Middle | Single | Asymmetric | High | 10 ms | ≈35 pJ | [32] |
| $MoS_2$ | PVA proton conductor | Low | ≈6 µS | – | Single | – | – | 10 ms | 23.6 pJ | [73] |
| $\alpha$-$MoO_3$ | $LiClO_4$/PEO | High | 75 nS | Low (≈6.5%) | Single | Asymmetric | Middle | 1 ms | ≈1.8 pJ | [23] |
| $WO_3$ | LiPON | High | ≈3 nS | Low | Single | Near symmetry | Low (0.35/0.27) | ≥5 ns | Projection: ≈1 fJ ($100 \times 100$ nm$^2$) | [21] |
| $WSe_2$ | $LiClO_4$/PEO | Middle | ≈20 µS | Low | Single | Asymmetric | Middle | 50 ms | ≈30 fJ | [28] |
| $WO_3$ | Ionic liquid | Low | ≈30 nS | Middle | Single | Asymmetric | High | 210 ms | ≈36 pJ | [75] |
| Graphene | $LiClO_4$/PEO | High | ≈1.1 mS | Low | Single | Asymmetric | Middle | 10 ms | Projection: ≈4 aJ ($30 \times 30$ nm$^2$) | [74] |
| ITO | Chitosan | Middle | ≈110 µS | Low | Single | Asymmetric | Middle | 10 ms | ≈7.5 nJ | [76] |
| IGZO | Chitosan | Low | ≈2 µS | – | Single | – | – | 25 ms | ≈1 nJ | [18] |
| PEDOT:PSS | Nafion | High | ≈100 nS | Low (≈10%) | $3 \times 3$ | Near symmetry | Low | ≥1 µs | ≈50 fJ | [22] |
| $WO_3$ | – | High | ≈16 µS | Low | $2 \times 2$ | Near symmetry | Low | ≥10 ns | Projection: ≈1 fJ ($100 \times 100$ nm$^2$) | [24] |
| $Li_xTiO_2$ | $LiClO_4$/PEO | High | ≈75 µS | Low | Single | Asymmetric | Middle | 10 ms | Projection: ≈30 aJ ($100 \times 100$ nm$^2$) | [78] |
| $MoS_2$ | $Li^+$ from n-butyl lithium solution | High | ≈500 nS | Middle | Single | Asymmetric | Middle | 1 ms | ≈45 pJ | [29] |
| W | $WO_{3-x}$ | Middle | ≈50 µS | – | Single | Asymmetric | Middle (1.3/−0.3) | ≈10 ms | ≈10 nJ | [30] |
| $SrCoO_x$ | Ionic liquid | High | ≈120 nS | Low | Single | Asymmetric | High | 5 s | ≈5 nJ | [77] |
| InAs nanowire | Ionic liquid | – | ≈60 µS | – | Single | – | – | – | – | [79] |
| $LiCoO_2$ | $Li_3PO_xSe_x$ | Middle | ≈40 nS | Low | Single | Asymmetric | Middle (1.33/−0.34) | 1 s | ≈5 nJ | [80] |
| $In_2O_3$ | Li doped in $Al_2O_3$ | Low | ≈50 µS | – | Single | – | – | 30 ms | ≈6.3 nJ | [83] |
| $WO_{2.7}$ | $Li_3PO_4$ | High | ≈3.5 µS | Low | Single | Asymmetric | Low (0.6/−0.58) | 1 s | ≈35 nJ | [82] |
| IZO | $C_3N_4$/PVP | Low | ≈400 nS | – | Single | – | – | 20 ms | ≈0.32 nJ | [84] |
| PQT-12: PEO electrospun fiber | Ionic liquid | Low | ≈6 µS | – | Single | – | – | 100 ms | ≈3.9 fJ | [85] |

**Table 1.** Continued.

| Channel material | Electrolyte | Nonvolatility | Conductance [$G$][a)] | Variation [$\sigma/\Delta G$] | Array size | Programming symmetry | Nonlinearity [$\nu$][b)] | Write pulse width | Programing energy | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|
| ITO | PSG | Low | ≈2.8 µS | – | Single | Asymmetric | Middle | 10 ms | ≈1.4 nJ | [86] |
| $VO_2$ | Ionic liquid | High | ≈10 µS | Low | Single | Asymmetric | Middle | 200 ms | ≈2.2 pJ | [81] |
| p(g2T-TT) | Ion gel | High | ≈10 µS | Low (≈10%) | Single | Near symmetry | Low | 20 ns | ≈80 fJ | [87] |
| $\alpha$-$Nb_2O_5$ | $Li_xSiO_2$ | High | ≈100 nS | Low (3.9%) | 32 × 32 | Asymmetric | Middle (0.68/1.65) | 100 ns | Projection: ≈200 aJ (100 × 100 $nm^2$) | This work |

[a)]The devices display both a low and a high conductance state, where the high conductance state is selected; [b)]The method of nonlinearity calculation is different in each work. Refs. [30], [80] and [82] use the same calculation method, while ref. [21] and this work use the same calculation method.

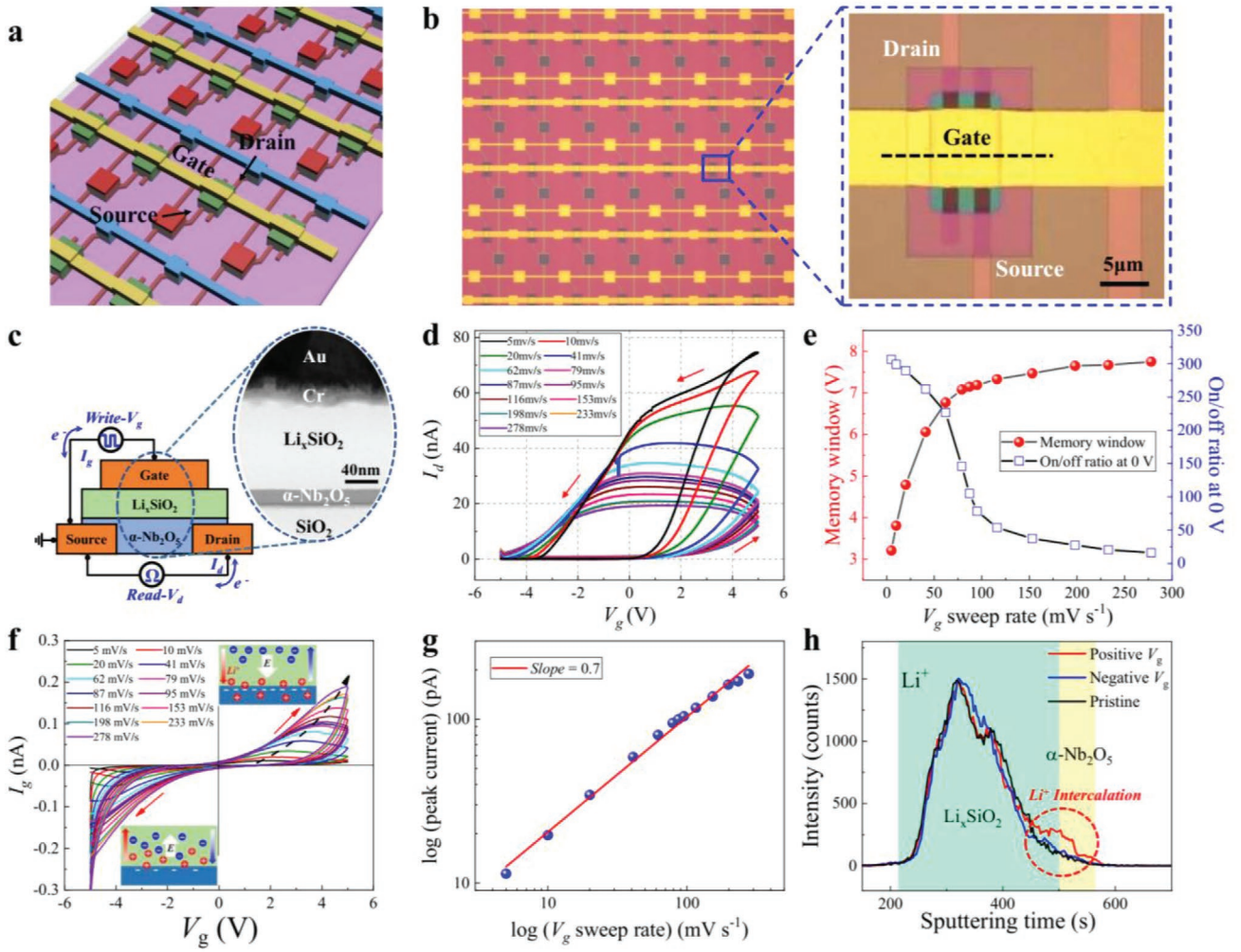


**Figure 1.** Structure and switching mechanism of EGT. a) Schematics of a 32 × 32 EGT array, where the drain, gate, and source lines are marked in the picture. b) Photography of the as-prepared EGT array (left) and the magnification of an individual EGT unit (right). The channel length and width of each EGT unit are 2 and 50 µm, respectively. c) Schematic of electrical measurement setup of EGT and the TEM image of cross section along the black dash line in (b). 80 nm $Li_xSiO_2$ and 20 nm $\alpha$-$Nb_2O_5$ were prepared as gate electrolyte and channel, respectively. d) The transfer curves ($I_d$–$V_g$) at different sweep rates, where a large counterclockwise hysteresis appeared, indicating nonvolatile switching of channel conductance. e) Memory window (red) and on/off ratio at 0 V (blue) as a function of the $V_g$ sweep rate. f) The gate leakage current curves ($I_g$–$V_g$) at different sweep rates, where oxidation and reduction peaks can be seen obviously under positive and negative $V_g$, respectively. Insets: schematics of the $Li^+$ intercalation into (extraction out of) the channel under positive (negative) $V_g$. g) Kinetics analysis of $\alpha$-$Nb_2O_5$-based EGT. The peak current versus $V_g$ sweep rate are logarithmically plotted and the fitted slope is 0.7. h) Depth profiles of $Li^+$ from the $Li_xSiO_2$ electrolyte to the $\alpha$-$Nb_2O_5$ channel under pristine, positive-gated, and negative-gated states, demonstrating the intercalation of $Li^+$ into the $\alpha$-$Nb_2O_5$ channel layer.

This behavior is electrochemical doping, where the valence of $Nb^{5+}$ is electrochemically reduced to $Nb^{4+}$ with the $Li^+$ intercalation into the channel under positive gate bias, which introduces external electron charges in the channel and raises the channel conductance. Under the negative gate bias, the $Li^+$ ions are extracted out of the channel leading to the electrochemical oxidation of the $Nb^{4+}$ to $Nb^{5+}$ and decrease of the channel conductance.[45] The amorphous structure of $Li_xSiO_2$ and $\alpha$-$Nb_2O_5$ facilitate $Li^+$ intercalation into (or extraction out of) the channel. The electrochemical reduction and oxidation processes occurring at the $Li_xSiO_2/\alpha$-$Nb_2O_5$ interface can be associated with the two broad peaks in the positive and negative region of the gate leakage current curve, respectively. To determine the kinetics in our device, we analyze the relationship between the observed current and sweep rate in Figure 1f according to the following law[37]

$$i = av^b \tag{2}$$

where $i$ is the current at a specific potential, $v$ is the $V_g$ sweep rate, $a$ and $b$ are adjustable parameters, and $b$ can be determined as the slope of $\log(i)$ versus $\log(v)$. Kinetic limitations can be estimated from $b$ value, whereas $b = 1$ indicates that the current is surface-controlled, $b = 0.5$ would indicate that the current is controlled by semi-infinite linear diffusion. The peak current of $I_g$ under positive gate bias versus $V_g$ sweep rate is logarithmically plotted in Figure 1g and the $b$ is ≈0.7, which indicates our device may be controlled by a mixed mechanism (a combination of surface-controlled kinetic and semi-infinite linear diffusion kinetic). To further verify the $Li^+$ doping process, secondary-ion mass spectroscopy (SIMS) was used to characterize the ion distribution in EGT under pristine, positive-gated, and negative-gated states (see the Experimental Section for detailed process). As shown in Figure 1h, the $Li^+$ depth profile indicates clearly the $Li^+$ intercalation into (extraction out of) the $\alpha$-$Nb_2O_5$ layer under positive (negative) gate bias. This mechanism we proposed here is also consistent with previously investigations in lithium-niobite-based analog memristor.[38,39]

Biological synapses are functional links connecting a pair of neurons. The key feature of synapses is tunability of synaptic weight, which is, connection strength between two neurons, underpinning the learning and memory abilities of the neural network.[46,47] Herein, the synaptic tunability can be emulated by the Li-based EGT, in which the synaptic weight can be expressed by the EGT channel conductance to be tuned by the gate voltage. **Figure 2**a shows the analog switching of the EGT under gate voltage pulses. By alternatively applying 32 identical positive and negative gate pulses (+3.6/−3.4 V,

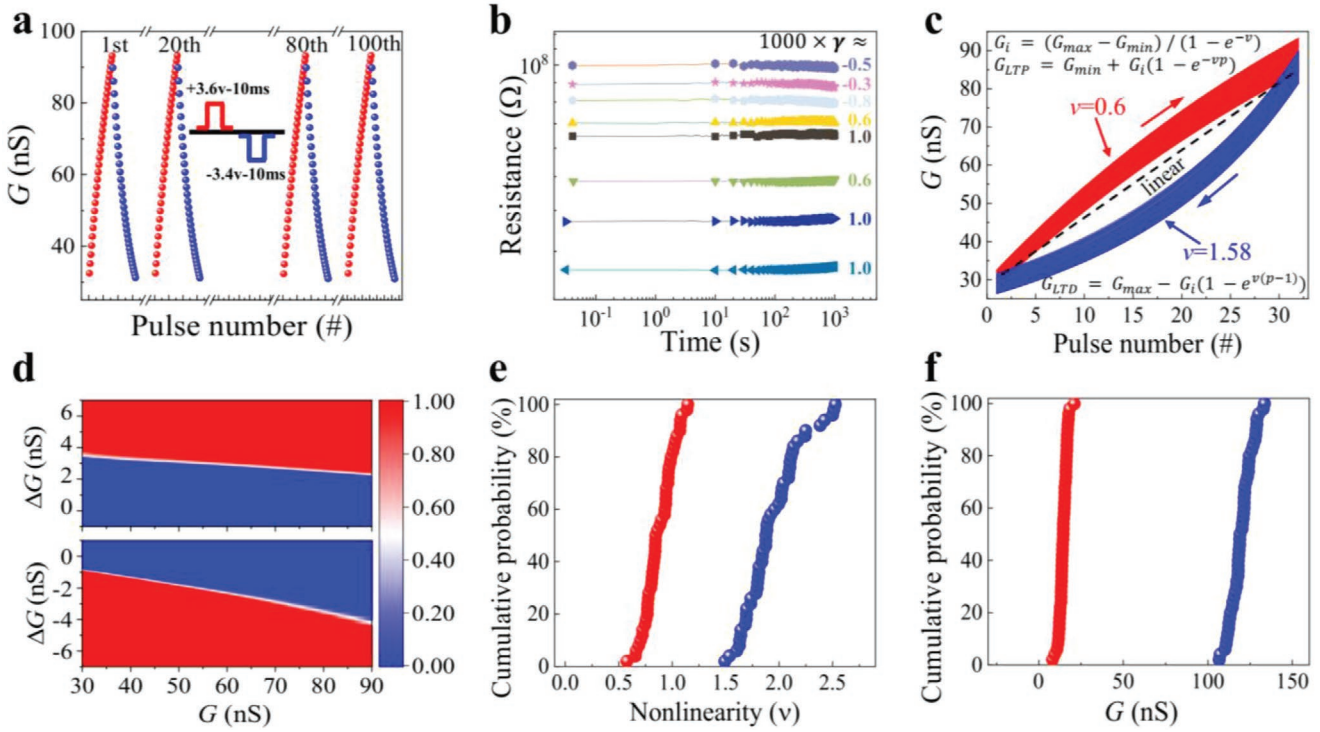


**Figure 2.** Analog switching performance. a) 100 cycles of channel conductance switching with 32 discrete states induced by $V_g$ pulses with +3.6/−3.4 V and 10 ms width. Each conductance state is readout for 5 s after the $V_g$ pulse. b) Retention performances of the device. Eight conductance states randomly distributing in the switching range are selected for retention measurement. The measurement was performed at room temperature. The change of resistance obeys the power law, $R(t) = R_0(t/t_0)^\gamma$, where $R_0$ is the initial resistance at $t_0$, and $\gamma$ is the fitted resistance drift coefficient. c) Nonlinearity analysis on the cycle-to-cycle switching characteristics yields small mean value of nonlinearity factors of $v = 0.6$ and $v = 1.58$ for channel conductance increasing and decreasing, respectively. d) CDF maps during channel conductance increasing (top) and decreasing (bottom). The average variation ($\sigma/\Delta G$) is as low as 3.9%, where $\sigma$ is the standard deviation of the conductance update. e) Device-to-device distribution of nonlinearity during channel conductance increasing (red) and decreasing (blue). f) Device-to-device distribution of the lowest conductance states (red) and the highest conductance states (blue). The statistical analysis in (e,f) is from 64 conductance states of 50 device, and the conductance states are extracted separately.

10 ms), 100 cycles of bidirectional analog switching through 32 discrete conductance states are sequentially programmed. The 32-level analog switching of EGT shows no significant degradation even after $10^6$ binary write pulse operation (see Figure S3 in the Supporting Information), indicating a competent endurance for neural network application, especially for learning process. At present, operation voltage lower than 1 V is expected for energy efficiency gains over CMOS.[31] The relatively large switching voltage of our devices can be mainly attributed to the large open circuit potential (OCP) resulting from difference in chemical potential between the channel ($\alpha$-$Nb_2O_5$) and the gate materials (Cr/Au). The large OCP impairs the control capability of gate, which is also common in other oxide-based electrochemical synaptic devices.[23,24,31] From the perspective of equivalent circuit, the capacitive behavior will occur at channel/electrolyte interface ($C_1$) and electrolyte/gate interface ($C_2$) when gating the EGT. When the system reaches equilibrium, the gate voltage drops mainly on these two capacitances. Since $C_1$ and $C_2$ are connected in series, in order to obtain stronger gate control capability, one of effective ways is to enlarge the $C_2$ to ensure more gate voltage drop on the channel. Therefore, conductive materials, which can react with ions or are permeable to ions, can better serve the gate to reduce OCP and then the gate voltage. In addition, reducing the conductance range ($G_{max}/G_{min}$), device encapsulation, downscaling of device size and the use of nonlinear selector may also help to reduce the gate voltage.[48,49] Retention is another important device criterion, especially for inference process of neural network. Here, eight conductance states randomly distributing in the switching range are selected for retention characterization. The retention measurements are performed by first programing the EGT to a particular conductance state followed by cutting off the gate circuit and applied a constant source-drain bias of $V_{ds}$ = 0.1 V to monitor the change in channel conductance. As shown in Figure 2b, each conductance state shows negligible deviation for 1000 s. The good retention characteristic of EGT is attributed to the "ion frozen" effect where no external electron is accessed to the electrolyte due to the gate cut-off.[50] Moreover, the reading fluctuation of eight conductance states within 1000 s is also examined (see Figure S4 in the Supporting Information). Each conductance state has a narrow distribution, ensuring discrete conductance states are distinguishable.

The continuous increase and decrease of channel conductance can emulate the long-term potentiation (LTP) and long-term depression (LTD), respectively, which are important synaptic plasticity behaviors.[8] For neuromorphic computing, a linear LTP and LTD processes with low variation are essential to improve the learning accuracy of neural network.[14,25] To analyze the linearity and variation of the EGT, the switching process in Figure 2a is condensed together and replotted in Figure 2c. The mean value of the nonlinearity factors ($\nu$) are calculated to be 0.6 and 1.58 for LTP and LTD, respectively, according to the fitting function (see Equations S7–S9, Supporting Information), indicating a quasi-linear analog switching of EGT. The variation is evaluated by the cumulative distribution function (CDF) maps, as shown in Figure 2d. Although the maximum on/off ratio is only ≈3, smaller than that of memristors (>10), the average variation of $\sigma/\Delta G$ is as low as 3.9%, where $\sigma$ is the standard deviation of the conductance update and $\Delta G$ is the mean of conductance change upon a given pulse. The quasi-linearity and low variation in weight update can be attributed to the electrochemical doping mechanism, which is more controllable than the stochastic filament formation and rupture process in two-terminal memristors.[13,16]

For efficient neural network computing, large-scale EGT crossbar array is highly demanded. To meet this need, we fabricate a $32 \times 32$ EGT array and statistically analyze the device-to-device uniformity. Our device shows the non-linear gate characteristic (see Figure S5 in the Supporting Information), which makes it possible to parallel programming operation in part of the crossbar array. For example, the parallel programming of a $1 \times 3$ EGT sub-array has been demonstrated (see Figure S6 in the Supporting Information), which was also used for the SNN implementation in our work. However, it should be noted that access devices are still needed in future to avoid discharging and crosstalk in fully operating the $32 \times 32$ EGT array.

The following statistical data is extracted separately. The detailed measurement method is described in the Experimental Section. Herein, nonlinearity and the maximum/minimum conductance distributions are analyzed, where each EGT was programed through 64 discrete conductance states in the statistical analysis. The device-to-device nonlinearity distributions of 50 EGT devices in LTP (red) and LTD (blue) are shown in Figure 2e. The nonlinearity of LTP has a narrow distribution from 0.57 to 1.14, lower than that of LTD distributed from 1.49 to 2.52. The minimum conductance states show a narrow device-to-device distributions around 10 nS, while the high conductance states are around 120 nS, resulting in a mean on/off ratio of ≈10, as shown in Figure 2f. The high device-to-device uniformity provide a promising platform for implementation of SNN. Thanks to the high insulating $\alpha$-$Nb_2O_5$ channel, the maximum conductance value is ≈135 nS, far lower than that of two-terminal resistive switching devices (typically > 1000 nS).[19] The low channel conductance is critical to crossbar arrays with a size beyond 1000×1000, where the loading current of each elements must lower than 10 nA (corresponding to 100 nS at 0.1 V) for parallel write/read operation when the wires are scaled down to 10 nm half pitch.[22] Moreover, the wire resistance impact to crossbar arrays can be mitigated since less voltage drops on the wire.

Modulation speed is another critical property of the synaptic devices, especially for the online training of neural network.[51] To confirm the high speed operation of our EGT devices, a high-speed measurement circuit consisting of one PMOS transistor (P-FET) and one NMOS transistor (N-FET) is adopted (see Figure S7, Supporting Information).[21] Here, the P-FET (N-FET) serves as a current source to supply current pulses by turning on the FETs exclusively to potentiate (depress) EGTs. With the aid of PMOS and NMOS, the involved charges for Li-ion intercalation/extraction can be controlled precisely, and then a trade-off between the switching time and switching ratio can be achieved. **Figure 3**a shows the results of reproducible programming through 64 discrete channel conductance state with pulse width from 10 ns to 1 ms, demonstrating the high-speed switching capability of our EGTs. The dynamic channel conductance change ($\Delta G$) has an approximate linear relationship with pulse width in log–log plot (see Figure 3b) and the $\Delta G$ reduces to ≈0.02 nS with decreasing pulse width to 10 ns, which can be attributed to the reduced Li-ion intercalation into (or extraction out of) the channel due to shortening the

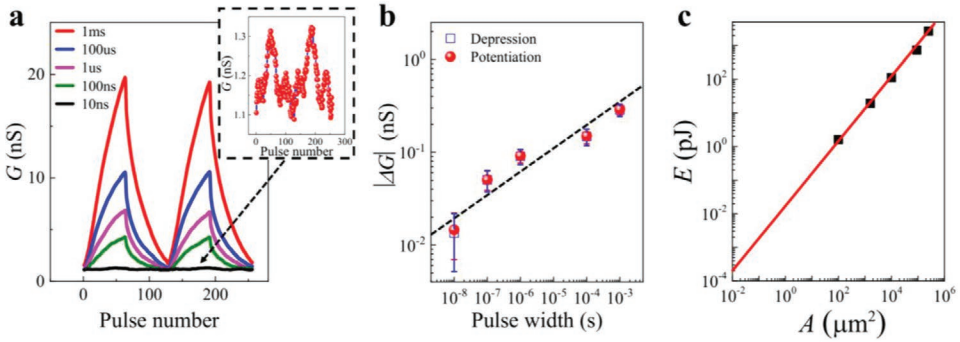


**Figure 3.** High-speed switching measurement and energy projection. a) High-speed switching of EGT is verified by reproducible cycling through 64 discrete levels with 1 ms, 100 µs, 1 µs, 100 ns, and 10 ns pulse widths. Inset: Zoom-in of channel conductance modulation at 10 ns timescale. Each conductance state is readout 1.5 s after the $V_g$ pulse, under $V_{ds} = 0.1$ V. b) The average changes in channel conductance $\Delta G$ scale with pulse width from 1 ms to 10 ns. The error bar is the standard deviation of the conductance update. c) The maximum dynamic switching energy ($E_{max}$) scales linearly with device area $A$. Projection of the required switching energy in a 100 × 100 nm$^2$ device can be as low as 200 aJ.

electrochemical reaction time. It should be noted that although the current prototype device can be programmed by 10 ns write pulses, a delay time from 10 ms to 1 s following a write operation is required to read the stable channel conductance (see Figures S3 and S7, Supporting Information), limiting the overall speed of the devices. This issue is also prevalent in other metal-oxide based EGTs.[21,23,24,31] The physical phenomena of write-read delay can be attributed to RC delay and Li-ion diffusion.[52] An equivalent circuit model of our device has been proposed to explain the origin of write-read delay (see Figure S8, Supporting Information). From the perspective of equivalent circuit, down-scaling device size, increasing electrolyte ionic conductivity and channel conductance are keys for improvement of operation speed of EGT devices.

The energy consumption of the EGTs can be estimated by calculating the energy of both weight programming and weight readout during the work cycle. Because of the decoupling of switching/reading operation in EGT, the switching and reading operations are executed through the gate and source/drain terminals, respectively. For the reading operation, since $V_d$ is always-on, the reading energy is more applicable to be expressed as reading power, which can be calculated simply by $I_d \times V_d$. Thanks to the high insulating property of $\alpha$-$Nb_2O_5$ channel, the channel conductance of our EGTs changes in a range of 1–100 nS, and thus the reading power is estimated to be lower than 1 nW at 0.1 V reading voltage, which is several orders of magnitude lower than that of other EGT synapses (≈µW).[30,31] Regarding the switching operation, because of the low gate leakage current (<50 pA), the switching energy is mainly caused by the gate capacitance charging and can be approximated by $E = C \times V^2$ for each switching, where $C$ is the gate capacitance and $V$ is applied gate voltage. Because the values of gate voltage during the switching are hard to measure, we use $V_{DD} = 4$ V to estimate the maximum energy consumption ($E_{max}$) for each weight programing. According to the measured gate capacitance values of EGTs with different device area (see Figure S9, Supporting Information), the switching energy is depicted as a function of the device area (see Figure 3c). Since the gate capacitance scales with device area, the switching energy is proportional to the device area with a slope of ≈20 fJ µm$^{-2}$. Thus, we project an energy consumption of 200 aJ for switching a 100 × 100 nm$^2$ device, which is far lower than the biological neural per-spike energy (1–10 fJ).[53]

It should be noted that the EGT introduced here can be programed under both voltage and current pulses. The gating process is essentially the charging of the gate capacitor and the change of carrier concentration in the channel which modulates the channel conductivity. When performing the high-speed operation of EGT, we need to precisely control the amount of charge delivered to the gate capacitor to obtain the same change of channel conductance ($\Delta G$) within different amount of time. Current pulse mode can deliver a well-defined amount of charge ($Q = I \times t$) and provide a wide current operation range (pA–A), while voltage pulse mode delivers dynamic amount of charge and provides a limited operating range (mV–V in normal instrument). This is because, under the voltage pulse mode, the applied voltage is dropped on several parts: the chemical potential difference between the gate and the channel electrodes (i.e., open circuit potential), ionic ohmic loss across the electrolyte, and the Nernst overpotential to drive the electron-ion exchange at the electrode/electrolyte interface.[54] The change of channel conductance is reflected by the first part, and the effective contribution of applied voltage on this part is dynamic. This is also the main reason why the device introduced here or in literature[23,26,31] usually exhibit nonlinear and asymmetrical switching behavior under voltage gating approach. Therefore, compared with voltage mode, current mode can provide a better condition to explore the limitation of operating speed of the EGT. However, current source is difficult to be implemented compared to voltage source and is usually not preferred in integrated circuits including the EGT array. Therefore, we use voltage pulses in other measurements to be closer to the practical situation.

Biological sensing signals including visual, auditory, olfactory and somatosensory have rich spatiotemporal dynamics and can be processed by neural networks in a highly effective way.[55–57] SNNs are designed to closely mimic natural neural networks. It incorporates the concept of timing into their computing model,[10] where neurons exchange information with sparse and asynchronous spikes in time domain (in SNNs, information can be encoded not only by rate coding, but also by spatiotemporal coding,[58,59] see Figure S10, Supporting

Information), and thus can be appropriately capitalized on spatiotemporal information processing. The spatiotemporal spikes can be recognized by the positive correlation between synaptic weight order and spike timing in SNN, that is, incremental synaptic weights with increasing arriving time of spikes (see Figure S11, Supporting Information). The positive weight–time correlation will induce a larger membrane potential ($V_m$) in post-neuron.

To verify the recognition model, a simple 3×1 SNN is constructed. As shown in **Figure 4**a, the SNN contains 3 pre-neurons connected to 1 post-neuron through 3 EGT synapses. We design a special voltage waveform as the pre-spikes ($V_s$) and post-neuron circuit (see Figure S12, Supporting Information) and set the synaptic weight value to an increasing order $w_1 < w_2 < w_3$ intentionally. Figure 4b shows the measured post-synaptic current $I_{syn}$ and calculated $V_m$ when inputting two 3-spike sequences with timing of $t_1 < t_2 < t_3$ and $t_1 > t_2 > t_3$, named as 1–2–3 and 3–2–1, respectively. A higher $V_m$ generates for spike sequence 1–2–3 due to the positive weight-time correlation. If the synaptic weight amplitude after training just satisfies the relationship of $V_m$ (3–2–1) < $V_{th}$ < $V_m$ (1–2–3), where $V_{th}$ is threshold potential for post-neuron firing, the spatiotemporal features of spike sequences can be discriminated according to the post-neuron output spike.

The weight order determines which spike sequence can be discriminated. To form the specific weight order for the positive weight-time correlation with the target spatiotemporal spikes, training of the EGT synaptic weight is required prior to recognition. Here, the Widrow–Hoff supervised learning rule is used to train synaptic weights[60] (see Figure S13, Supporting Information). When the target spike sequence is present, a teacher signal labeling the sequence as "true" is applied to the post-neuron, being compared with the actual output of the post-neuron (see Figure 4a). The comparison can lead to three cases: if both the output and the teacher spikes are present, the true pattern has been correctly detected (true fire), thus requiring no further weight update; if the output spike is present without any teacher spike, a false pattern has been erroneously detected (false fire), thus requiring depression of the synaptic weights; if the output spike is not present while the teacher is, the true pattern has been erroneously missed (false silence), thus requiring potentiation of the synaptic weights. The weight update can be implemented by the spiking-time-dependent-plasticity (STDP).[61,62] As shown in Figure 4c, by changing the relative timing ($\Delta t$) between $V_s$ and $V_g$ waveforms, different effective $V_{gs}$ is applied to EGT, resulting in different amplitude of weight update (see Figure 4d). Note that the potentiation and depression of synapses depend on the polarity of $V_g$, which is determined by comparing the output spike with teacher spike. For potentiation (depression), a positive (negative) $V_g$ is generated.

Figure 4e shows the weight evolution during the spatiotemporal spike sequence learning process, including calculated membrane voltage $V_m$, the indication of true fire, false fire, and false silence events (see Figure S14 (Supporting Information) for the measurement details). The spike sequence 1–2–3 is used as the target sequence for training. The weights of the synapses are set to lowest values (low conductance state) initially. In each training cycle with a duration of 500 ms, a 3-spike sequence with time interval of 20 ms is randomly generated from pulse sequences dataset as an input. The synaptic weights are adjusted according to the Widrow–Hoff rule and the STDP characteristics of the EGT devices. It can be seen that the false silence and false fire events lead to potentiation and depression of the synapses, respectively. After 65 training cycles, the $V_m > V_{th}$ takes place only when the teacher spikes appear (i.e., true fire events), indicating that the target spike sequence can be identified correctly.

The energy efficiency of the spatiotemporal SNN is mainly determined by the training process, which depends not only on the energy consumption of each weight update operation, but also on the weight update nonlinearity and variation. We analyze the impact of weight update nonlinearity and variation on the training cycle number, and find that it increases rapidly with the deterioration of these two characteristics (see Figure S15, Supporting Information). Therefore, the quasi-linear weight update and low variation empower our EGTs to implement the spatiotemporal SNN with the high-energy efficient training paradigm.

Orientation detection is a well-known example of spatiotemporal information processing of cortical cells.[63] The EGT-based spatiotemporal SNN shows similar capabilities and can be used to build a tactile sensing system by its ability to learn and recognize spike timing sequences. **Figure 5**a shows a schematic touchpad made by a 5 × 5 artificial tactile sensor array to determine eight moving orientations. Spikes can be generated by the tactile sensors once they are touched and output to the EGT array for computing. Each orientation can be determined by three tactile sensors with a specific sensing timing, which generates a 3-spike sequence. For example, the azimuth angle 0° can be represented by a 13–14–15 spike sequence produced by touching 13–14–15 tactile sensors in sequence. Based on this scenario, an SNN is built by connecting 25 input neurons to 8 output neurons via EGT synapses to form a 25×8 network (Figure 5b). Each input neuron corresponds to one tactile sensor in the touchpad, while each output neuron corresponds to one azimuth angle of moving orientation. Similar to Figure 4e, the EGT synapses connected with each output neuron corresponding to a particular orientation have been trained to form a weight increasing order prior to orientation detection (see Figure S16, Supporting Information). Figure 5c displays the $V_m$ of output neurons for all eight orientations. For each output neuron, $V_m$ shows the highest value and exceeds $V_{th}$ only when the spike sequence corresponding to the orientation learned by this neuron is the input, confirming the capability of orientation detection of the EGT-based spatiotemporal SNN. It should be pointed out that the EGT array and the associated computing paradigm are not restricted to tactile sensor system. In fact, it can be combined with visual sensors, auditory sensors and biosensors to build more complex applications, such as character recognition, spell checking, DNA analysis, etc. In addition, the tactile sensor system proposed here is comprised of separated sensing and processing unit. Future work can integrate sensing function for the proposed EGT-based spatiotemporal SNN, which may lead to more time- and energy-efficient real time sensing and signal processing.

In summary, we have successfully fabricated a 32 × 32 oxide-based EGT array that emulates synaptic weight modulation with quasi-linearity, low variation, high endurance, high

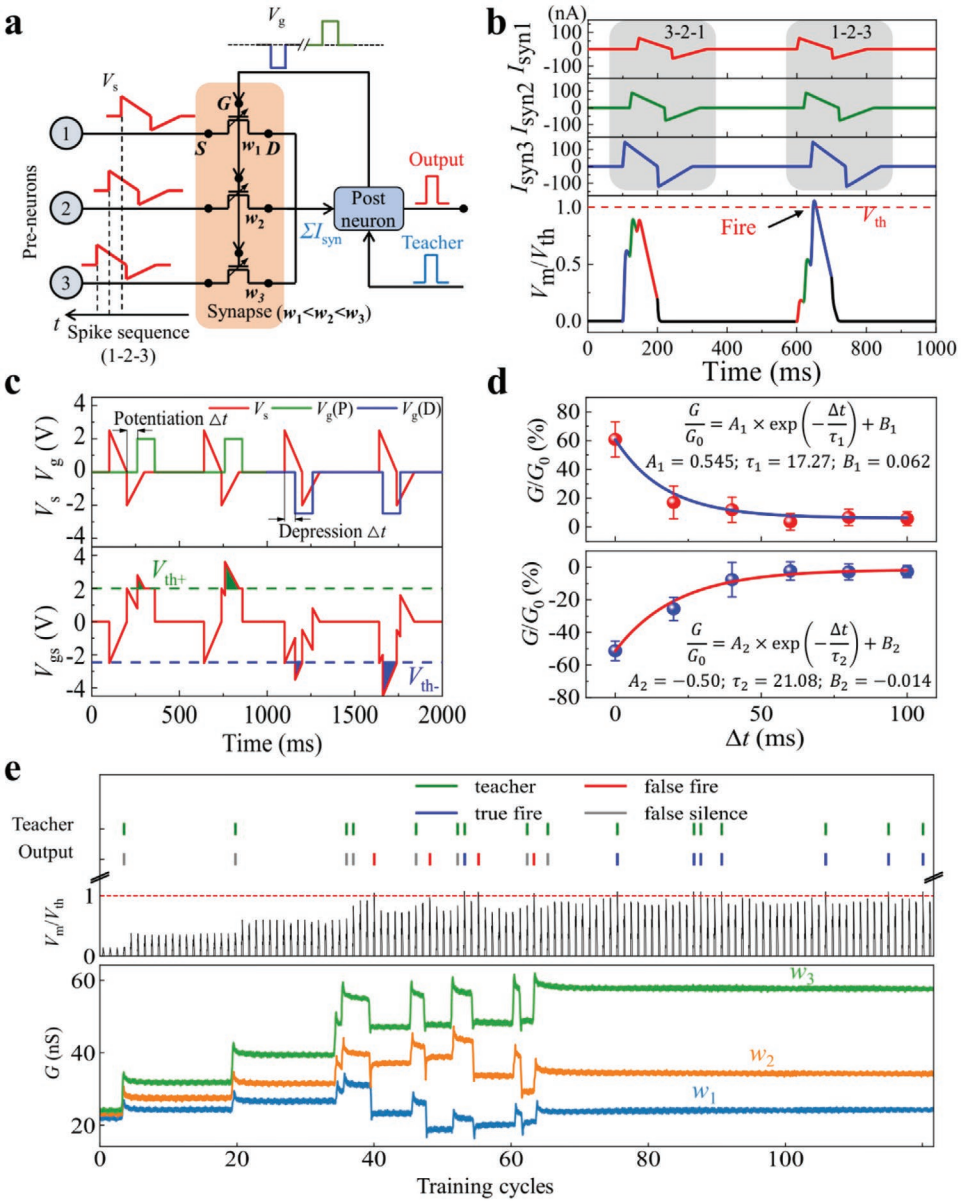


**Figure 4.** Spatiotemporal SNN based on EGT synapses. a) Schematic of a simple 3 × 1 SNN with 3 pre-neurons connected with 1 post-neuron via 3 EGT synapses. The 3 pre-neurons fire a spike sequence consisting of 3 pre-spikes ($V_s$) with increasing spike timing $t_1 < t_2 < t_3$, named as 1–2–3. The spike sequence passes the synapses with increasing weights $w_1 < w_2 < w_3$ to form post-synaptic current $\Sigma I_{syn}$, which flows into post-neuron generating output spike. The output spike is compared with the teacher spike to determine the polarity of post-spikes ($V_g$), which are applied to the EGT gate to update the synaptic weights. For potentiation (depression), a positive (negative) $V_g$ generates. b) The measured synaptic currents flowing through each synapse (top three panels) and the simulated evolution of membrane potential ($V_m$) with inputs of spike sequence 3–2–1 and 1–2–3 (bottom panel). $V_m$ induced by spike sequence 1–2–3 exceeds spike threshold ($V_{th}$) due to the positive weight-time correlation, enabling the spatiotemporal recognition of the SNN. c) Overlapping strategy of $V_s$ and $V_g$ waveforms for STDP realization. $\Delta t$ is relative spike time between $V_s$ and $V_g$. $V_{th}^+$ and $V_{th}^-$ are the threshold voltage that can induce potentiation and depression of synapses, respectively. By superimposing $V_s$ and $V_g$ waveforms, the overall potential on the synapse will be above $V_{th}^+$ / $V_{th}^-$, resulting in the change of the synaptic weight. d) Measured relative change of synaptic weight as a function of $\Delta t$ for potentiation (top) and depression (bottom). $G_0$ is the initial channel conductance. e) (Top) Teacher, true fire, false fire, false silence events, and simulated $V_m$ during the learning process. (Bottom) The measured evolution of synaptic weights with input of training spatiotemporal spike sequences. False silence and false fire events lead to synaptic potentiation and depression, respectively. True fire leads to no weight change. After training, the synaptic weights form an increasing order ($w_1 < w_2 < w_3$).

speed, low readout conductance, and low switching energy density, as summarized in Table 1. The synaptic performance improvement lies primarily in three aspects: the decoupled switching/reading operation, the highly insulating amorphous $Nb_2O_5$ channel and $Li_xSiO_2$ dielectric, and the stable Li-ion electrochemical intercalation/extraction mechanism. The prominent analog switching performance has been used for hardware implementation of SNN with spatiotemporal coding,

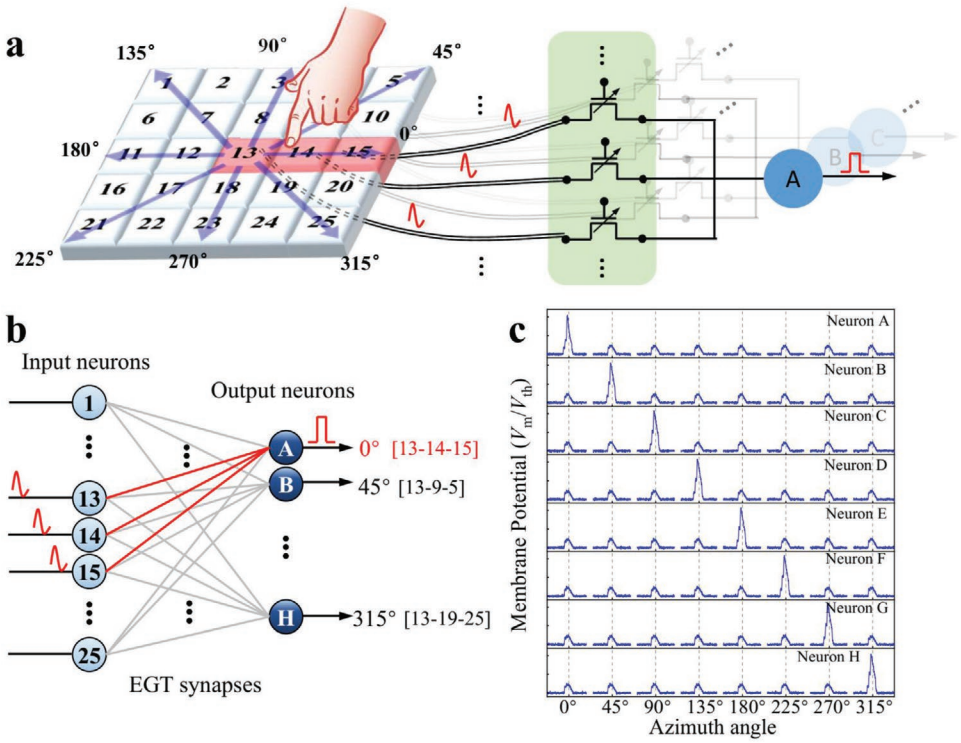


**Figure 5.** Moving orientation detection. a) Schematic of a touchpad made by a 5 × 5 artificial tactile sensor array and the spatiotemporal information processing in SNN with EGTs. The tactile sensors are given a function to detect 2D spatiotemporal touch information, and transmit the touch-triggered spikes to EGT synaptic array. Then the SNN can intelligently recognize the touch orientation and drive the corresponding output neuron to emit an output spike. b) The diagram of two-layer SNN architecture composing of input neurons and output neurons connected by EGT synapses for spatiotemporal orientation information recognition. c) The membrane potentials ($V_m$) of the eight output neurons as a function of azimuth angle of moving orientation, where different pulse sequences representing different orientations are input. The output neurons show higher $V_m$ value only when the spike sequence corresponding to the orientation learned by this neuron is input. For example, as for neuron *A* which has been trained for recognizing azimuth angle 0°, $V_m$ increases obviously when spike sequence 13–14–15 is input.

demonstrating highly efficient learning and recognition with the EGT array. Based on that, we demonstrated that this EGT-based SNN can be used to develop a tactile sensory system with capability of moving orientation detection. These results provide an inspiration for future development of neuromorphic computing using such EGT devices to support edge application such as intelligent sensing systems serving as an interactive interface for internet of things.

## Experimental Section

*Device Fabrication*: The EGT array fabrication processes are as follows: 1) 40 nm TiN thin film was deposited by ion-beam sputtering on $SiO_2$/p-Si substrate (300 nm/500 µm). 2) Source and drain electrodes were patterned by standard lithography process; the channel length and width of individual EGT unit are 2 and 50 µm, respectively. 3) Source and drain electrode formed by wet etching of TiN. 4) 100 nm $SiO_2$ thin film was selected as isolation layer and deposited by ion-beam sputtering. 5) After patterning by second lithography process, alignment etch was performed for exposure of channel region and source and drain contact. 6) 20 nm $\alpha$-$Nb_2O_5$ and 80 nm $Li_xSiO_2$ were prepared by magnetron sputtering as channel materials and electrolyte, respectively. 7) EGT array was finished after gate/source/drain metallization by e-beam evaporation and lift-off process.

Among all the tested 1024 individual EGT units, 737 devices had the nonvolatile analog switching characteristics, indicating a yield ≈72% of the as-prepared EGT array. The yield of the EGT array still has room to improve, which is mainly an engineering challenge to minimize the process variation in the clean room. Nevertheless, the 72% yield is able to demonstrate prototypical neural network functions, for example, the 25 × 8 SNN shown in this work.

*Measurement Method*: The elemental composition of $Li_xSiO_2$ and $\alpha$-$Nb_2O_5$ were characterized by X-ray photoelectron spectroscopy (XPS, Thermo Scientific ESCALAB 250Xi). Atomic force microscopy (AFM, Bruker MultiMode 8) was used to analyze the film morphology. The crystallinity of $Li_xSiO_2$ and $\alpha$-$Nb_2O_5$ thin films were characterized by Grazing incidence X-ray diffraction (GIXRD, Rigaku D/max-2500). Second ion mass spectroscopy (SIMS, ION-TOF GmbH TOF.SIMS 5–100) was carried out to characterize the ion distribution in EGT. The SIMS measurement was performed in an ex-situ method. Before the SIMS measurement, three types of samples were prepared. One type is the EGT under positive gating for several seconds, i.e., positive-gated EGT. The second type is the EGT under positive gating for several seconds and then negative gating for several seconds, i.e., negative-gated EGT. The last type is the pristine EGT without any electrical treatment, i.e., pristine EGT. Then, the SIMS measurement was carried out to characterize the ion distribution in all three types of EGTs. The electrical measurements of EGTs were carried out using semiconductor parameter analyzer (Agilent B1500 and B1530A) in ambient environment.

*SNN Implementation*: Artificial synapses are implemented with EGT array. The EGT array is measured by probing the source, drain, and gate electrodes of each EGT devices individually. Semiconductor parameter analyzer (Keysight B1500) is used to send pre-spike $V_s$ to the source electrode of EGT and measure the post-synaptic current ($I_{syn}$) through drain electrode at the same time. The measured $I_{syn}$ is integrated

by output neuron circuits, which is simulated by MATLAB Simulink software platform in computer. The supervised learning algorithm are also performed by MATLAB Simulink software platform. According to the simulation results, the polarity of the post-spike ($V_g$) can be determined. Then, $V_g$ is sent to the gate electrode of EGT by the Semiconductor Parameter Analyzer to update the channel conductance, that is, synaptic weight, according the STDP property.

The STDP characteristics are obtained through device measurement. The detailed description about the neuron circuit, supervised learning algorithm, and measurement system can be seen in Figures S11–S14 (Supporting Information).

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

analog switching, electrolyte-gated transistors ion intercalation, spatiotemporal information processing

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