IMAGES USED TO AID IN DESIGN FLOW FOR MINI SRC

PHASE 1:

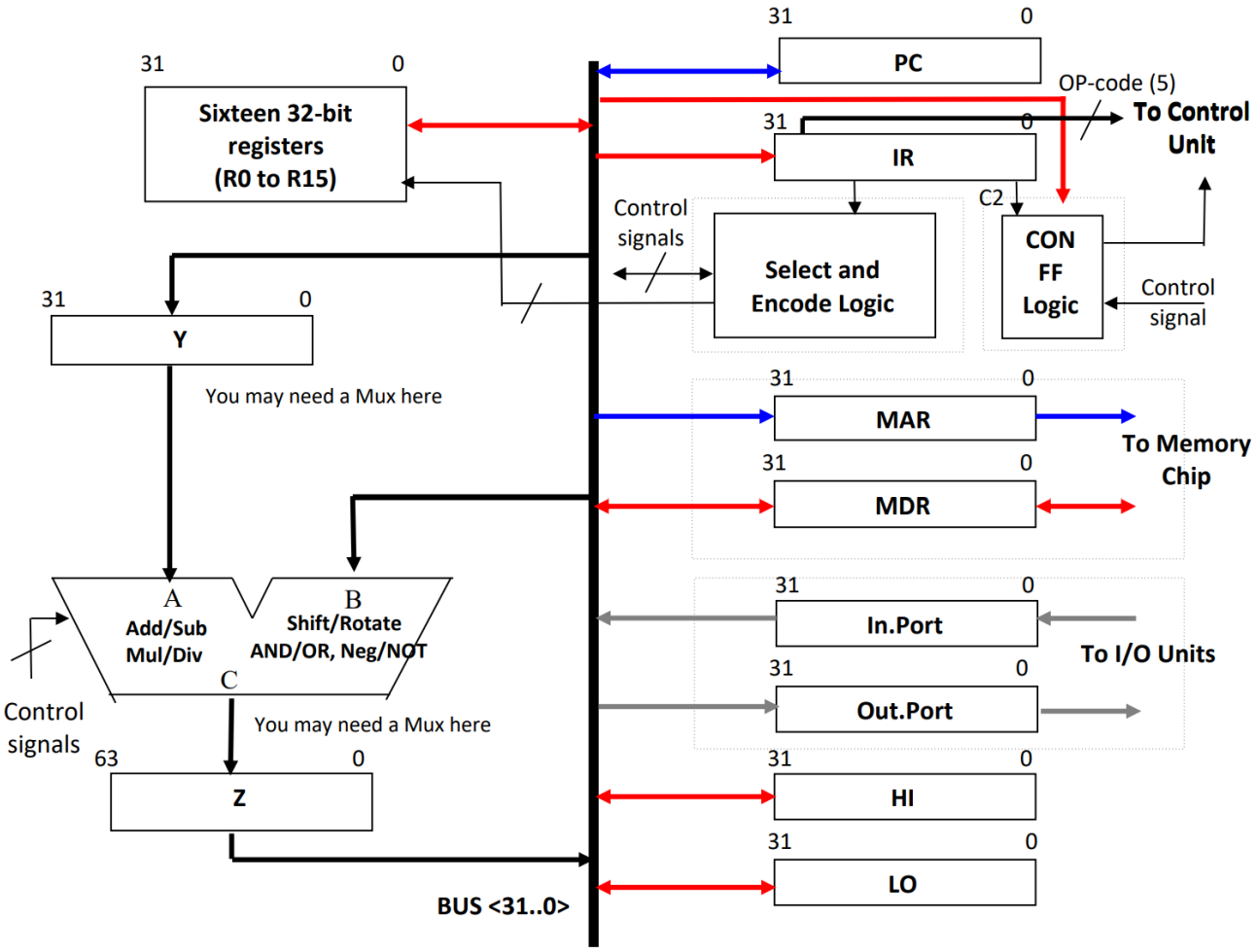

Figure 1: Simplified datapath

Figure 3: A typical Bus

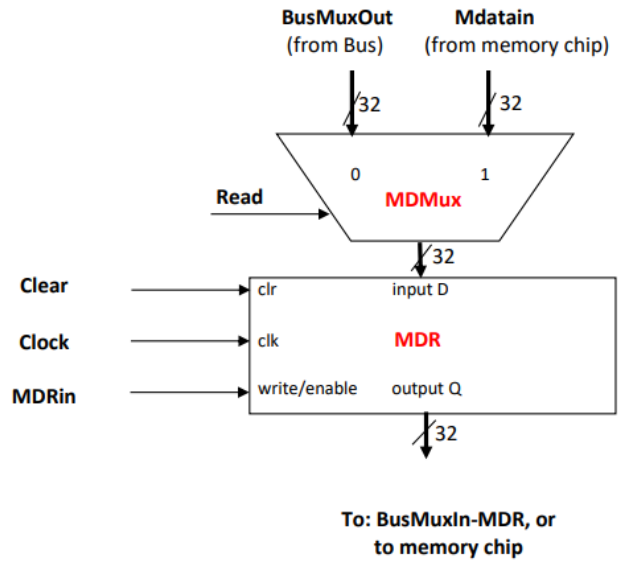

Figure 4: The MDR unit

PHASE 2:

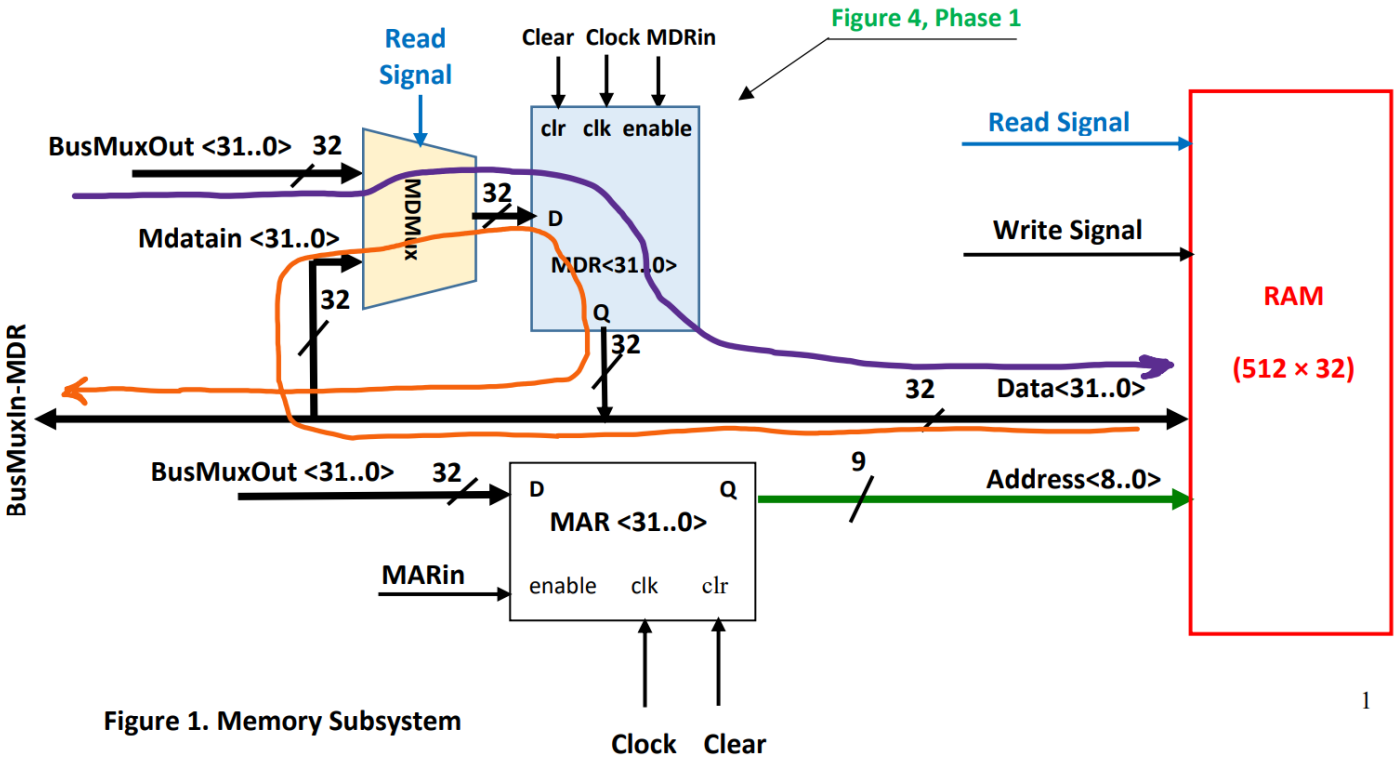

Figure 1. Memory Subsystem

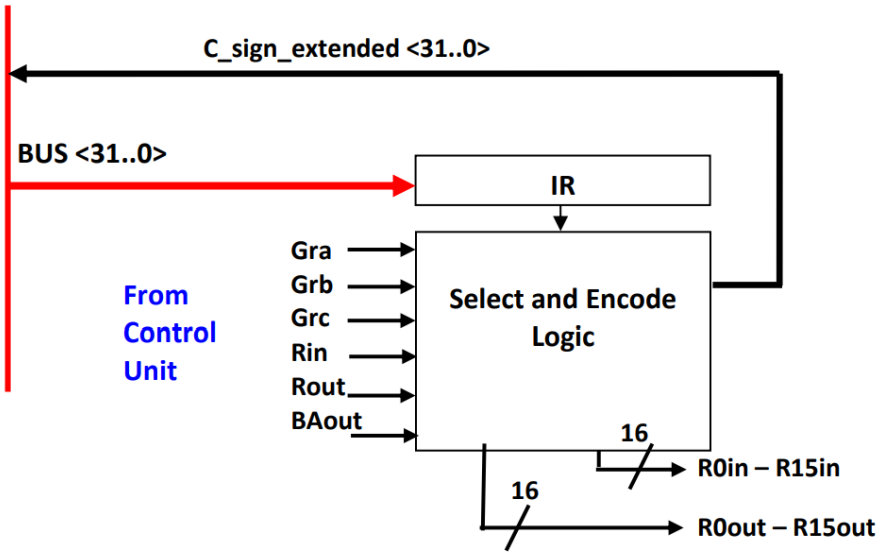

Figure 2. Select and Encode block diagram

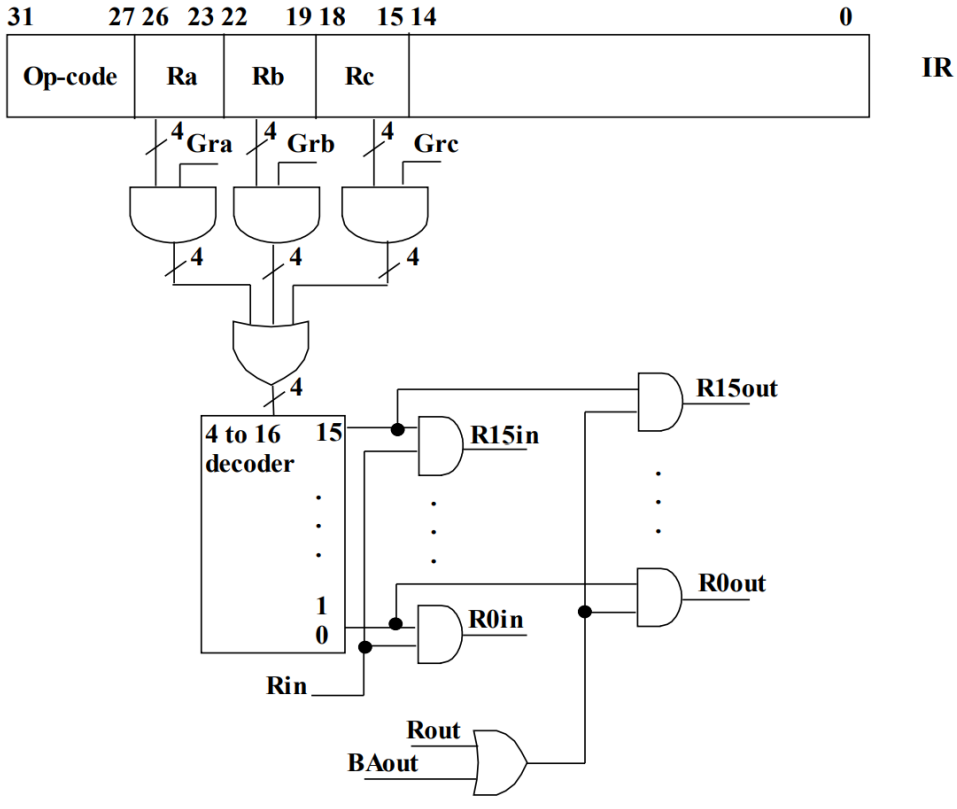

Figure 3. "Select and Encode" logic to generate R0in-R15in and R0out-R15out

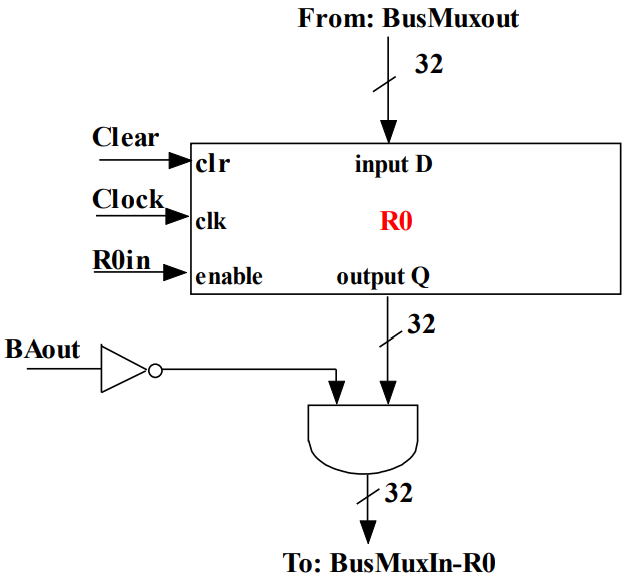

Figure 5. Revised register R0

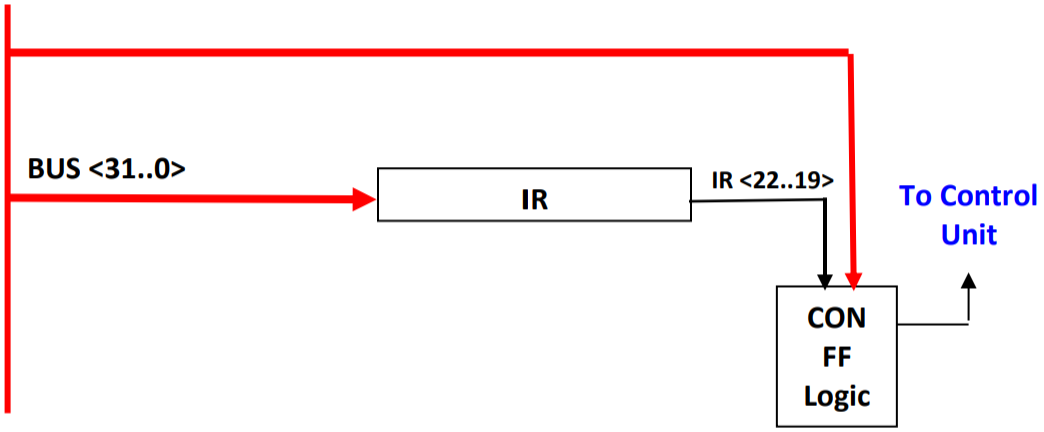

Figure 6. CON FF logic

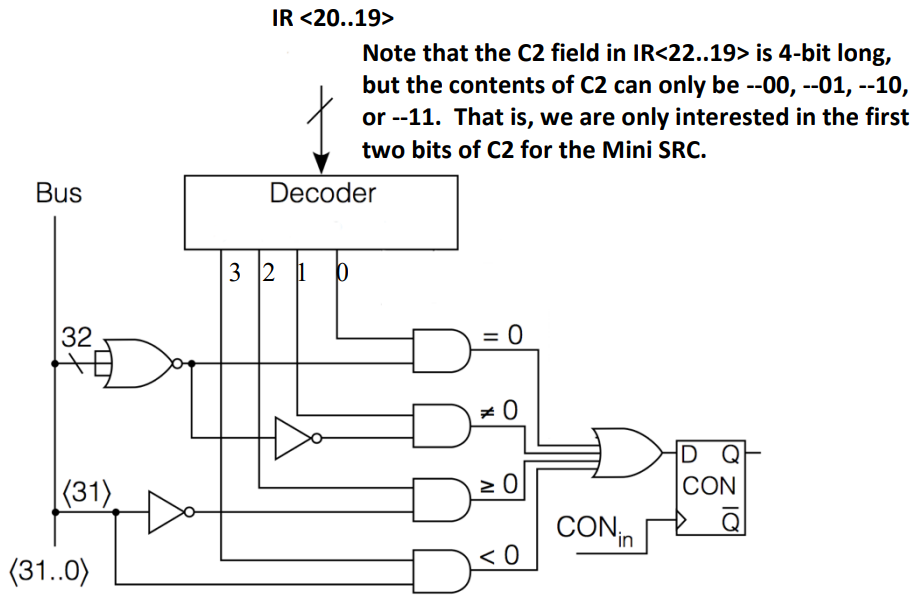

Figure 7. Computation of the conditional value CON in the CON FF Logic

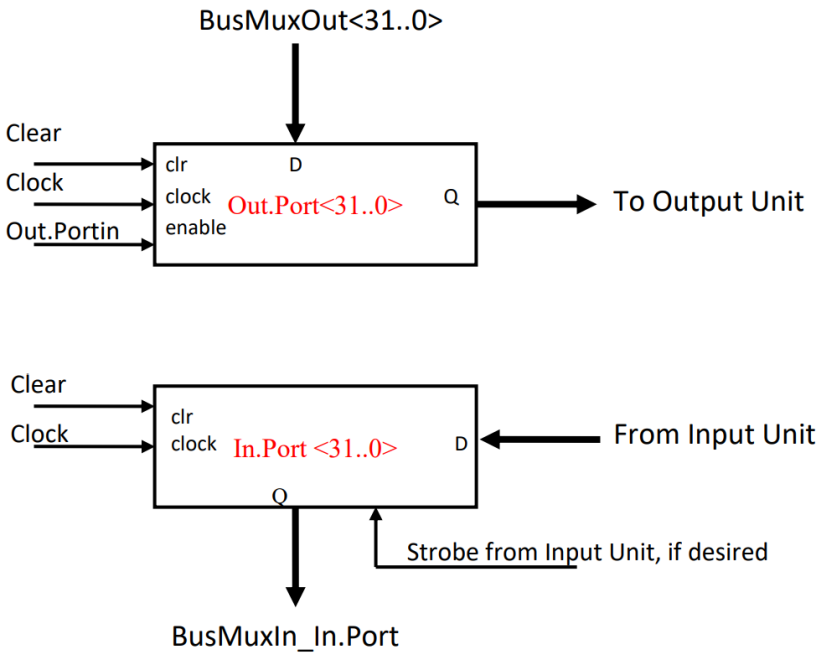

Figure 8. Input and Output ports

PHASE 3:

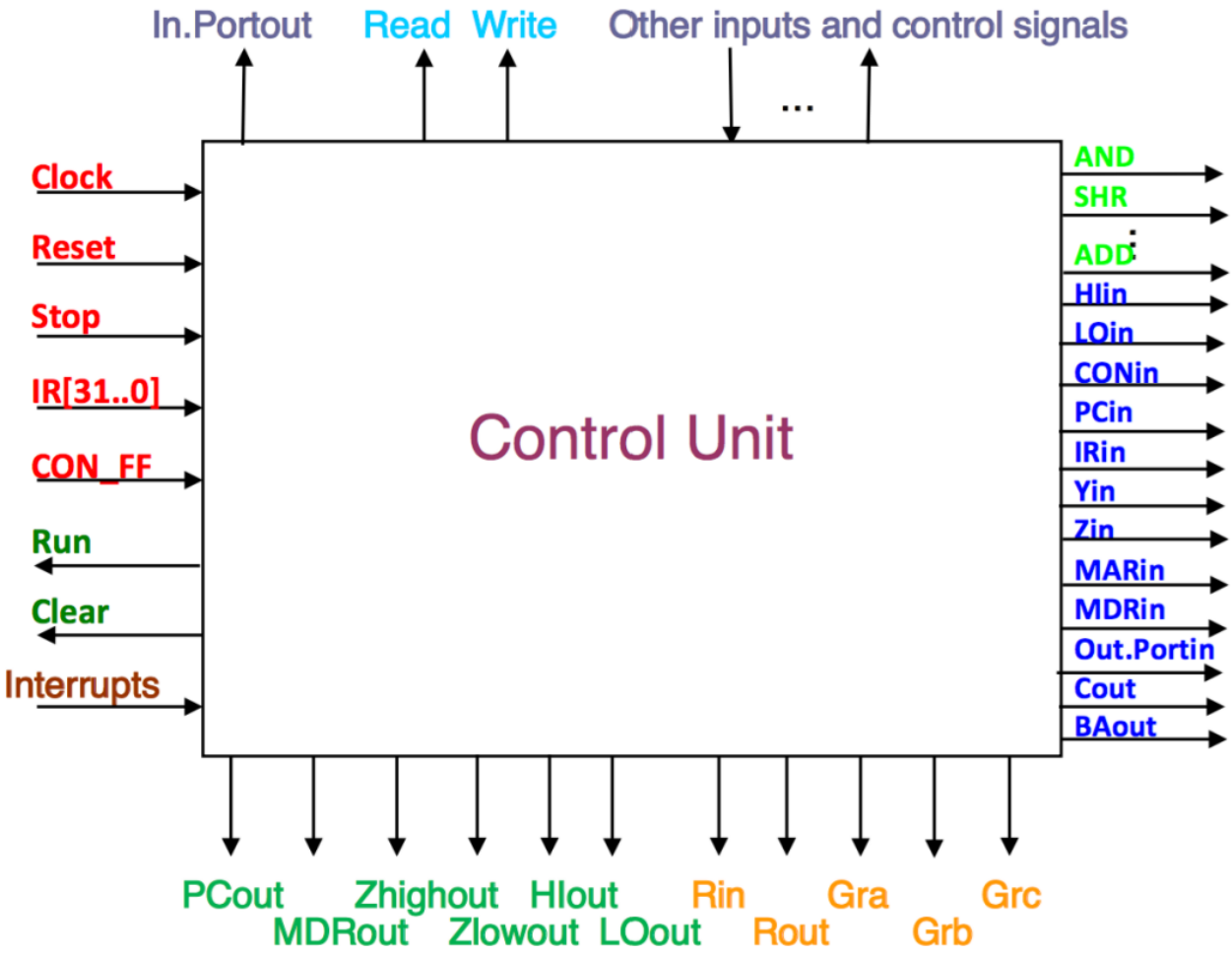

Figure 1: Block diagram of the Control Unit