



SPECIFICATION FOR LCD MODULE

MODULE NO: BTG-12832BI-FBWB-G-G-B3

CUSTOMER NO:L16018

Doc.Version:03

Customer Approval:

☐ Accept

☐ Reject

YEEBO	NAME	SIGNATURE	DATE
Prepare	Electronic Engineer	张钧泉	2021-10-12
Check	Mechanical Engineer	林明威	2021-10-12
Verify		林国超	2021-10-14
Approval		Samuel	2021-10-15

☐ APPROVAL FOR SPECIFICATIONS ONLY

☒ APPROVAL FOR SPECIFICATIONS AND SAMPLE

WIMRD005-02-D

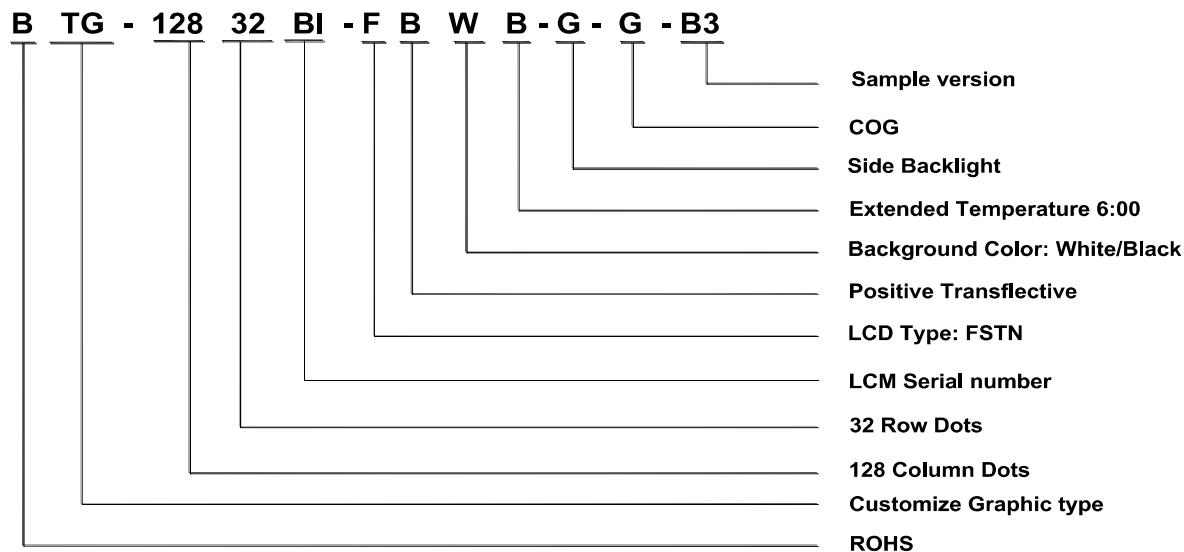
DOCUMENT REVISION HISTORY

Sample Version	DOC. Version	DATE	DESCRIPTION		CHANGED BY
B0	00	2021-4-23	Full Spec	First sample	ZJQ
B1	01	2021-6-16	Full Spec	Change the glass thick and some dim	ZJQ
B2	02	2021-7-23	Full Spec	Changed the LCD	ZJQ
B3	03	2021-9-28	Full Spec	Modified the FPC & IC; changed the package	ZJQ



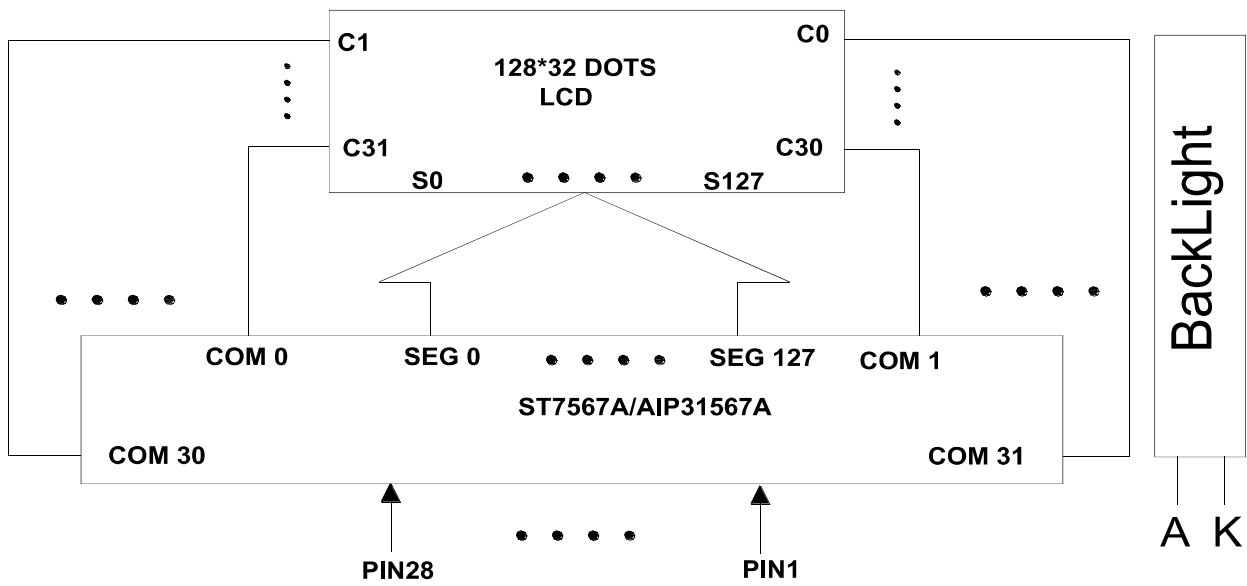
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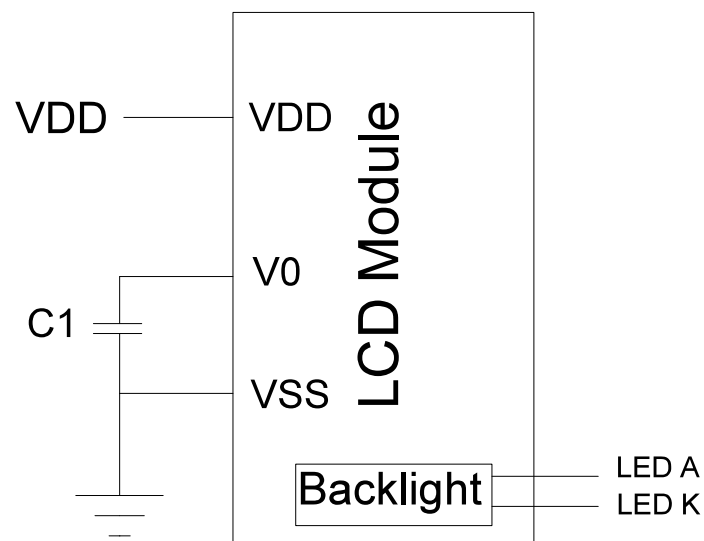
1.NOTATION OF THE MODULE NUMBER:**2.MECHANICAL SPECIFICATIONS**

ITEM	SPECIFICATION
LCD Description	128*32 DOTS
Module dimension	53.50(W)*25.50(H)*4.35 (T)
Viewing area	50.40(W)*17.20(H)
Active area	43.50(W)*13.10(H)
Character dot pitch	0.34(W)* 0.41(H)
Character dot size	0.32(W)* 0.39 (H)
Duty/Bias	1/33 duty, 1/6 bias
LCD display mode	FSTN/White-Black mode/Positive/ Transflective
Viewing direction	6 o'clock
Driver IC	ST7567A/AIP31567A
Interface	MCU and SPI
Module weight	8.5g±10%

3.BLOCK DIAGRAM

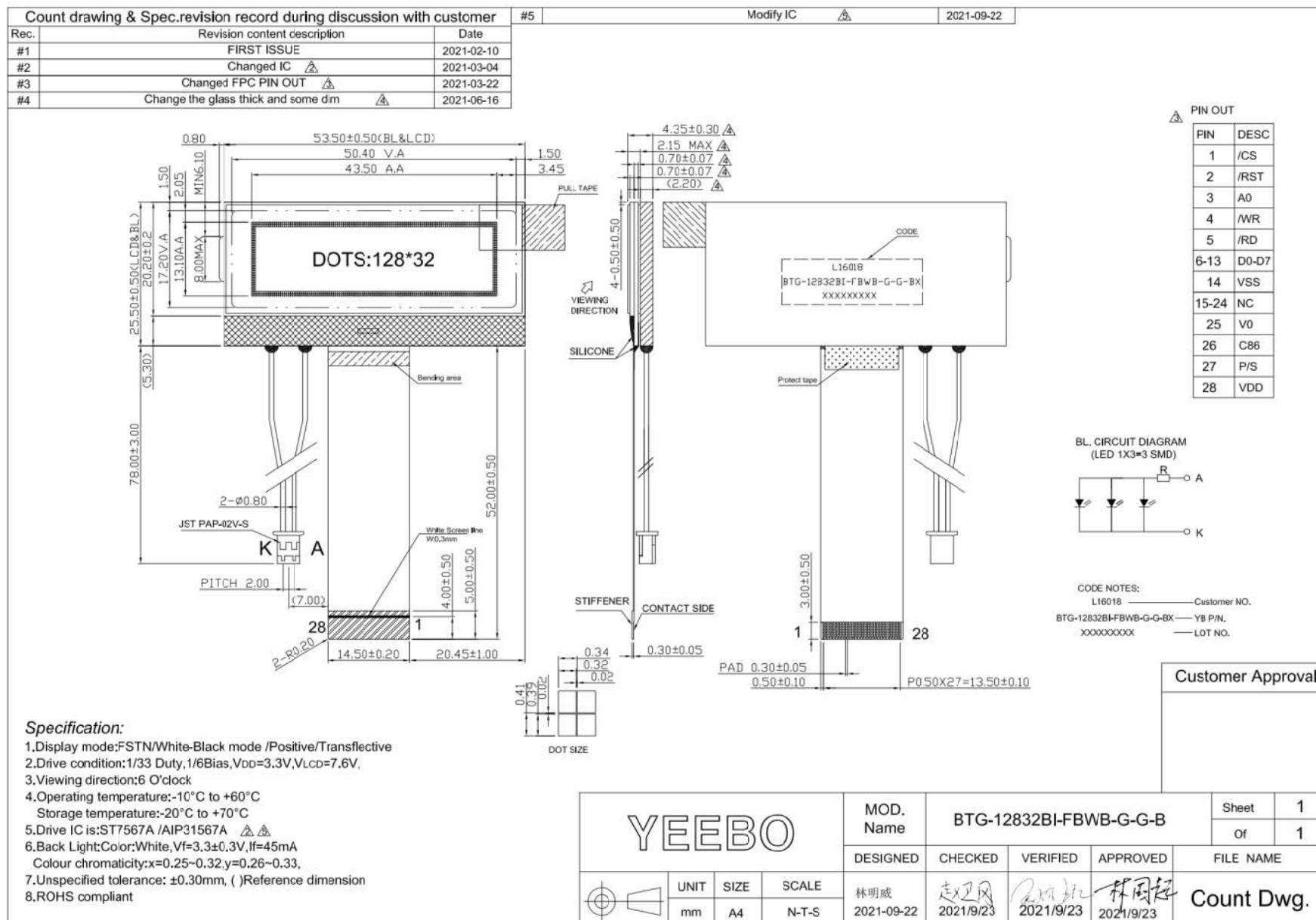


4.POWER SUPPLY



$C1=0.01\sim 4.7\mu F$

5. DIMENSIONAL OUTLINE



6. PIN DESCRIPTION

Pin no.	Symbol	Function													
1	/CS	Chip select input pin. Interface access is enabled when CSB is “L”. When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.													
2	/RST	Hardware reset input pin. When RSTB is “L”, internal initialization is executed and the internal registers will be initialized													
3	A0	It determines whether the access is related to data or command. A0=“H” : Indicates that signals on D[7:0] are display data. A0=“L” : Indicates that signals on D[7:0] are command.													
4	/WR	Read/Write execution control pin. When PSB is “H”,RWR is used to decide slave address (SA1) in I2C serial interface. RWR is not used in 3-line and 4-line SPI interface and should fix to “H” by VDD1 or VDDH	<table><tr><th>C86</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr><tr><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin. R/W=“H”: read. R/W=“L”: write.</td></tr><tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin. Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr></table>	C86	MPU Type	RWR	Description	H	6800 series	R/W	Read/Write control input pin. R/W=“H”: read. R/W=“L”: write.	L	8080 series	/WR	Write enable input pin. Signals on D[7:0] will be latched at the rising edge of /WR signal.
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L	8080 series	/WR	Write enable input pin. Signals on D[7:0] will be latched at the rising edge of /WR signal.												
5	/RD	Read/Write execution control pin. When PSB is “H”,ERD is used to decide slave address (SA0) in I2C serial interface. ERD is not used in 3-Line and 4-Line SPI interface and should fix to “H” by VDD1 or VDDH	<table><tr><th>C86</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr><tr><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin. R/W=“H”: When E is “H”, D[7:0] are in output mode. R/W=“L”: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr><tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin. When /RD is “L”, D[7:0] are in output mode.</td></tr></table>	C86	MPU Type	ERD	Description	H	6800 series	E	Read/Write control input pin. R/W=“H”: When E is “H”, D[7:0] are in output mode. R/W=“L”: Signals on D[7:0] are latched at the falling edge of E signal.	L	8080 series	/RD	Read enable input pin. When /RD is “L”, D[7:0] are in output mode.
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L	8080 series	/RD	Read enable input pin. When /RD is “L”, D[7:0] are in output mode.												
6~13	D0~D7	When using 8-bit parallel interface: (6800 or 8080 mode) 8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor. When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.													
14	VSS	Ground													
15~24	NC	No Connect													
25	V0(VG)	VG is the LCD driving voltage for segment circuits. VGO is the output of VG regulator. VGI is the VG input of segment circuits. VGO, VGI should be connected together in ITO layout. 1.6V ≤ VG < VDD2-0.2V, TSEL=L. VDD2-0.2V ≤ VG < 3.8V, TSEL=H													
26	C86	C86 selects the microprocessor type in parallel interface mode.													
27	P/S	PSB selects the interface type: Serial or Parallel													
28	VDD	Power supply													

7. ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Min	Max	Unit
Power supply voltage for logic	V _{DD}	-0.3	+4.0	V
LCD driver voltage	V _{LCD}	-0.3	V _{DD1} +0.3	V
Operating temperature	T _{OPR}	-10	+60	°C
Storage temperature	T _{STG}	-20	+70	°C

Note: Voltage greater than above may damage the module
All voltages are specified relative to V_{SS}=0V

8.ELECTRICAL CHARACTERISTICS.

8-1DC Characteristics(Ta=25°C)

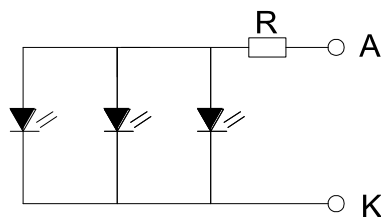
Item	Symbol	Min	Typ	Max	Unit	Applicable terminal	Test condition
Operating voltage	V _{DD}	3.1	3.3	3.5	V	-	-
Supply current	I _{DD}	-	0.2	0.3	mA	-	-
Input voltage	V _{IL}	V _{SS}	-	0.3V _{DD1}	V	A0,/WR,/RD ,D0~D7	-
	V _{IH}	0.7V _{DD1}	-	V _{DD1}	V		-
Output voltage	V _{OL}	V _{SS}	-	0.2V _{DD}	V	D0~D7	I _{OL} =-1mA
	V _{OH}	0.8V _{DD1}	-	V _{DD1}	V		I _{OH} =1mA
Input leakage current	I _{IL}	-1	-	1	μA	MPU Interface	-
LCD driving voltage	V _{LCD}	7.4	7.6	7.8	V	-	Ta=25°C

Optimum LCD driving voltage will varies and control within the above specified range.

8-2. Backlight Characteristics (Ta=25°C)

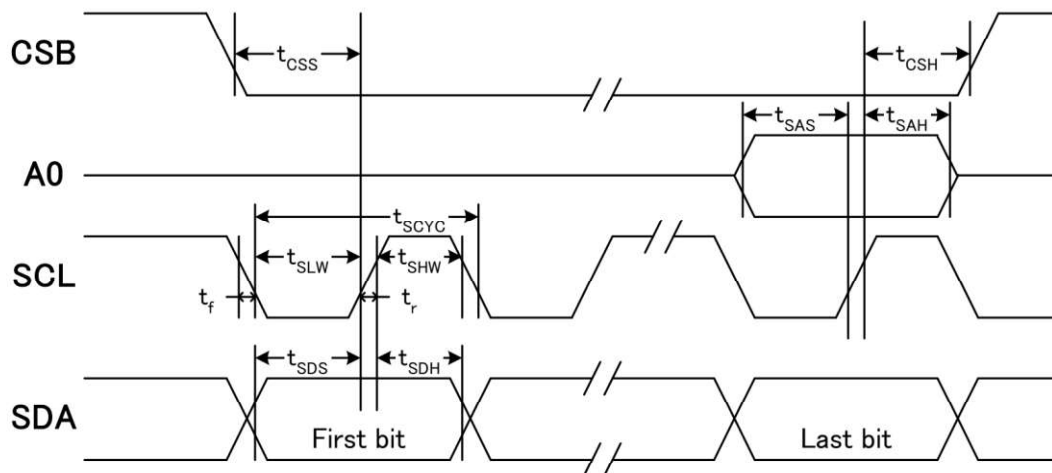
Item	Symbol	Min	Typ	Max	Units	Condition
Forward Voltage	Vf	3.0	3.3	3.6	V	Ta=25°C
Forward Current	If	-	45	60	mA	
Colour chromaticity (Central point)	X	0.25	-	0.32	-	
	Y	0.26	-	0.33	-	
Module luminance	Lv	160	250	—	cd/m²	
Uniformity	Avg	70	-	-	%	
Color	White					

BL. CIRCUIT DIAGRAM (LED 1X3=3 SMD)



8-3 AC Characteristics (Ta=25°C).

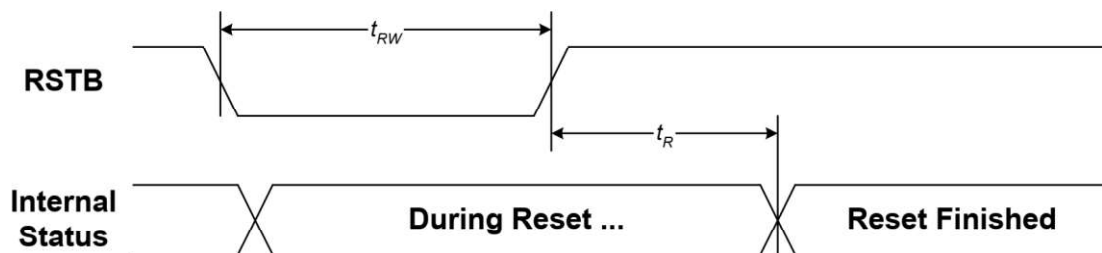
8-3-1 System Bus Timing for 4-Line Serial Interface



(VDD1 = 3.3V, Ta = 25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		50	—	ns
SCL "H" pulse width		tSHW		25	—	
SCL "L" pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CSB-SCL time	CSB	tCSS		20	—	
CSB-SCL time		tCSH		40	—	

8-3-2 Hardware Reset Timing



(VDD1 = 3.3V, Ta = 25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1.0	us
Reset "L" pulse width	tRW		1.0	—	

9. INSTRUCTION DESCRIPTION

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
(2) Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
(3) Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
(4) Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
(5) Read Status	0	1	0	MX	D	RST	0	0	0	0	Read IC Status
(6) Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
(7) Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
(8) SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
(9) Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
(10) All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
(11) Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
(12) Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
(13) END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
(14) RESET	0	0	1	1	1	0	0	0	1	0	Software reset
(15) COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
(16) Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
(17) Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
(18) Set EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
	0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
(19) Set Booster	0	0	1	1	1	1	1	1	0	0	Double command!! Set booster level: BL=0: 4X BL=1: 5X
	0	0	0	0	0	0	0	0	0	BL	
(20) Power Save	0	0	Compound Command								Display OFF + All Pixel ON
(21) NOP	0	0	1	1	1	0	0	0	1	1	No operation
(22) Set N-Line	0	0	1	0	0	0	0	1	0	1	Set N-Line inversion
	0	0	0	0	0	NL4	NL3	NL2	NL1	NL0	
(23) Release N-Line	0	0	1	0	0	0	0	1	0	0	Exit N-Line inversion
(24) SPI Read Status	0	1	1	1	1	1	1	1	0	0	SPI read status command
	0	1	0	MX	D	RST	ID3	ID2	ID1	ID0	
(25) SPI Read DDRAM	0	1	1	1	1	1	1	1	0	1	SPI read DDRAM command
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	

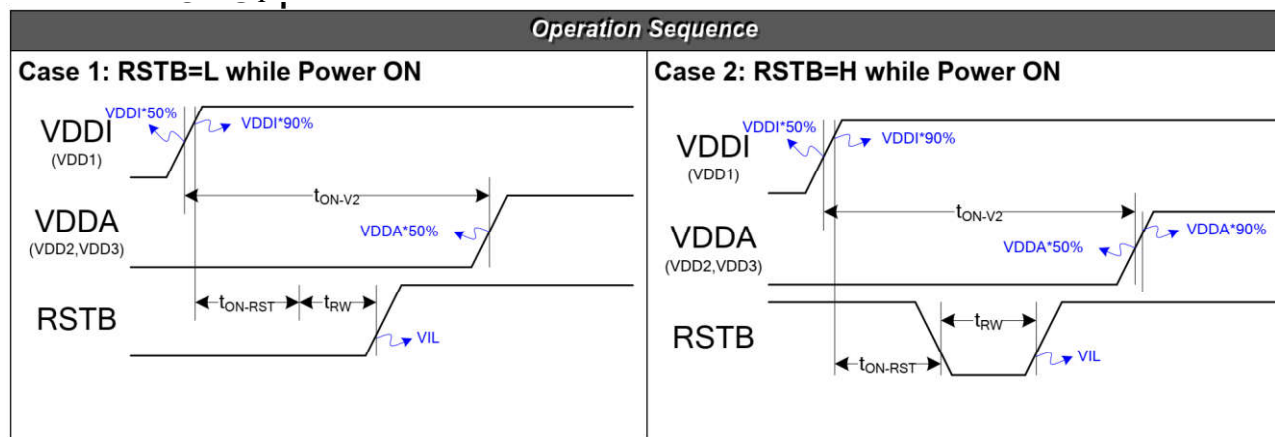
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
EXTENSION COMMAND SET											
Extension Command Set	0	0	1	1	1	1	1	1	1	Mode	Mode=1: Enter extension command table Mode=0: Exit extension command table
(1) High Power Mode ON	0	0	0	1	1	0	1	0	1	1	Enter high power mode
(2) High Power Mode OFF	0	0	0	1	1	0	0	1	0	0	Exit high power mode
(3) Display Setting Mode	0	0	0	1	1	1	-	-	DSM	0	Complex command
	0	0	1	1	0	1	DT3	DT2	DT1	DT0	DSM=1: Enter display setting DSM=0: Exit display setting
	0	0	1	0	0	1	0	BA2	BA1	BA0	When DSM=1, Set
	0	0	1	0	0	1	1	FR2	FR1	FR0	duty(DT[3:0]), bias(BA[2:0]), frame rate(FR[2:0])

Note: 1. Symbol “-” means this bit can be “H” or “L”.

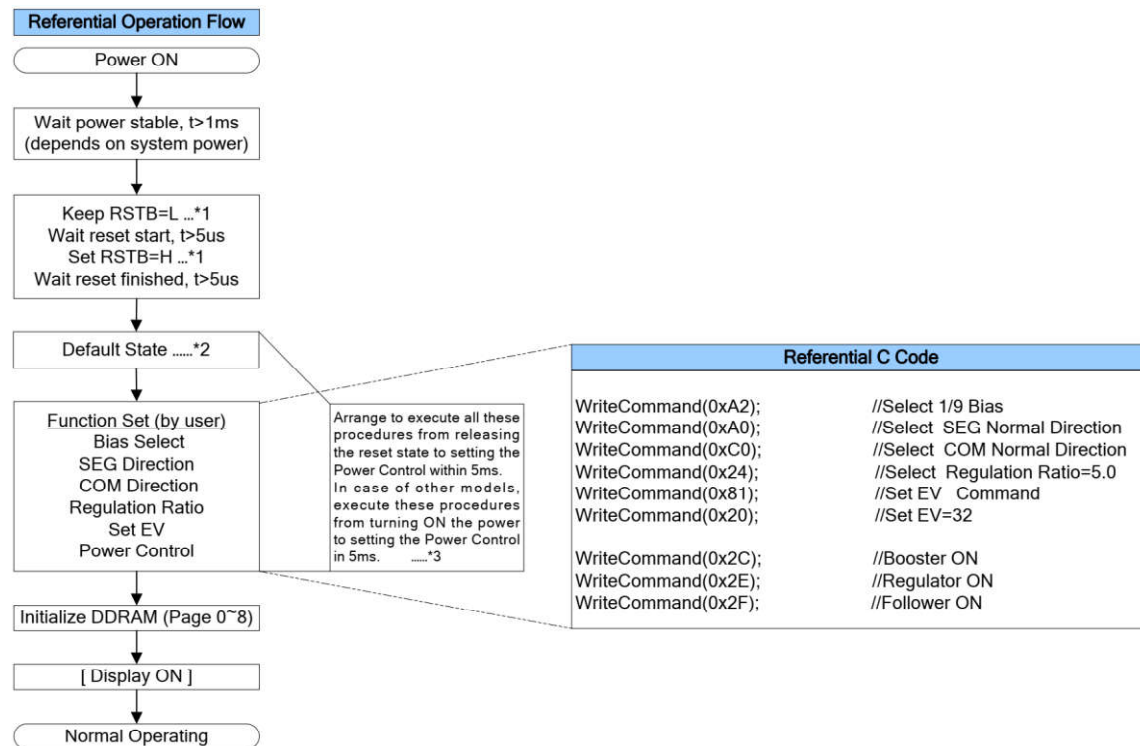
2. Do not use instructions not listed in these tables.

10. Power ON/OFF Flow and Sequence

10-1. Power ON Sequence



Power ON Operation Flow



Note: The detailed description can be found in the respective sections listed below.

1. Please refer to the timing specification of t_{RW} and t_R .
2. Refer to Section 8 Reset Circuit.
3. The 5ms requirement depends on the characteristics of LCD panel and the external component of the power circuit. It is recommended to check with the real products with external component.
4. The detailed instruction functionality is described in Section 9-2 INSTRUCTION INTRODUCTION;
5. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.

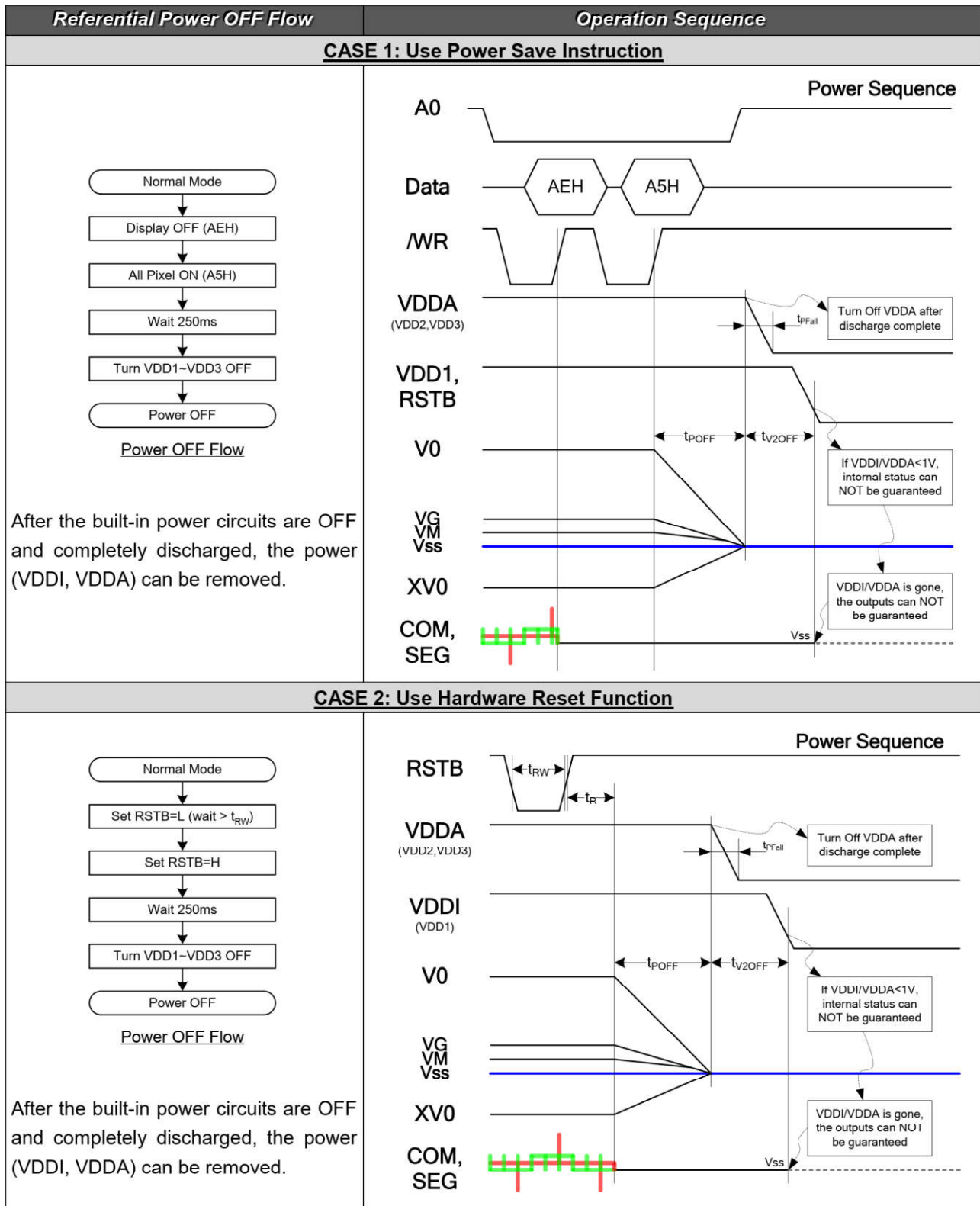
Timing Requirement:

Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-V2}	$0 \leq t_{ON-V2}$	<ul style="list-style-type: none"> Applying VDDI and VDDA in any order will not damage IC.
RSTB input time	t_{ON-RST}	No Limitation	<ul style="list-style-type: none"> If RSTB is Low, High or unstable during power ON, a successful hardware reset by RSTB is required after VDDI is stable. RSTB=L can be input at any time after power is stable. t_{RW} & t_R should match the timing specification of RSTB. To prevent abnormal display, the recommended timing is: $1\text{ms} \leq t_{ON-RST} \leq 30\text{ms}$.

- The requirement listed here is to prevent abnormal display on LCD module.

10-2. Power OFF Flow and Sequence

In power save mode, LCD outputs are fixed to VSS and all analog outputs are discharged. The power can be turned OFF after ST7567A is in the power save mode. The power save mode can be triggered by the following two methods.



Note:

1. t_{POFF} : Internal Power discharge time. \Rightarrow 250ms (max).
2. t_{V2OFF} : Period between VDDI and VDPA OFF time. \Rightarrow 0 ms (min).
3. It is NOT recommended to turn VDDI OFF before VDPA. Without VDDI, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDDI or VDPA is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.4" without capacitor.
7. When turning VDPA OFF, the falling time should follow the specification: $20\text{ms} \leq t_{Pfall} \leq 0.2\text{sec}$

11. PACKAGE

Part No.: BTG-126368-FWB-G-Bx	
Customer: XXXXXXXXXX	
<div>BARCODE</div>	
QTY: XXX	<div>BARCODE</div>
LOT NO: XXX	<div>Year/Month: XXX</div> <div>Capacity: XXX</div>
G.W: XXX	Net: XXX
<div>BARCODE</div>	
XXXXXXXXXXXX	

YB label information

試料用紙: 200000000000	資料出庫用紙: 2000000000
材料系統: BANCODE	資料出庫系統: 2000000000
材料品名: 20000000000000000000	材料品名: 200000000000
材料品類別: 20000000000000000000	材料品類別: 200000000000
單位/單位: 20000000000000000000	單位/單位: 200000000000
製造方法: 20000000000000000000	製造方法: 200000000000
材料加工: 20000000000000000000	材料加工: 200000000000
指示用紙: 20000000000000000000	指示用紙: 200000000000
Printed on 200000000000	Printed on 200000000000

"A" label information

Label specification:

YB & A label on the Sub-Carton , the position refer to the drawing.

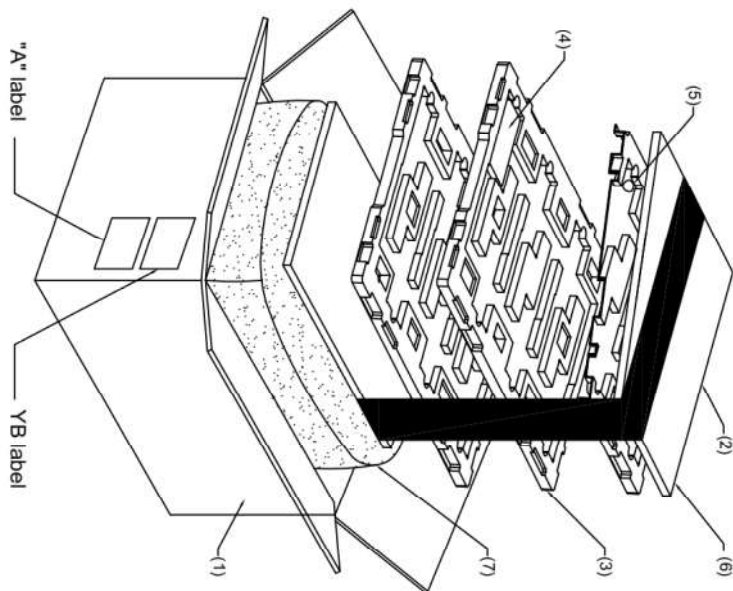
NO.	ITEM	UNIT	QTY PER	REMARK
1	SUB-CARTON	PCS	1	485*400*290
2	STRAPPING TAPE	M	3	III SHAPE
3	PSK TRAY	PCS	27	ESD 10 ⁻⁶ ~10 ⁻¹¹
4	MODULE	PCS	624	BE CAREFUL IN PUT
5	DRYER	PCS	8	
6	PEURL PAD	PCS	2	475*375*10
7	PE BAG	PCS	1	ESD 10 ⁻⁶ ~10 ⁻¹¹

Specification:

The package material can be recycling used.

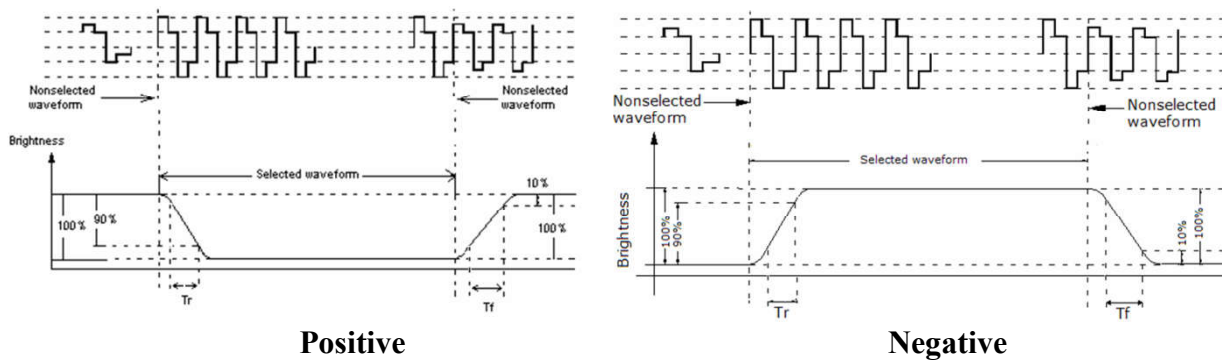
One sub-carton contains 27 layers packings. 24 modules in each PSPK tray of 26 layers. 8 packets of dryers lie put on the upper empty PSPK tray. A pearl pad is put on bottom and top side to stiffen the packings and it is adhered together with strapping tape. Load the whole product into the PE bag and seal it. Put the whole package in the sub-carton and seal the box.

One carton can contain $24 \times 26 = 624$ modules.

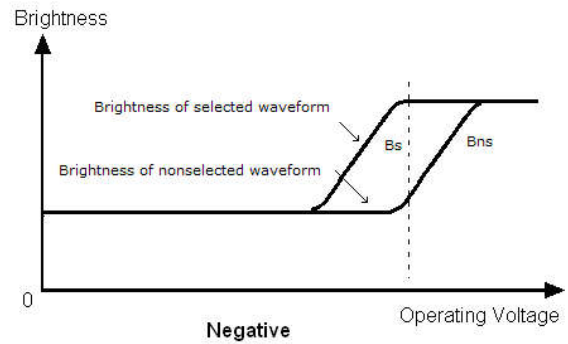
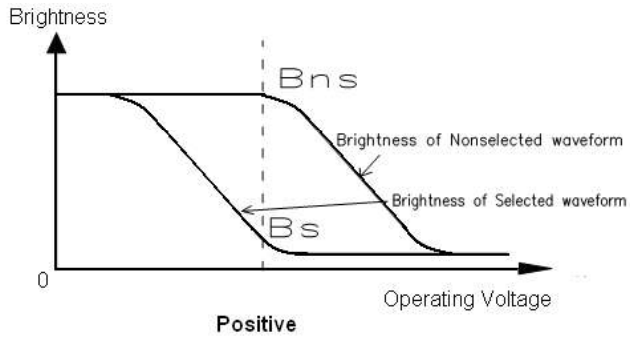


13. ELECTRO-OPTICAL CHARACTERISTICS

NO	ITEM		Symbol	Temp [°] C	Rating			Unit
					Min	Typ	Max	
1	Response time	Rise time	Tr	25	-	150	200	ms
		Fall time	Tf	25	-	200	300	
2	Operating Frequency		Fr	25	-	75	-	Hz
3	Contrast Rate		Cr	25	2	12	-	-
4	Viewing Direction		6 O'CLOCK					
5	Viewing Angle Cr \geq 2	12H ϕ =90 $^{\circ}$	$\theta 1$	25	35	45	-	Deg
		6H ϕ =270 $^{\circ}$	$\theta 2$		40	50	-	
		3H ϕ =0 $^{\circ}$	$\theta 3$		35	40	-	
		9H ϕ =180 $^{\circ}$	$\theta 4$		35	40	-	
6	Current Consumption		Is	25	-	5.7	11.4	μ A
7	Capacitance		C	25	-	2.3	-	nF

Response Time**Measuring Condition:**

1. Driving waveform: Duty, Bias selected waveform.
2. Driving Frequency: Typical value in Individual specification.
3. Operating Voltage: LCD driving voltage getting maximum contrast rate.
4. Measuring Angle: See Individual Specification.
5. Measuring Temperature: See Individual Specification.

Contrast Ratio Definition

$$\text{Contrast Ratio(Cr)} = \frac{\text{Brightness of non-selected waveform(Bns)}}{\text{Brightness of selected waveform(Bs)}}$$

Positive

$$\text{Contrast Ratio(Cr)} = \frac{\text{Brightness of selected waveform(Bs)}}{\text{Brightness of non-selected waveform(Bns)}}$$

Negative

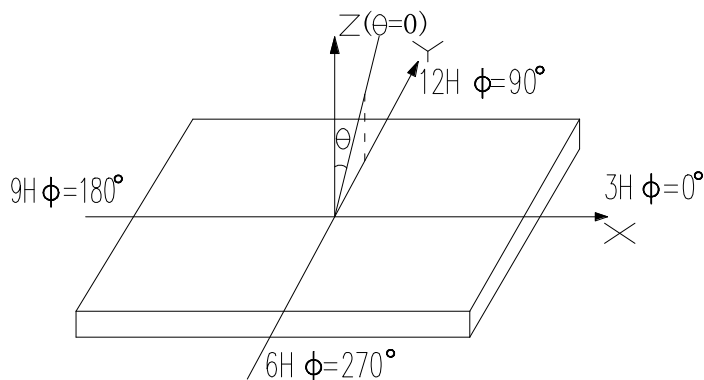
Viewing Angle

θ : Angle between Viewer Direction and Normal.

$$(-90^\circ \leq \theta \leq 90^\circ)$$

ϕ : Angle between Projection of Viewer Direction to X-Y plane and Y axis.

$$(0^\circ \leq \phi \leq 360^\circ)$$

**Measuring Condition**

1. Driving Voltage: Same as V_{LCD}
2. Driving Frequency: Same as Frame Frequency

Type	Direction	θ°	ϕ°
FSTN/STN	Any one angle	0	0
HTN/TN	6 O' Clock	20	270
	12 O' Clock	20	90
	3 O' Clock	20	0
	9 O' Clock	20	180

14. QUALITY SPECIFICATION

14-1. Specification of quality assurance

14-1-1. Purpose

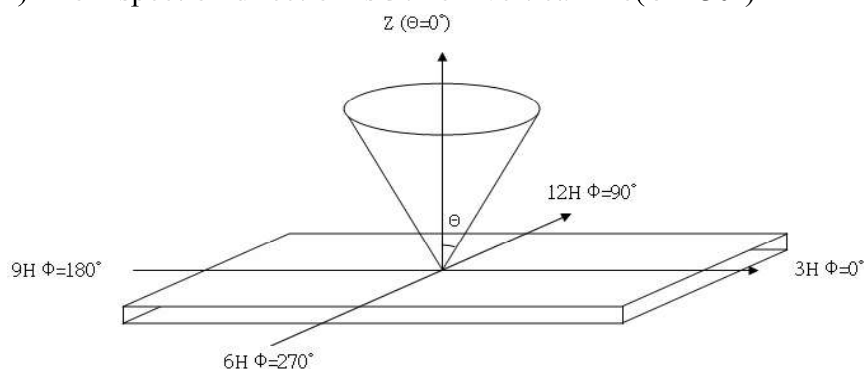
Standardize the Quality Assurance of LCD module products supply to purchaser by YEEBO CORPORATION (Supplier).

14-1-2. Type of Quality Test

- a. Inspection:
Before delivering, the supplier should take the following tests, and affirm the quality of product.
- b. Electro-Optical Characteristics:
Test the product according to the individual specification.
- c. Test of Appearance Characteristics:
Check the product according to the individual specification.
- d. Test of Reliability Characteristics:
According to the definition of reliability on the specification for testing products.
- e. Delivery Test:
The supplier should take the test for electrical performance & appearance before delivery.
(I) Test method: According to ISO 2859-1. General Inspection Level II take a single time.
(II) The defects classify of AQL as following:
Major defect: AQL = 0.65
Minor defect: AQL = 2.5
Total defects: AQL = 2.5

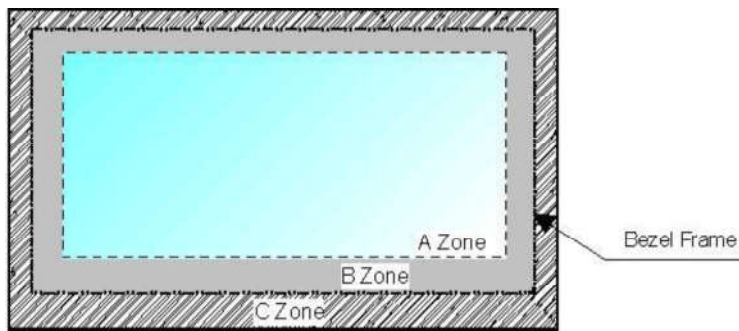
14-1-3. Standard of Product Appearance Inspection

- a. Conditions of appearance inspection :
(I) The inspection must be under 20W × 2 or 40W fluorescent light, and the distance of view must be at 30±5cm.
(II) When inspecting the model of transmissive product must add the reflective plate.
(III) The inspection direction is 30° off vertical line ($\Theta \leq 30^\circ$).



(IV) Temperature: 25±5°C Humidity: 60±10%RH

(V) Definition of Applicable Zones:



A Zone : Active display area

B Zone : Area from outside of "A Zone" to validity viewing area

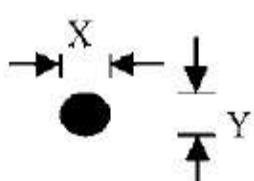
C Zone : Rest parts

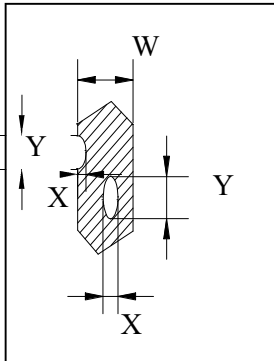
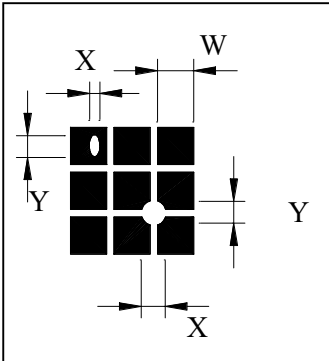
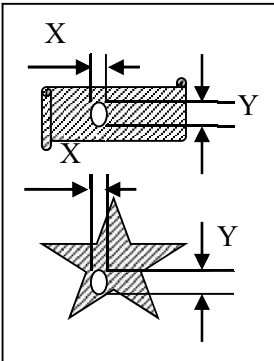
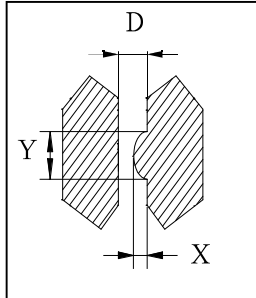
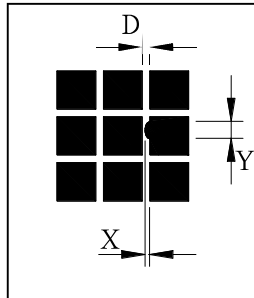
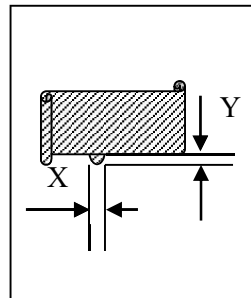
A Zone + B Zone = Validity viewing area

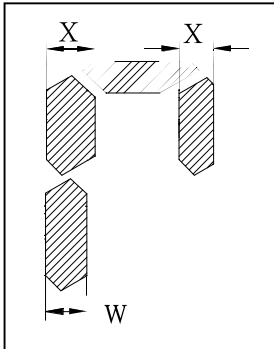
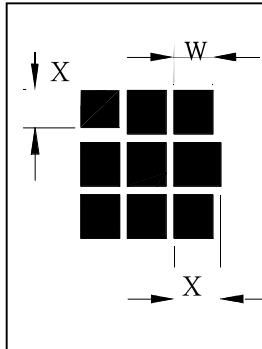
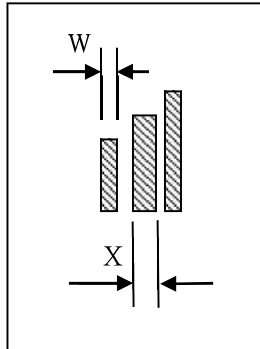
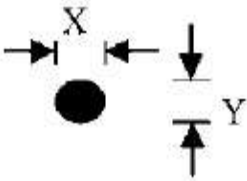
b. Unit of inspection : mm

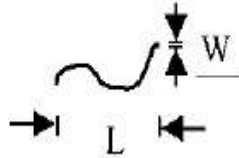
14-1-4. Defect Inspection Specification

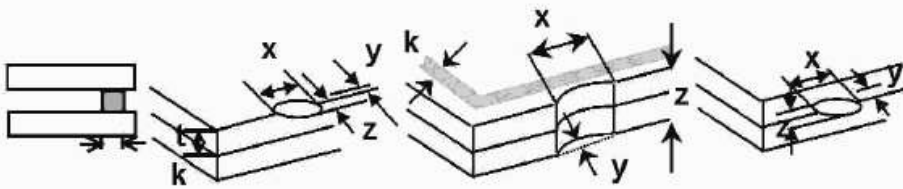
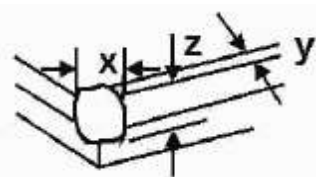
Defect out of viewing area can be neglected

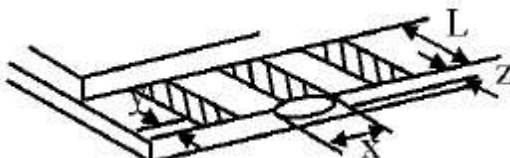
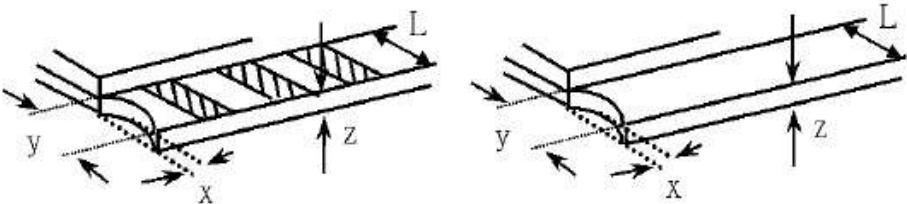
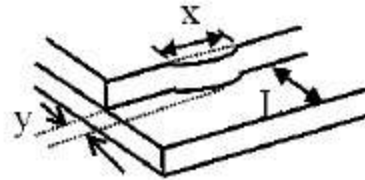
NO	Item	Criterion	AQL								
01	Electrical Testing	1.1 Missing line. 1.2 Missing character, dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 LCD viewing angle defect.	0.65								
02	Black or White spots or Bright spots or Color spots on LCD (Display “ON”)	<div> <div> $\Phi = (X+Y) / 2$  </div> <table border="1"> <thead> <tr> <th>Size(mm)</th> <th>Acceptable Q'ty</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.15$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.15 < \Phi \leq 0.3$</td> <td>5</td> </tr> <tr> <td>$0.3 < \Phi$</td> <td>0</td> </tr> </tbody> </table> </div> <div> * For “Accept no Dense”, no more than five spots within 5mm. * The distance between two defects should more than 5mm. * Spot during display switching is considered as acceptable. </div>	Size(mm)	Acceptable Q'ty	$\Phi \leq 0.15$	Accept no dense	$0.15 < \Phi \leq 0.3$	5	$0.3 < \Phi$	0	2.5
Size(mm)	Acceptable Q'ty										
$\Phi \leq 0.15$	Accept no dense										
$0.15 < \Phi \leq 0.3$	5										
$0.3 < \Phi$	0										

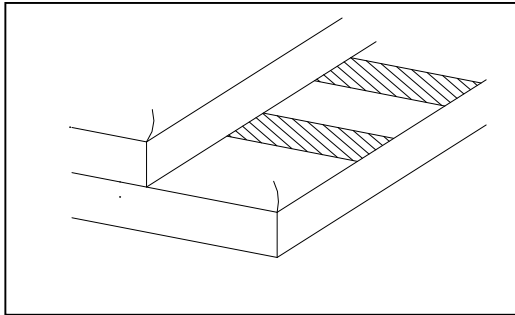
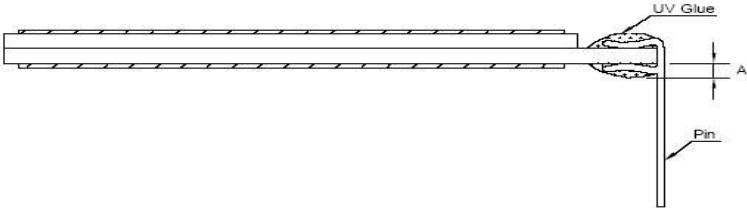
NO	Item	Criterion	AQL												
03	Pin Hole or Distortion	<div><div>3.1 Pin Hole:</div><div><div><div>Segment</div></div><div><div>Dot Matrix</div></div><div><div>Pattern</div></div></div><div>$\varnothing=(X+Y)/2$</div><table><tr><th>Wide (W)</th><th>Dimension (Ø)</th><th>Acceptable Number</th></tr><tr><td>-----</td><td>$\varnothing<0.10$</td><td>Accept no dense</td></tr><tr><td>$W\leq 0.4$</td><td>$\varnothing\leq 0.15$ and $X\leq 1/2W$</td><td>2</td></tr><tr><td>$W>0.4$</td><td>$\varnothing\leq 0.20$ and $X\leq 1/3W$</td><td>2</td></tr></table><div><div>* For “Accept no Dense”, no more than 3 spots within 5mm.</div><div>* Shall not more than 2 defects and the distance between two defects should more than 10mm.</div></div></div>	Wide (W)	Dimension (Ø)	Acceptable Number	-----	$\varnothing<0.10$	Accept no dense	$W\leq 0.4$	$\varnothing\leq 0.15$ and $X\leq 1/2W$	2	$W>0.4$	$\varnothing\leq 0.20$ and $X\leq 1/3W$	2	2.5
		Wide (W)	Dimension (Ø)	Acceptable Number											
-----	$\varnothing<0.10$	Accept no dense													
$W\leq 0.4$	$\varnothing\leq 0.15$ and $X\leq 1/2W$	2													
$W>0.4$	$\varnothing\leq 0.20$ and $X\leq 1/3W$	2													
<div><div>3.2 Distortion (Dot Shape)</div><div><div><div>Segment</div></div><div><div>Dot Matrix</div></div><div><div>Pattern</div></div></div><div><div>D: Space</div>$\varnothing=(X+Y)/2$</div><table><tr><th>Size (Ø)</th><th>Acceptable Qty</th></tr><tr><td>$\varnothing<0.10$</td><td>Disregard</td></tr><tr><td>$\varnothing\leq 0.20$ and $X\leq 1/2D$</td><td>2</td></tr><tr><td>$\varnothing>0.20$ or $X>1/2D$</td><td>0</td></tr><tr><td colspan="2">IF $Y>0.5$, follow Item 3.3-</td></tr></table></div>	Size (Ø)	Acceptable Qty	$\varnothing<0.10$	Disregard	$\varnothing\leq 0.20$ and $X\leq 1/2D$	2	$\varnothing>0.20$ or $X>1/2D$	0	IF $Y>0.5$, follow Item 3.3-		2.5				
Size (Ø)	Acceptable Qty														
$\varnothing<0.10$	Disregard														
$\varnothing\leq 0.20$ and $X\leq 1/2D$	2														
$\varnothing>0.20$ or $X>1/2D$	0														
IF $Y>0.5$, follow Item 3.3-															

NO	Item	Criterion	AQL												
03	Pin Hole or Distortion	<div>3.3 Distortion (Thick or Thin):</div> <div><div><div>Segment</div></div><div><div>Dot Matrix</div></div><div><div>Pattern</div></div></div> <table><tr><th>Wide(W)</th><th>Distortion Wide (X)</th><th>Acceptable Qty</th></tr><tr><td>-----</td><td>$X - W \leq 0.10$</td><td>Disregard</td></tr><tr><td>$W \leq 4\text{mm}$</td><td>$X - W \leq 0.20$ and $X \geq 1/2 W$</td><td>2</td></tr><tr><td>$W > 4\text{mm}$</td><td>$X - W \leq 0.30$</td><td>2</td></tr></table> <div><div>* Total defects shall not exceed 3.</div><div>* Distortion thickness cannot over 1/2 width of dot gap.</div></div>	Wide(W)	Distortion Wide (X)	Acceptable Qty	-----	$ X - W \leq 0.10$	Disregard	$W \leq 4\text{mm}$	$ X - W \leq 0.20$ and $X \geq 1/2 W$	2	$W > 4\text{mm}$	$ X - W \leq 0.30$	2	2.5
Wide(W)	Distortion Wide (X)	Acceptable Qty													
-----	$ X - W \leq 0.10$	Disregard													
$W \leq 4\text{mm}$	$ X - W \leq 0.20$ and $X \geq 1/2 W$	2													
$W > 4\text{mm}$	$ X - W \leq 0.30$	2													
04	LCD and Touch Panel black spots, white spots, contamination (Display “OFF”)	<div>4.1 Round type: As following drawing</div> <div>$\Phi = (X+Y) / 2$</div> <div></div> <table><tr><th>Size(mm)</th><th>Acceptable Q'ty</th></tr><tr><td>$\Phi \leq 0.1$</td><td>Accept no dense</td></tr><tr><td>$0.1 < \Phi \leq 0.2$</td><td>3</td></tr><tr><td>$0.2 < \Phi \leq 0.25$</td><td>2</td></tr><tr><td>$0.25 < \Phi \leq 0.35$</td><td>1</td></tr><tr><td>$0.35 < \Phi$</td><td>0</td></tr></table> <div><div>* For “Accept no Dense”, no more than five spots within 5mm.</div><div>* The distance between two defects should more than 5mm.</div><div>* Outside of the V.A. is disregard.</div></div>	Size(mm)	Acceptable Q'ty	$\Phi \leq 0.1$	Accept no dense	$0.1 < \Phi \leq 0.2$	3	$0.2 < \Phi \leq 0.25$	2	$0.25 < \Phi \leq 0.35$	1	$0.35 < \Phi$	0	2.5
Size(mm)	Acceptable Q'ty														
$\Phi \leq 0.1$	Accept no dense														
$0.1 < \Phi \leq 0.2$	3														
$0.2 < \Phi \leq 0.25$	2														
$0.25 < \Phi \leq 0.35$	1														
$0.35 < \Phi$	0														

NO	Item	Criterion	AQL															
04	LCD and Touch Panel black spots, white spots, contamination (Display “OFF”)	<div> <div> 4.2 Line type: (As following drawing) <div>  <table> <tr> <th>Length(mm)</th> <th>Width(mm)</th> <th>Acceptable Q'ty</th> </tr> <tr> <td>---</td> <td>$W \leq 0.02$</td> <td>Accept no dense</td> </tr> <tr> <td>$L \leq 3$</td> <td>$0.02 < W \leq 0.05$</td> <td>2</td> </tr> <tr> <td>$L \leq 2$</td> <td>$0.05 < W \leq 0.08$</td> <td>1</td> </tr> <tr> <td>---</td> <td>$0.08 < W$</td> <td>Rejection</td> </tr> </table> </div> <div> <p>* For “Accept no Dense”, no more than 2 lines within 5mm.</p> <p>* The distance between two defects should more than 5mm.</p> <p>* Outside of the V.A. is disregard.</p> </div> </div> </div>	Length(mm)	Width(mm)	Acceptable Q'ty	---	$W \leq 0.02$	Accept no dense	$L \leq 3$	$0.02 < W \leq 0.05$	2	$L \leq 2$	$0.05 < W \leq 0.08$	1	---	$0.08 < W$	Rejection	2.5
Length(mm)	Width(mm)	Acceptable Q'ty																
---	$W \leq 0.02$	Accept no dense																
$L \leq 3$	$0.02 < W \leq 0.05$	2																
$L \leq 2$	$0.05 < W \leq 0.08$	1																
---	$0.08 < W$	Rejection																
05	Polarizer bubbles	<table> <tr> <th>Size Φ(mm)</th> <th>Acceptable Q'ty</th> </tr> <tr> <td>$\Phi \leq 0.20$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.50$</td> <td>3</td> </tr> <tr> <td>$0.50 < \Phi \leq 1.00$</td> <td>2</td> </tr> <tr> <td>$1.00 < \Phi$</td> <td>0</td> </tr> <tr> <td>Total Q'ty</td> <td>3</td> </tr> </table> <div> <p>* For “Accept no Dense”, no more than 2 bubbles within 5mm.</p> <p>* The distance between two defects should more than 5mm.</p> <p>* Outside of the V.A. is disregard.</p> </div>	Size Φ (mm)	Acceptable Q'ty	$\Phi \leq 0.20$	Accept no dense	$0.20 < \Phi \leq 0.50$	3	$0.50 < \Phi \leq 1.00$	2	$1.00 < \Phi$	0	Total Q'ty	3	2.5			
Size Φ (mm)	Acceptable Q'ty																	
$\Phi \leq 0.20$	Accept no dense																	
$0.20 < \Phi \leq 0.50$	3																	
$0.50 < \Phi \leq 1.00$	2																	
$1.00 < \Phi$	0																	
Total Q'ty	3																	
06	Polarizer Scratches/ Puncture	Follow Item 4.	2.5															
07	Polarizer dirt	Dirt on polarizer which can be clean or blow away is acceptable.	2.5															

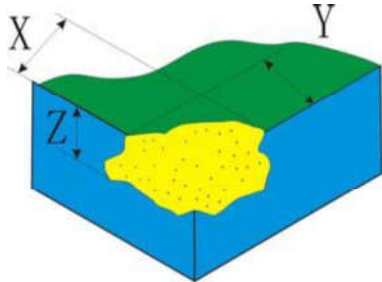
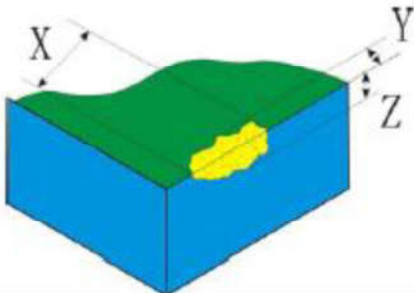
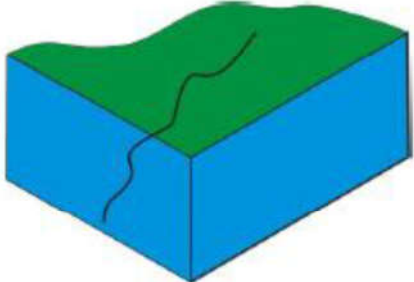
NO	Item	Criterion	AQL																		
08	Chipped glass	<p>Symbols: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length</p> <p>8.1 General glass chip:</p> <p>8.1.1 Chip on panel surface and crack between panels:</p>  <table> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td>$Z \leq 1/2t$</td> <td>Not over viewing area</td> <td>$x \leq 1/8a$</td> </tr> <tr> <td>$1/2t < z \leq 2t$</td> <td>Not exceed $1/3k$</td> <td>$x \leq 1/8a$</td> </tr> </table> <p>⊙ Unit: mm ⊙ If there are 2 or more chips, x is the total length of each chip</p> <p>8.1.2 Corner crack:</p>  <table> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td>$Z \leq 1/2t$</td> <td>Not over viewing area</td> <td>$x \leq 1/8a$</td> </tr> <tr> <td>$1/2t < z \leq 2t$</td> <td>Not exceed $1/3k$</td> <td>$x \leq 1/8a$</td> </tr> </table> <p>⊙ Unit: mm ⊙ If there are 2 or more chips, x is the total length of each chip</p>	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed $1/3k$	$x \leq 1/8a$	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$	$1/2t < z \leq 2t$	Not exceed $1/3k$	$x \leq 1/8a$	2.5
z: Chip thickness	y: Chip width	x: Chip length																			
$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$																			
$1/2t < z \leq 2t$	Not exceed $1/3k$	$x \leq 1/8a$																			
z: Chip thickness	y: Chip width	x: Chip length																			
$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$																			
$1/2t < z \leq 2t$	Not exceed $1/3k$	$x \leq 1/8a$																			

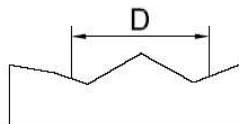
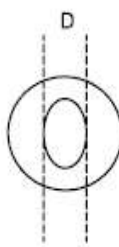
NO	Item	Criterion	AQL																
09	Glass crack	<p>Symbols: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length</p> <p>9.1 Protrusion over terminal: 9.1.1 Chip on electrode pad:</p>  <table><tr><td>y: Chip width</td><td>x: Chip length</td><td>z: Chip thickness</td></tr><tr><td>$y \leq 0.5\text{mm}$</td><td>$x \leq 1/8a$</td><td>$0 < z \leq t$</td></tr></table> <p>9.1.2 Non-conductive portion:</p>  <table><tr><td>y: Chip width</td><td>x: Chip length</td><td>z: Chip thickness</td></tr><tr><td>$y \leq L$</td><td>$x \leq 1/8a$</td><td>$0 < z \leq t$</td></tr></table> <p>⊙ If there chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.</p> <p>⊙ Heatseal alignment mark must not be damaged.</p> <p>9.1.3 Substrate protuberance and internal crack</p>  <table><tr><td>y: width</td><td>x: length</td></tr><tr><td>$y \leq 1/3L$</td><td>$X \leq a$</td></tr></table>	y: Chip width	x: Chip length	z: Chip thickness	$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$	y: Chip width	x: Chip length	z: Chip thickness	$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$	y: width	x: length	$y \leq 1/3L$	$X \leq a$	2.5
		y: Chip width	x: Chip length	z: Chip thickness															
		$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$															
		y: Chip width	x: Chip length	z: Chip thickness															
$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$																	
y: width	x: length																		
$y \leq 1/3L$	$X \leq a$																		

NO	Item	Criterion	AQL
10	Progressive crack line	 <p>10.1 Crack is crack line extend to inner edge . 10.2 Crack round epoxy frame will be rejected. 10.3 Crack on the terminal will be rejected: $Z=T$ length $>1\text{mm}$ or $Z<T$ length $>2\text{mm}$ 10.4 Crack at ITO will be rejected.</p>	2.5
11	PIN	<p>11.1 PIN slant not per specification. If the specification does not describe this item , the slant of PIN to ITO pad must $\leq 0.25\text{mm}$. 11.2 The UV glue of PIN cannot higher than upper polarizer. 11.3 The UV glue height of A shall be $\leq 2\text{mm}$</p>  <p>11.4 The terminal of PIN cannot have UV glue. 11.5 Damage of PIN such as scratch affect customer soldering. 11.6 The inclination tolerance of PIN $\leq \pm 5^\circ$ unless otherwise stated. 11.7 Pin type not according to specification sheet. 11.8 LCD pin loose or missing pins.</p>	2.5

NO	Item	Criterion	AQL														
12	Marking (Printing & Silkscreen)	<div> <div> 12.1The marking pattern different from specification. 12.2Marking colour wrong or different from colour limit sample 12.3Marking line not consistence in thickness or broken line 12.4Marking position deviated. Base on tolerance specified and unspecified tolerance base on ±0.20mm. Marking line should not overlap with display unless otherwise specified. 12.5Marking Line Width Criteria: <table> <tr> <td>W: Designed Width</td> <td>P: Actual Width</td> </tr> <tr> <td>W ≤ 0.40</td> <td> W-P ≤ 1/2W</td> </tr> <tr> <td>W>0.40</td> <td> W-P ≤ 0.2</td> </tr> </table> <div>Note: Unless otherwise specified.</div> 12.6Marking Pinhole or Distortion: <table> <tr> <td>Size</td> <td>Accepted Qty</td> </tr> <tr> <td>Ø<0.10</td> <td>Disregard</td> </tr> <tr> <td>0.10<Ø ≤ 0.20</td> <td>2</td> </tr> <tr> <td>0.20<Ø</td> <td>0</td> </tr> </table> <div>Note: The distance between two defects should be greater than 5mm</div> 12.7Marking Black spot or Scratches controlled base on inspection specification Item 4. 12.8Smear allowed: ≤ 0.20mm </div> </div>	W: Designed Width	P: Actual Width	W ≤ 0.40	W-P ≤ 1/2W	W>0.40	W-P ≤ 0.2	Size	Accepted Qty	Ø<0.10	Disregard	0.10<Ø ≤ 0.20	2	0.20<Ø	0	2.5
W: Designed Width	P: Actual Width																
W ≤ 0.40	W-P ≤ 1/2W																
W>0.40	W-P ≤ 0.2																
Size	Accepted Qty																
Ø<0.10	Disregard																
0.10<Ø ≤ 0.20	2																
0.20<Ø	0																
13	Bezel	<div> Bezel not complies with product specifications. Note: Scratch or prick which does not affect customer assembly is considered as acceptable. </div>	2.5														
14	FPC	<div> 14.1 FPC terminal damage ≤ 1/2 FPC terminal width and does not affect functional is considered acceptable. 14.2 FPC alignment hole damage ≤ 1/2 alignment area and does not affect the functional and assembly of customer are considered acceptable. 14.3 Foreign material or dirt on conductor pads which can be clean and does not affect functional is consider acceptable. </div>	2.5														

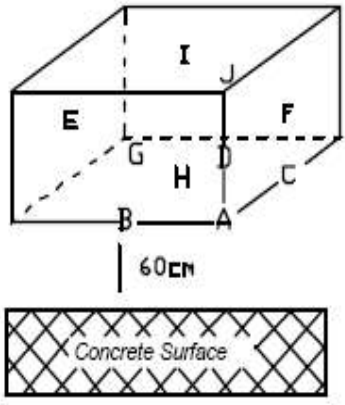
NO	Item	Criterion	AQL
15	SMT、COB	15.1 COB epoxy with pinholes larger than 0.5mm. 15.2 COB epoxy with exposed IC. 15.3 The height of the COB should not exceed the height indicated in the assembly diagram. 15.4 Epoxy encap exceed more than 3mm of the silkscreen printing 15.5 Wrong parts, missing parts or excess parts. 15.6 Jumper on the PCBA not conformed to the product characteristic chart. 15.7 PCBA cosmetic control base on latest IPC standard, IPC-A-610, acceptable limit of grade 2. 15.8 Cold solder joints, missing solder connections. 15.9 Short circuits in components on PCB or FPC. 15.10 Bezel loose assembly Note: Bend angle for bezel assembly should be within the range of 15°~60°	2.5 0.65 2.5 2.5 0.65 0.65 2.5 0.65 0.65 0.65 2.5
16	Backlight	16.1 Spots or scratches that appear when backlight on to be reviewed using Item .4 standards. 16.2 Backlight unable to light-up.	2.5
17	TAB	Oxidation on pin surface that result solderability issue Note: a) Solderability condition: 310°C±10°C, 3sec (hand solder) or 280°C±10°C, 3sec (DIP) b) Wrinkles on TAB pin but not broken is consider as acceptable.	2.5

NO	Item	Criterion	AQL
18	Touch Panel Chipped glass	<p>18.1 Chip And Crack Corner crack: $X < 3.0\text{mm}$ and $Y < 3.0\text{mm}$ and $Z < \text{GT}$ ignored 18.1.1 Corner crack in the golden finger that seriously affects the product function. 18.1.2 Corner crack in the circuit that seriously affects product function .</p>  <p>GT : Glass Thickness</p> <p>18.2 Side crack: $X < 4.0\text{mm}$ and $Y < 2.0\text{mm}$ and $Z < \text{GT}$ ignored 18.2.1 Side crack in the golden finger that seriously affects the product function. 18.2.2 Side crack in the circuit that seriously affects product function</p>  <p>18.3 Progressive crack line.</p> 	2.5

NO	Item	Criterion	AQL										
19	Touch Panel(Fish eye、dent and bubble on film)	<table> <tr> <th>SIZE(mm)</th> <th>Acceptable Qty</th> </tr> <tr> <td>$\Phi \leq 0.2$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.2 < D \leq 0.4$</td> <td>5</td> </tr> <tr> <td>$0.4 < D \leq 0.5$</td> <td>2</td> </tr> <tr> <td>$0.5 < D$</td> <td>0</td> </tr> </table> <div>   </div>	SIZE(mm)	Acceptable Qty	$\Phi \leq 0.2$	Accept no dense	$0.2 < D \leq 0.4$	5	$0.4 < D \leq 0.5$	2	$0.5 < D$	0	2.5
SIZE(mm)	Acceptable Qty												
$\Phi \leq 0.2$	Accept no dense												
$0.2 < D \leq 0.4$	5												
$0.4 < D \leq 0.5$	2												
$0.5 < D$	0												
20	Touch Panel Newton ring	Newton ring dimension < 1/2 touch panel area and affect font and line distortion(<1.5%).	2.5										
21	Touch Panel Linearity	Linearity <2.0% .	2.5										
22	General appearance	<p>22.1 Product packaging not the same as the Specification</p> <p>22.2 Product dimension and structure not conform to product specification sheet.</p> <p>Note:</p> <p>a) Wrinkles on protective tape or corner lifted $\leq 5\text{mm}$ is considered acceptable.</p> <p>b) Dirt or scratches on protective film which does not transfer to polarizer is consider as acceptable</p> <p>c) Datecode position unless otherwise specified by customer, Yeebo will decide for it.</p> <p>d) Datecode on module which is slight blur but still can be differentiated is considered as acceptable.</p>	2.5										

14.2 Standard Specification for Reliability

14.2 – 1. Standard Specifications for Reliability of LCD Module

Item	Description	
	Condition	Time (hrs)
High temp. (Storage)	70°C	240
High temp. (Operating)	60°C	240
Low temp. (Storage)	-20°C	240
Low temp. (Operating)	-10°C	240
High temp and high humidity .(Storage)	40°C/ 90%RH	240
Thermal shock (Storage)	-20°C → 20°C → 70°C → 20°C (30 min → 5 min → 30 min → 5 min)	10 cycles
Packing vibration	Frequency range : 10Hz ~ 55Hz Amplitude of vibration : 1.5mm Sweep time: 12 min X,Y,Z direction each 2 hours .	
Packing drop test	<p>To be measured after dropping from 60cm high on the concrete surface in packing state.</p> <div style="display: flex; align-items: center;">  <div style="margin-left: 20px;"> <p>Dropping method:</p> <p>Corner dropping : A Corner : once</p> <p>Edge dropping : B,C,D edge : once</p> <p>Face dropping: E, F, G, H, I, J face : once</p> </div> </div>	
Electrical Static Discharge	Air: ±6KV 150pF/330Ω 5 times Contact: ±4KV 150pF/330Ω 5 times	

*Sample size for each test is 5pcs except Packing vibration & Packing drop test.

14.2 - 2. Testing Conditions and Inspection Criteria

For the final test the testing sample must be stored at room temperature for 4 hours, after the tests listed in the above table, Standard specifications for Reliability have been executed in order to ensure stability.

No	Item	Test Model	In section Criteria
01	Current Consumption	Refer To Specification	The current consumption should conform to the product specification.
02	Contrast	Refer To Specification	After the tests have been executed, the contrast ratio must be larger than 2.
03	Appearance	Visual inspection	Defect free.
04	ESD	Function test	After reset, no abnormalities in functions.

14.2 - 3. MTBF

MTBF	Functions, performance, appearance, etc. shall be free from remarkable deterioration within 100,000 hours under ordinary operating and storage conditions room temperature ($25\pm 5^{\circ}\text{C}$), normal humidity ($50\pm 10\%$ RH), and in area not exposed to direct sun light.
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***The half life of EL backlight is 1200hours Min.**

14.3.Warranty

This product has been manufactured to specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we will not take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect arise after additional process of the product (including disassembly and reassembly), after product delivery.
2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.
4. We can not accept responsibility for industrial property , which may arise through the use of your product , with exception to those issues relating directly to the structure or method of manufacturing of our product within one year from YEEBO shipment.
5. For Heatseal Product which required to heatseal by customer side, parts must be used within three months after delivery from factory.

6. For TAB Product which required to solder by customer side, parts must be used within three months after delivery from factory.
7. The liability of YB is limited to repair or replacement on the terms set forth below. YB will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between YB and the customer, YB will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with YB GENERAL LCD INSPECTION STANDARD.

14.4 Precautions in Use of LCM

14.4-1 Handling of LCM

- Do not give external shock.
- Do not apply excessive force on the surface.
- Liquid Crystal in LCD is hazardous substance. Do not swallow it and when contact to hand, skin, cloth etc. Wash it out thoroughly and immediately.
- Do not operate it above the absolute maximum rating.
- Do not disassemble the LCM.
- The operators should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.
- The modules should be kept in antistatic bags or other containers resistant to static for storage.
- The module is coated with a film to protect the display surface. Be careful when peeling off this protective film as static electricity may be generated.

14.4-2 Storage

- Store in ambient temperature of $25\pm5^{\circ}\text{C}$, and relative humidity of $50\pm10\%\text{RH}$. Do not expose to sunlight or fluorescent light.
- Storage in a clean environment, free from dust, active gas, and solvent.
- Store in anti-static electricity container.
- Store without any physical load.
- Heat-seal must be stored at 25°C or less and 50% R.H. or less in a sealed condition, and must be used within three months after delivery from our factory.

14.4-3 Soldering

- Use only soldering irons with proper grounding and no leakage.
- Soldering: Not higher than $310\pm10^{\circ}\text{C}$ and less than 3 sec during for hand soldering.
- Resoldering: no more than 2 times.

14.5 Guarantee

Our products meet requirements of the environment.

YEEBO ROHS requirement is based on European Union Directive 2011/65/EU (ROHS) Requirements and Update.