Chapter 1 Introduction to Digital Design Methodology

- ***Language-based*** **designs:**

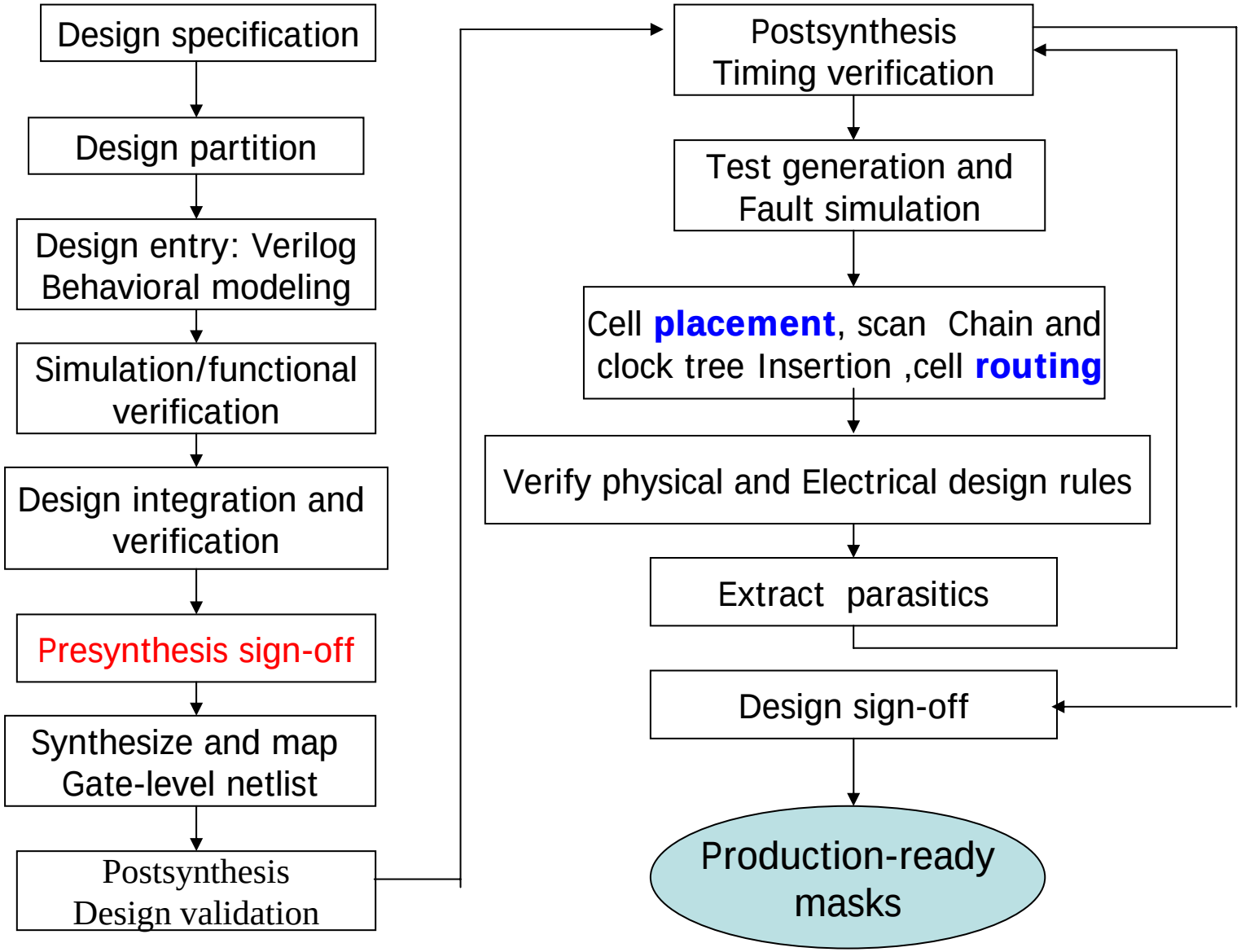
  potable and independent of technology.

- ***HDL-based*** **synthesis :**

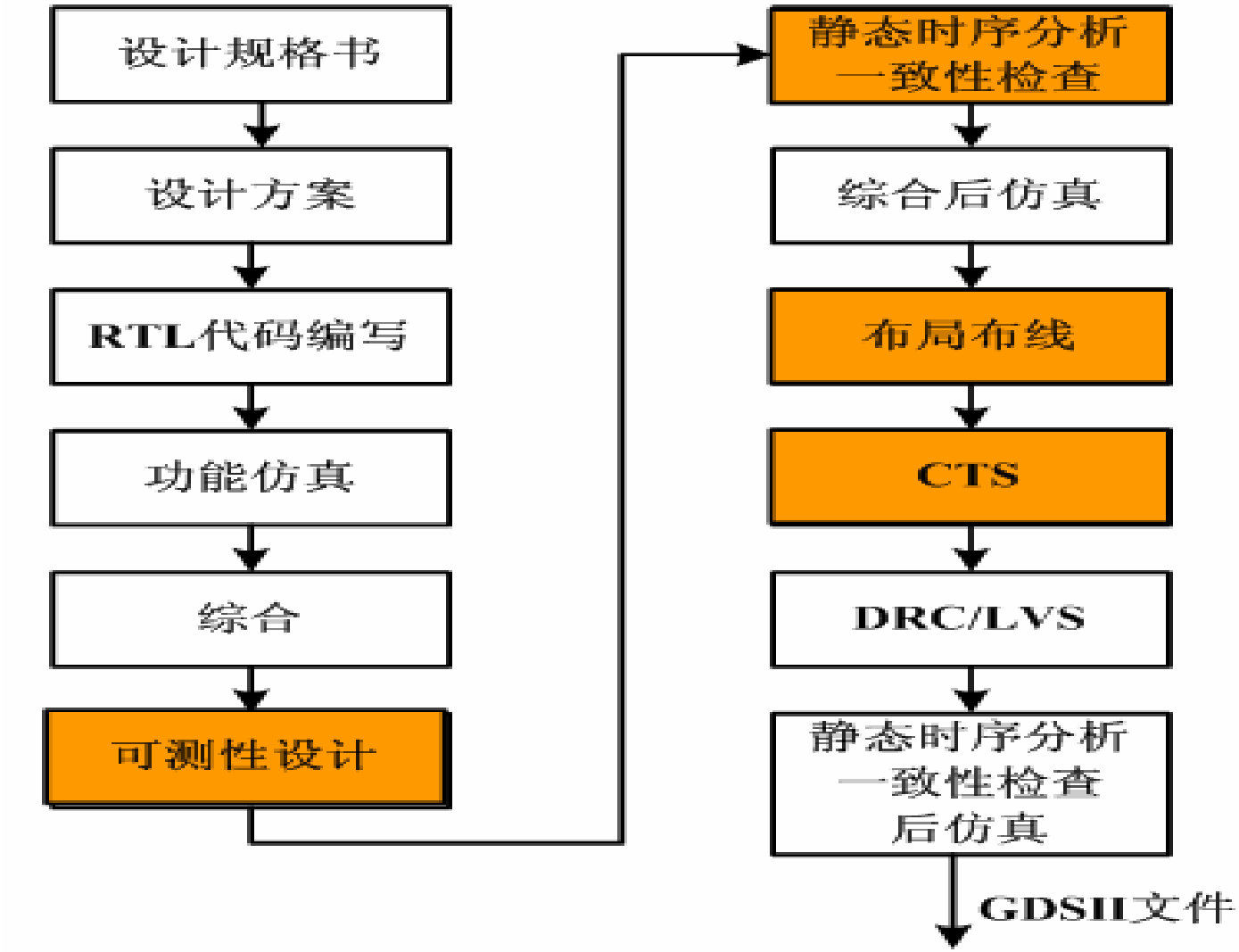
  the dominant design paradigm used by industry.

- **Two languages enjoy widespread industry support:** ***Verilog*** **,** ***VHDL***
- **System C**
- **System Verilog**

1.1 Design Methodology - An Introduction



IC Design Flow



1. Design Specification

- The specification describes the *functional characteristics* that are to be implemented in a design
- The documents include:
  - Functionality
  - Timing
  - Silicon area
  - Power consumption
  - Testability
  - Fault coverage …

2. Design Partition

- **Architecture & Design Partition**
- ***Engineering Spec., Architecture***
- *Top-down design*
- the process by which **a complex design** is progressively partitioned **into *smaller and simpler* functional units(blocks).**

3. Design Entry

- **RTL Coding & Testbench**
- *Design entry* means composing a language-based description of the design and storing it in an electronic format in a computer
- Behavioral modeling description
- Structure modeling description
- RTL modeling description

The general steps of Design Entry

(1)Create a RTL prototype of a design

(2)Verify its functionality

(3)Use a synthesis tool to optimize and map the design into a selected physical technology

4. Simulation and Function Verification

- The functionality of a design is verified either by *simulation* or by *formal methods*.

(1) Test Plan Development

(2) Testbench development

(3) Test Execution and Model Verification

5. Design Integration and Verification

- Must promise the integrated design is verified to have *correct functionality*.
- This step in the design flow is *crucial* and must be executed thoroughly **to ensure the design is correct.**

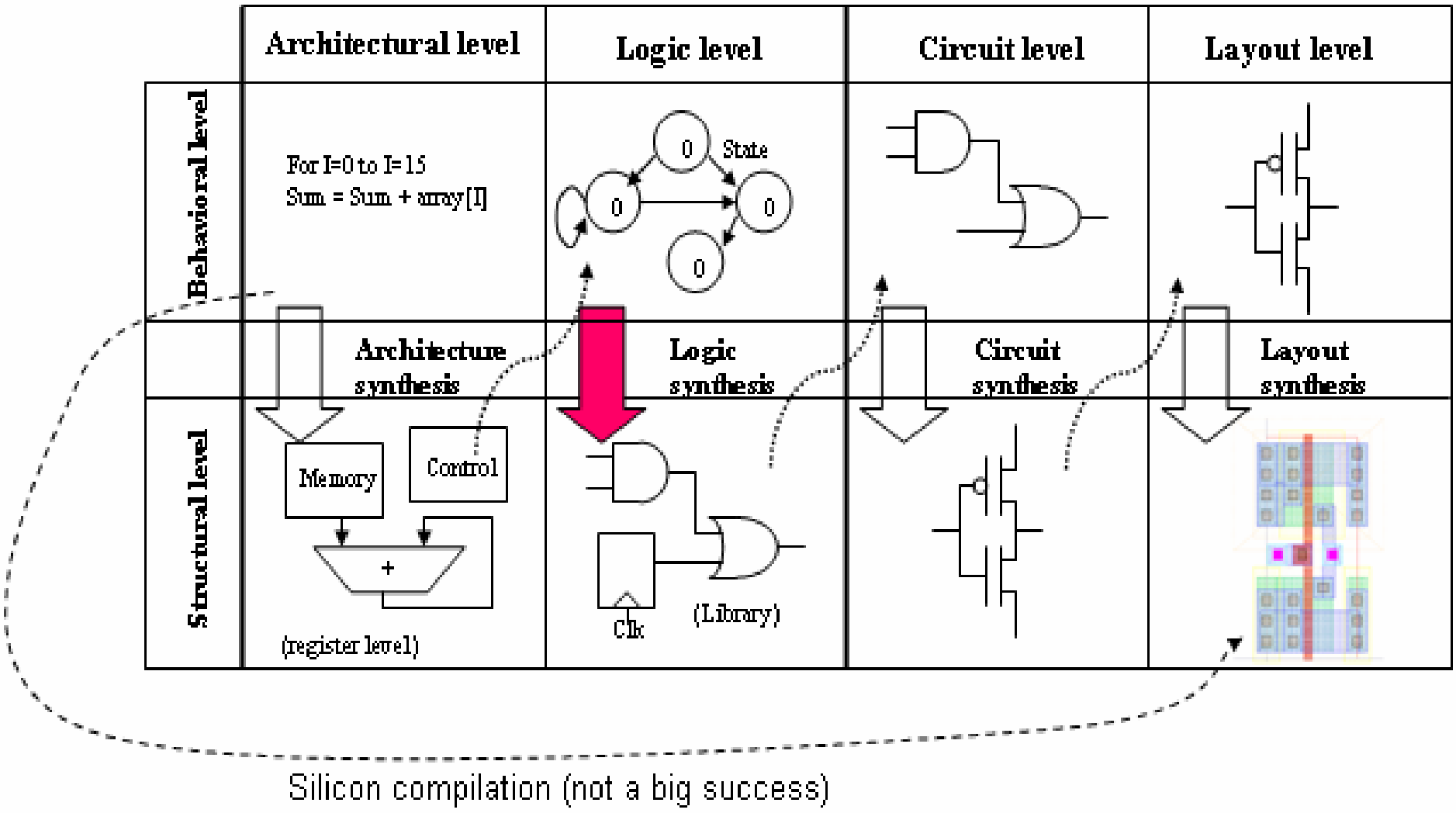
6. Presynthesis Sign-Off

- A demonstration of full functionality is to be provided by the testbench
- Any discrepancies between the functionality of the Verilog model and the design specification must be resolved
- Sign-off occurs after all known functional errors have been eliminated

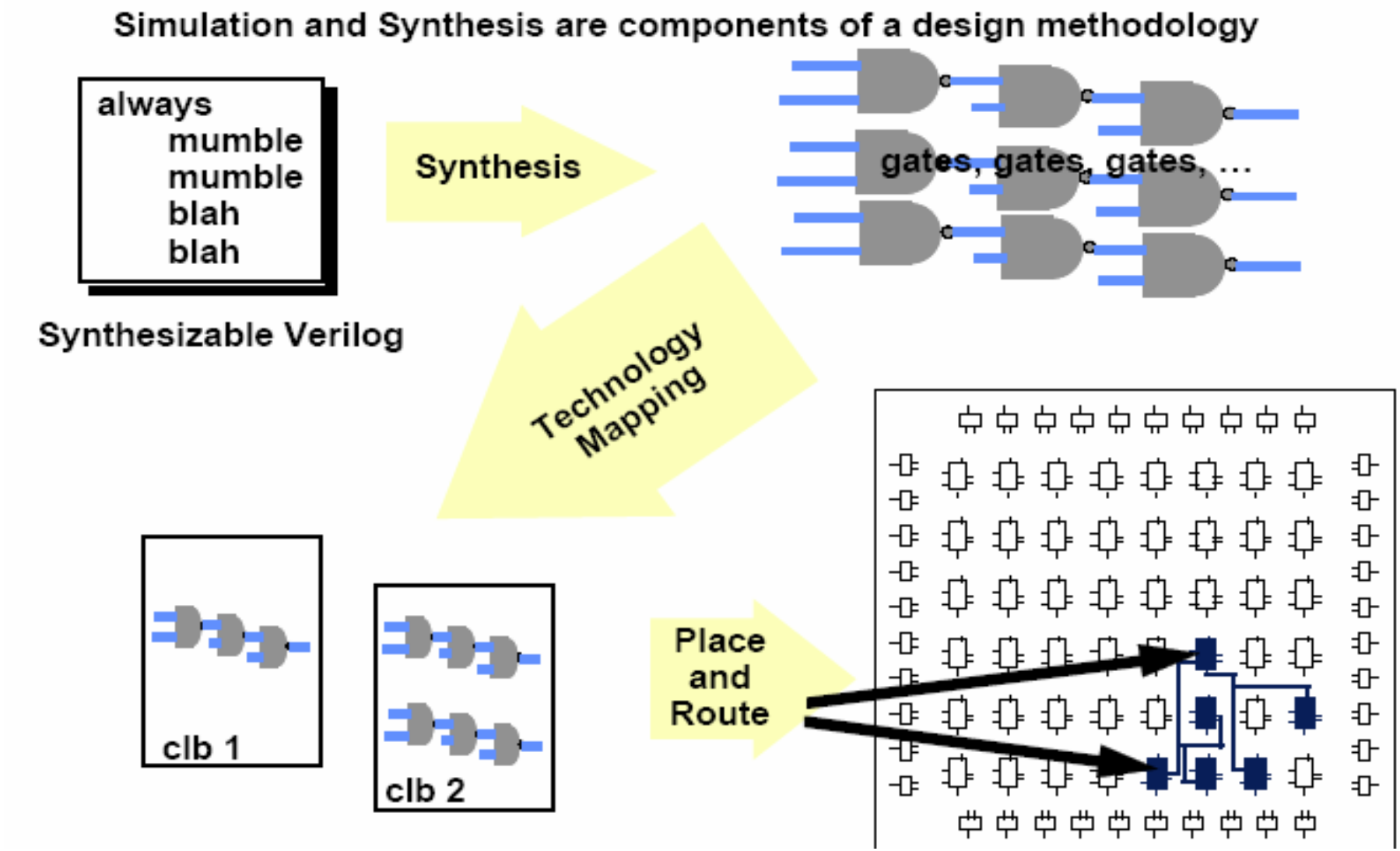
7. Gate-Level Synthesis and Technology Mapping

- A synthesis tool is used to create **an optimal Boolean description** and compose it **in an available technology**
- The synthesis tool removes redundant logic and seeks **to reduce the area** of the logic needed to implement the functionality and **satisfy performance (speed) specifications**
- This step produces a netlist of standard cells or a database that will configure a target FPGA

Abstraction levels and synthesis



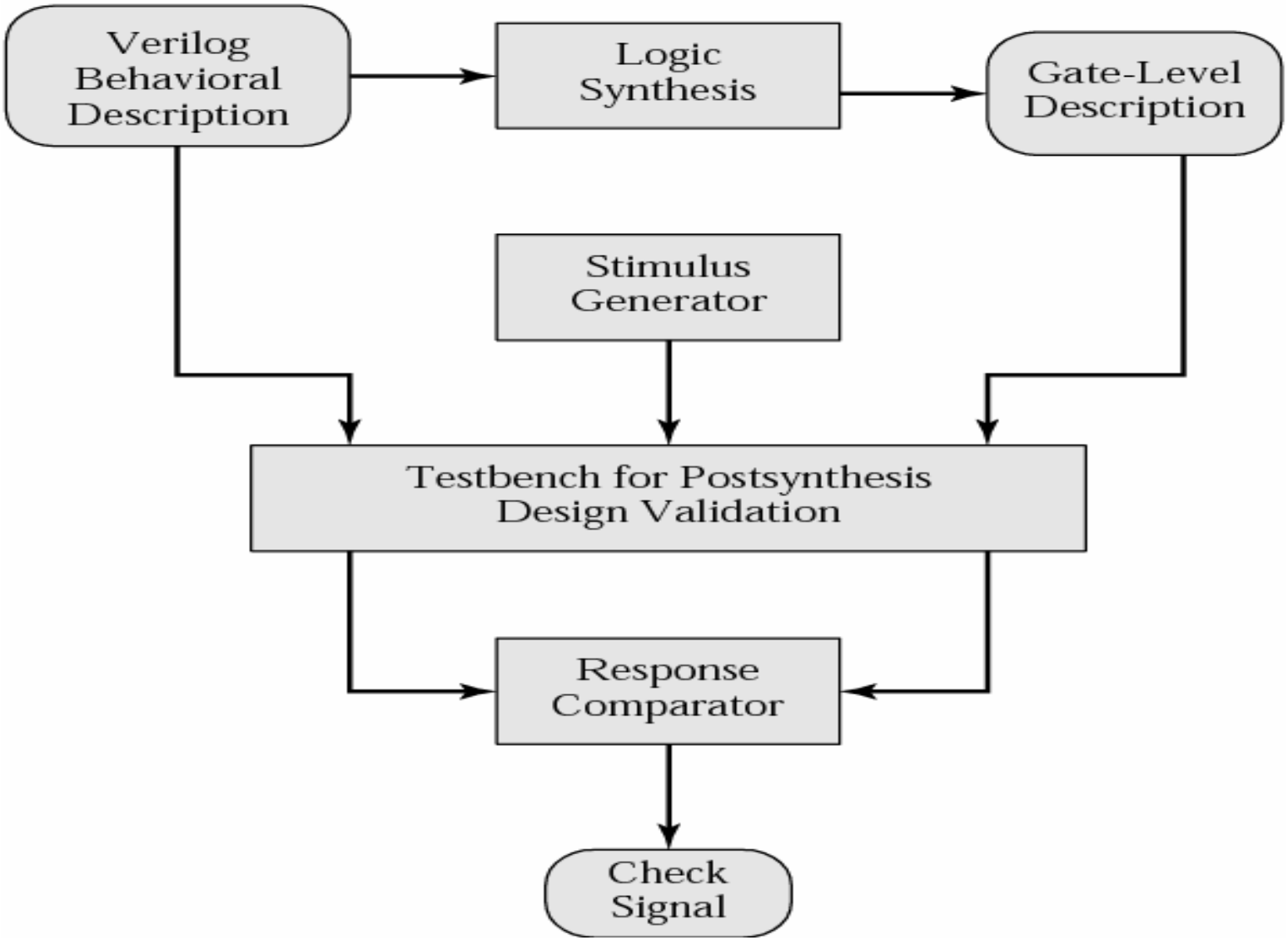
Synthesis and Technology Mapping (FPGA)



8. Post-synthesis Design Validation

- **Compares the response of the synthesized gate-level description to the response of the behavioral model**
- If the functionality and the synthesized realization do not match, **painstaking work** must be done to resolve the discrepancy

Post-synthesis Design Validation



9. Post-synthesis Timing Verification

- The synthesis tools do not accurately anticipate the effect of the capacitive delays induced by interconnect metalization in the layout
- The delays must be **extracted from the properties of the materials and the geometric details of the fabrication masks**
- Re-synthesis might require :
- (1) transistor resizing
- (2) architectural modifications/substitutions
- (3) device substitution (more speed at the cost of more area)

10. Test Generation and Fault Simulation

- To design a set of test vectors,to measured the circuit and the response of the circuit after fabrication
- **Testing considers process-induced faults, not design errors**
- Testing is daunting, for an ASIC chip might have millions of transistors, but only a few hundred package pins that can be used to probe the internal circuits
- The designer might have to embed additional, special circuits to test the entire internal circuitry of the ASIC

11. Placement and Routing

- **To arranges the cells on the die and connects their signal paths**
- In cell-based technology **the individual cells are integrated to form a global mask** that will be used to pattern the silicon wafer with gates
- **Inserting a clock tree into the layout**, to provide a skew-free distribution of the clock signal to the sequential elements of the design
- If a scan path is to be used, it will be inserted in this step too

12. Physical and Electrical Design Rule Checks

- **The physical layout** of a design must be checked
- To verify **that constraints on material widths, overlaps, and separations are satisfied**.
- **Electrical rules** are checked to verify :
- **Fanout constraints**
- **Signal integrity:**
  - **Timing ,Noise,EMI**
  - Determine whether electrical transients are problematic
- **Power dissipation** : to verify that the heat generated by the chip will not damage the circuitry

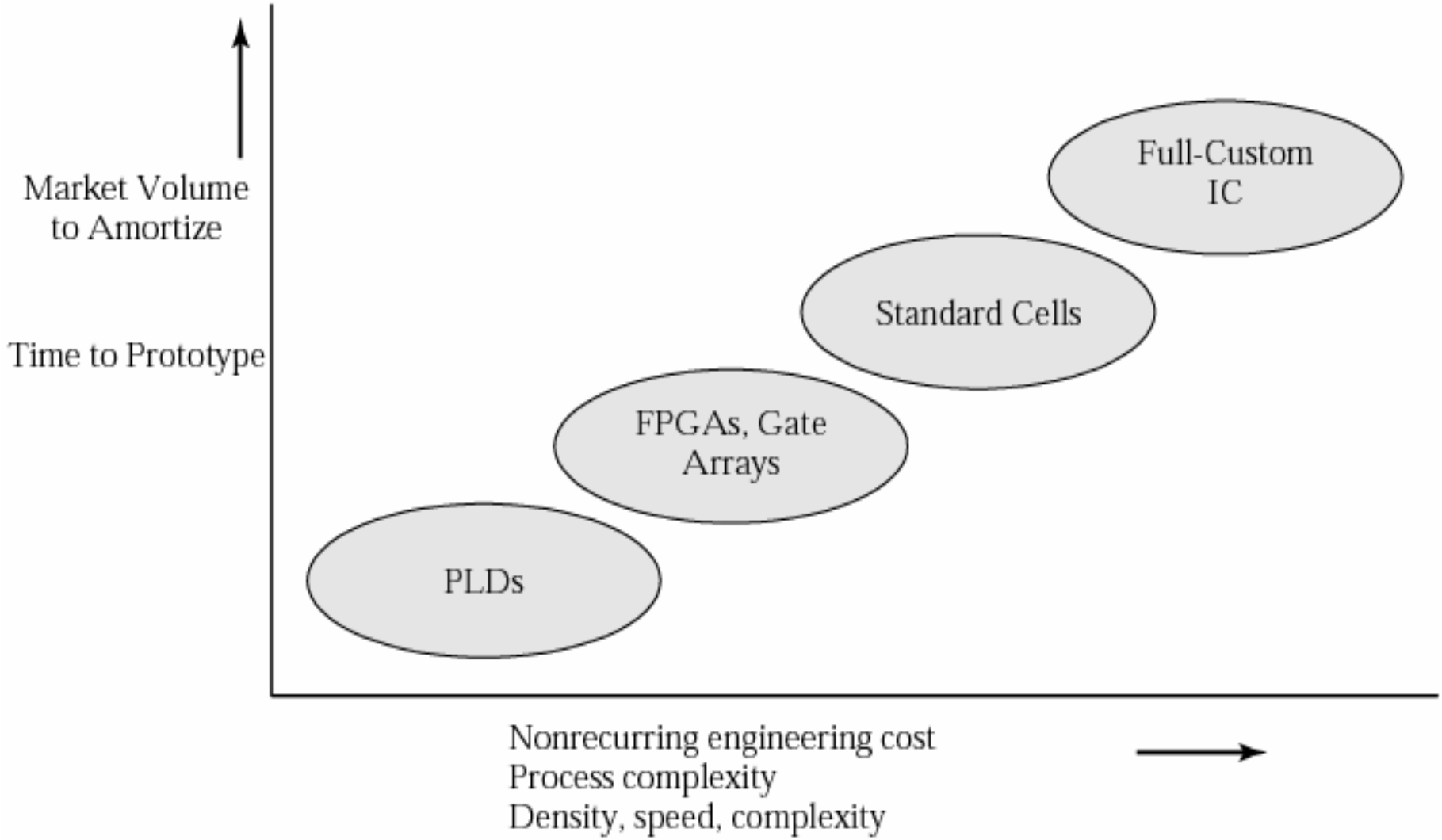
13. Parasitic Extraction

- **Parasitic capacitance** induced by the layout is extracted by a tool and then used to produce a more accurate verification of the electrical characteristics and timing performance of the design
- The results of the extraction step are used to update the loading models that are used in timing calculations
- Then **the timing constraints are checked** again to confirm that the design

14. Design Sign-Off

- Final sign-off occurs after **all of the design constraints have been satisfied and timing closure has been achieved**
- **The mask set is ready for fabrication**
- The description consists of the geometric data (usually in **GDS-II format**) that will determine the photo-masking steps of the fabrication process
- At this point significant resources have been expended to ensure that the fabricated chip will **meet the specifications for its functionality and performance**

1.2 IC Technology Options

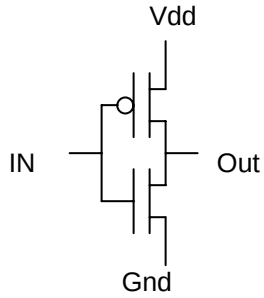


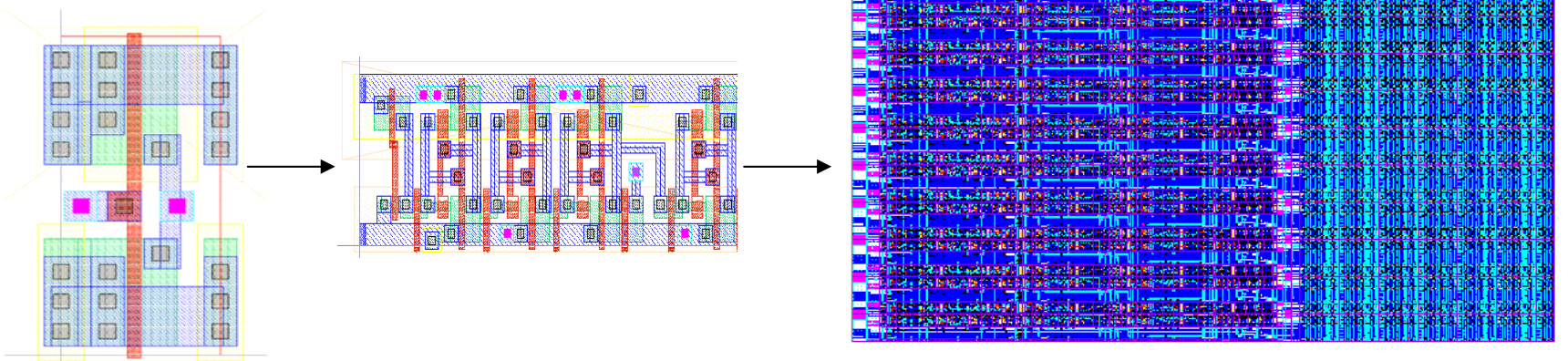
The physical database of a design might be implemented as

- **(1) a full-custom layout of high-performance circuitry**
- **(2) a configuration of standard cells, or**
- **(3) gate arrays (field- or mask-programmable**)
- **Depending on** whether the anticipated market for the ASIC **offsets the cost** of designing it, and **the required profit**

Full custom

- Hand drawn geometry
- All layers customized
- Digital and analog
- Simulation at transistor level (analog)
- High density
- High performance
- Long design time

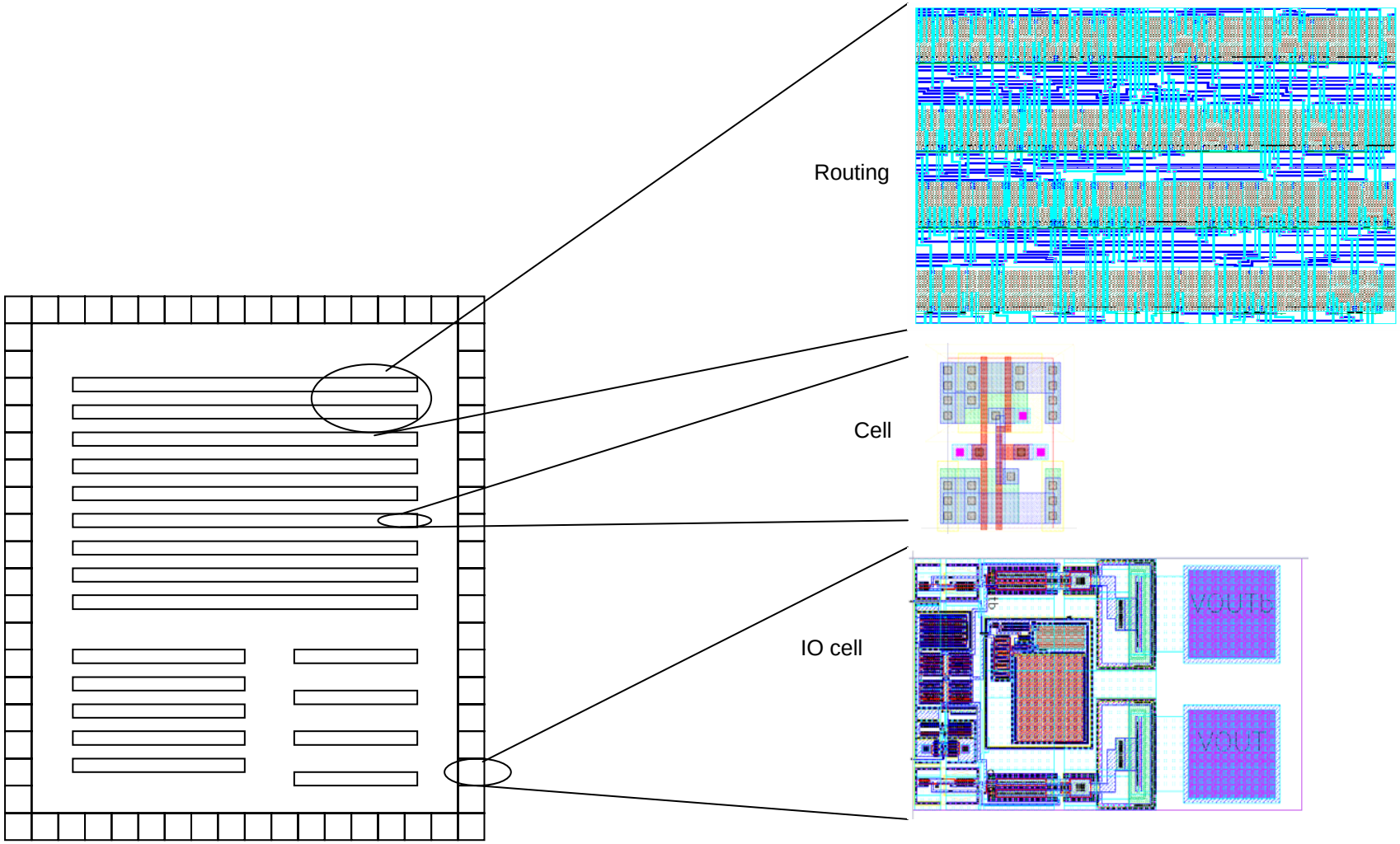




Standard cells

- Standard cells organized in rows (and, or, flip-flops,etc.)
- Cells made as full custom by vendor (not user).
- All layers customized
- Digital with possibility of special analog cells.
- Simulation at gate level (digital)
- Medium- high density
- Medium-high performance
- Reasonable design time

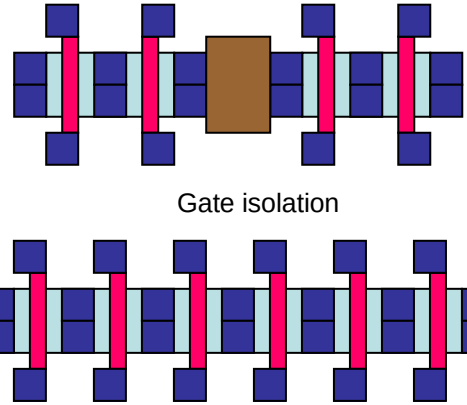
Standard cells

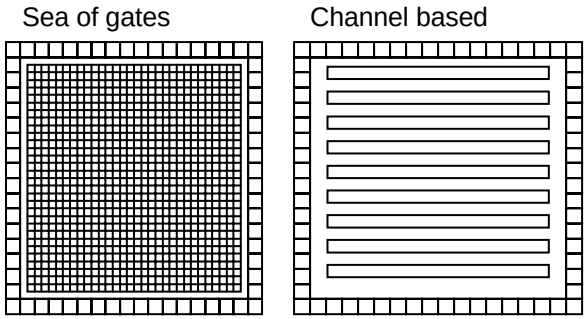


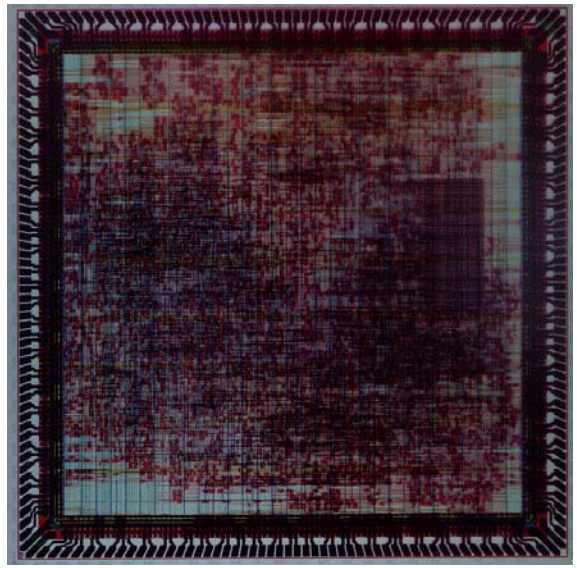
Gate-array

- Predefined transistors connected via metal
- Two types: Channel based, Sea of gates
- Only metal layers customized
- Fixed array sizes (normally 5-10 different)
- Digital cells in library (and, or, flip-flops,etc.)
- Simulation at gate level (digital)
- Medium density
- Medium performance
- Reasonable design time

Gate-array

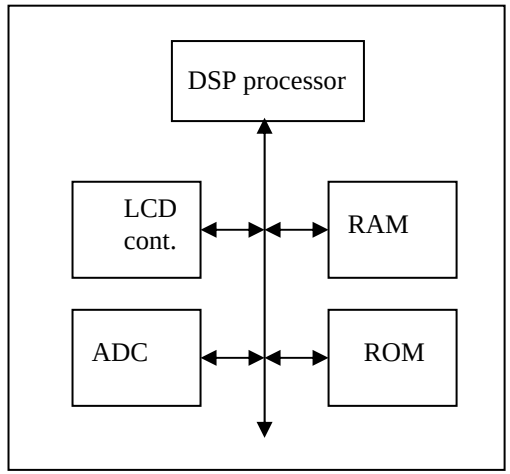






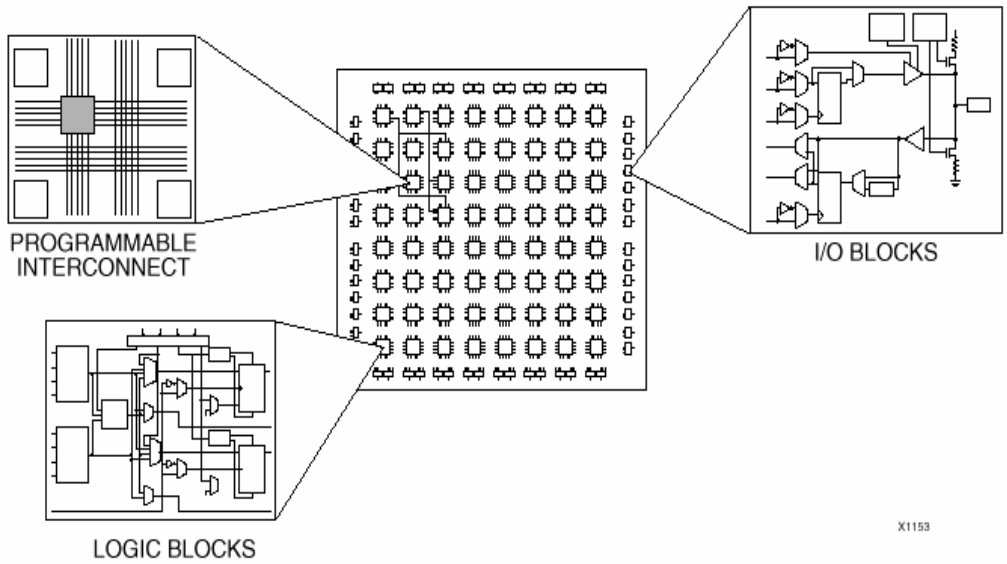
Macro cell: IP

- Predefined macro blocks (Processors, RAM,etc)
- Macro blocks made as full custom by vendor (Intellectual Property blocks = IP blocks)
- All layers customized
- Digital and some analog (ADC)
- Simulation at behavioral or gate level (digital)
- High density
- High performance
- Short design time
- Use standard on-chip busses
- “System on a chip” (SOC)



FPGA : Field Programmable Gate Array

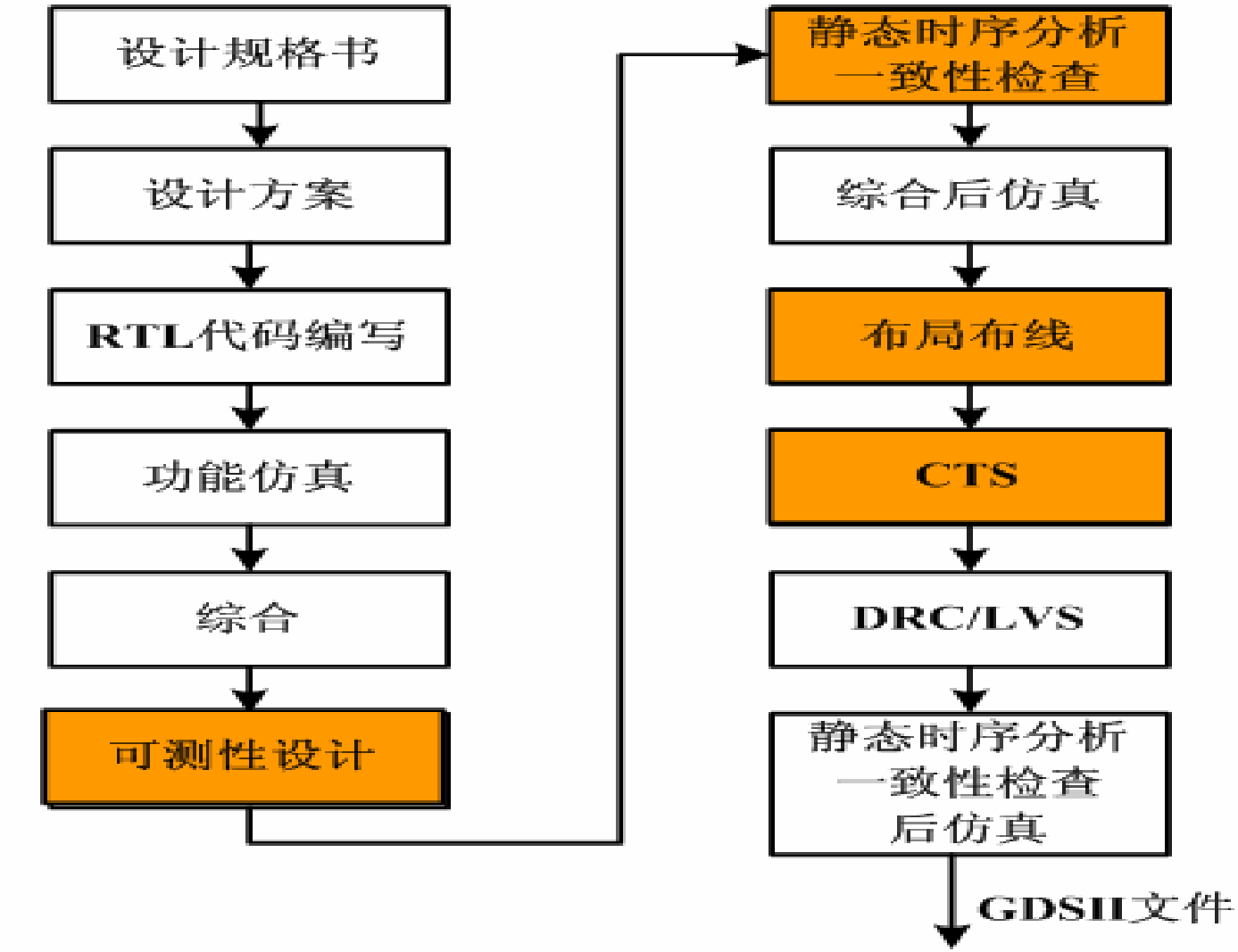
- Programmable logic blocks
- Programmable connections between logic blocks
- Digital most (analog types also exist)
- Programmable: SRAM, EEROM, Flash, Anti-fuse, etc
- Easy and quick design
- Cheap design tools
- Low development cost
- High device cost
- NOT a real ASIC



Comparison

	FPGA	Gate array	Standard cell	Full custom	Macro cell
Density	Low	Medium	Medium	High	High
Flexibility	Low (high)	Low	Medium	High	Medium
Analog	No	No	No	Yes	Yes
Performance	Low	Medium	High	Very high	Very high
Design time	Low	Medium	Medium	High	Medium
Design costs	Low	Medium	Medium	High	High
Tools	Simple	Complex	Complex	Very complex	Complex
Volume	Low	Medium	High	High	High

1.3 IC Design Example



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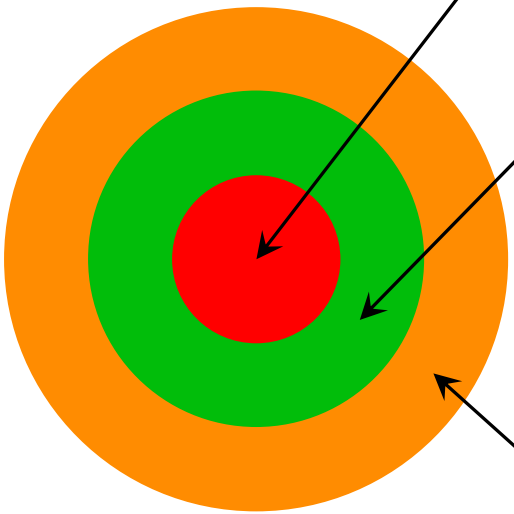

- 关键指标如最大输入采样数据率、最大处理信号带宽超过HSP50214B
- 主要功能和性能参数如无杂散动态范围、NCO频率分辨率、抽取因子、FIR阶数、采样率分数倍变换、芯片可编程能力等达到HSP50214B的水平
- 主体结构以美国Intersil公司HSP50214B数字下变频芯片作为参考

产品名称Product name	密级Confidentiality level
DDC IP	机密
产品版本Product version	Total 1 pages 共1页
V1.0	

DDC IP规格书

DDC IP SPECIFICATION

拟制: Prepared by	DDC IP TEAM		日期: Date	2006-12-20
审核教师1: Reviewed by	姓名		日期: Date	yyyy-mm-dd
审核教师2: Reviewed by	姓名		日期: Date	yyyy-mm-dd

通信IC与信号处理研究室 UESTC

Communicate IC & signal process laboratory of UESTC

修订记录Revision record

日期 Date	修订版本 Revision version	修改描述 change Description	作者 Author
2000-12-20	1.00	初稿完成 initial transmittal	

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验证、测试平台

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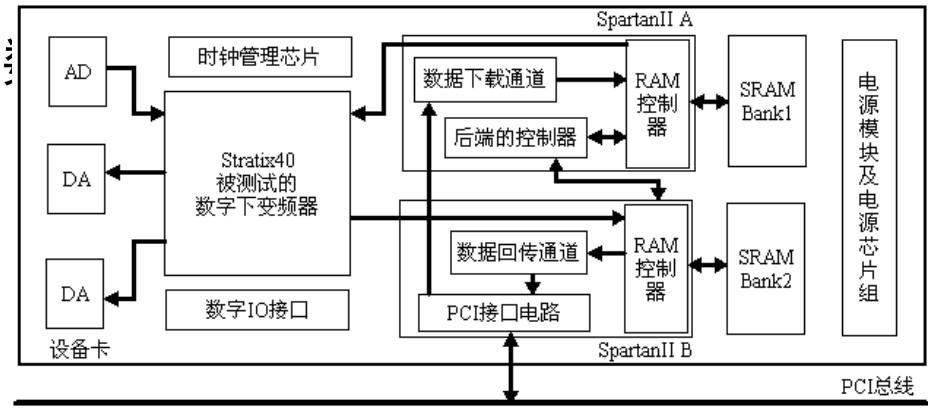
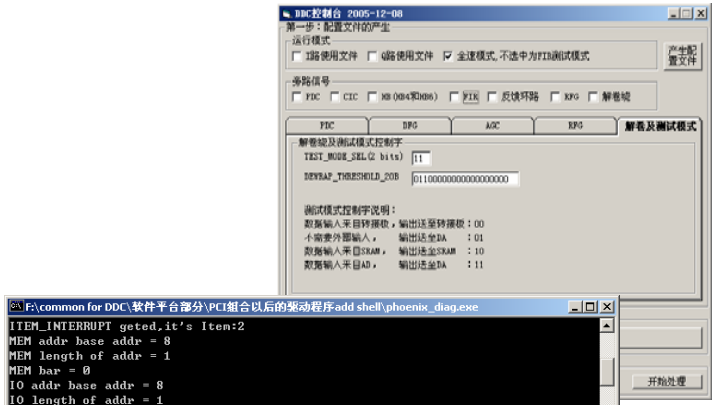
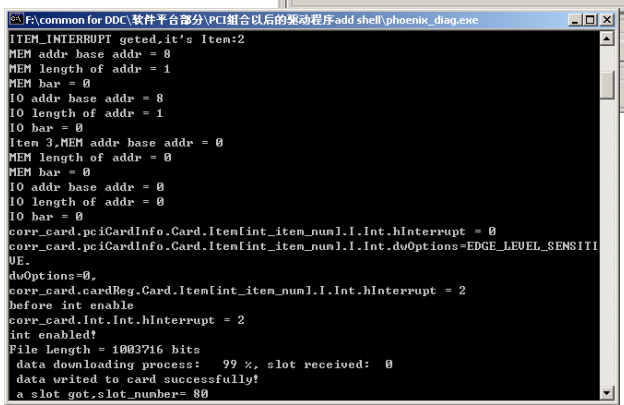
  - 三部分构成：
    - PCI接口电路
    - 数据下载通路
    - 数据回传通路



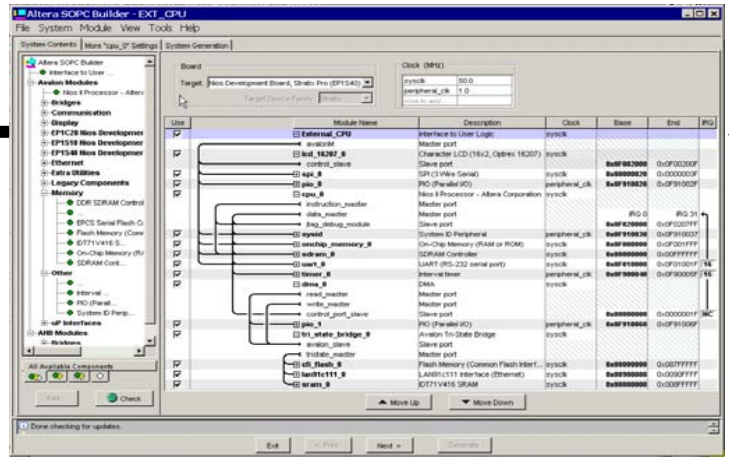
- **软件测试平台**
  - PCI接口与PC机之间的数据交互
  - VB开发的用户界面：生成电路的配置信息
  - C语言开发的驱动程序：控制PC与PCI接口的数据交互



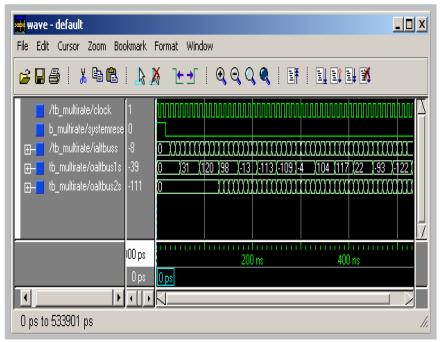


设计步骤

功能仿真



Verilog代码编写

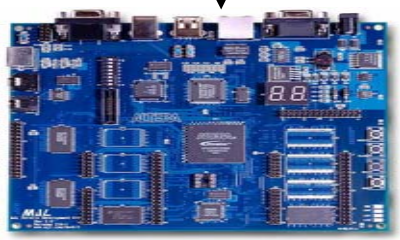


时序仿真

综合、布局布线

QUARTUS® II

FPGA配置



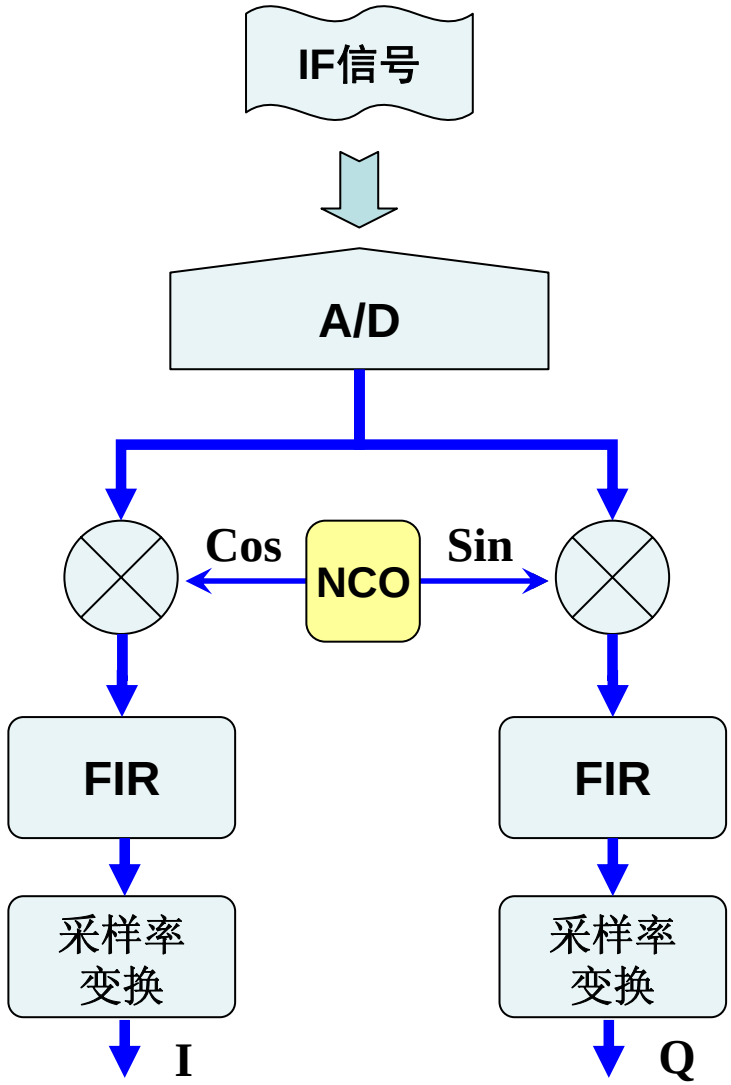
测试数据下载和回传

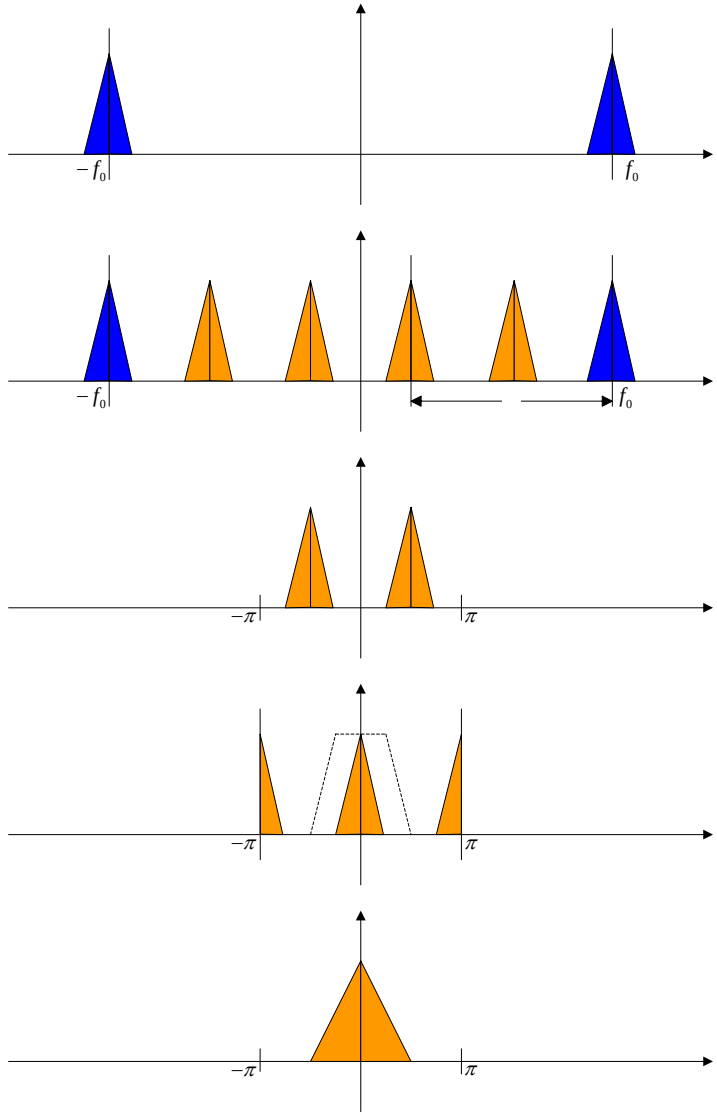
MATLAB

- **算法仿真**
- **测试激励生成**
- **测试结果分析**

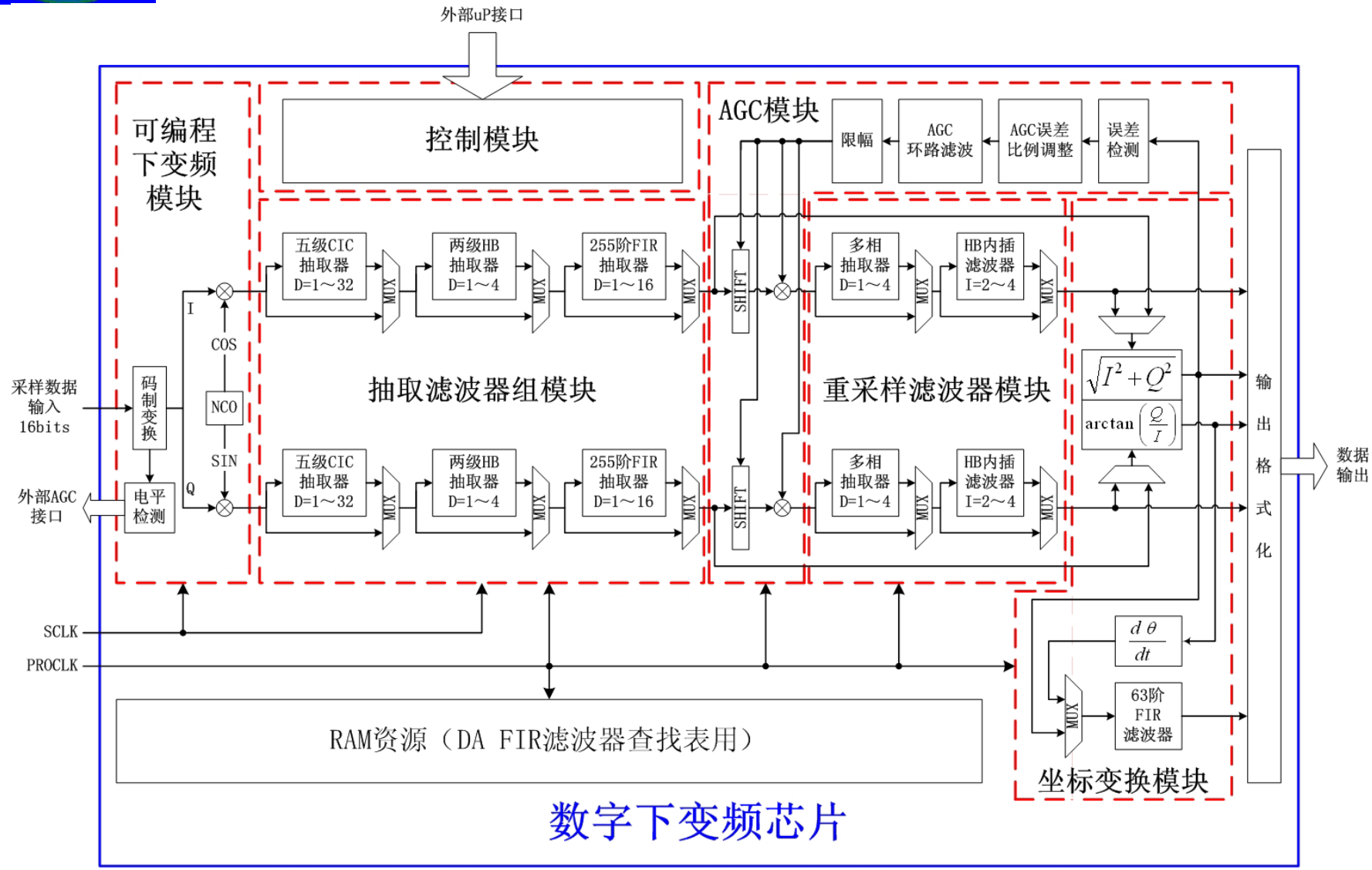
Model Technology
A MENTOR GRAPHICS COMPANY

数字下变频基本原理


IF信号
A/D
Cos
NCO
Sin
FIR
FIR
采样率
变换
采样率
变换
I
Q


$-f_0$
f_0
$-f_0$
f_0
$-\pi$
π
$-\pi$
π
$-\pi$
π

DDC系统结构框图


外部uP接口
可编程
下变频
模块
控制模块
AGC模块
限幅
AGC
环路滤波
AGC误差
比例调整
误差
检测
五级CIC
抽取器
D=1～32
两级HB
抽取器
D=1～4
255阶FIR
抽取器
D=1～16
MUX
SHIFT
多相
抽取器
D=1～4
HB内插
滤波器
I=2～4
采样数据
输入
16bits
码
制
变
换
I
COS
NCO
SIN
Q
外部AGC
接口
电平
检测
抽取滤波器组模块
重采样滤波器模块
$\sqrt{I^2+Q^2}$
$\arctan\left(\frac{Q}{I}\right)$
输
出
格
式
化
数据
输出
SCLK
PROCLK
RAM资源（DA FIR滤波器查找表用）
$\frac{d\theta}{dt}$
63阶
FIR
滤波器
坐标变换模块
数字下变频芯片

主要算法及其实现

- CORDIC 算 法 *(COordinate Rotation DIgital Compute)*
- CIC滤波器 *（Cascaded Integrator Comb ）*
- HB滤波器 *（Half-Band）*
- DA-FIR *（Distributed Arithmatic）*
- 分数倍重采样滤波器
- AGC

CIC模块算法设计

CIC滤波器原理

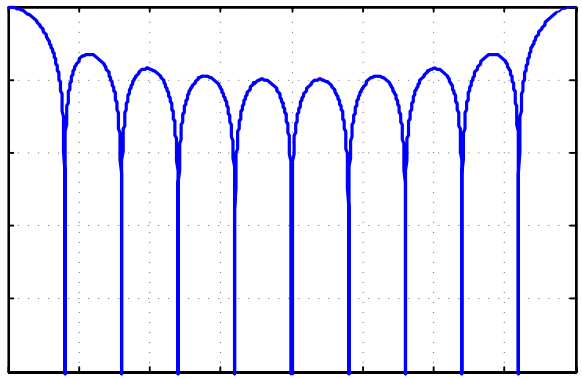
$$h(n)=\begin{cases}1, & 0\le n\le D-1\\ 0, & \text{其他}\end{cases}$$

$$H(e^{j\omega})=\frac{1}{1-e^{-j\omega}}\cdot(1-e^{-j\omega D})$$

$$=\frac{\sin\left(\frac{\omega D}{2}\right)}{\sin\left(\frac{\omega}{2}\right)}$$

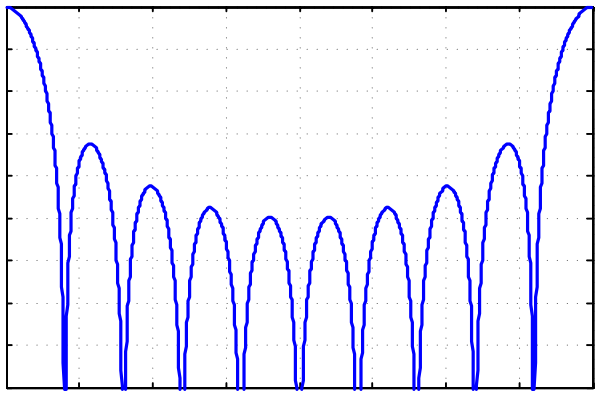
$$=D\cdot Sa\left(\frac{\omega D}{2}\right)\cdot Sa^{-1}\left(\frac{\omega}{2}\right)$$

单级CIC



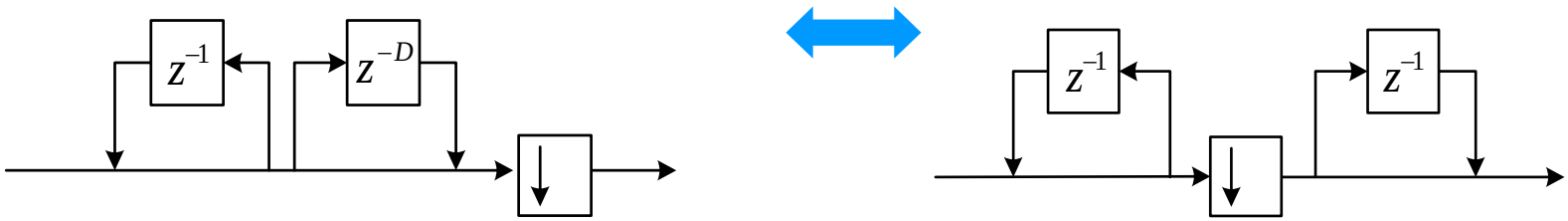
$$H_Q(e^{j\omega})=D^Q\cdot Sa^Q\left(\frac{\omega D}{2}\right)\cdot Sa^{-Q}\left(\frac{\omega}{2}\right)$$

5级CIC

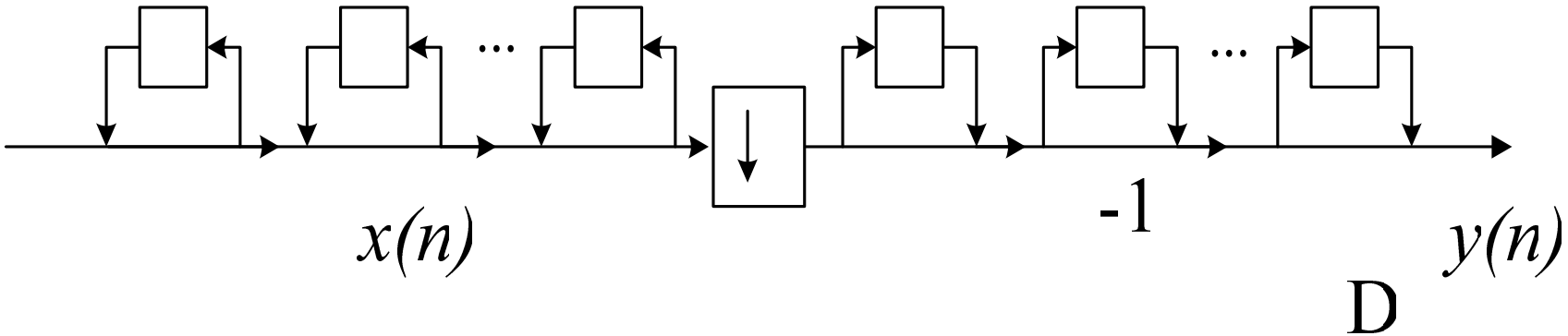


CIC滤波器结构

- 单级CIC滤波器等效结构

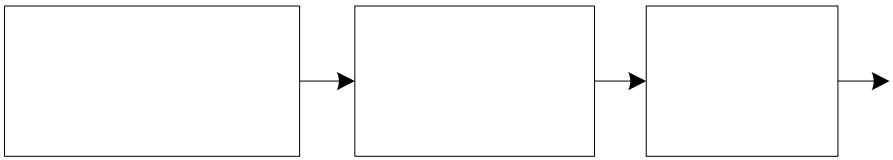


- 5级CIC滤波器结构



CIC模块设计

- 输入数据的位宽扩展
  - 避免由滤波器处理增益造成输出数据溢出
  - 当*D*较小时滤波器输出的有效位数少



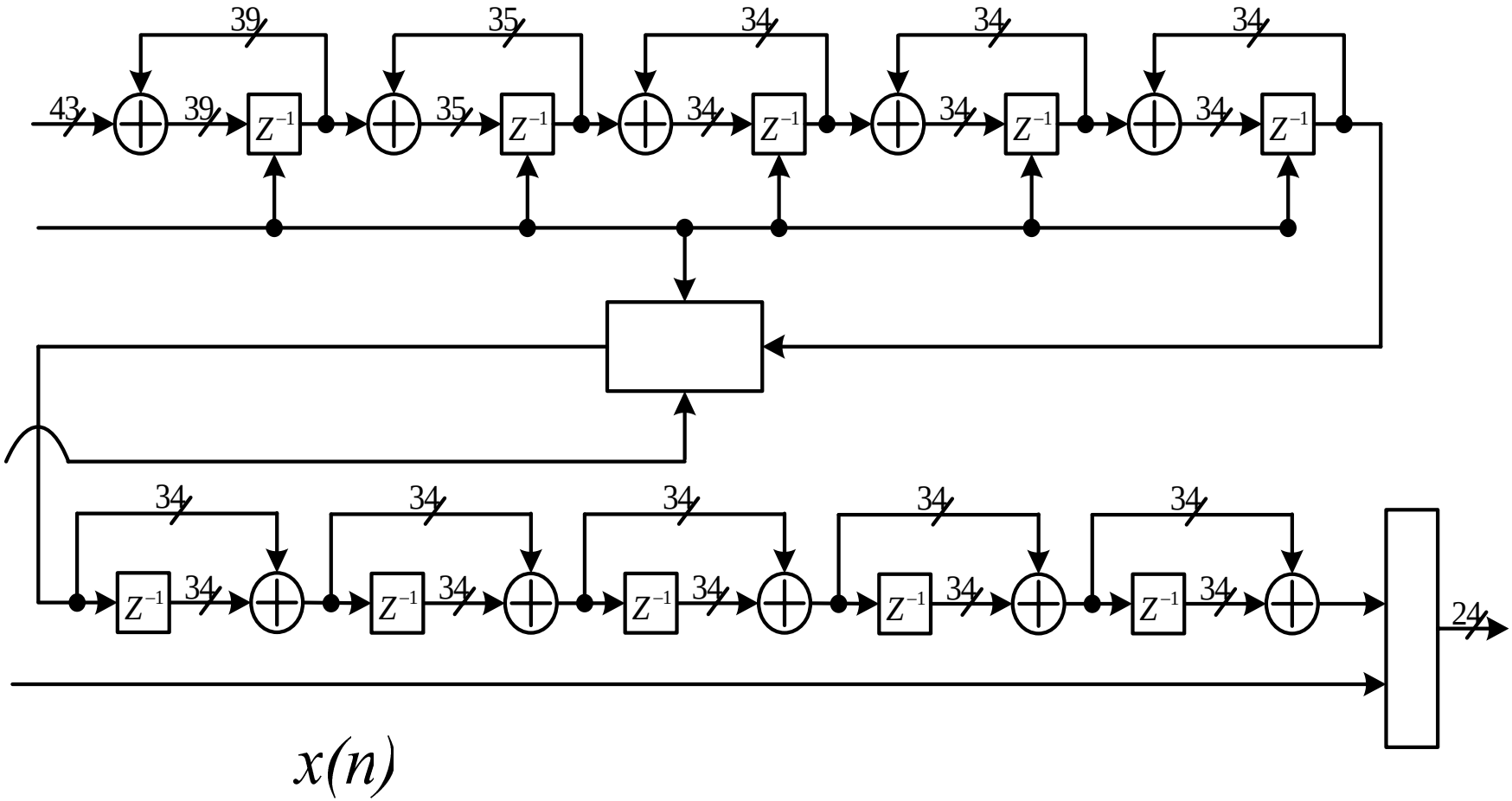
  - 移位值：$SN=fix[25-\log_2(D^5)]$
- 时钟域变换
  - 抽取滤波后进行
  - 两个数据穿越了时钟域：
    - CIC滤波器抽取后数据：打两拍传递
    - CIC滤波器抽取指示信号：特殊策略

可编程下变频　　桶型

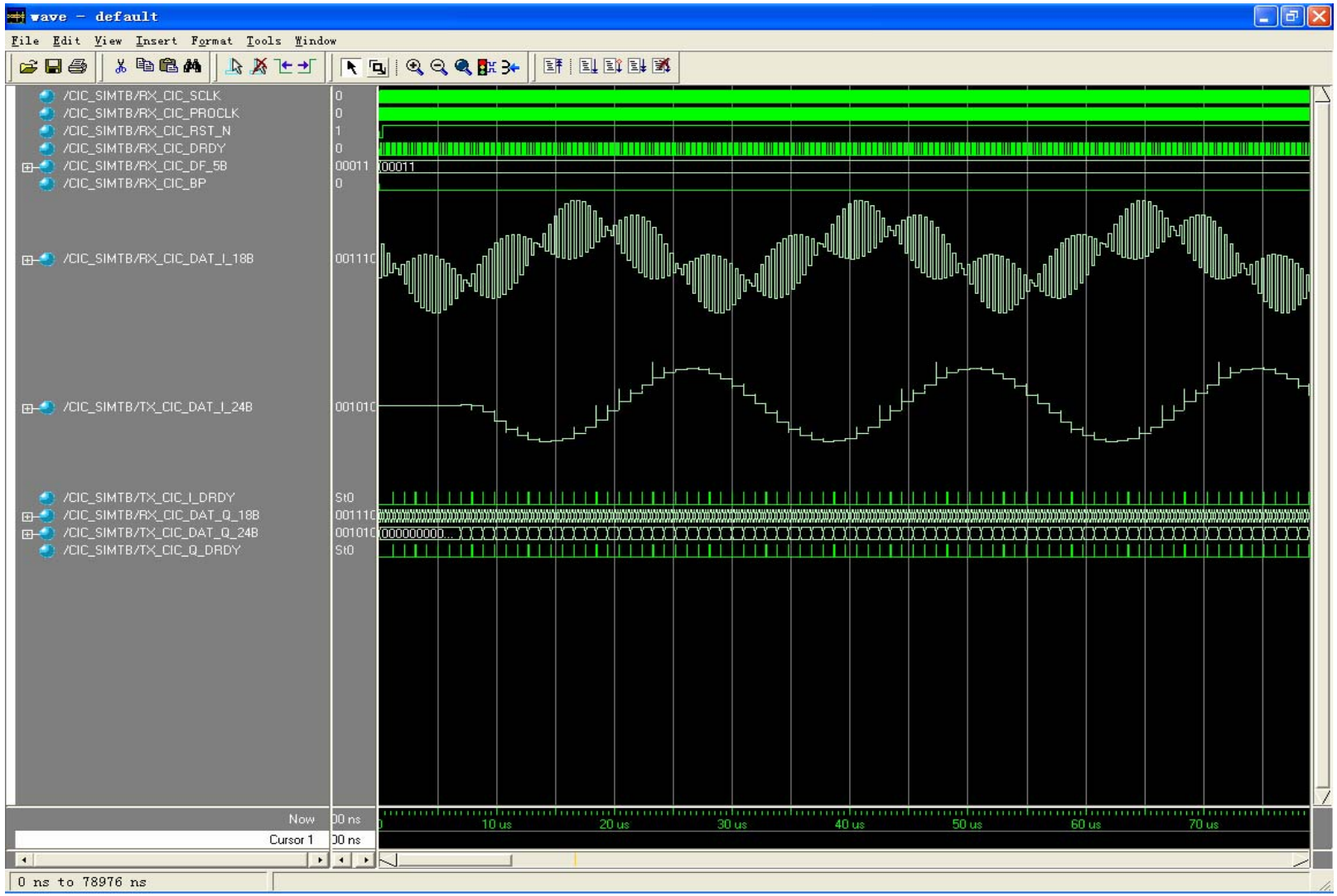
模块　　在

CIC模块RTL实现与仿真

CIC模块实现框图



CIC模块仿真波形（Modelsim)



DDC验证评估板

NCO模块（混频功能）硬件测试

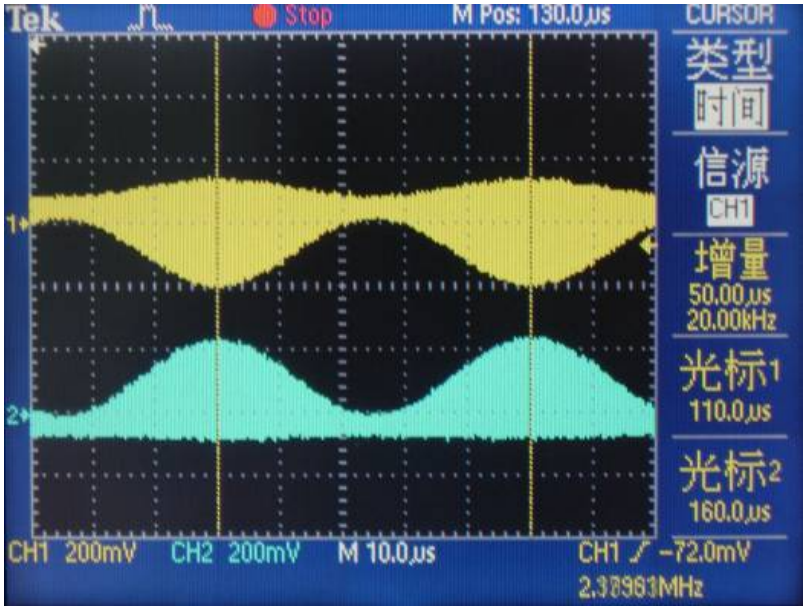
测试参数配置：

■输入信号：AM信号，f_C＝2.5MHz；

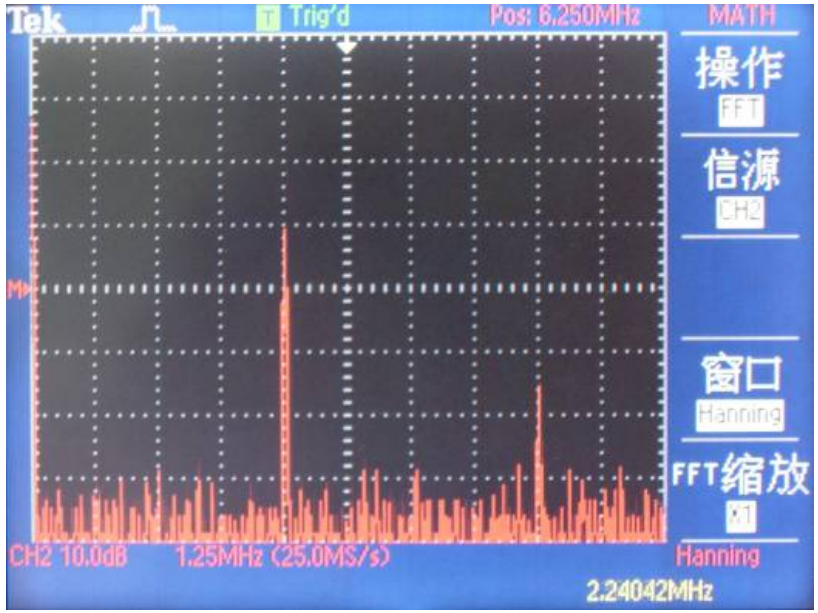
■调制信号：20kHz正弦；调制系数：80％；

■NCO输入采样频率：f_S＝80MHz；

■NCO本振频率：f_{NCO}＝f_C＝2.5MHz



AM信号混频后时域波形



AM信号混频后频谱

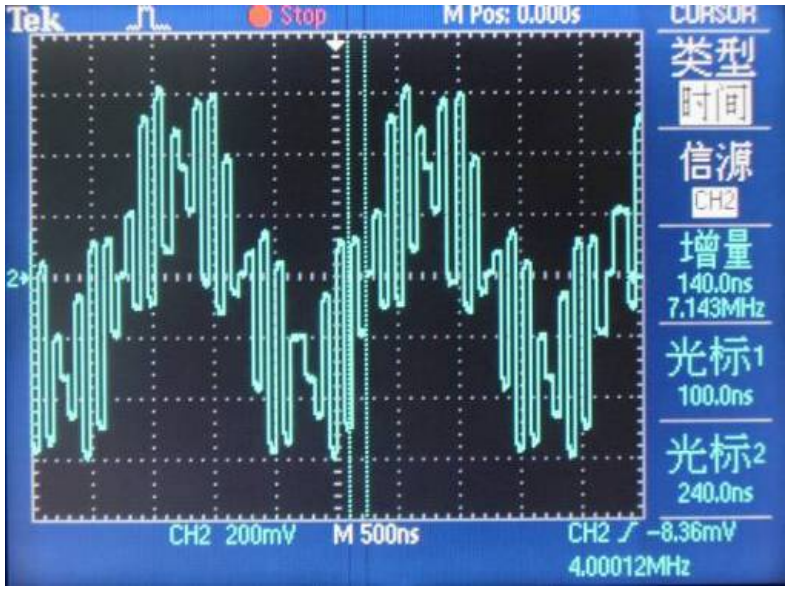
CIC模块硬件测试

测试参数配置：

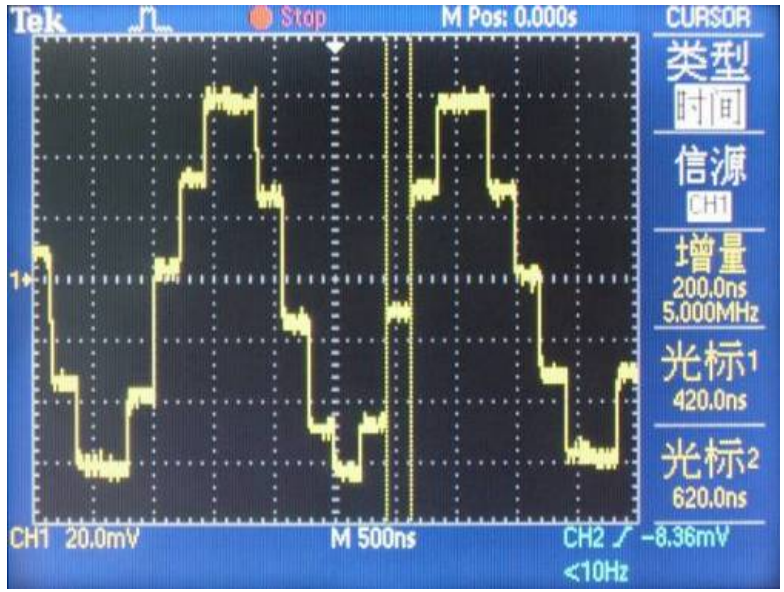
■输入信号：500kHz正弦＋7MHz正弦；

■CIC输入采样频率： f_S＝80MHz ；

■CIC抽取因子：D=16



CIC模块输入波形



CIC模块输出波形

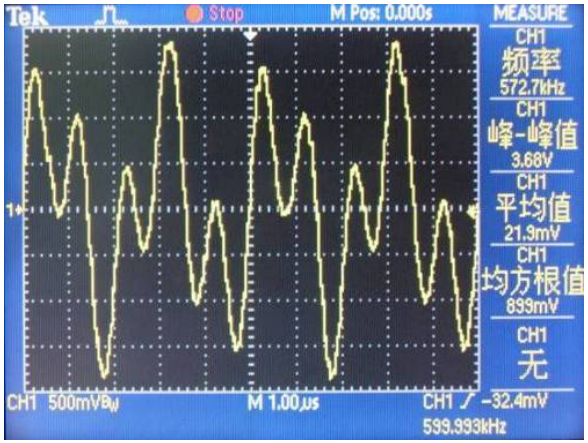
DA-FIR模块硬件测试

测试参数配置：

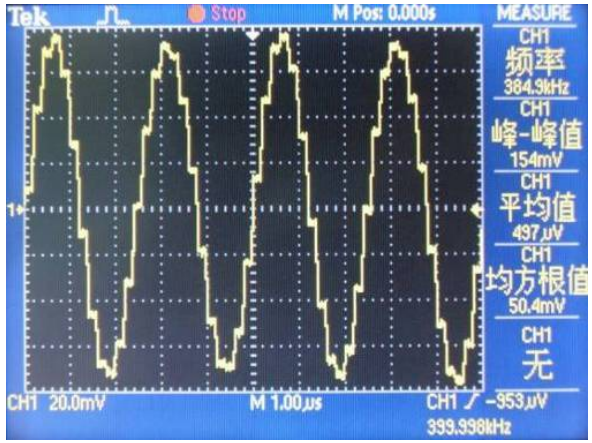
■输入信号：400kHz正弦＋1MHz正弦；

■FIR输入采样速率： f_S＝80MHz ； FIR处理时钟：f_{PRO}＝80MHz

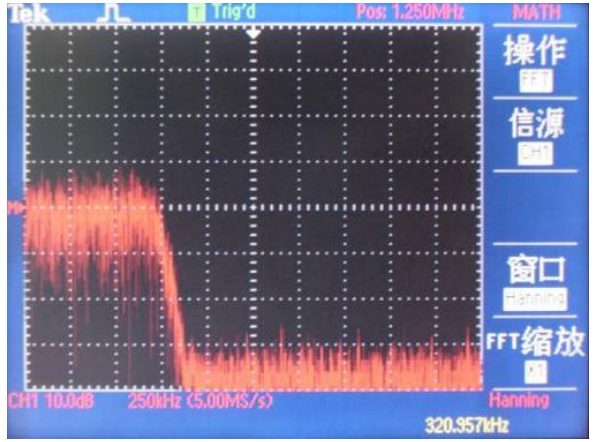
■FIR设置：256阶，f_{pass}=500kHz，f_{stop}＝1MHz



FIR模块输入波形



FIR模块输出波形

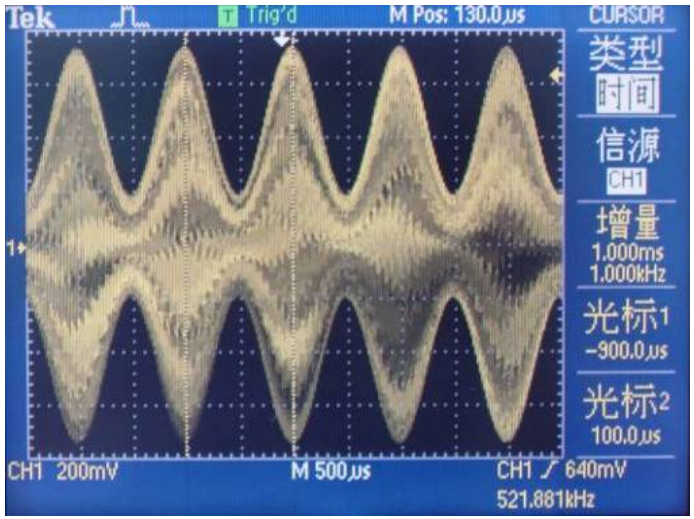


白噪声通过FIR模块后的输出频谱

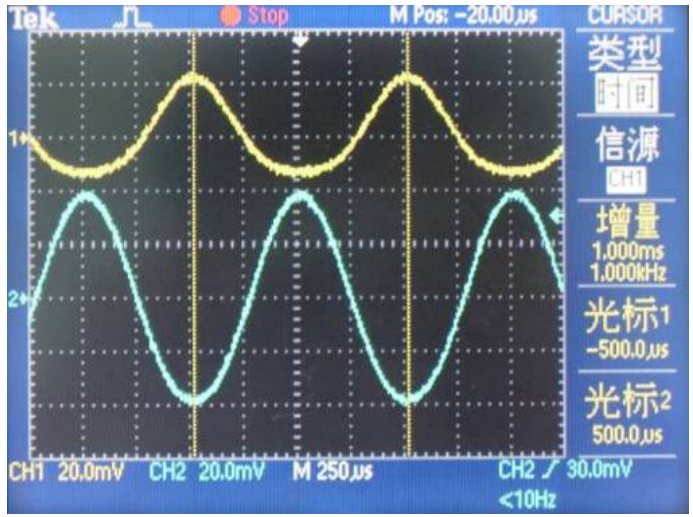
系统整合后测试－1

测试参数配置：

- 输入信号：AM信号，载波频率2.500,072,6MHz（信号发生器实际值）
- 调制信号：1kHz正弦；调制深度：60％
- 输入采样频率：f_S＝80MHz ；系统处理时钟：f_{PRO}＝80MHz
- NCO本振频率：f_{NCO}=f_C= 2.5MHz （计算设定值）
- CIC滤波器：8倍抽取
- FIR设置：256阶，f_{PASS}=500kHz，f_{STOP}＝1MHz
- 重采样：1.6倍抽取



输入**AM**信号波形

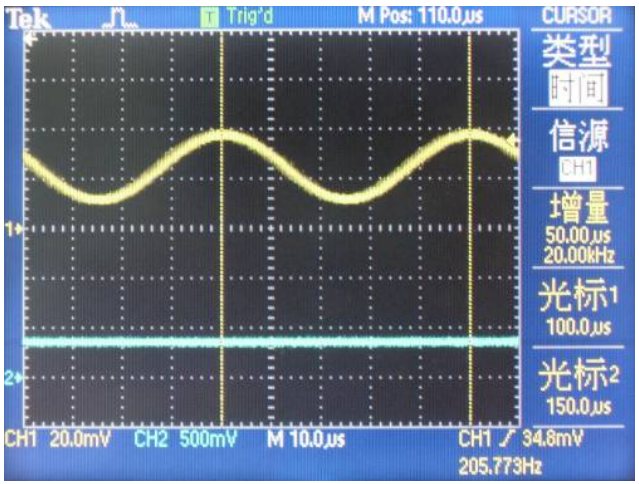


AM解调后的**I/Q**基带波形

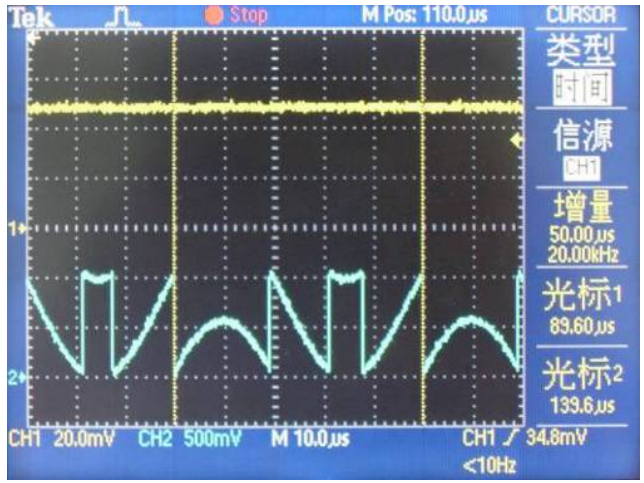
系统整合后测试－2

测试参数配置：

- 输入信号：FM信号/AM信号，载波频率2.500,072,6MHz（信号发生器实际值）
- 调制信号：20kHz正弦；频率偏移：100kHz（FM） / 调制深度：60％（AM）
- 输入采样频率：f_S＝80MHz ； 系统处理时钟：f_{PRO}＝80MHz
- NCO本振频率：f_{NCO}=f_C= 2.5MHz （计算设定值）
- CIC滤波器：8倍抽取
- FIR设置：256阶，f_{PASS}=500kHz，f_{STOP}＝1MHz
- 重采样：1.6倍抽取

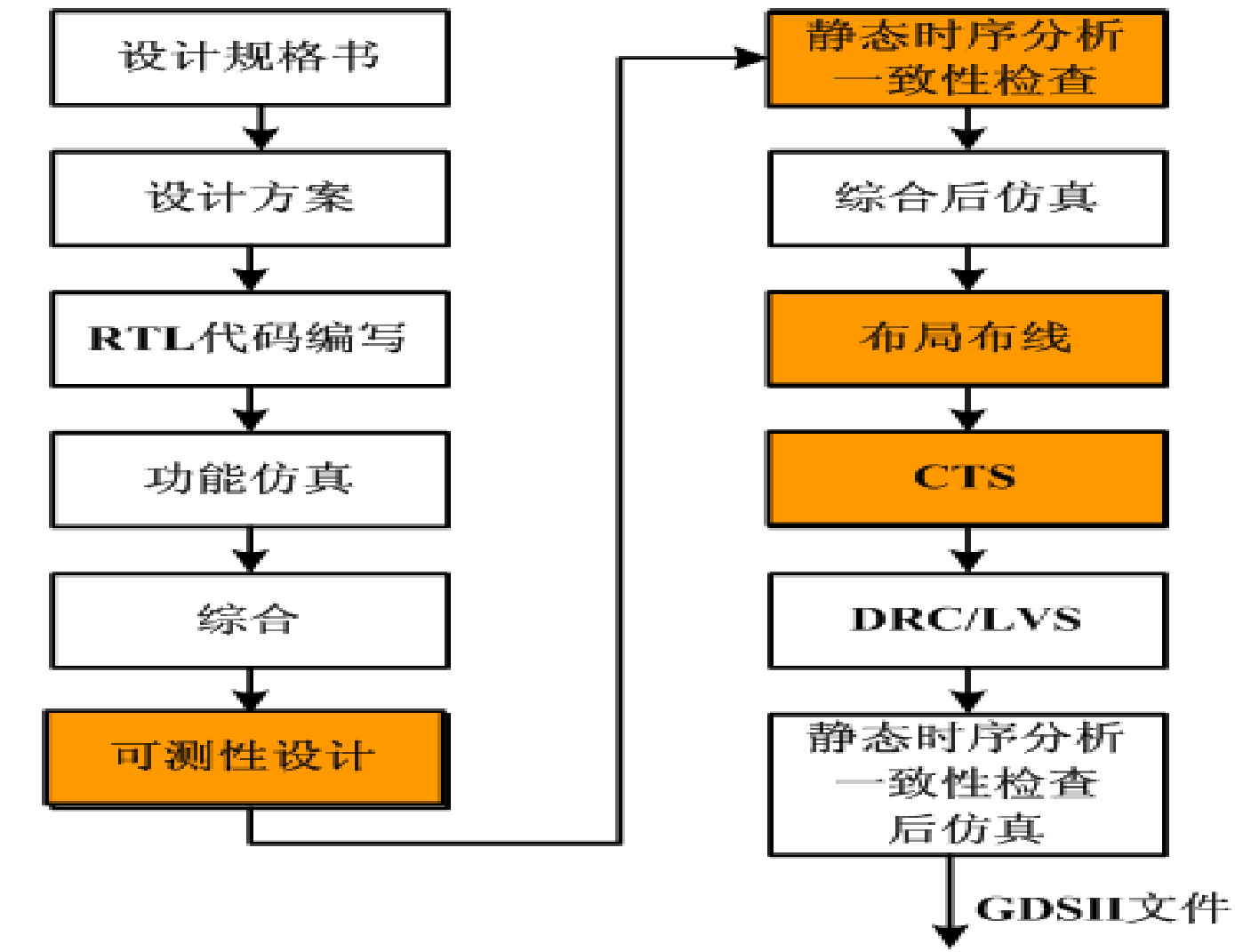


AM解调的幅值和相角输出



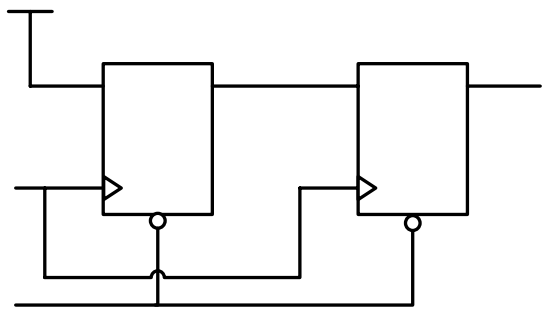
FA解调的幅值和相角输出
（输出相位未解卷绕 ）

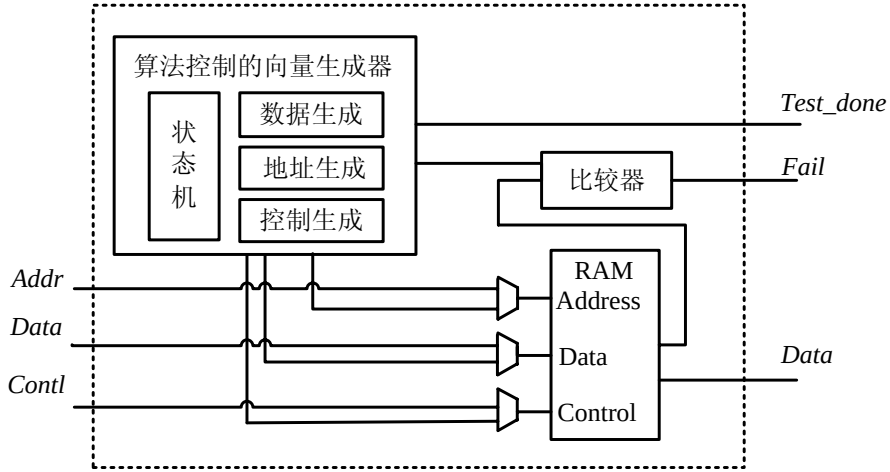
Back End Design



时钟、复位信号存储器设计

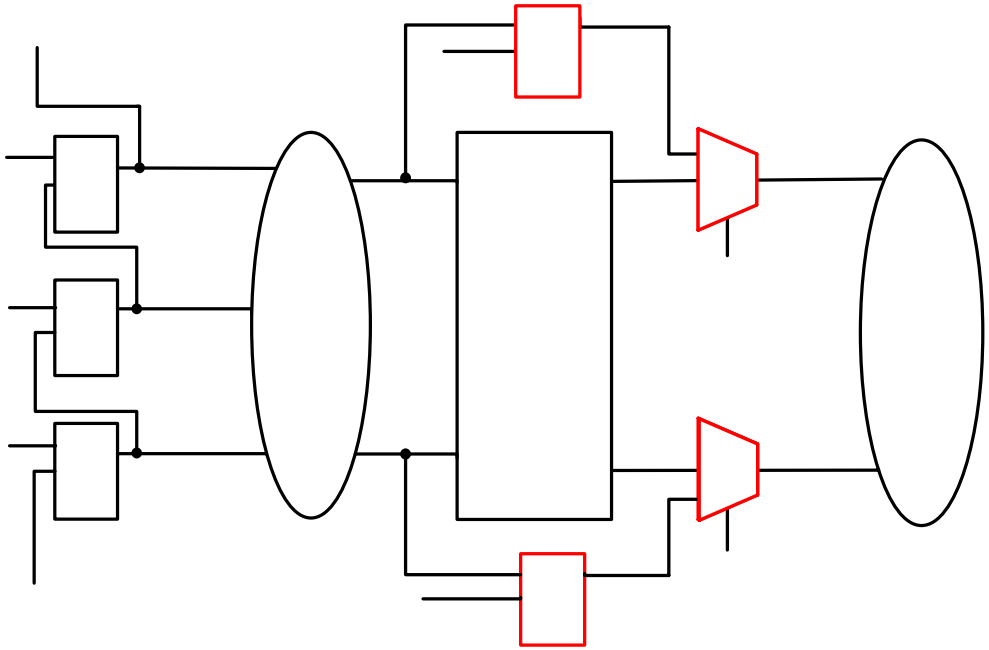
- 异步复位、同步撤离机制
  - 不同时钟域使用不同的复位信号
- 存储器内建自测试
  - 不影响正常功能
  - March算法
  - 99个RAM使用一组向量生成器和比较器
  - 芯片测试时：Test_done信号为1时，若Fail信号变为1，则存储器有物理缺陷





可测性设计（DFT）

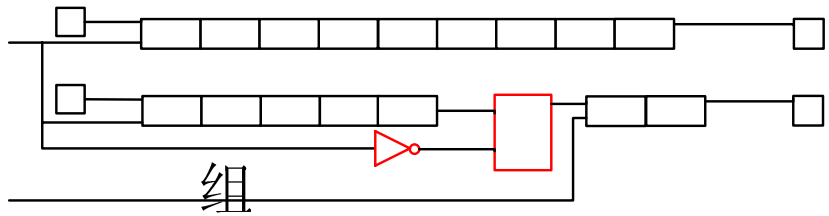
- 对存储器的处理



D
SI

- 两条不同时钟域扫描链的连接

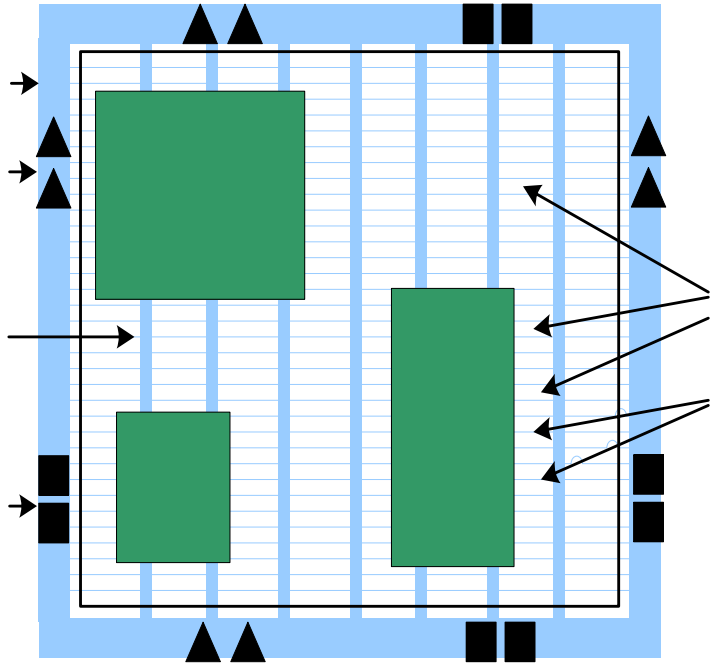
D
SI



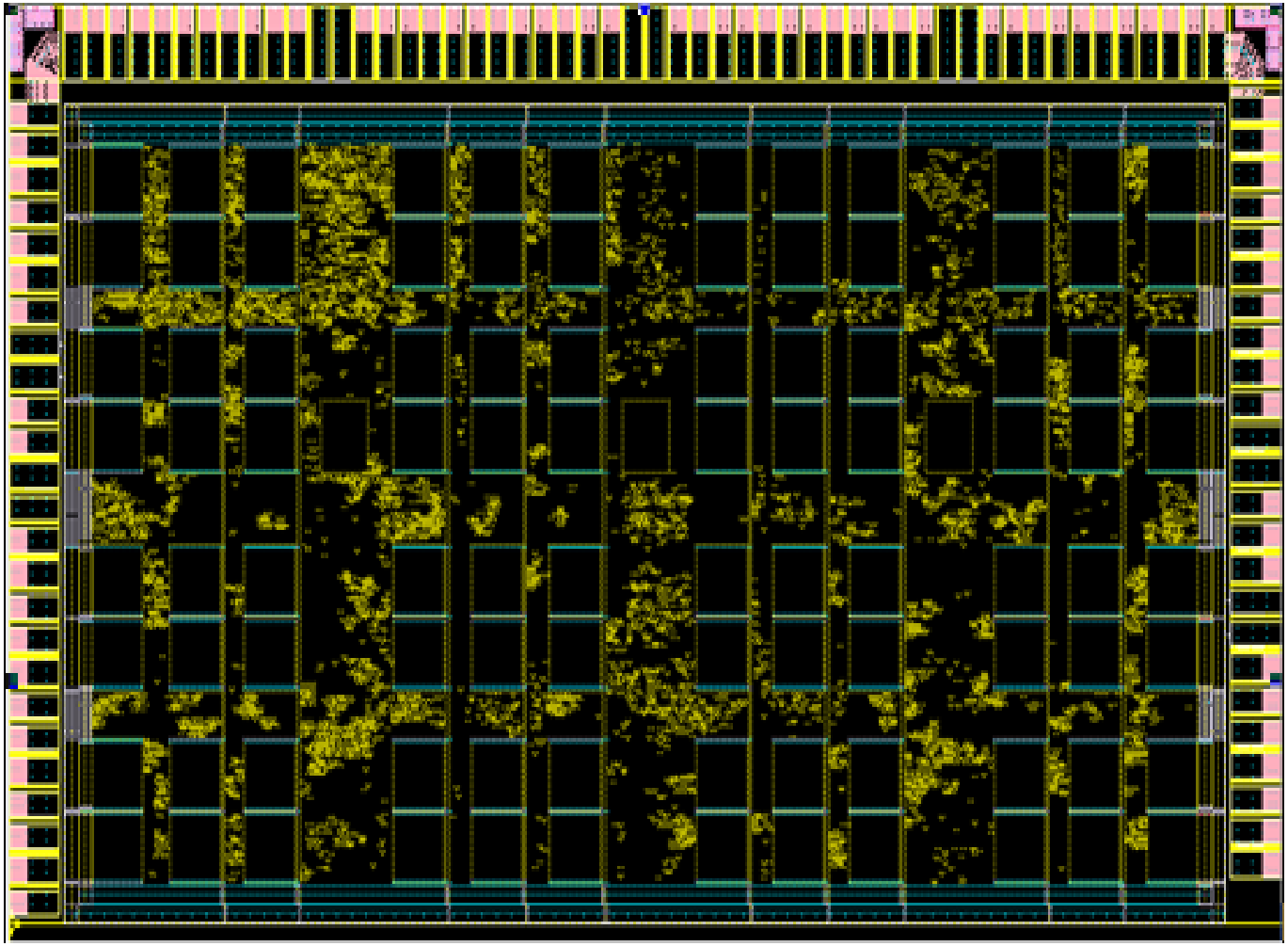
D

布局布线

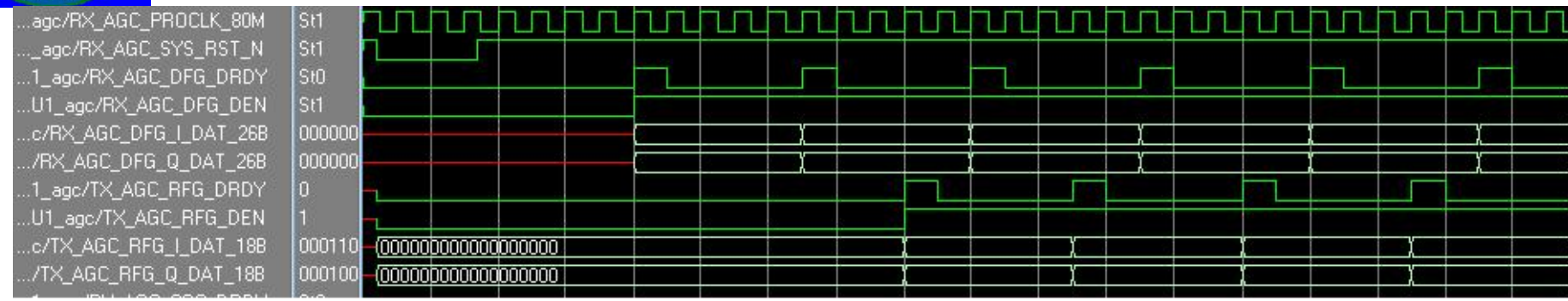
- 电源设计
- 宏模块布局
  - 要供电充分
  - 不能太分散
- 时钟树综合
  - 对大扇出信号做时钟树
  - 四棵时钟树：两个时钟，两个复位
  - 按驱动能力从大到小选择专门的时钟buffer构造时钟树
  - clock skew应低于0.2us

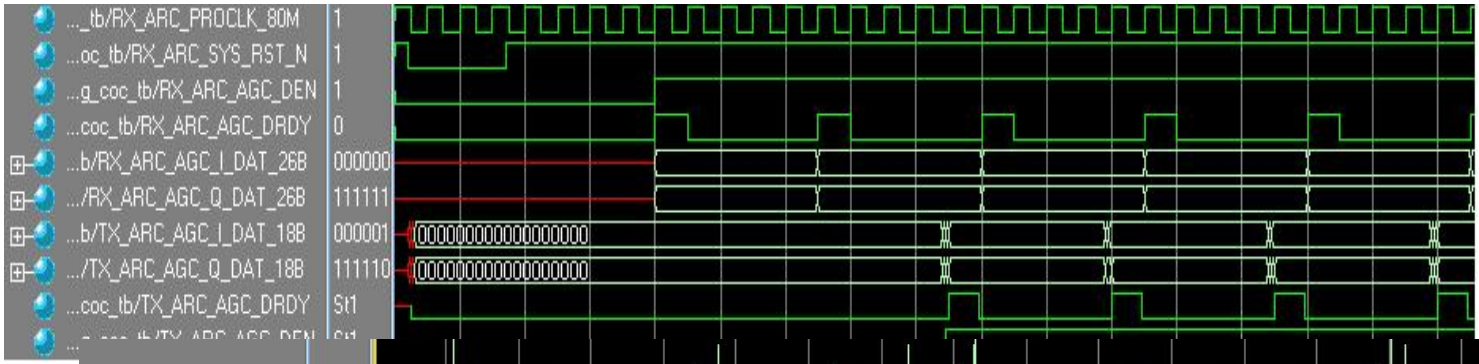


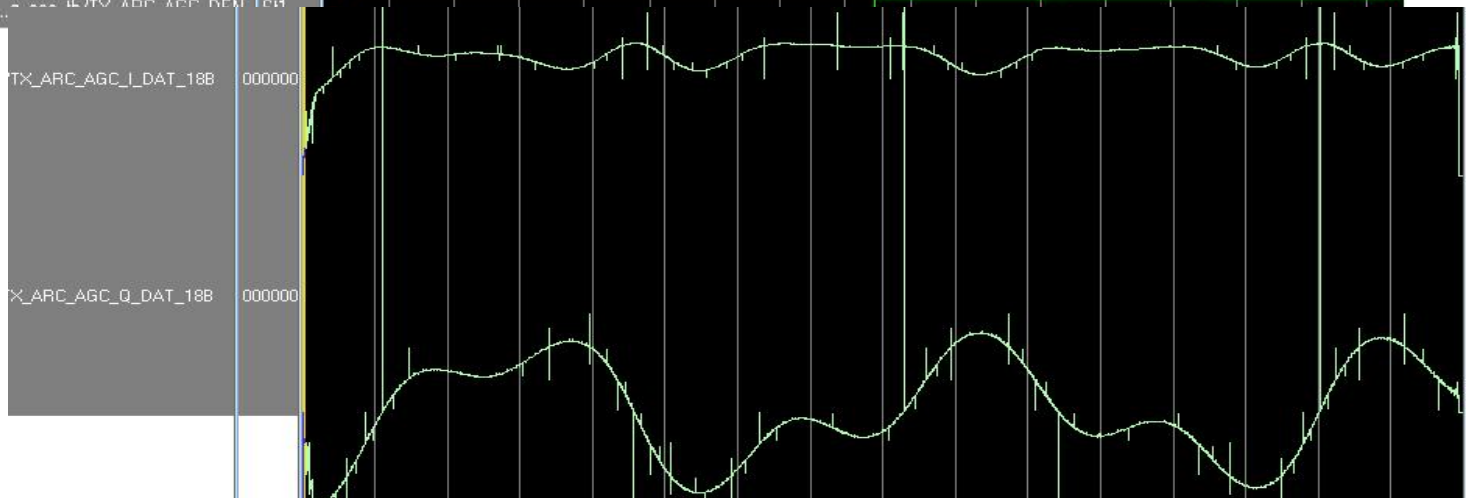
版图



版图综合后的仿真


...agc/RX_AGC_PROCLK_80M
...agc/RX_AGC_SYS_RST_N
...1_agc/RX_AGC_DFG_DRDY
...U1_agc/RX_AGC_DFG_DEN
...c/RX_AGC_DFG_I_DAT_26B
.../RX_AGC_DFG_Q_DAT_26B
...1_agc/TX_AGC_RFG_DRDY
...U1_agc/TX_AGC_RFG_DEN
...c/TX_AGC_RFG_I_DAT_18B
.../TX_AGC_RFG_Q_DAT_18B
St1
St1
St0
St1
000000
000000
0
1
000110
000100


..._tb/RX_ARC_PROCLK_80M
...oc_tb/RX_ARC_SYS_RST_N
...g_coc_tb/RX_ARC_AGC_DEN
...coc_tb/RX_ARC_AGC_DRDY
...b/RX_ARC_AGC_I_DAT_26B
.../RX_ARC_AGC_Q_DAT_26B
...b/TX_ARC_AGC_I_DAT_18B
.../TX_ARC_AGC_Q_DAT_18B
...coc_tb/TX_ARC_AGC_DRDY
1
1
1
0
000000
111111
000001
111110
St1


TX_ARC_AGC_I_DAT_18B
000000
X_ARC_AGC_Q_DAT_18B
000000

芯片测试

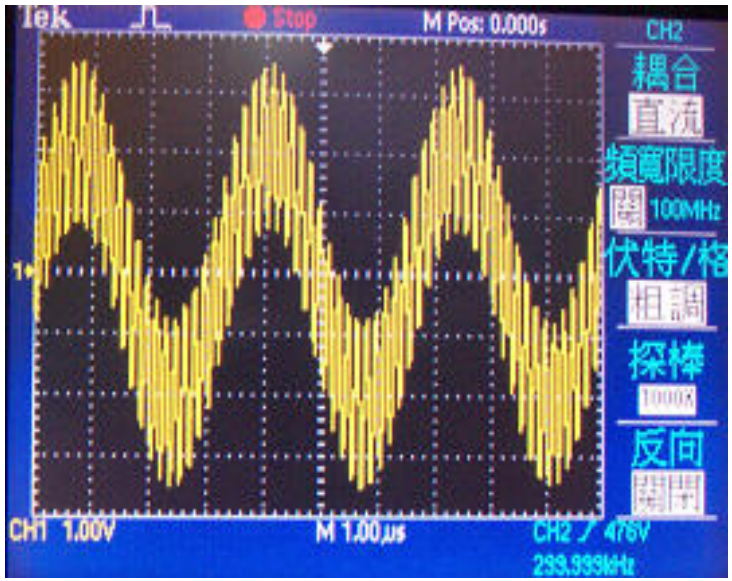
CIC模块测试结果

测试参数配置：

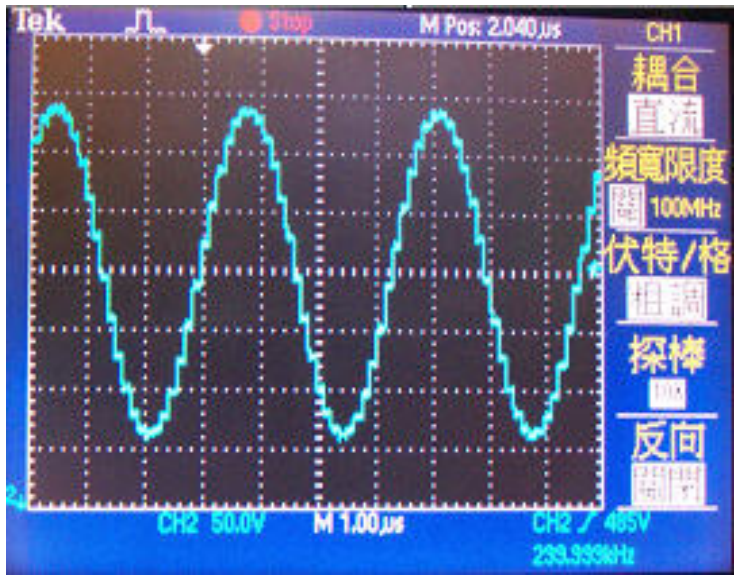
■输入信号：200kHz正弦＋5MHz正弦；

■CIC滤波器输入采样频率：f_s＝60MHz ；

■CIC滤波器抽取因子：D=4



CIC模块输入波形



CIC模块输出波形

FIR模块测试结果

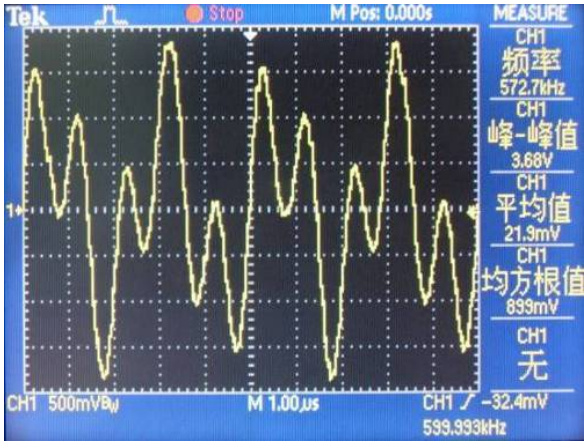
测试参数配置：

■输入信号：200kHz正弦＋1MHz正弦、白噪声；

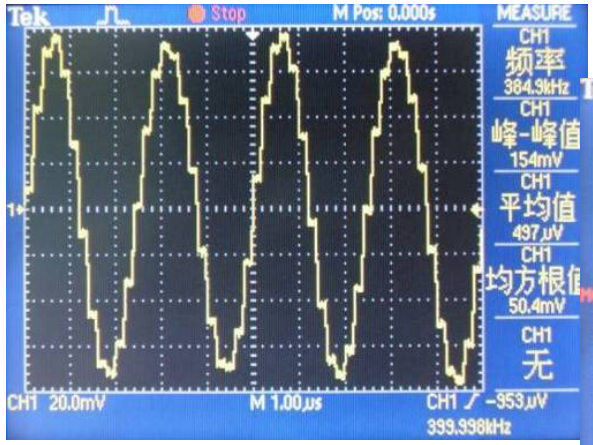
■FIR滤波器输入采样速率： f_S＝80MHz ；

■FIR滤波器处理时钟：f_{PRO}＝80MHz；

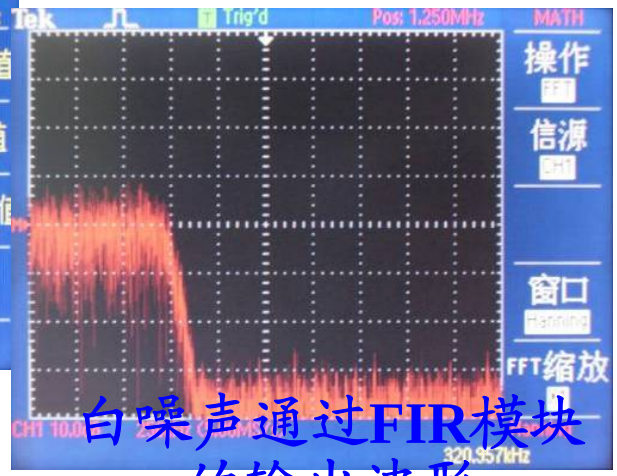
■FIR滤波器设置：128阶，f_{pass}=2MHz，f_{stop}＝4MHz



FIR模块输入波形



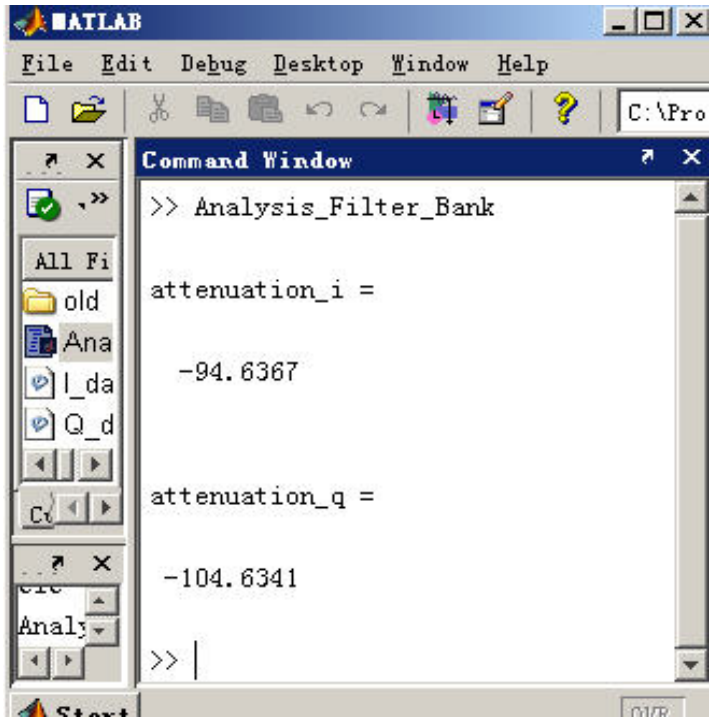
FIR模块输出波形

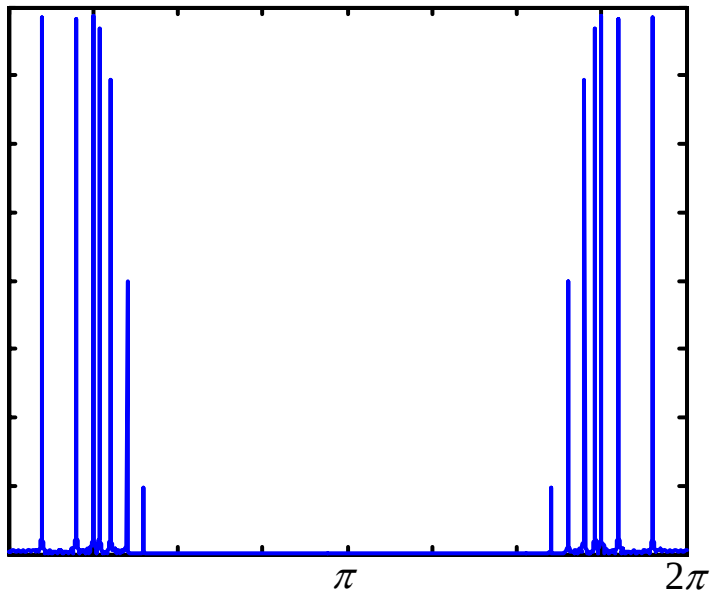


白噪声通过FIR模块的输出波形

噪声抑制比测试结果

- 输入多个单频叠加的信号，用Matlab分析回收数据，并绘出其FFT变换后的频谱
- Analysis_Filter_Bank=20lg(max_pass/max_stop)

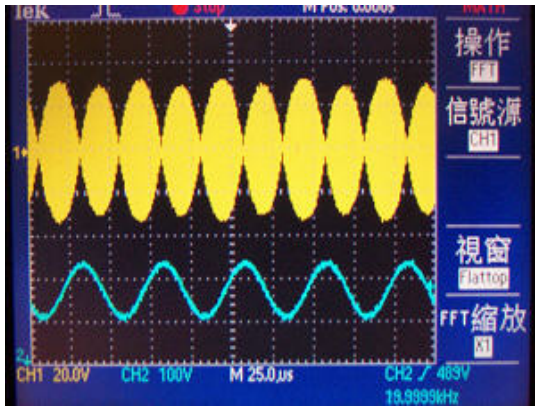




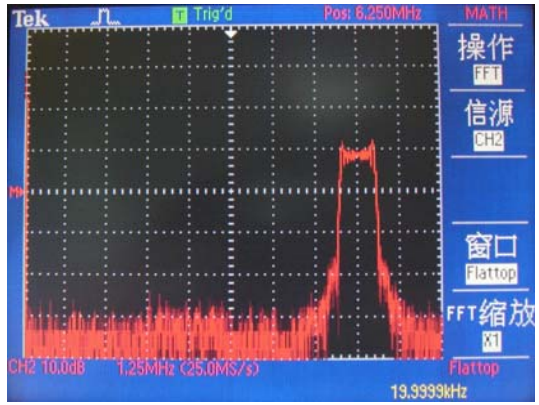
下变频功能测试结果

测试参数配置：

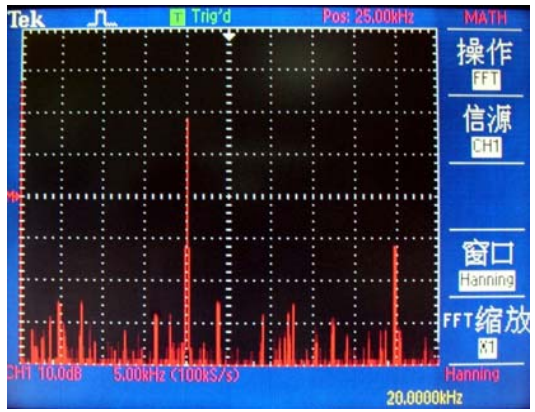
- ■输入信号：FM信号，载波频谱5MHz，调制信号频率20KHz；
- ■输入采样速率：f_S＝60MHz；
- ■系统处理时钟：f_{PRO}＝80MHz；
- ■FIR滤波器设置：128阶，f_{pass}=2MHz，f_{stop}＝4MHz
- ■抽取因子：16



DDC输入与输出波形



DDC输入频谱



DDC输出频谱

Problems

Study Altera's FPGA design environment and see their simulation and synthesis environments.

How do you compare Altera's environment with the simulation and synthesis environments discussed in this chapter?

Ch 2 Review of Combinational Logic Design

- 2.1 Combinational Logic and Boolean Algebra
- **2.1.1 ASIC Library Cells**
- 2.1.2 Boolean Algebra
- 2.1.3 DeMorgan's Laws
- 2.2 Theorems for Boolean Algebraic Minimization
- 2.3 Representation of Combinational Logic
- 2.4 Simplification of Boolean Expressions
- 2.5 Glitches and Hazards
- 2.6 Building Blocks for Logic Design

Ch3 Fundamentals of Sequential Logic Design

- 3.1 Storage Elements
- 3.2 Flip-Flops
- 3.3 Busses and Three-State Devices
- 3.4 Design of Sequential Machines
- 3.5 State-Transition Graphs
- 3.6 Design Example: BCD to Excess-3 Code Converter
- 3.7 Serial-Line Code Converter for Data Transmission
- 3.8 State Reduction and Equivalent States